Configuration of XOSC integrated load capacitances in SPC58 device lines

Introduction

The aim of this document is to give recommendations for hardware designers using STMicroelectronics SPC58 device lines for the right selection of XOSC components.

The next sections explain the root cause of the defect DAN-0042615, impacting the devices listed in Table 1. List of impacted devices, and its workarounds.

Refer to the proper Errata sheet document for details (see Section Appendix A Reference documents).

Table 1. List of impacted devices

Device line	Cut version	Errata sheet	JTAG_ID
SPC58xNx	Cut1.1	ES0398	0x1011_2041
SPC58xGx	Cut2.1	ES0399	0x1111_0041
SPC58xCx	Cut1.1	ES0400	0x1014_2041
SPC582Bx	Cut2.1	ES0413	0x1114_0041

1 Selection of XOSC capacitances

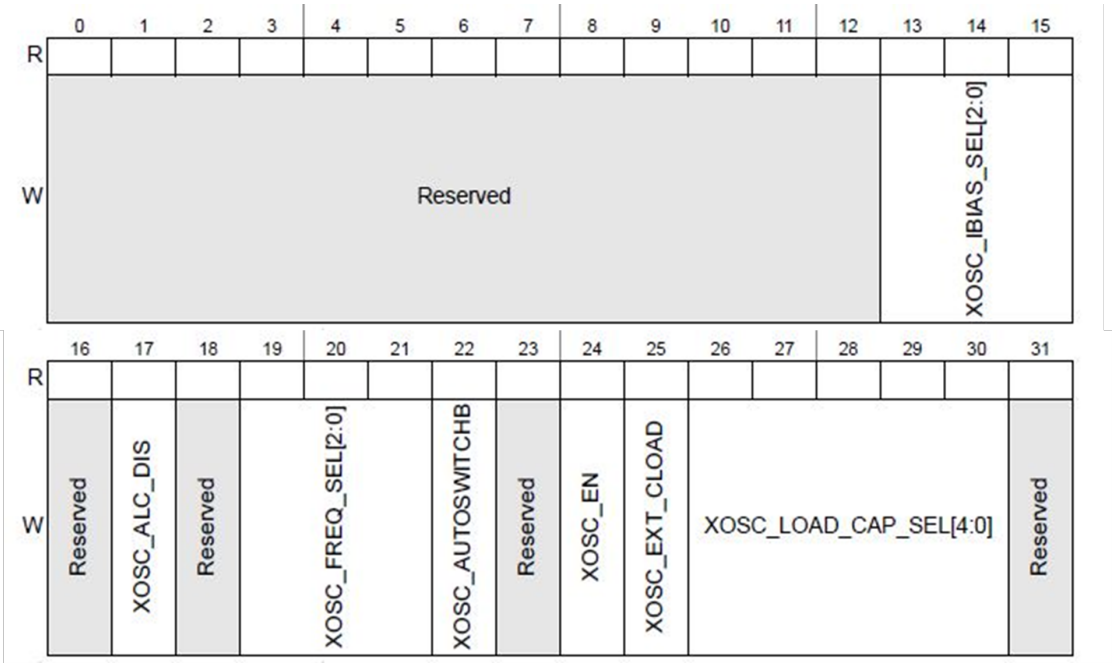
The external oscillator (XOSC) of the SPC58 lines provides integrated load capacitances (in the following section named like internal capacitances).

The selection between the internal or the external load capacitors on the XTAL/EXTAL pins and the trimming of internal capacitances is determined by programming the UTEST Miscellaneous DCF (here reported for convenience in Figure 1. UTEST Miscellaneous DCF client) in the UTEST flash memory, by means of the bit fields:

- MISC_DCF.XOSC_EXT_CLOAD
- MISC_DCF. XOSC_LOAD_CAP_SEL

Refer to device RMs for details on how to configure the register field.

Figure 1. UTEST Miscellaneous DCF client



1.1 Working scenarios

The XTAL operates as expected in case of:

Step 1. Selected external capacitances, with internal ones disabled.

UTEST MISC DCF configuration is:

- MISC_DCF.XOSC_EXT_CLOAD = 1
- INTERNAL CAP = N/A

Step 2. Selected internal capacitances with default trimming values. The resulting capacitance is aligned to the expected one.

UTEST MISC DCF configuration is:

- MISC_DCF.XOSC_EXT_CLOAD = 0
- MISC_DCF.XOSC_LOAD_CAP_SEL = 0
- INTERNAL CAP aligned with expectation

1.2 Current scenario due to DAN-0042615

If internal capacitances are used with a trim value different from 0 the resulting capacitance is lower than the expected one.

- MISC_DCF.XOSC_EXT_CLOAD = 0
- MISC_DCF.XOSC_LOAD_CAP_SEL > 0
- INTERNAL CAP < expected value

1.2.1 Typical internal capacitance values

The following table reports the typical internal capacitance values across crystal frequencies, in the case of working configuration (refer to Working scenarios). The values were measured in the IP standalone, so they can differ across sample. As example, the effective internal capacitance typical value for 20 MHz crystal is 10 pF, with the following configuration.

- MISC_DCF.XOSC_EXT_CLOAD = 0
- MISC_DCF.XOSC_LOAD_CAP_SEL = 0

Table 2. Expected internal capacitances in recommended configuration

XTAL	4 MHz	8 MHz	16 MHz	20 MHz	30 MHz	40 MHz
Capacitance (pF)	11	11	10.3	10	8.7	7.8

Note: This configuration allows a total variation of +/- 15% across process, voltage and temperature.

Capacitance value and variation cannot be granted if:

- MISC_DCF.XOSC_LOAD_CAP_SEL > 0

So this configuration is not recommended.

2 DAN-0042615 workarounds

The following actions can be taken to avoid the described problem.

- Configure the oscillator to use external capacitances only
  - MISC_DCF.XOSC_EXT_CLOAD = 1

OR

- Configure the oscillator to use internal capacitances with default trimming value
  - MISC_DCF.XOSC_EXT_CLOAD = 0
  - MISC_DCF.XOSC_LOAD_CAP_SEL = 0

The constraint in the application is to check if the internal capacitance variation is compatible with the XTAL PPM drift requirements. It is not recommended to use internal capacitances with a trim value different from 0.

These containment actions are summarized in DAN-0042615 available in the Errata sheet.

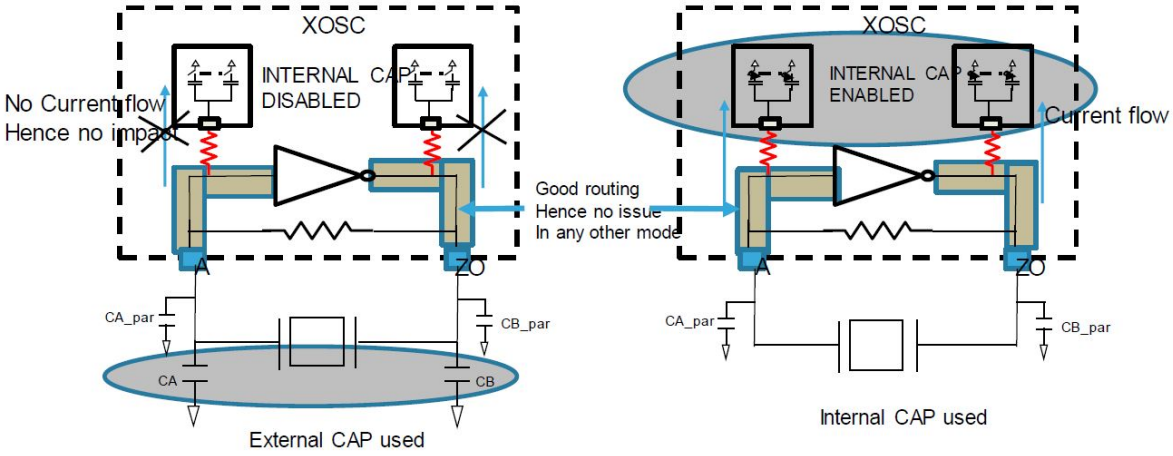
3 Root Cause of DAN-0042615

Analyzing the oscillator IP, the connection of XTAL pins to internal cap bank is too resistive.

Resistive path is for XTAL pins to internal cap bank only, hence issue is only in case the internal cap bank is enabled.

Note: This has no impact on any other mode of operation.

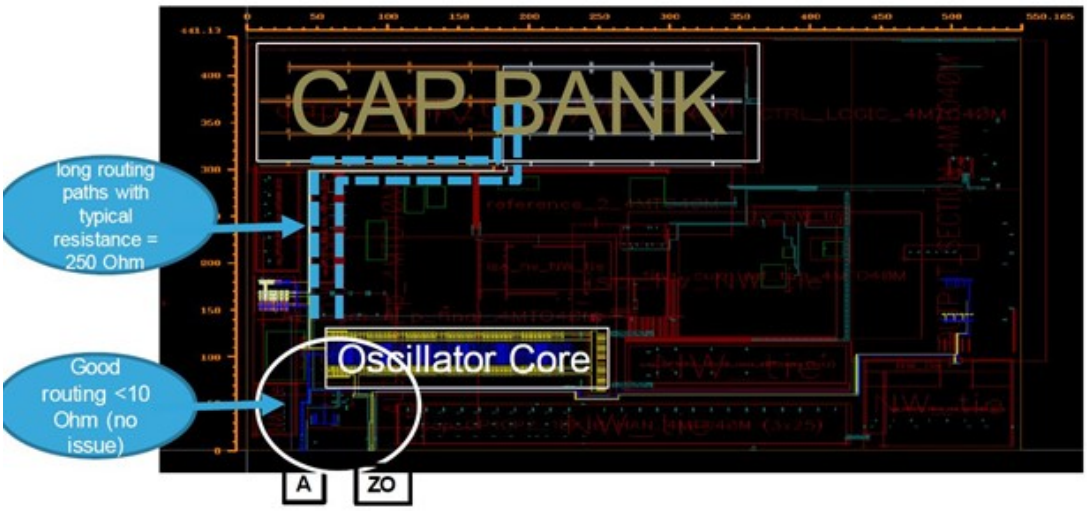
Figure 2. XOSC Internal cap enabled/disabled circuitry



3.1 XOSC layout and routing path

As said in the previous paragraphs, reducing the resistive path is the key to correctly activate internal capacitance support. The following figure reports the XOSC layout with the routing path highlighted.

Figure 3. Routing path in XOSC layout



4 Example of fix: data comparison between SPC58xCx cut1.1 vs cut2.0

The reported issue was fixed in hardware in the new SPC58xCx cut2.0.

The following tables report the tests performed on cut1.1 and cut2.0 by changing the default internal capacitance feature in the UTEST miscellaneous DCF register.

The expected Delta PPM is achieved in cut2.0 and not in cut1.1, demonstrating the feature was finally fixed.

Note: results show that no PCB changes are expected to be put in place moving from cut1.1 part to cut2.0 part.

Table 3. Cut1.1 PPM data

DCF Config	Nominal (MHz)	Mean (MHz)	PPM	Delta (PPM)
0x49E41 (int caps off)	40	39.99392	152	-
0x49E01 (int caps on)	40	39.99413	146.75	5.25
0x49E05 (int caps on)	40	39.99422	144.5	7.5
0x49E0B (int caps on)	40	39.99425	143.75	8.25
0x49E13 (int caps on)	40	39.99427	143.52	8.75
0x49E1D (int caps on)	40	39.99412	147	5
0x49E25 (int caps on)	40	39.99396	151	1

Note: test was made with 2x6.8 pF external caps applied. Frequency mean was taken after 5 min since the test has started (to make it stable).

Table 4. Cut2.0 PPM data

DCF Config	Nominal (MHz)	Mean (MHz)	PPM	Delta (PPM)
0x49E41 (int caps off)	40	39.99431	142.25	-
0x49E01 (int caps on)	40	39.99277	180.75	-38.5
0x49E05 (int caps on)	40	39.99371	182.25	-40
0x49E0B (int caps on)	40	39.99262	184.5	-42.25
0x49E13 (int caps on)	40	39.99235	191.25	-49
0x49E1D (int caps on)	40	39.99194	201.5	-59.25
0x49E25 (int caps on)	40	39.99194	201.5	-59.25

Note: test was made with 2x6.8 pF external caps applied. Frequency mean was taken after 5min since the test has started (to make it stable).

Appendix A Reference documents

Table 5. **Reference documents**

Doc name	ID	Title
ES0398	030711	SPC584Nx, SPC58ENx, SPC58NNx devices errata JTAG_ID = 0x1011_2041
ES0399	030832	SPC58xGx devices errata JTAG_ID = 0x1111_0041
ES0400	030833	SPC58xCx devices errata JTAG_ID = 0x1014_2041
ES0413	031246	SPC582Bx devices errata JTAG_ID = 0x1114_0041

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
07-Dec-2021	1	Initial release.

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