SR5 E1 line – Interfacing 5 V sensor to device SAR ADCs

Introduction

This document describes how to interface external sensors providing outputs with voltage ratings higher than the maximum allowable to the SAR ADCs of the SR5 E1 line products. This design targets applications using the SR5 E1 line products listed in the following table.

Table 1. Device list

Line	Part numbers
SR5E1	SR5E1E3, SR5E1E5, SR5E1E7

1 Overview

The SR5 E1 line products embed up to five successive approximation register (SAR) ADCs. Refer to the SR5E1x reference manual (for details see Appendix A Reference documents) for SAR ADC detailed features.

The products' supply and the input voltage range of SAR ADCs are both limited to 3.3 V to optimize cost and performance. This input voltage range is adequate for most applications, however, some automotive sensors, generally still used for legacy reasons, may require a higher ADC input voltage range of 5 V.

The user must preliminarily check if the sensor output voltage is really out of the ADC input voltage range because many sensors require a 5 V supply, but their output voltage will not go beyond 3.3 V in the practical use case. As an example, some temperature sensors operate on 5 V or higher supply but within the desired -40 C° to 150 C° operating window the maximum analog output voltage will be below 3.3 V. So, these sensors can easily be connected to a SAR ADC channel of the SR5 E1 line products without any additional hardware.

2 SAR ADC input impedance

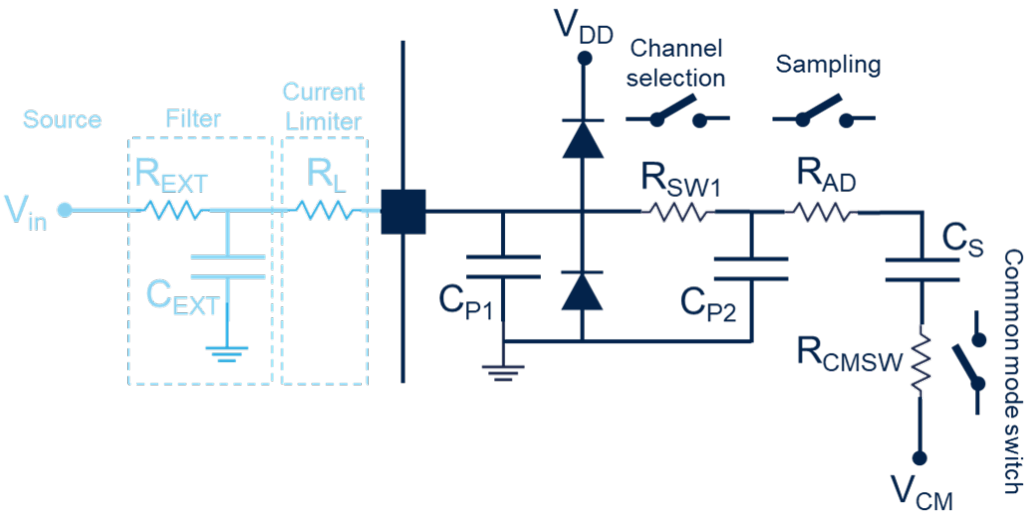
A low AC impedance must be connected to the ADC input pin to preserve accuracy.

Placing an RC filter including a capacitor with good high-frequency characteristics can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input signal and the charge it accumulates will charge the ADC internal capacitor during the signal sampling phase. However, this high impedance can limit the ADC's sampling rate.

Furthermore, a current limiter resistance is usually placed after the RC filter, to control the current spike when the sampling phase begins and to minimize the current request. However, also the current limiter resistance will affect the ADC's sampling rate.

The following figure shows a typical external network and the input equivalent circuit for each SAR ADC channel. The SAR ADC samples the input voltage through an internal capacitive network not providing resistive loading and hence given enough sampling time, the sampled value will be settled to the correct voltage.

Figure 1. SAR ADC input equivalent circuit and external network



C_S is the sampling capacitance, and C_{P1} and C_{P2} are the two contributions of the pin capacitance. R_{SW1}, R_{AD} and R_{CMSW} are the series resistances of the ADC internal switches, V_{CM} is the common mode voltage, R_L is the current limiter resistance, R_{EXT} is the parasitic resistance of the input capacitor C_{EXT}, which acts as an RC filter.

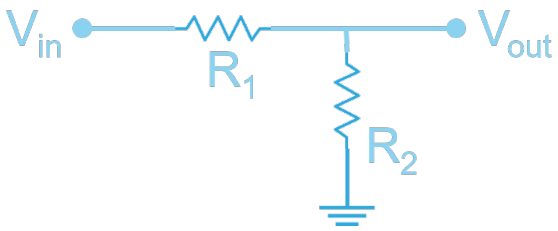
The values of the ADC internal parameters are given by the SR5E1x datasheet and the application note for the SPC58x (see Appendix A Reference documents) provides an example of how to design the current limiter and the RC filter and their design is a trade-off between accuracy and sampling rate.

3 Interfacing the sensor

3.1 Passive voltage divider

The simplest and low-cost method to reduce the maximum voltage of a signal from 5 V (or from any other higher voltage level) to 3.3 V is through a passive voltage divider as shown in the following figure.

Figure 2. Passive voltage divider



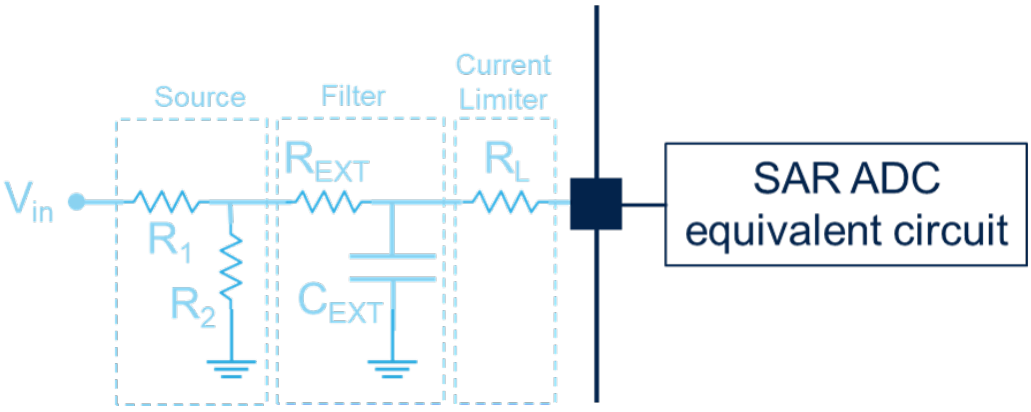
The following formulas define the relationship between V_{in} and V_{out} and the relationship between R_2 and R_1 in case the maximum voltage of the signal must be reduced from 5 V to 3.3 V:

$$V_{out} = V_{in} \cdot R_2/(R_1 + R_2) \quad (1)$$

$$R_2 \cong 1.94 \cdot R_1 \quad (2)$$

Source output impedance can be part of the resistor R_1 and the ground of the resistor R_2 is shorted to the clean analog ground (for example, the ADC reference ground). The following figure shows how the sensor output is connected to the ADC input by a passive voltage divider.

Figure 3. Sensor interfaced by a passive voltage divider

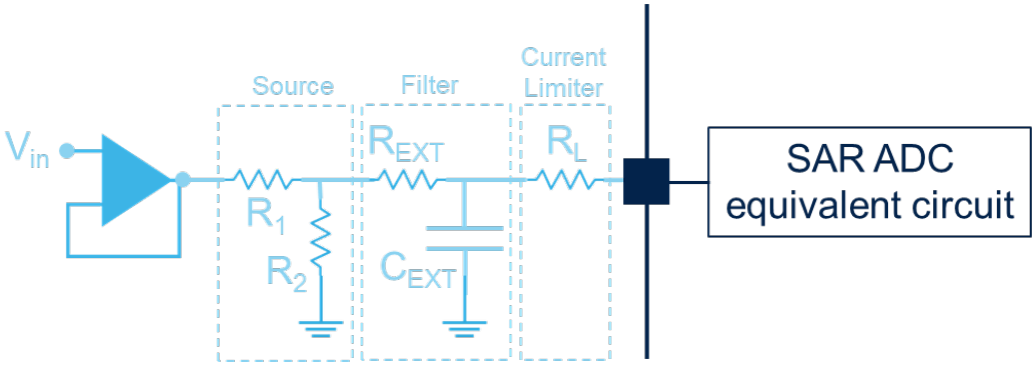


The mentioned scheme is for single-ended implementation but can be easily extended for differential inputs.

3.2 Handling high impedance sensor

Some sensors may require a relatively high impedance and they may not be able to drive a low direct-loading passive voltage divider. The user can increase the loading of the passive voltage divider to meet the desired loading constraints, but this can affect the ADC's sampling rate. A better but less cheap solution is to use an operational amplifier (OPAMP) with a high input impedance and a low output impedance as shown in the following figure. This high impedance unity gain OPAMP drives the passive voltage divider with its low output impedance and provides isolation from the sensor output and the ADC input.

Figure 4. Sensor interfaced by an OPAMP



ST has a wide portfolio of high-performance low-cost OPAMPs as the ones of the LMV82xA series.

4 Effects of the attenuation

This section looks at the effects of the attenuation by the voltage divider on some ADC performance metrics.

Assume that the ADC has an offset of x LSB where LSB is the step size of the SAR ADC. Without the voltage divider, if $V_{IN} = V_1$, V_1 is the voltage at the input of the ADC, and it generates an output code C_1. The following formulas define the relation between V_1 and C_1:

$$C_1 = V_1/LSB + x \quad (3)$$

$$V_1 = C_1 \cdot LSB + x \cdot LSB \quad (4)$$

With the voltage divider, if $V_{IN} = V_2$, V_{2_ADC} will be the voltage at the input of the ADC, and it generates an output code C_2. The following formulas define the relation between V_{2_ADC} and C_2:

$$V_{2\_ADC} = V_2 \cdot R_1/(R_1 + R_2) \quad (5)$$

$$C_2 = V_{2\_ADC}/LSB + x \quad (6)$$

$$V_2 = C_2 \cdot (LSB \cdot (R1 + R2)/R1 + x \cdot (LSB \cdot (R_1 + R_2)/R_1) \quad (7)$$

Comparing equations 4 and 7, the voltage divider simply scales the LSB size. In other words, if the ADC has an offset error of x LSB (with LSB = 3.3 / 4096), the offset error at the input of the voltage divider is still x LSB (with a slightly larger LSB = 5 / 4096). Other errors such as the DNL can be proven to be scaled in the same way.

Any noise affecting the signal V_{IN} gets attenuated by the voltage divider, hence it will not affect the overall SNR. On the contrary, the common ground noise will not be attenuated by the voltage divider, hence the attenuation of the signal V_{IN} has an impact on the SNR. In our case, the SNR degradation is:

$$20 \cdot \log(3.3/5) = -3.6\,dB \quad (8)$$

In general, an N-bit ADC's ideal SNR is equal to:

$$SNR = (6.02 \cdot N + 1.76)\,dB \quad (9)$$

Considering that the SNR of an ideal 12-bit ADC is 74 dB, the scaling from 5 V to 3.3 V will cause an SNR degradation from 74 dB to 70.4 dB, that is, an SNR loss of about ½ LSB. This degradation is usually negligible.

5 Conclusion

The SR5 E1 line products embed 3.3 V SAR ADCs with a step size much less (≈ 33% less) than the step size of a similar 5 V SAR ADC and this is a significant advantage. Moreover, supporting a high-voltage sensor does not always require a high-voltage ADC, anyway, if it is necessary, the described solutions are a low-cost, efficient way of interfacing 5 V signals to a 3.3 V SAR ADC of the SR5 E1 line products with a negligible signal degradation for most applications.

Appendix A Reference documents

Table 2. Reference documents

Document name	Document title
DS13808	SR5 E1 line of Stellar electrification MCUs — 32-bit Arm® Cortex®-M7 automotive MCU 2x cores, 300 MHz, 2 MB flash, rich analog, 104 ps 24-ch high-resolution timer, HSM, and ASIL D
RM0483	SR5E1x 32-bit Arm® Cortex®-M7 architecture microcontroller for electrical vehicle applications
AN5527	SPC58xx SAR ADC

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
15-Apr-2024	1	First release.

Contents

List of tables

List of figures