UM0938
User manual

L6460 configuration guide

Introduction

The L6460 is optimized to control and drive multimotor system providing a unique level of integration in term of control, power and auxiliary features.

Thanks to the high configurability L6460 can be customized to drive different motor architectures and to optimize the number of embedded features, such as the voltage regulators, the high precision A/D converter, the operational amplifier and the voltage comparators.

The possibility to drive simultaneously stepper and DC motor makes L6460 the ideal solution for all the application featuring multi motors.

The start up configuration can be defined by the GPIOs and then through the serial interface all device features can be configured.

This document describes in details how to program the L6460 registers to obtain desired functions.

For information about the L6460 electrical characteristics please refer to the datasheet.

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1 General description

At the startup the device performs the following operations only:

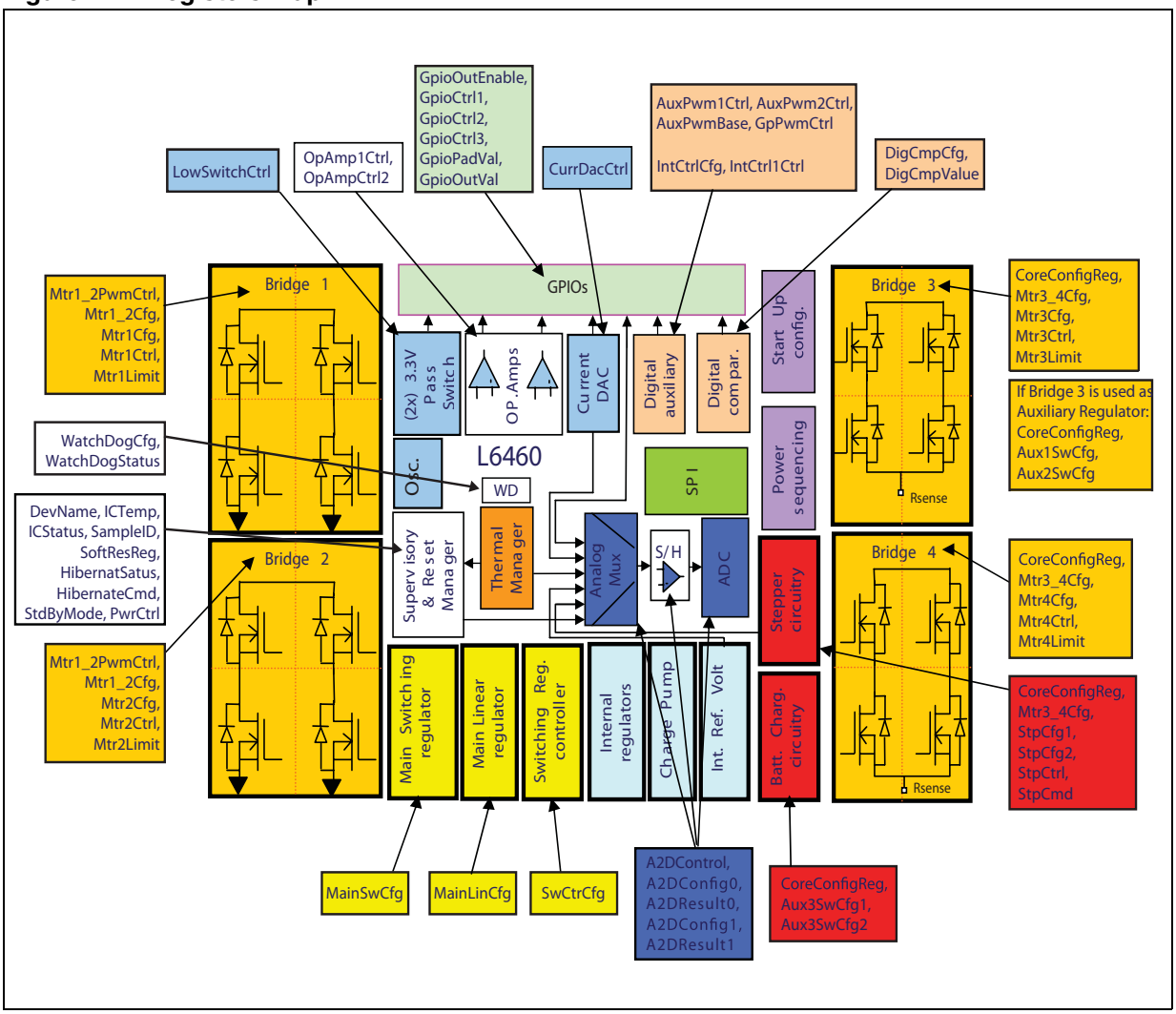
- samples startup configuration: GPIO0, GPIO3 and GPIO4 status;
- waiting enable if slave device;
- starts system regulators;
- sends enable to slave device, if master.

All other operations must be enabled and driven by the serial port, using the internal registers.

1.1 Registers overview

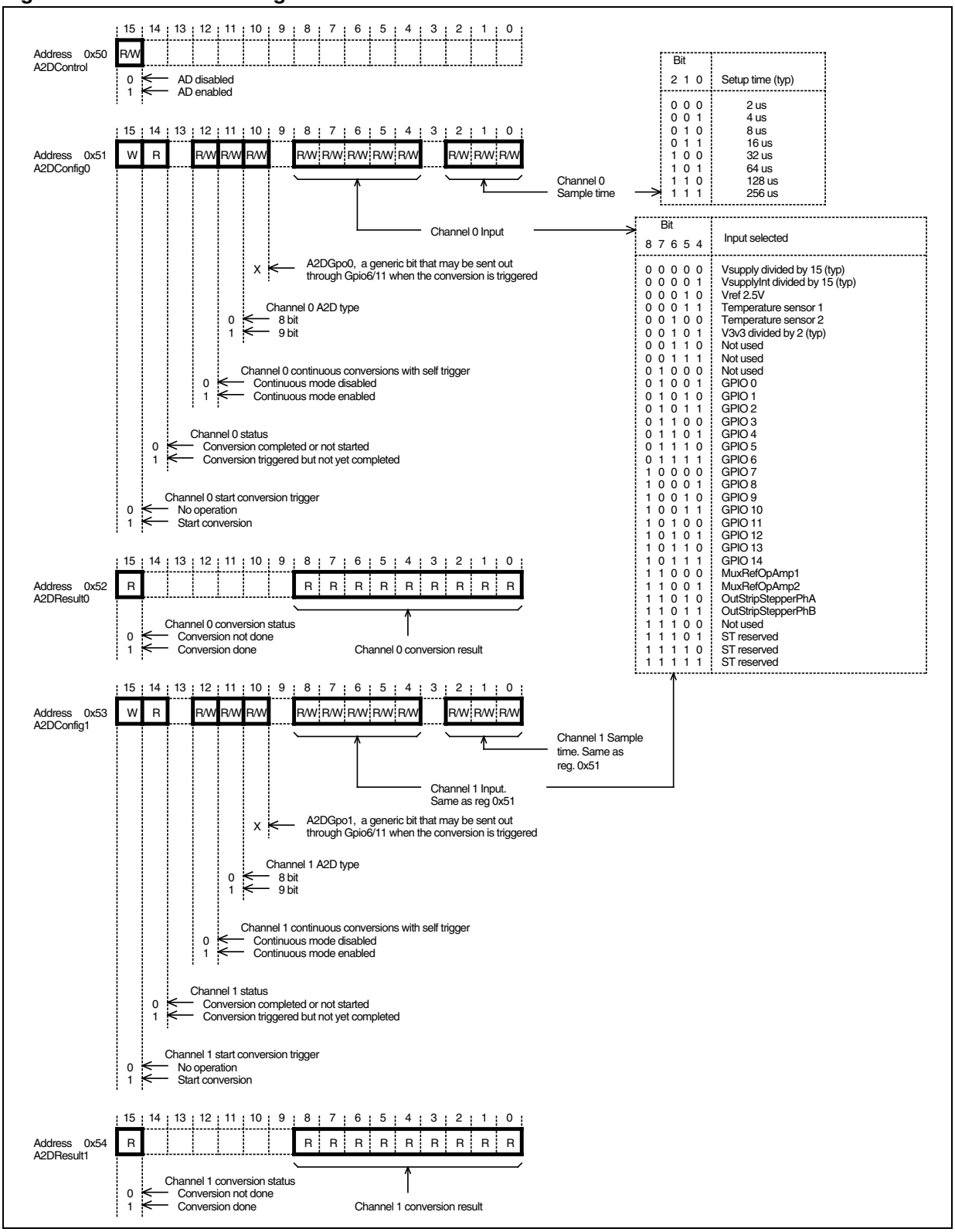
In the *Figure 1* is shown the L6460 register map providing the relationship between the registers and the correspondent section in the IC.

Figure 1. Registers map



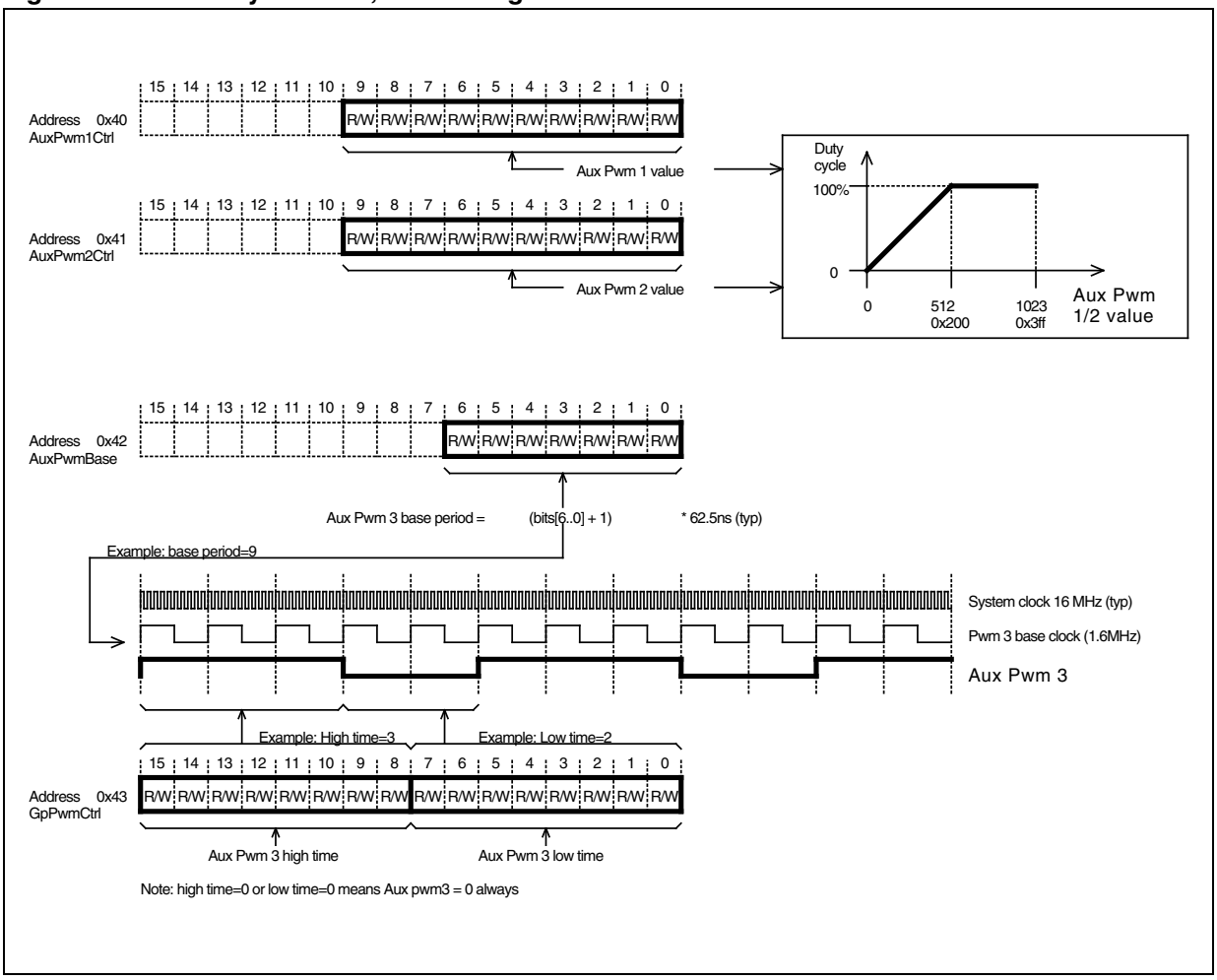
1.1.1 AD converter registers

Figure 2. AD converter registers



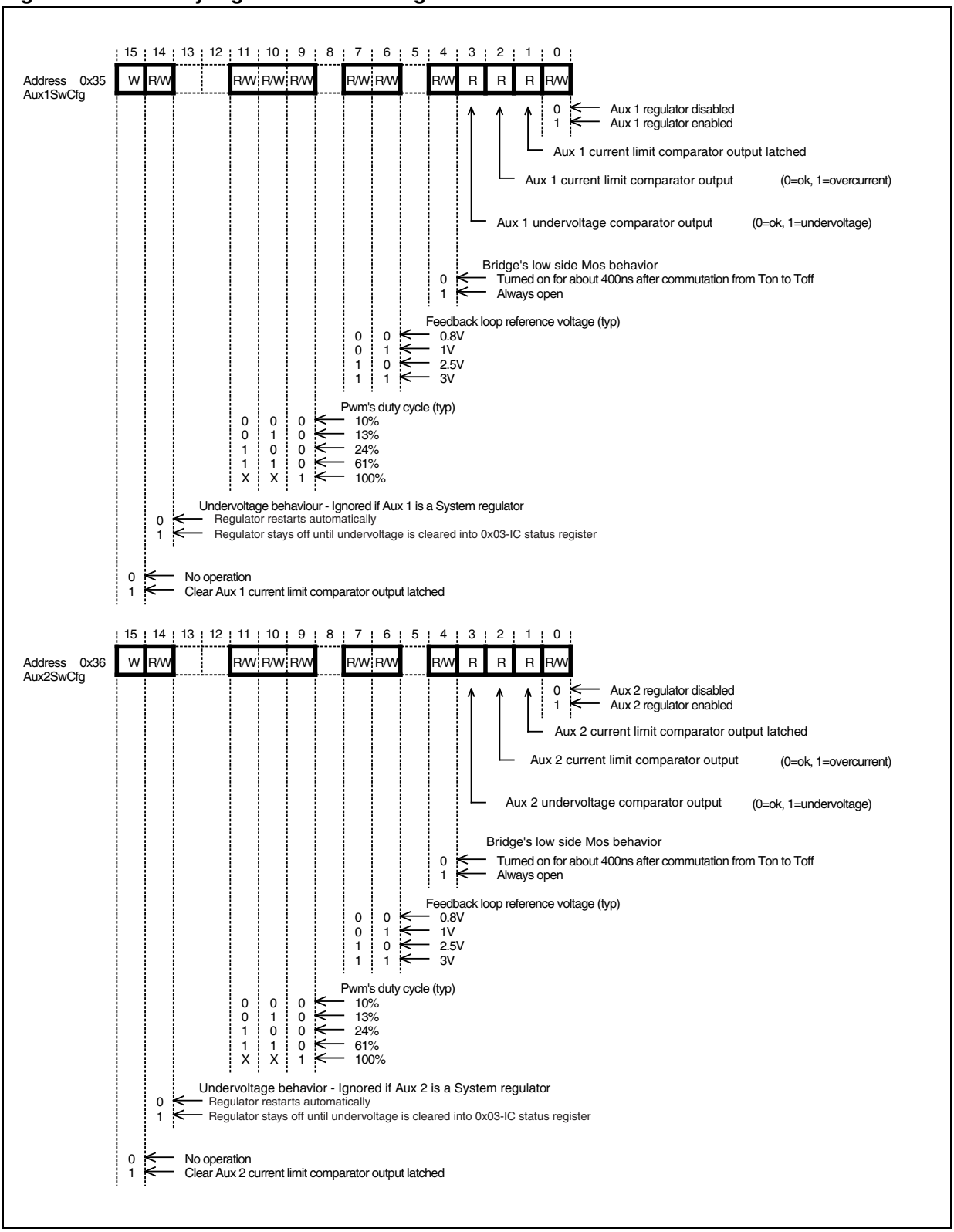
1.1.2 Auxiliary PWMs 1, 2 and 3 registers

Figure 3. Auxiliary PWMs 1, 2 and 3 registers



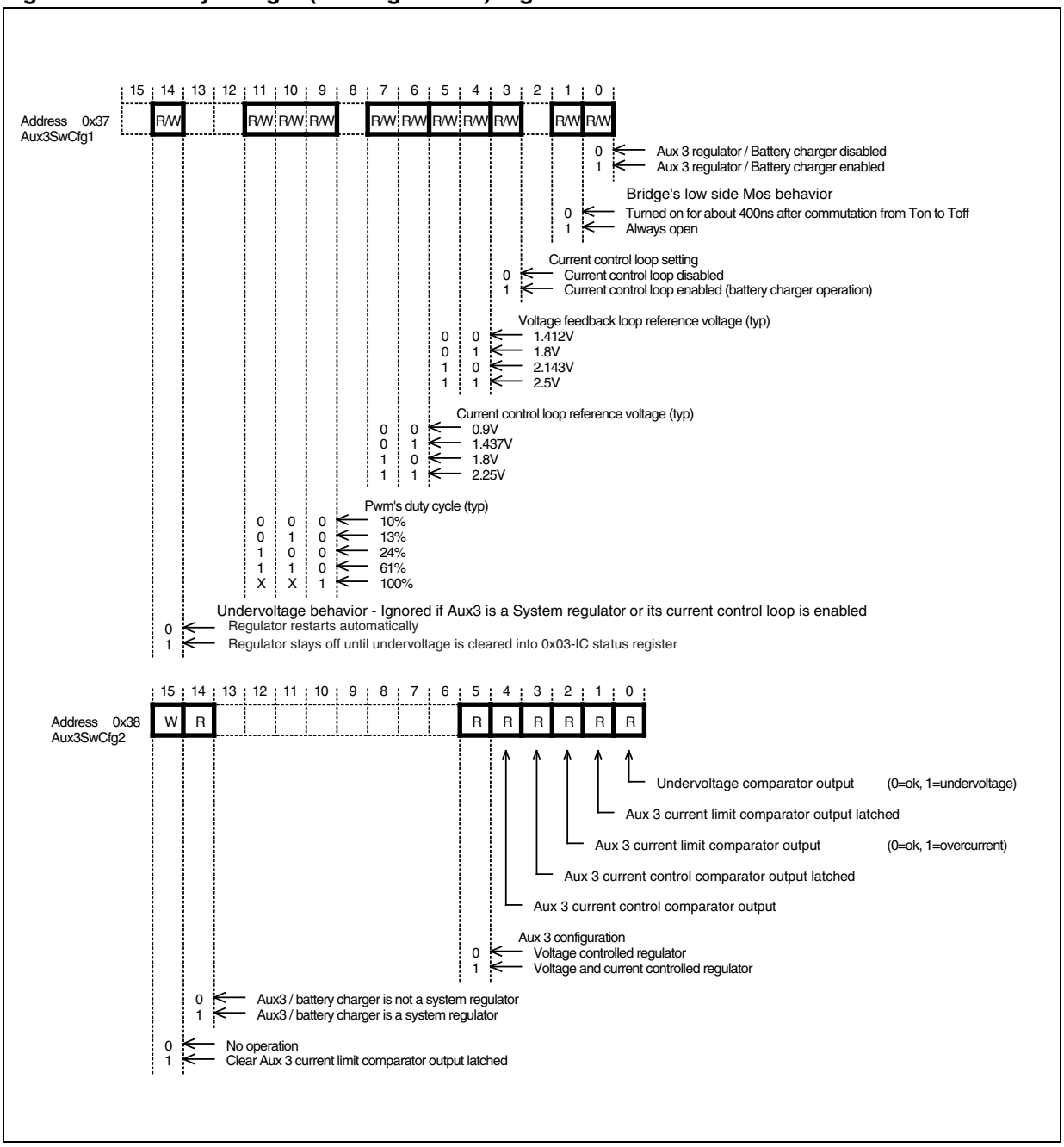
1.1.3 Auxiliary regulators 1 and 2 registers

Figure 4. Auxiliary regulators 1 and 2 registers



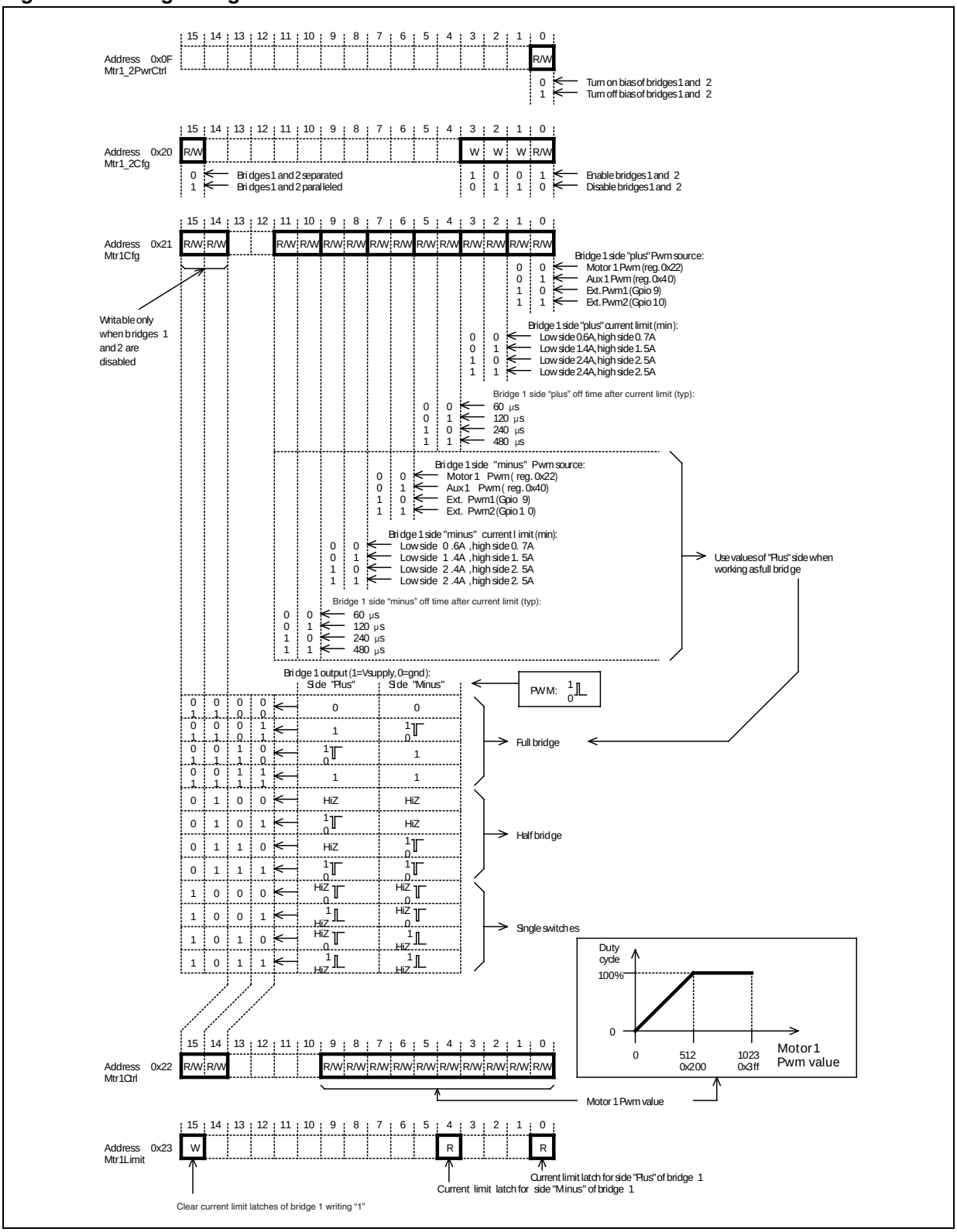
1.1.4 Battery charger (Aux regulator 3) registers

Figure 5. Battery charger (Aux regulator 3) registers



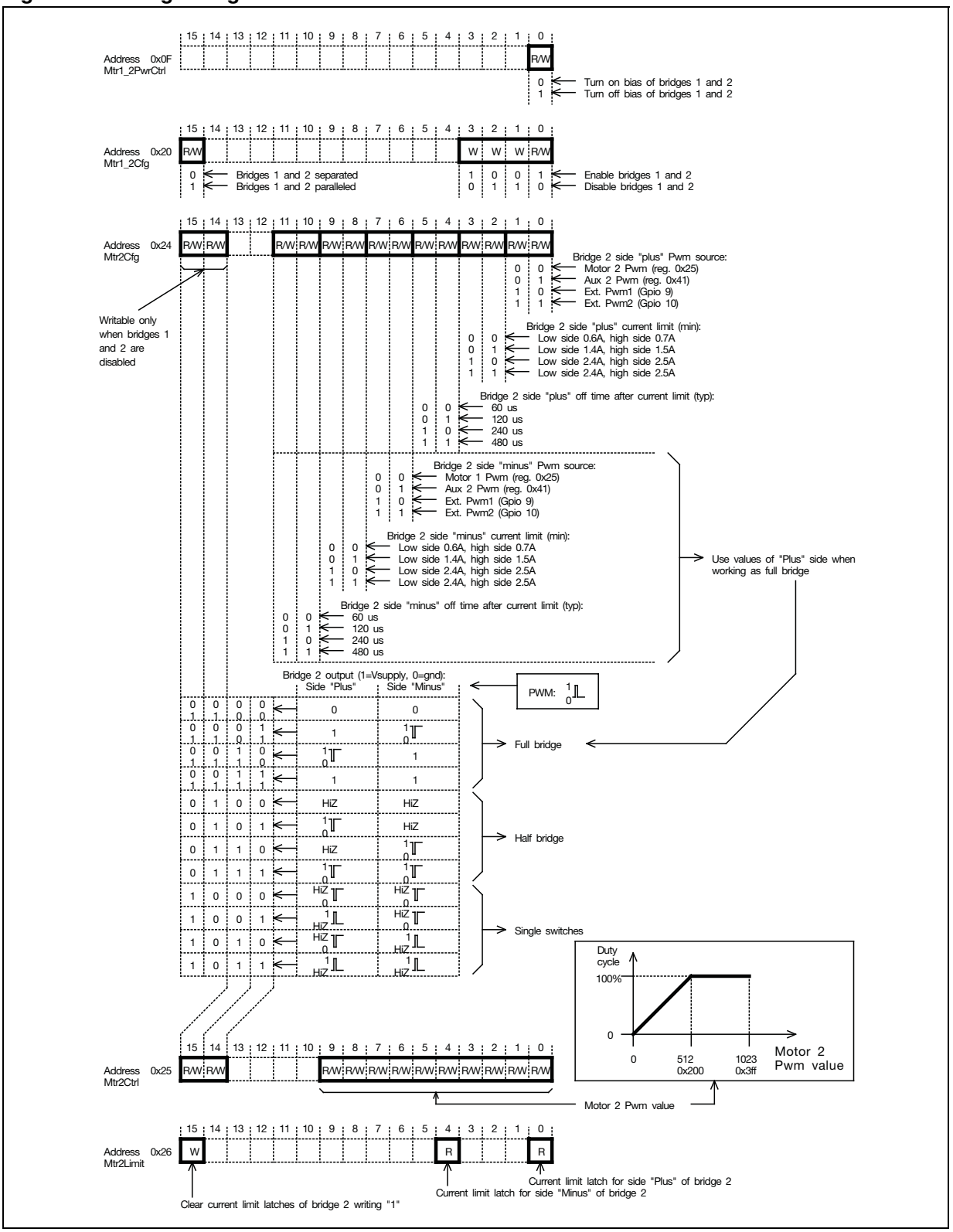
1.1.5 Bridge 1 registers

Figure 6. Bridge 1 registers



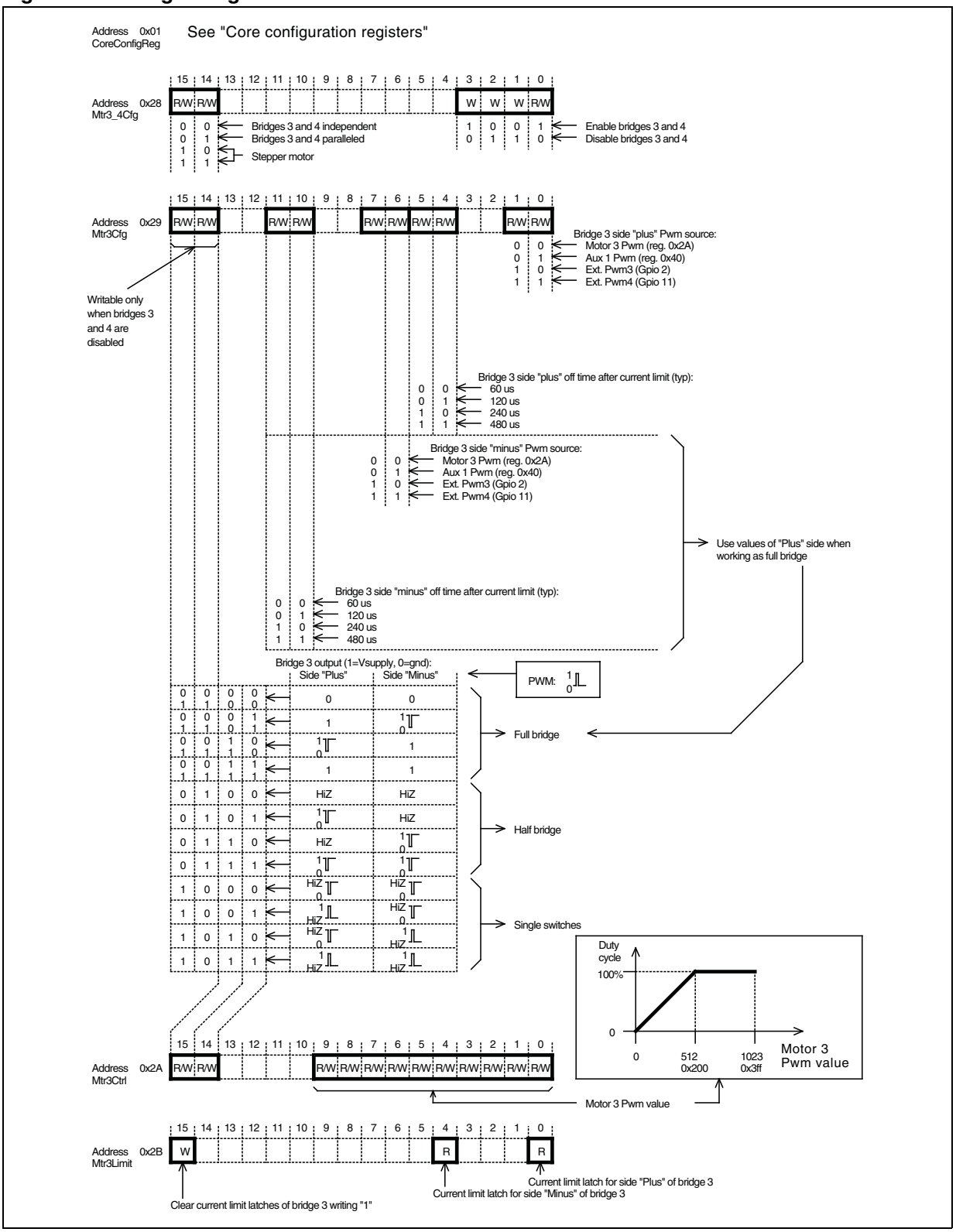
1.1.6 Bridge 2 registers

Figure 7. Bridge 2 registers



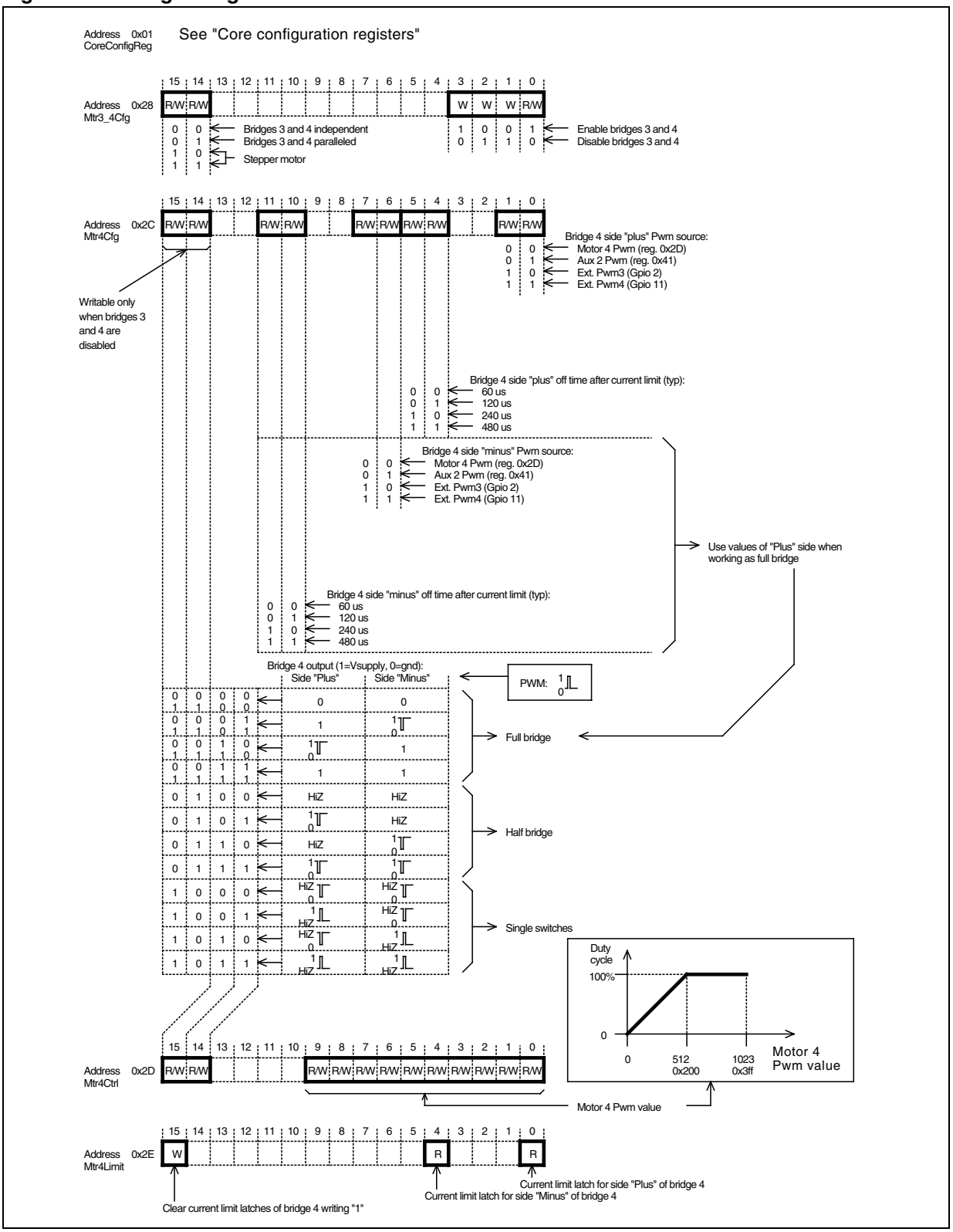
1.1.7 Bridge 3 registers

Figure 8. Bridge 3 registers



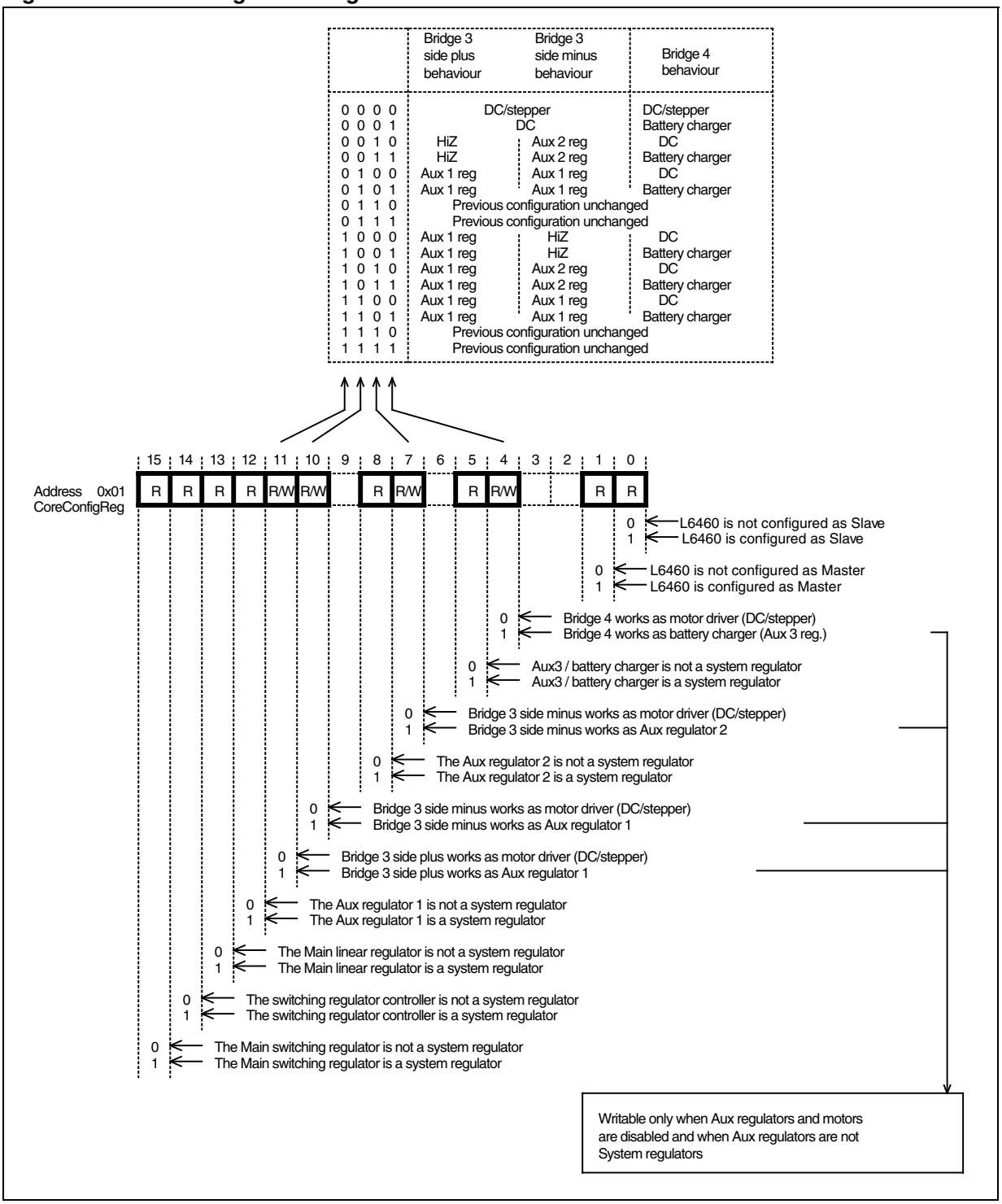
1.1.8 Bridge 4 registers

Figure 9. Bridge 4 registers



1.1.9 Core configuration registers

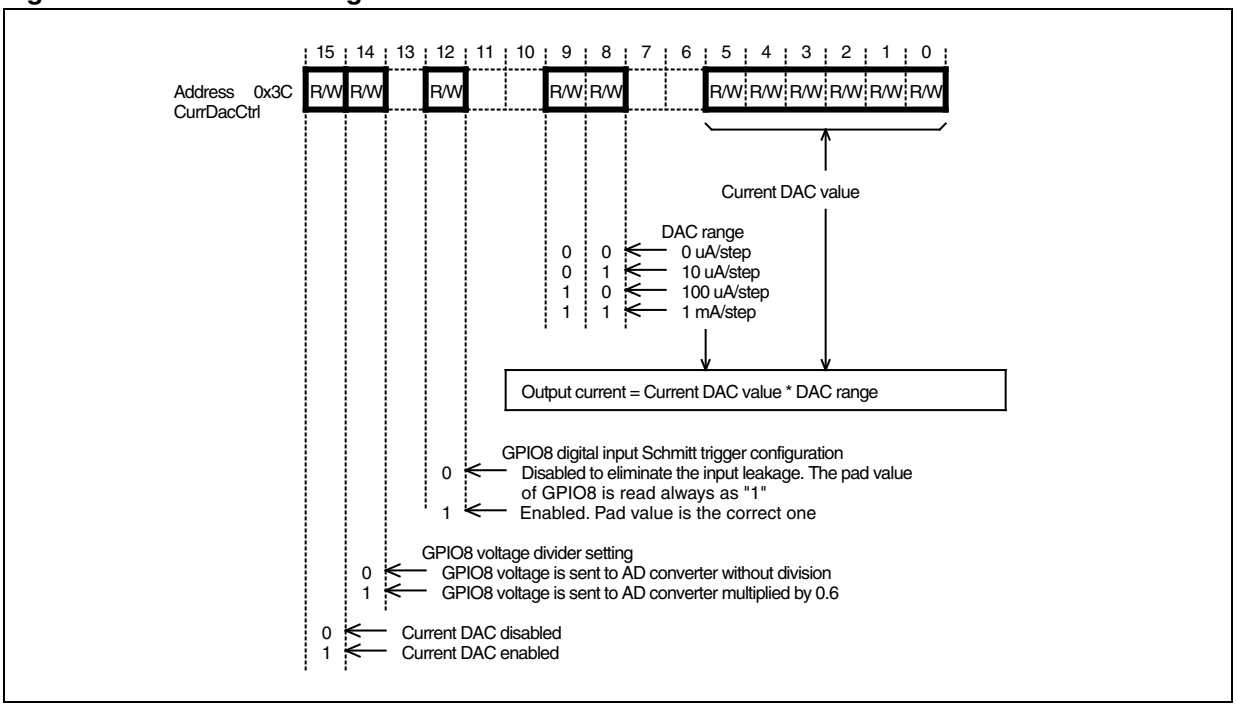
Figure 10. Core configuration registers



Note: If Aux regulators 1, 2 or 3 are system regulators and they are not connected to L6460's bridges, then their regulation loop will exits on Gpio5 (Aux1), Gpio12 (Aux2) or Gpio9/13 (Aux3)

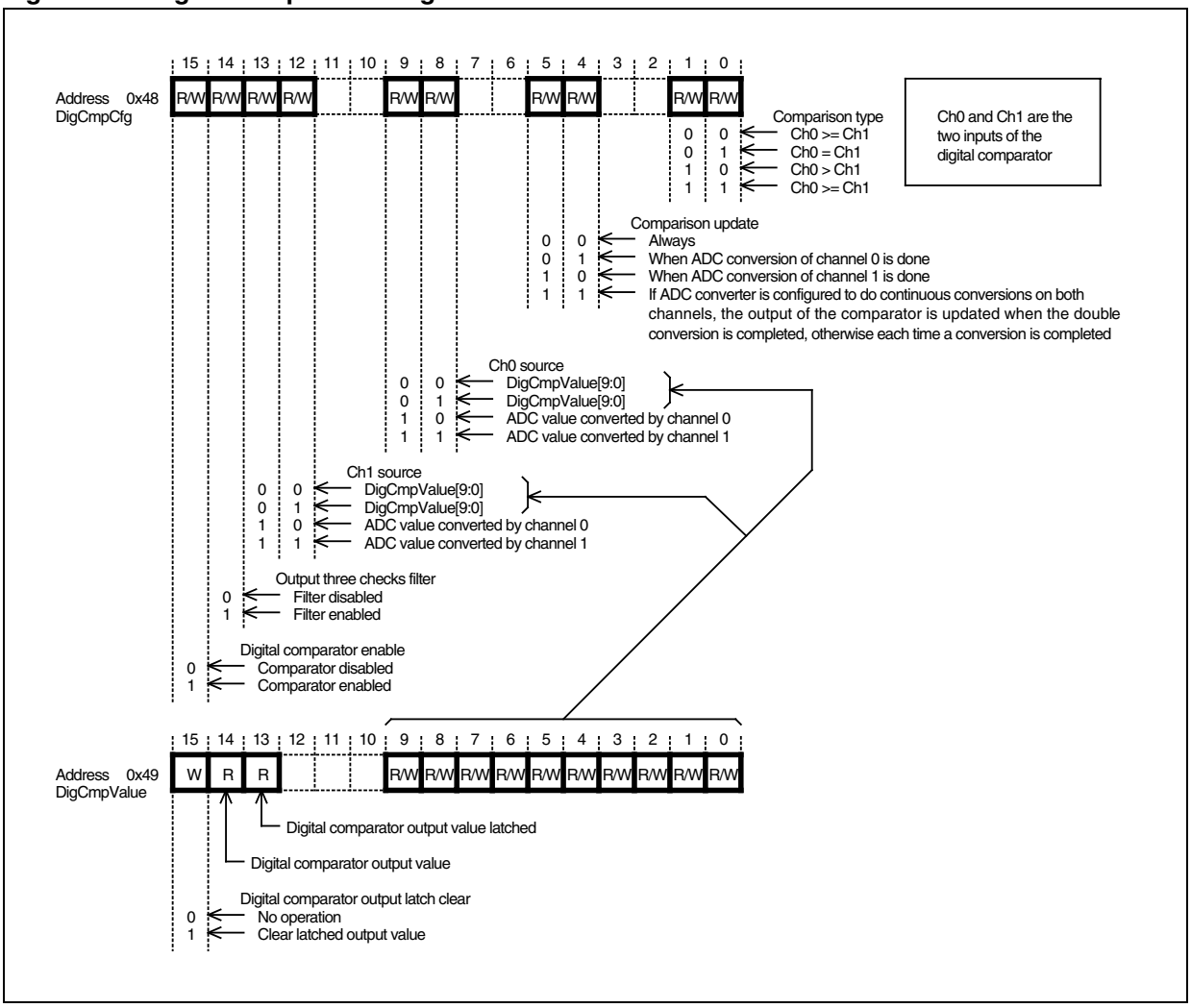
1.1.10 Current DAC registers

Figure 11. Current DAC registers



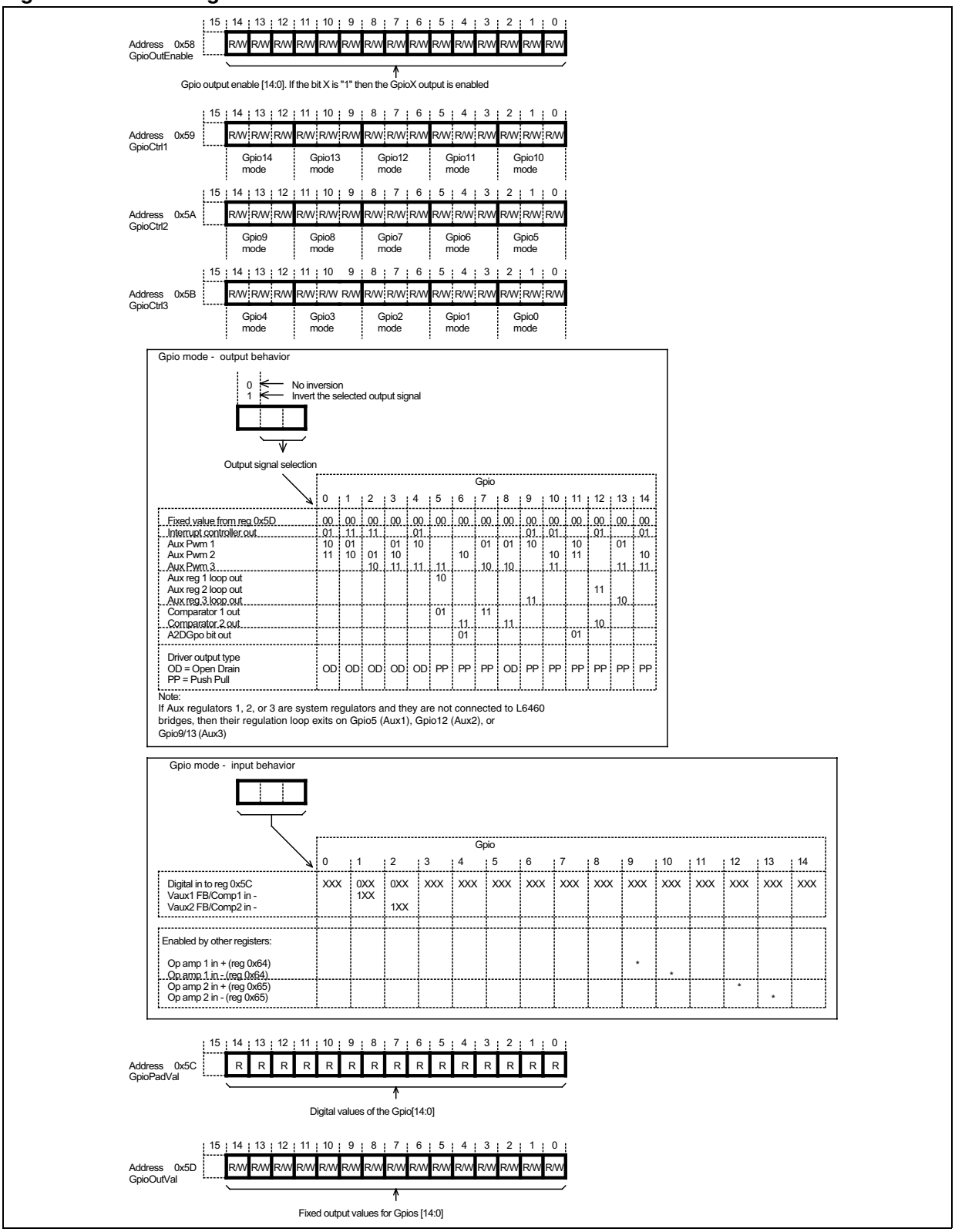
1.1.11 Digital comparators registers

Figure 12. Digital comparators registers



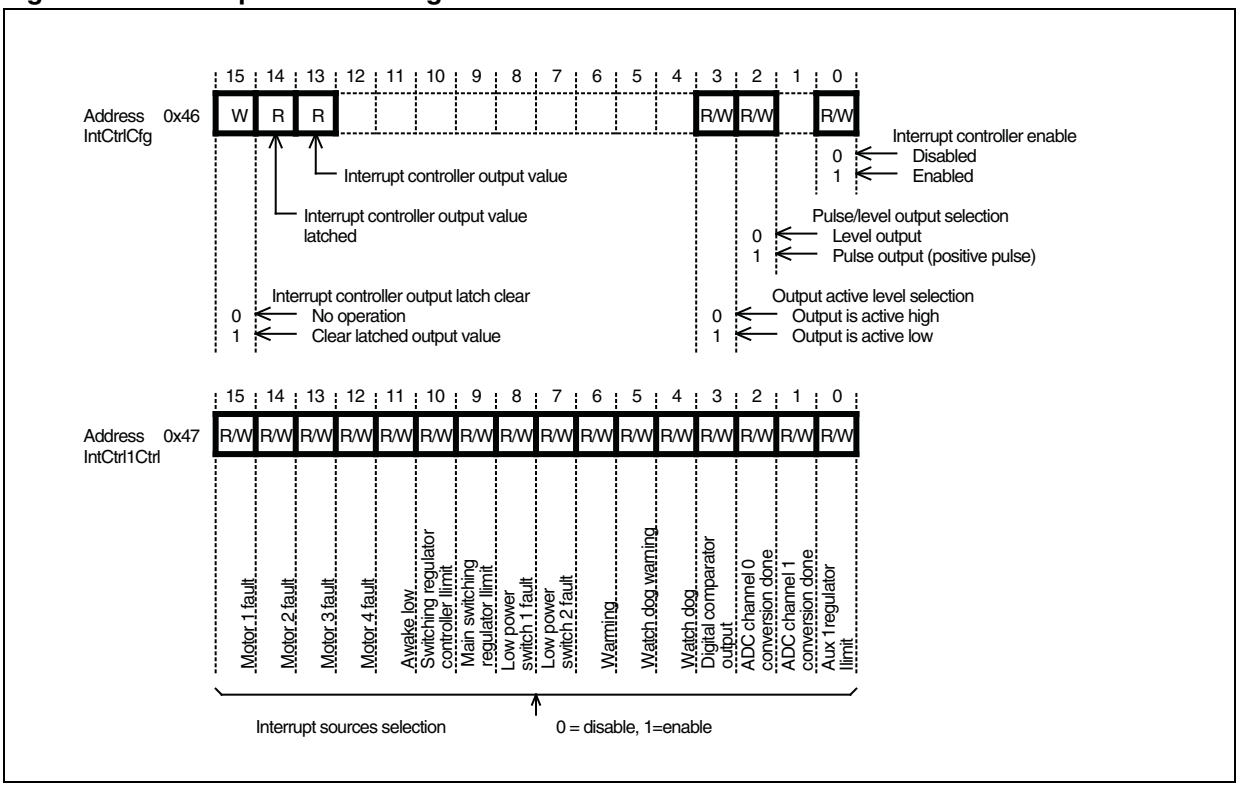
1.1.12 GPIOs registers

Figure 13. GPIOs registers



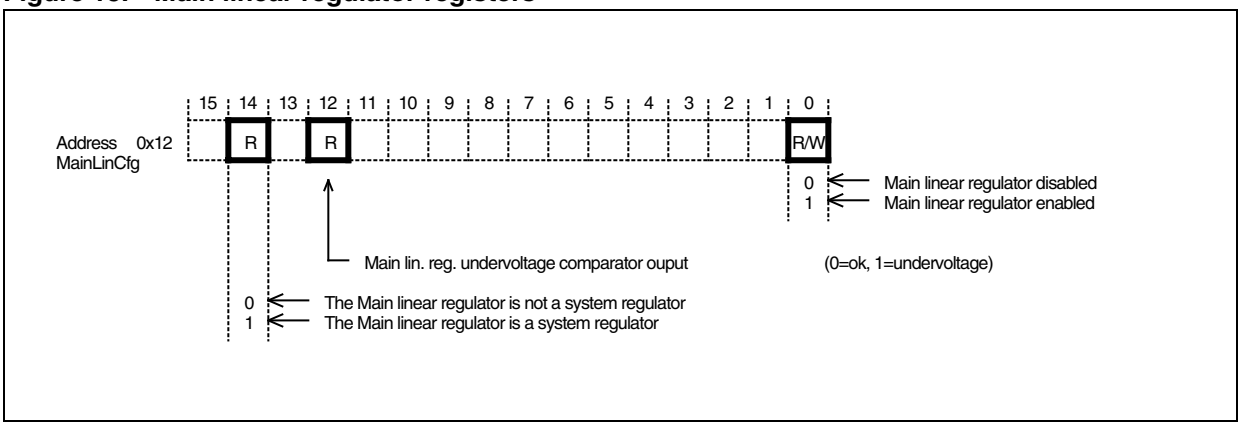
1.1.13 Interrupt controller registers

Figure 14. Interrupt controller registers



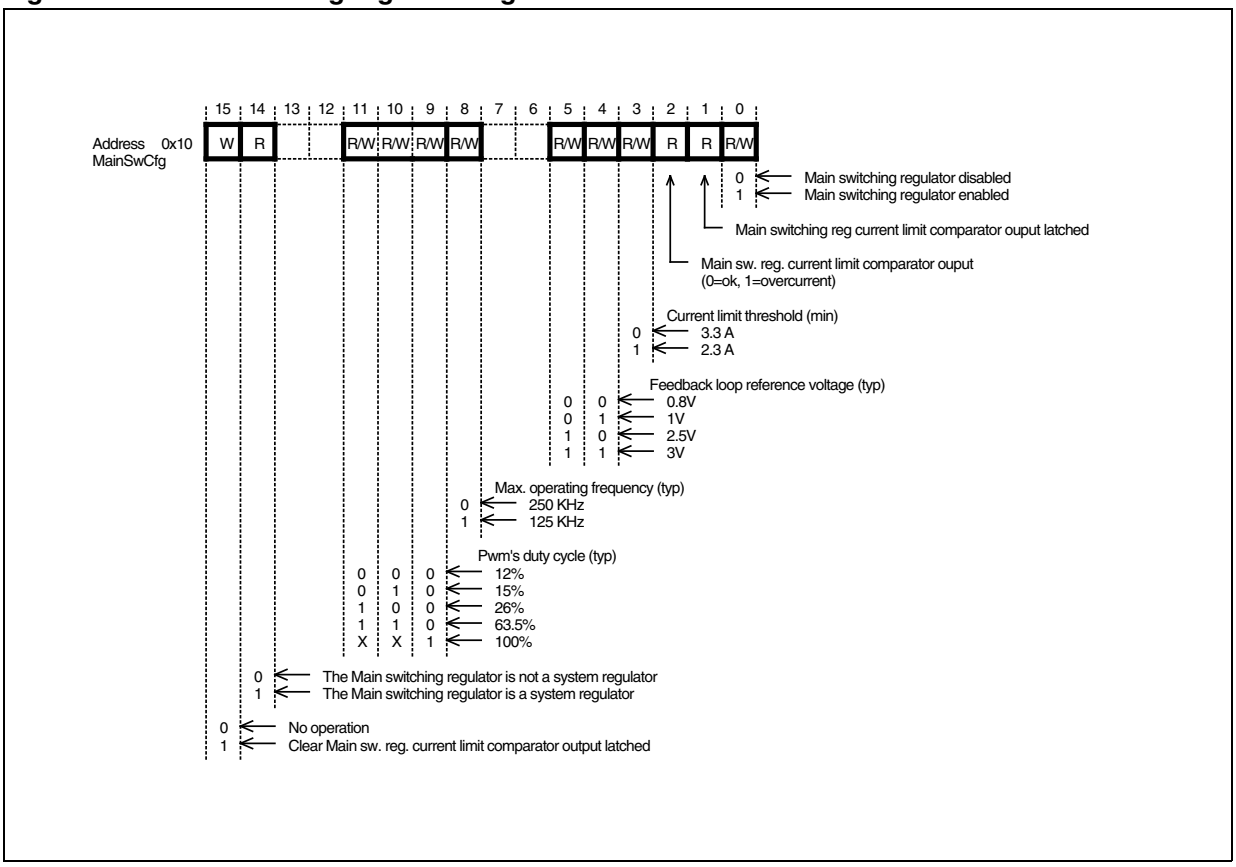
1.1.14 Main linear regulator registers

Figure 15. Main linear regulator registers



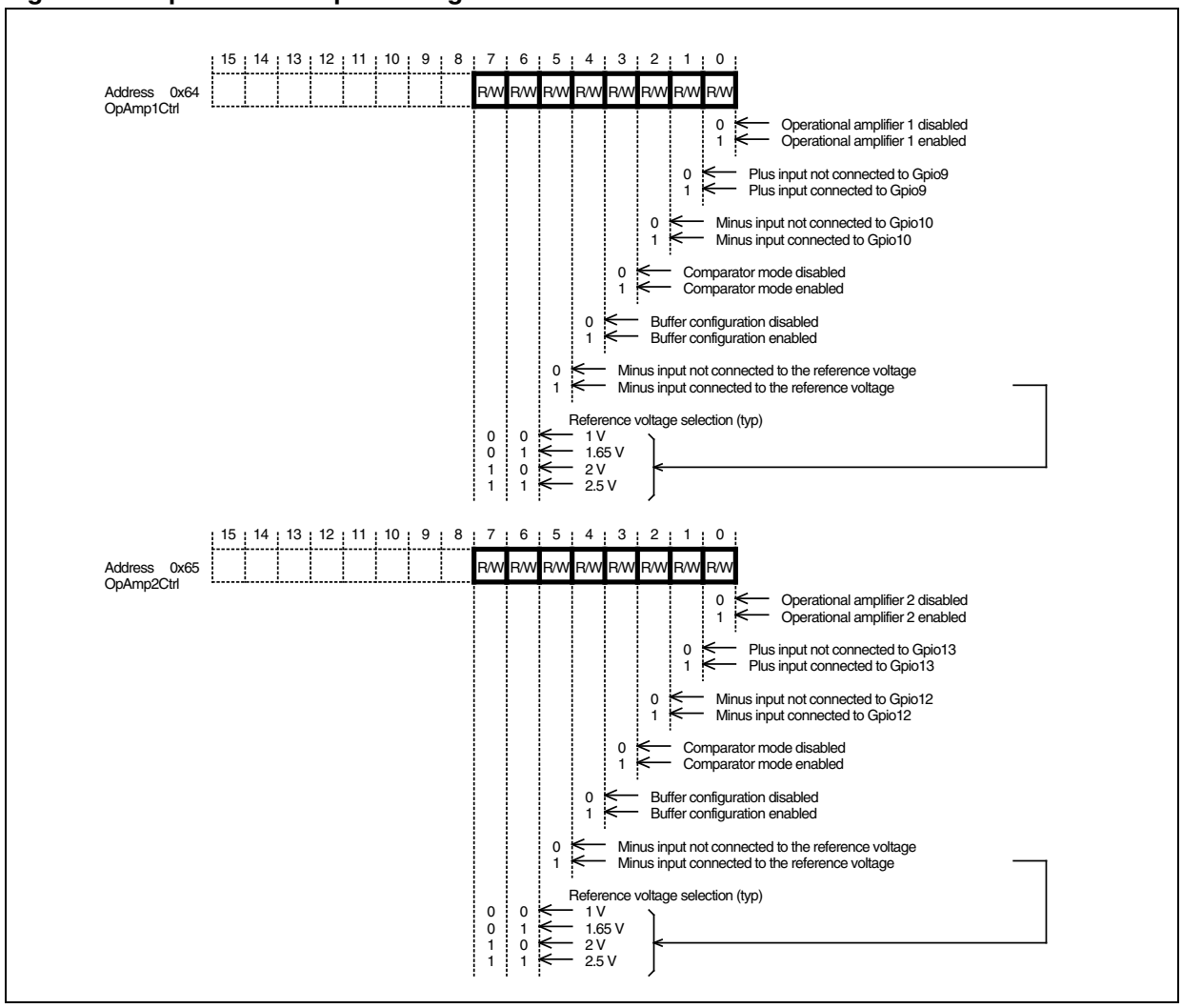
1.1.15 Main switching regulator registers

Figure 16. Main switching regulator registers



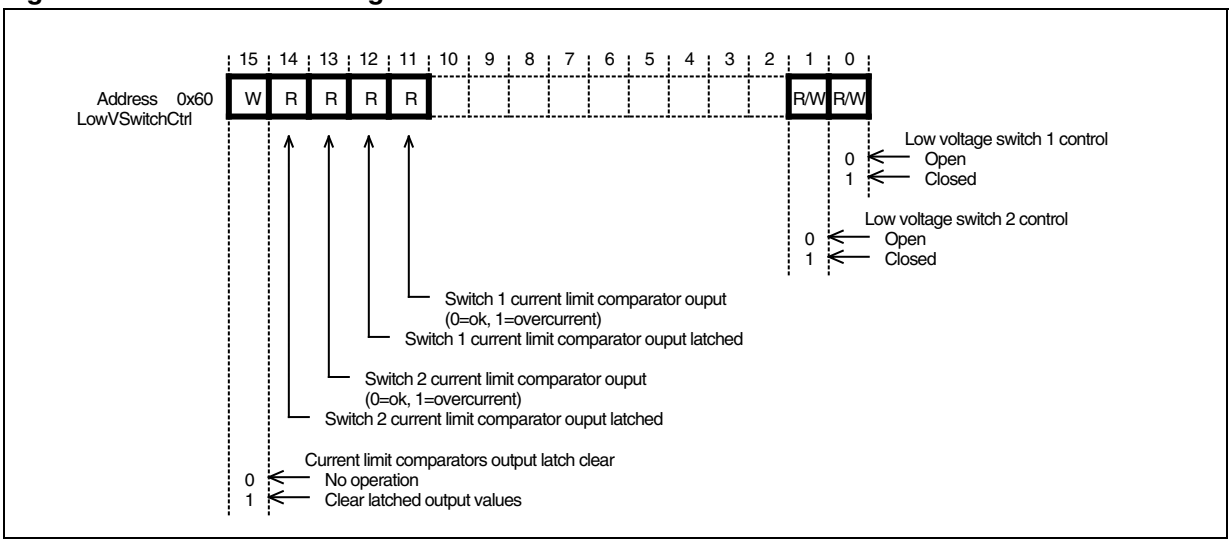
1.1.16 Operational amplifiers registers

Figure 17. Operational amplifiers registers



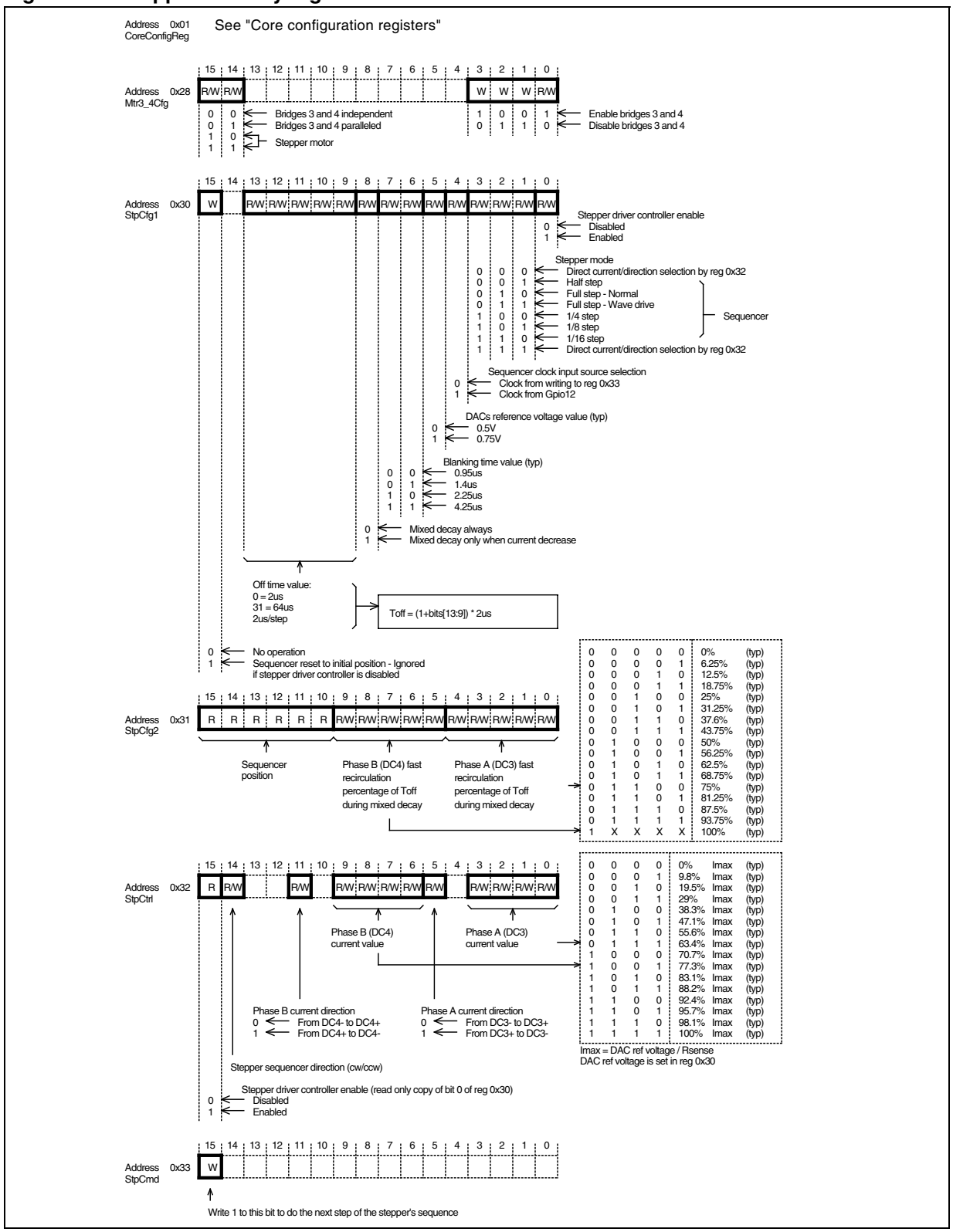
1.1.17 Pass switches registers

Figure 18. Pass switches registers



1.1.18 Stepper circuitry registers

Figure 19. Stepper circuitry registers



1.1.19 Supervisor & reset manager registers

Figure 20. Supervisor & reset manager registers first part

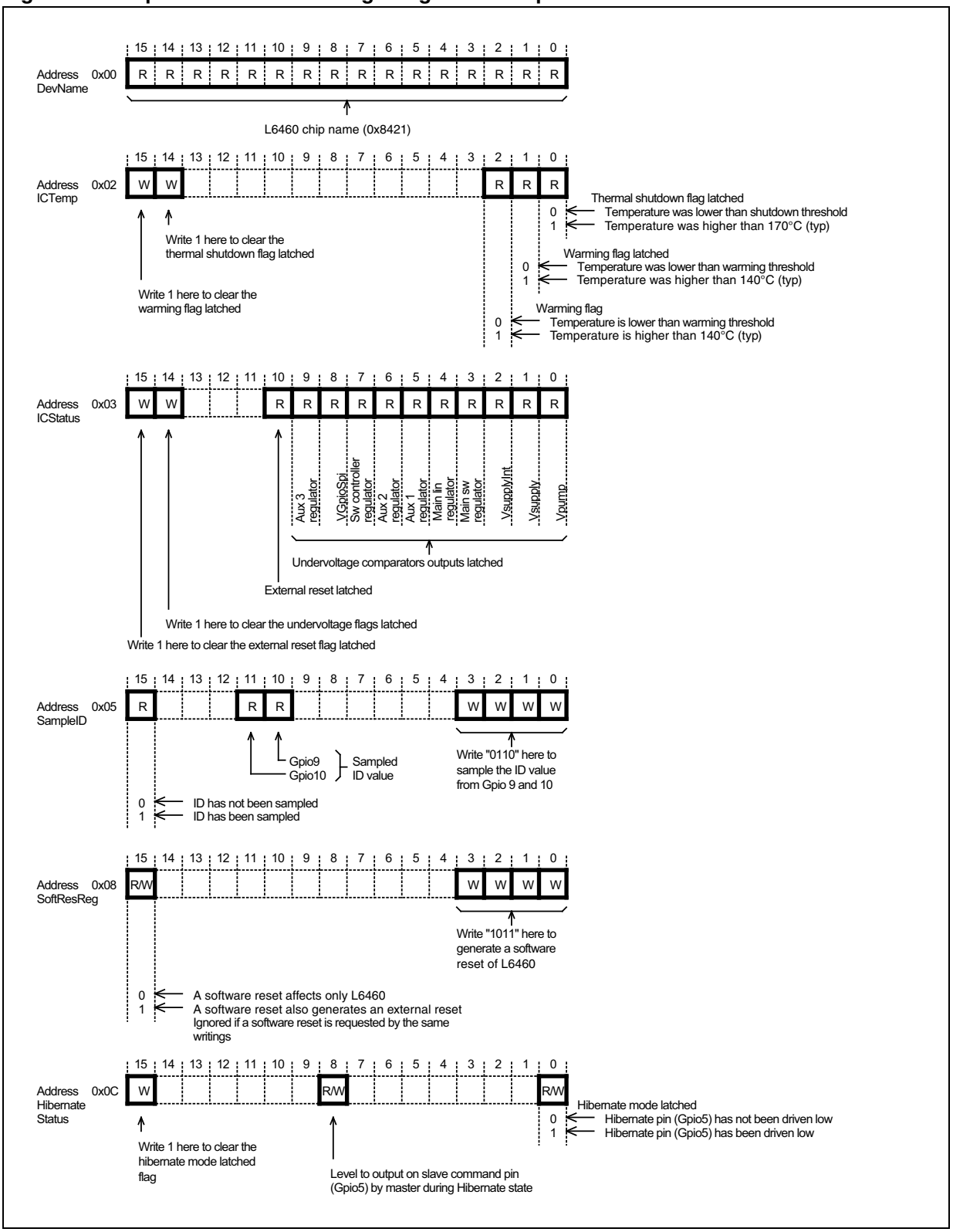
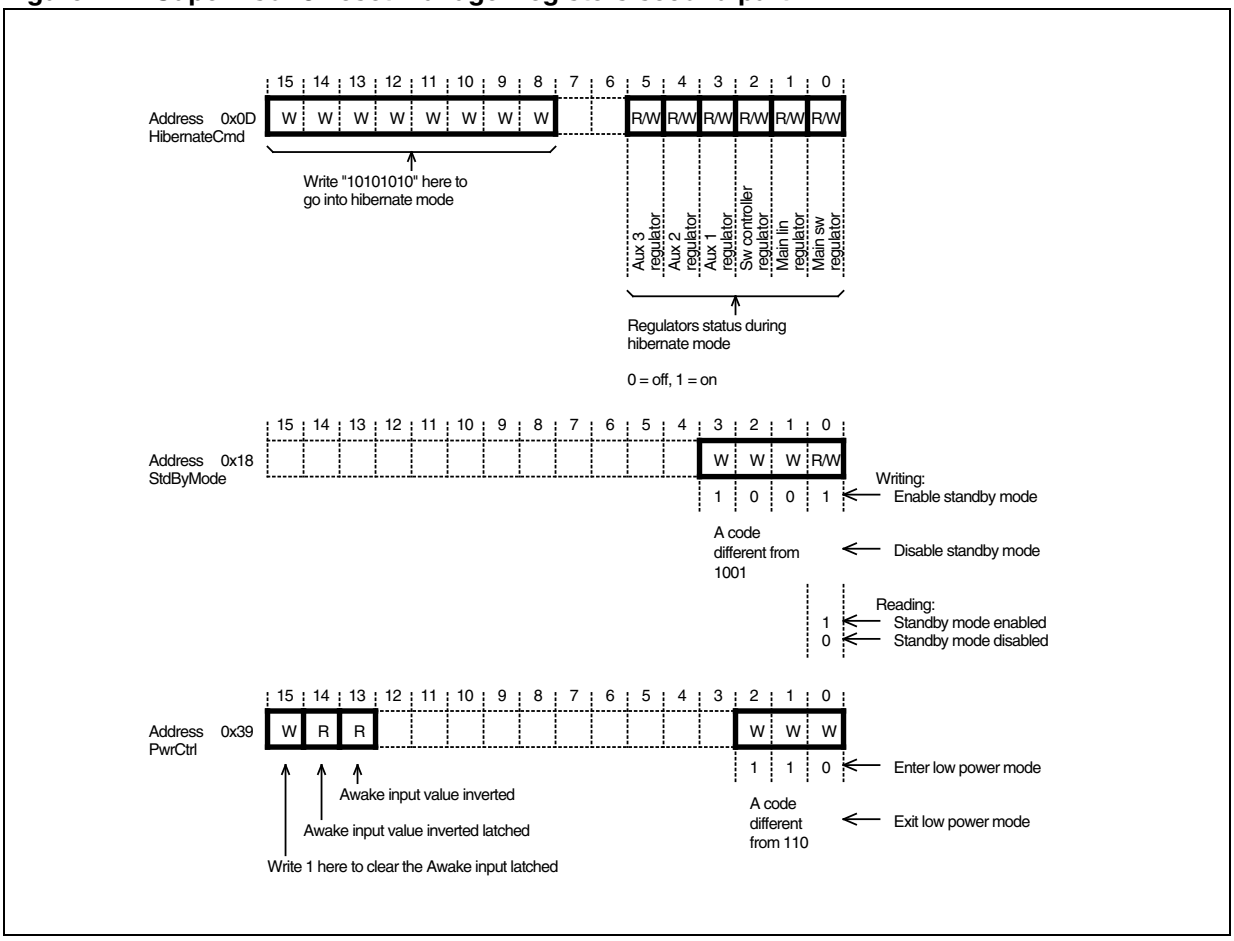
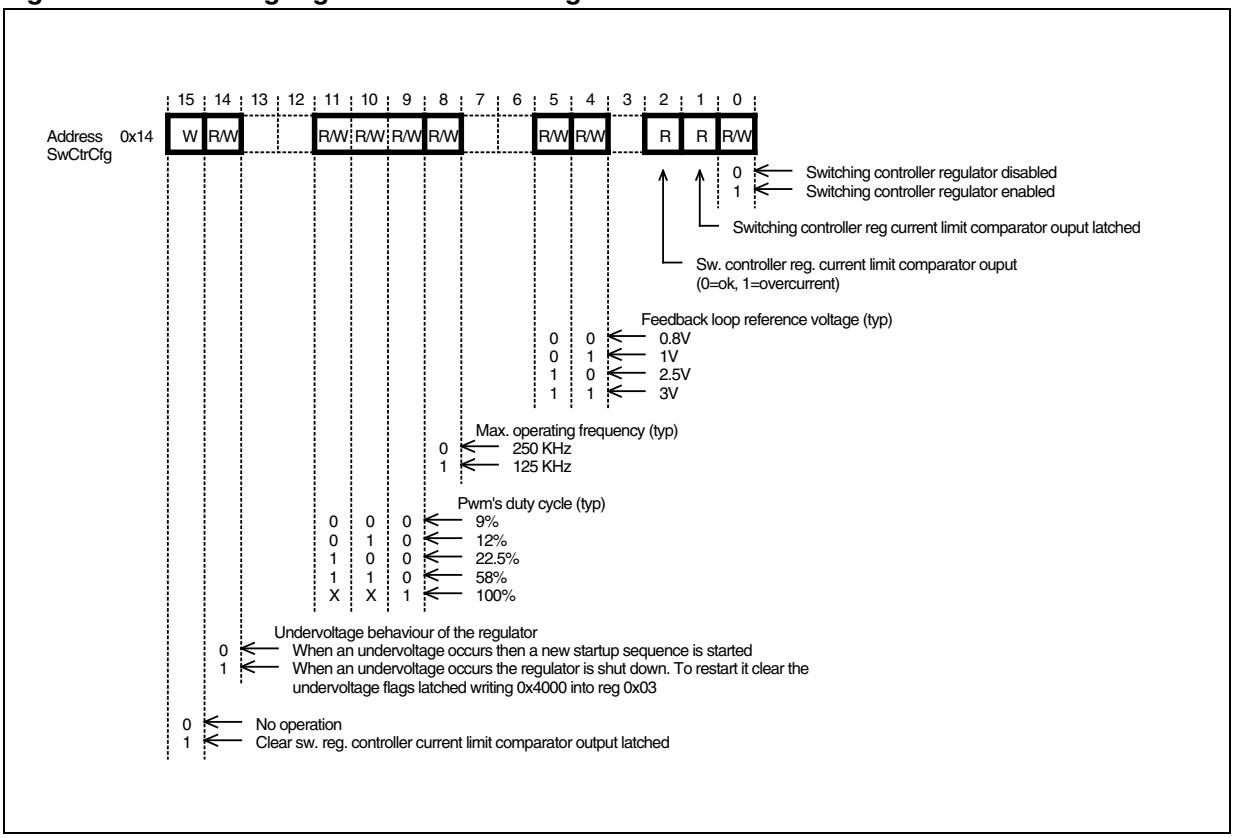


Figure 21. Supervisor & reset manager registers second part



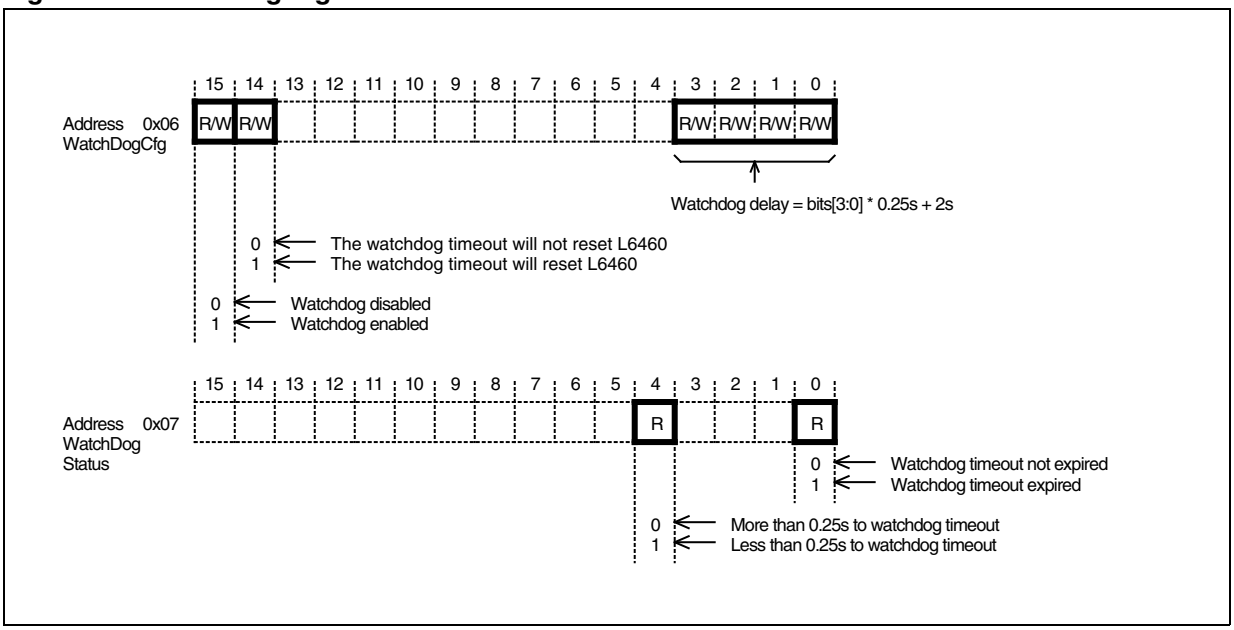
1.1.20 Switching regulator controller registers

Figure 22. Switching regulator controller registers



1.1.21 Watchdog registers

Figure 23. Watchdog registers



2 Registers description

Table 1. L6460 registers table

Address[6:0] (binary)	Name	Comment	Address[6:0] (binary)	Name	Comment
000_0000	DevName	Read Only	100_0000	AuxPwm1Ctrl	
000_0001	CoreConfigReg		100_0001	AuxPwm2Ctrl	
000_0010	ICTemp		100_0010	GpPwm3Base	
000_0011	ICStatus		100_0011	GpPwm3Ctrl	
000_0100			100_0100		
000_0101	SampleID		100_0101		
000_0110	WatchdogWatchdogCfg		100_0110	IntCtrlCfg	
000_0111	WatchdogStatus		100_0111	IntCtrlCtrl	
000_1000	SoftResReg		100_1000	DigCmpCfg	
000_1001			100_1001	DigCmpValue	
000_1010			100_1010		
000_1011			100_1011		
000_1100	HibernateStatus		100_1100		
000_1101	HibernateCmd		100_1101		
000_1110			100_1110		
000_1111	Mtr1_2PwrCtrl		100_1111		
001_0000	MainVSwCfg		101_0000	A2DControl	
001_0001			101_0001	A2DConfig1	
001_0010	MainlinCfg		101_0010	A2DResult1	
001_0011			101_0011	A2DConfig2	
001_0100	SwCtrCfg		101_0100	A2DResult2	
001_0101			101_0101		
001_0110			101_0110		
001_0111			101_0111		
001_1000	StdByMode		101_1000	GpioOutEnable	
001_1001			101_1001	GpioCtrl1	
001_1010			101_1010	GpioCtrl2	
001_1011			101_1011	GpioCtrl3	
001_1100			101_1100	GpioPadVal	Read only
001_1101			101_1101	GpioOutVal	
001_1110			101_1110		
001_1111			101_1111		

Table 1. L6460 registers table (continued)

Address[6:0] (binary)	Name	Comment	Address[6:0] (binary)	Name	Comment
010_0000	Mtrs1_2Cfg		110_0000	LowVSwitchCtrl	
010_0001	Mtr1Cfg		110_0001		
010_0010	Mtr1Ctrl		110_0010		
010_0011	Mtr1Limit		110_0011		
010_0100	Mtr2Cfg		110_0100	OpAmpCtrl1	
010_0101	Mtr2Ctrl		110_0101	OpAmpCtrl2	
010_0110	Mtr2Limit		110_0110		
010_0111			110_0111		
010_1000	Mtrs3_4Cfg		110_1000		
010_1001	Mtr3Cfg		110_1001		
010_1010	Mtr3Ctrl		110_1010		
010_1011	Mtr3ILimit		110_1011		
010_1100	Mtr4Cfg		110_1100		
010_1101	Mtr4Ctrl		110_1101		
010_1110	Mtr4ILimit		110_1110		
010_1111			110_1111		
011_0000	StpCfg1		111_0000		
011_0001	StpCfg2		111_0001		
011_0010	StpCtrl		111_0010		
011_0011	StpCmd		111_0011		
011_0100			111_0100		
011_0101	Aux1SwCfg		111_0101		
011_0110	Aux2SwCfg		111_0110		
011_0111	Aux3SwCfg1		111_0111		
011_1000	Aux3SwCfg2		111_1000		
011_1001	Power mode control		111_1001		
011_1010			111_1010		
011_1011			111_1011		
011_1100	CurrDacCtrl		111_1100		
011_1101			111_1101		
011_1110			111_1110		
011_1111			111_1111		

2.1 DevName: device name register [0x00]

Table 2. Device name register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
000_0000	DevName	15	1	Chip Name[15:0]	-
		14	0		-
		13	0		-
		12	0		-
		11	0		-
		10	1		-
		9	0		-
		8	0		-
		7	0		-
		6	0		-
		5	1		-
		4	0		-
		3	0		-
		2	0		-
		1	0		-
		0	1		-

Device name register bit description:

- Chip name[15:0] :
  - These bits are fixed and cannot be written. They are used to identify L6460 IC.

2.2 CoreConfigReg: core configuration register [0x01]

Table 3. Core configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
000_0001	CoreConfigReg	15	-	$V_{mainSwIsSys}$	
		14	-	$V_{SwCtrlIsSys}$	
		13	-	$V_{MainLinIsSys}$	
		12	-	$V_{loop1IsSys}$	
		11	-	$V_{loop1OnMtr3SideA}$	$V_{loop1OnMtr3SideA}$
		10	-	$V_{loop1OnMtr3SideB}$	Vloop1OnMtr3SideB
		9	0		
		8	-	$V_{loop2IsSys}$	
		7	-	$V_{loop2OnMtr3SideB}$	$V_{loop2OnMtr3SideB}$
		6	0		
		5	-	$V_{loop3IsSys}$	
		4	-	$V_{loop3OnMtr4}$	Vloop3OnMtr4
		3	0		
		2	0		
		1	-	Master	
		0	-	Slave	

1. The reset value of the bits not indicated on above table is strictly depending on start up configuration as follow:

Figure 24. Regulators startup order and type

		Gpio			Regulator's startup order and type (Sys=system)					
		0	3	4	Main sw	Main lin	Sw ctrl	Aux1	Aux2	Aux3
Basic		Z	X	X	4'	3' Sys		1' Sys	2' Sys	
Single	Bridge	0	0	0	1' Sys	2' Sys				
	Primary regulator	0	0	Z	2' Sys	2' Sys		1' Sys	3'	
	Regulators	0	0	1	1' Sys			2' Sys	3' Sys	
	Simple regulator	0	Z	0	4'	3' Sys		1' Sys	2' Sys	
	Bridge + VEXT	0	Z	Z	1' Sys	3' Sys	2' Sys			
	Secondary regulators	0	Z	1	1' Sys	3' Sys		2' Sys	2' Sys	
Master	Bridge	0	1	0	1' Sys	2' Sys				
	Primary regulator	0	1	Z	2' Sys	2' Sys		1' Sys	3'	
	Regulators	0	1	1	1' Sys			2' Sys	3' Sys	
	Simple regulator	1	0	0	4'	3' Sys		1' Sys	2' Sys	
	Bridge + VEXT	1	0	Z	1' Sys	3' Sys	2' Sys			
	Secondary regulators	1	0	1	1' Sys	3' Sys		2' Sys	2' Sys	
Slave	Bridge	1	Z	0	1' Sys	2' Sys				
	Primary regulator	1	Z	Z	2' Sys	2' Sys		1' Sys	3'	
	Regulators	1	Z	1	1' Sys			2' Sys	3' Sys	
	Simple regulator	1	1	0	4'	3' Sys		1' Sys	2' Sys	
	Bridge + VEXT	1	1	Z	1' Sys	3' Sys	2' Sys			
	Secondary regulators	1	1	1	1' Sys	3' Sys		2' Sys	2' Sys	

Core configuration register bit description:

- $V_{mainSwIsSys}$:
  - This bit is read only.
  - If it is read as “1” it means that main switching regulator is a system regulator.
- $V_{SwCtrlIsSys}$:
  - This bit is read only.
  - If it is read as “1” it means that the switching regulator controller is a system regulator.
- $V_{MainLinIsSys}$:
  - This bit is read only.
  - If it is read as “1” it means that linear main regulator is a system regulator.
- $V_{loop1IsSys}$:
  - This bit is read only.
  - If it is read as “1” it means that the first switching regulator control loop (Vloop1) included into bridge 3 is a system regulator.
- $V_{loop1OnMtr3SideA}$:
  - This bit is read only if Vloop1 is a system regulator. If Vloop1 is not a system regulator this bit can be written only if bridge 3 is disabled.
  - If it is written as “1” it means that Vloop1 will use the side A of bridge 3.
- $V_{loop1OnMtr3SideB}$:
  - This bit is read only if Vloop1 is a system regulator. If Vloop1 is not a system regulator this bit can be written only if bridge 3 is disabled.
  - If it is written as “1” it means that Vloop1 will use the side B of bridge 3.
  - If it is written as “1” also the bit Vloop1OnMtr3SideA will be considered as “1”.
- $V_{loop2IsSys}$:
  - This bit is read only.
  - If it is read as “1” it means that the second switching regulator control loop (Vloop2) included into bridge 3 is a system regulator.
- $V_{loop2OnMtr3SideB}$:
  - This bit is read only if Vloop2 is a system regulator. If V_{loop2} is not a system regulator this bit can be written only if bridge 3 is disabled.
  - If it is written as “1” it means that Vloop2 will use the side B of bridge 3 (Vloop2 can’t use the side A of bridge 3).
- $V_{loop3IsSys}$:
  - This bit is read only.
  - If it is read as “1” it means that the switching regulator control loop (Vloop3) included into bridge 4 is a system regulator.
- $V_{loop3OnMtr4}$:
  - This bit is writable when all the following conditions are met:
    - Vloop3 is not a system regulator (Vloop3IsSys=’0’).
    - bridges 3 & 4 enable = ‘0’.
    - Vloop3Enable =’0’.
  - When written to “1” Vloop3 uses bridges 3 & 4 as power stage.

- Master:
  - This bit is read only.
  - If it is read as “1” it means that L6460 is configured as master.
- Slave:
  - This bit is read only.
  - If it is read as “1” it means that L6460 is configured as slave.

2.3 ICTemp: IC temperatures register [0x02]

Table 4. Device name register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
000_0010	ICTemp	15	0		Clear warming latch
		14	0		Clear TSD latch
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		
		2	0	Warming	
		1	0	Warming latch(1)	
		0	0	TSD latch(1)	

1. Warming latch and TSD latch bits will be reset only by a power on reset event.

IC temperatures register bits description:

- Clear warming latch:
  - This is a write only bit. It will be always read as “0”.
  - If it is written as “1” it will clear warming latch bit.
- Clear TSD latch:
  - This is a write only bit. It will be always read as “0”.
  - If it is written as “1” it will clear TSD latch bit.
- Warming:
  - This is a read only bit: any writing to this bit will be ignored.
  - It will be “1” when the IC temperature is higher than the warming threshold. (See *Chapter 1.1.19*)
- Warming latch:
  - This is a read only bit: any writing to this bit will be ignored.
  - It will be “1” if the IC temperature has been higher than the warming threshold at least one time starting from the last register reset. (See *Chapter 1.1.19*)
- TSD latch:
  - This is a read only bit: any writing to this bit will be ignored.
  - It will be “1” if the IC temperature has been higher than the TSD threshold at least one time starting from the last register reset. (See *Chapter 1.1.19*)

2.4 ICStatus: IC statuses register [0x03]

Table 5. IC statuses register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
000_0011	ICStatus	15	0		ClrExtRstLth
		14	0		ClrUVLOLth
		13	0		
		12	0		
		11	0		
		10	0	ExtRstLth	
		9	0	$V_{loop3UvloLth}$	
		8	0	$V_{GpioSPiUvloLth}$	
		7	0	SwCtrUvloLth	
		6	0	Aux2SwUvloLth	
		5	0	Aux1SwUvloLth	
		4	0	$V_{mainLinUvloLth}$	
		3	0	$V_{MainSwUVLOLth}$	
		2	0	$V_{SupplyIntUVLOLth}$	
		1	0	SupplyUvloLth	
		0	0	$V_{PumpUVLOLth}$	

Note: When multiple UVLOs of same or different system regulator happen, only the first one is latched.
When one of the UVLOs latched bits of a system regulator is set, no other system regulator UVLO latched bit will be set.
All latched bits in this register will be reset only by a power on reset event.

IC statuses register bits description:

- ClrExtRstLth:
  - If it is written as “1” it will clear ExtRstLth bit.
- ClrUVLOLth:
  - If it is written as “1” it will clear all UVLO latch bits.
- ExtRstLth:
  - If it is read as “1”, it means that the last reset event was caused by an external reset.
- $V_{loop3UvloLth}$:
  - This bit represents the latched output of Vloop3 UVLO circuit.
- $V_{gpioSpiUvloLth}$:
  - This bit represents the latched output of VGPIOSPI UVLO circuit.
- SwCtrUvloLth:
  - This bit represents the latched output of switching controller UVLO circuit.
- Aux2SwUvloLth:
  - This bit represents the latched output of auxiliary switching regulator 2 UVLO circuit.
- Aux1SwUvloLth:
  - This bit represents the latched output of auxiliary switching regulator 1 UVLO circuit.
- Main linear UVLO latch:
  - This bit represents the latched output of main linear regulator UVLO circuit.
- $V_{MainSwUVLOLth}$:
  - This bit represents the latched output of main switching regulator UVLO circuit.
- SupplyIntUVLOLth:
  - This bit represents the latched output of supplyint UVLO circuit.
- SupplyUVLOLth:
  - This bit represents the latched output of supply UVLO circuit.
- $V_{PumpUVLOLth}$:
  - This bit represents the latched output of charge pump UVLO circuit.

2.5 SampleID: chip ID sample register [0x05]

Table 6. ID sample register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
000_0101	SampleID	15	0	EnID	
		14	0		
		13	0		
		12	0		
		11	0	ID[1]	
		10	0	ID[0]	
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		SampleID[3]
		2	0		SampleID[2]
		1	0		SampleID[1]
		0	0		SampleID[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering power down mode.

Chip ID sample register bits description:

- EnID:
  - This bit is read only.
  - Writing sampleID[3:0]=B”0110” will cause EnID to be read as “1”.
- SampleID[3:0]:
  - Writing SampleID[3:0]=B”0110” will cause L6460 to sample ID value from Gpio9 and Gpio10: starting from that moment L6460 will accept only SPI commands containing the sampled ID in the IC address field. (See *Chapter 1.1.19*).
- ID[1:0]:
  - These bits are read only.
  - They represent the sampled value of Gpio9 (ID[0]) and Gpio10 (ID[1]).

2.6 WatchdogCfg: watchdog configuration register [0x06]

Table 7. Watchdog configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
000_0110	WatchdogCfg	15	0	WDEnable	WDEnable
		14	0	WDEnnRst	WDEnnRst
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	1	WDDelay[3]	WDDelay[3]
		2	1	WDDelay[2]	WDDelay[2]
		1	1	WDDelay[1]	WDDelay[1]
		0	1	WDDelay[0]	WDDelay[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering power down mode.

Watchdog configuration register bits description:

- WDEnable:
  - If this bit is written to “1”, watchdog is enabled.
- WDEnnRst:
  - If this bit is written to “1”, watchdog timeout event will cause L6460 nRESET.
- WDDelay[3:0]:
  - These bits set the watchdog timeout interval: 4sec+0.25sec*WDDelay. (See *Chapter 1.1.21*).
  - The values written in these bits are passed to the watchdog delay circuit only in the moment when ClrWDog bit is written to “1” in the 0x07-WatchdogStatus register.

2.7 WatchDogStatus: watchdog status register [0x07]

Table 8. Watchdog status register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
000_0110	WatchDogStatus	15	0		ClrWDog
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0	WDWarning	
		2	0		
		1	0		
		0	0	WDTimeOut	

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering power down mode.
   - Software reset command in the 0x08-SoftResReg register.

Watchdog status register bits description:

- ClrWDog:
  - This bit is write only.
  - This bit is used to service watchdog circuit. The watchdog timer is reset by writing a “1”.
- WDWarning:
  - This bit is read only.
  - It represents the warning signal status of watchdog circuit.
- WDTimeOut:
  - This bit is read only.
  - It represents the timeout signal status of watchdog circuit.

2.8 SoftResReg: software reset register [0x08]

Table 9. Software reset register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
000_1000	SoftResReg	15	1	EnExtSoftRst	EnExtSoftRst
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		SoftRes[3]
		2	0		SoftRes[2]
		1	0		SoftRes[1]
		0	0		SoftRes[0]

Software reset register bits description:

- EnExtSoftRst:
  - This bit enables the SoftReset command to cause an external reset too.
  - The writing of this bit is accepted only if the customer is not requiring a SoftReset in the same write command.
- SoftRes[3:0]:
  - These bits are write only.
  - Writing SoftRes[3:0]= B“1011” will act similarly to nRESET and therefore it disables the same L6460 circuits disabled by nRESET. (See *Chapter 1.1.19*).
  - Any writing of SoftRes[3:0] different from B“1011” will be ignored.

2.9 HibernateStatus: hibernate status register [0x08 0x0C]

Table 10. Hibernate status register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
000_1000	HibernateStatus	15	0	ClrHibLth	
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	1	HibSlaveState	HibSlaveState
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		
		2	0		
		1	0		
		0	0	HibModeLth	HibModeLth

Hibernate status register bits description:

- ClrHibLth:
  - This bit is write only.
  - Writing a logic level “1” into this bit will clear HibModeLth.
- HibSlaveState:
  - This bit decides the status in which L6460 has to force the slave command pin (GPIO5 output in master device) when entering hibernate state.
- HibModeLth:
  - This bit indicates the hibernate input pin (GPIO5 pin in slave device) has been forced low.

2.10 HibernateCmd: hibernate command register [0x0D]

Table 11. Hibernate command register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
000_1101	HibernateCmd	15	0		EnHibMode[7]
		14	0		EnHibMode[6]
		13	0		EnHibMode[5]
		12	0		EnHibMode[4]
		11	0		EnHibMode[3]
		10	0		EnHibMode[2]
		9	0		EnHibMode[1]
		8	0		EnHibMode[0]
		7	0		
		6	0		
		5	-	HibEnVloop3	HibEnVloop3
		4	-	HibEnVloop2	HibEnVloop2
		3	-	HibEnVloop1	HibEnVloop1
		2	-	HibEnSwCtrl	HibEnSwCtrl
		1	-	HibEnVMainLin	HibEnVMainLin
		0	-	HibEnVMainSw	HibEnVMainSw

Hibernate command register bits description:

- EnHibMode[7:0]:
  - These are write only bits.
  - Writing these bits with “10101010” enables the hibernate mode; all other values will cause the whole write operation to be ignored by this register.
- HibEnVloop3:
  - The reset value of this bit depends on L6460 startup configuration and reflects the status of Vloop3 regulator. This bit decides the status of AUX3 regulator in hibernate mode.
  - During normal operation this bit reflects the status of Vloop3.
- HibEnVloop2:
  - The reset value of this bit depends on L6460 startup configuration and reflects the status of Vloop2 regulator. This bit decides the status of AUX2 regulator in hibernate mode.
  - During normal operation this bit reflects the status of Vloop2.
- HibEnVloop1:
  - The reset value of this bit depends on L6460 startup configuration and reflects the status of Vloop1 regulator. This bit decides the status of AUX1 regulator in hibernate mode.
  - During normal operation this bit reflects the status of Vloop1.
- HibEnSwCtrl:
  - The reset value of this bit depends on L6460 startup configuration and reflects the status of switching controller regulator. this bit decides the status of switching controller regulator in hibernate mode.
  - During normal operation this bit reflects the status of switching controller.
- HibEnVMainLin:
  - The reset value of this bit depends on L6460 startup configuration and reflects the status of main linear regulator. This bit decides the status of main linear regulator in hibernate mode.
  - During normal operation this bit reflects the status of main linear regulator.
- HibEnVMainSw:
  - The reset value of this bit depends on L6460 startup configuration and reflects the status of main switching regulator. This bit decides the status of main switching regulator in hibernate mode.
  - during normal operation this bit reflects the status of main switching regulator.

2.11 Mtr1_2PwrCtrl: motor 1 & 2 power control register [0x0F]

Table 12. Motor 1 & 2 power control register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
000_1111	Mtr1_2PwrCtrl	15	0		
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		
		2	0		
		1	0		
		0	0	Mtr1_2Off	Mtr1_2Off

Motor 1 & 2 power control register bits description:

- Mtr1_2Off:
  - When set to 1 the biasing of H bridge drivers 1 and 2 is removed.
  - Writes of 1 into this bit are only accepted when EnMtr12 is set to 0.

2.12 MainSwCfg: main switching configuration register [0x10]

Table 13. Main switching configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
001_0000	MainSwCfg	15	0		ClrMainSwIlimLth
		14		$V_{MainSwIsSys}$	
		13	0		
		12		$V_{mainSwUvlo}$	
		11	0	$V_{mainSwSelPWM[1]}$	$V_{mainSwSelPWM[1]}$
		10	1	$V_{mainSwSelPWM\ [0]}$	$V_{mainSwSelPWM[0]}$
		9		$V_{MainSwOneHundredDuty}$	$V_{MainSwOneHundredDuty}$
		8	0	Freq_div_2	Freq_div_2
		7	0		
		6	0		
		5	0	SelFBRef[1]	SelFBRef[1]
		4	1	SelFBRef[0]	SelFBRef[0]
		3	0	SelIlimit	SelIlimit
		2	0	MainSwIlimit	
		1	0	MainSwIlimitLth	
		0	1	MainSwEnable	MainSwEnable

Main switching configuration register bits description:

- ClrMainSwIlimLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear MainSwIlimitLth bit.
- $V_{MainSwIsSys}$:
  - This bit is read only.
  - If this bit is read as “1” it means that main switching regulator is a system regulator.
- $V_{mainSwUvlo}$:
  - This bit is read only.
  - It represents the main switching UVLO signal status.
- $V_{mainSwSelPWM[1:0]}$:
  - These bits allow the selection of the duty cycle used by main switching regulator.
- $V_{mainSw\ OneHundredDuty}$:
  - When this bit is written to “1”, main switching regulator will use 100% duty cycle.
- $V_{MainSwFreqDiv2}$:
  - When this bit is written to “1”, main switching regulator will switch with a period doubled respect to the nominal one.
  - Any writing of this bit is ignored.
- SelFBRef[1:0]:
  - These bits allow the selection of the feedback reference voltage (VFBRef) used by main switching regulator.
- SelIlimit:
  - This bit allows the selection of the current limit range for main switching regulator.
- MainSwIlimit:
  - This bit is read only.
  - It represents the instantaneous main switching regulator current limit signal status.
- MainSwIlimitLth:
  - This bit is read only.
  - It represents the latched MainSwIlimit signal status.
- MainSwEnable:
  - This bit allows the enabling and disabling of main switching regulator. Particular care must be taken when disabling this regulator if it is a system regulator because it can cause unwanted system resets.

2.13 MainLinCfg: main linear regulator configuration register [0x12]

Table 14. Main linear regulator configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
001_0010	MainLinCfg	15	0	$V_{MainLinIsSys}$	
		14	0	0	
		13	0	$V_{mainLinUvlo}$	
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		
		2	0		
		1	0	MainLinEnable	MainLinEnable
		0	1	$V_{MainLinIsSys}$	

Main linear regulator configuration register bits description:

- $V_{MainLinIsSys}$:
  - This bit is read only.
  - If this bit is read as “1” it means that main linear regulator is a system regulator.
- $V_{mainLinUvlo}$:
  - This bit is write only.
  - It represents the main linear UVLO signal status.
- MainLinEnable:
  - This bit allows the enabling and disabling of main linear regulator. Particular care must be taken when disabling this regulator if it is a system regulator because it can cause unwanted system resets.

2.14 SwCtrCfg: switching regulator controller configuration register [0x14]

Table 15. Switching regulator controller configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
001_0100	SwCtrCfg	15		0	ClrSwCtrIlimLth
		14	0	SwCtrUvLthBhv	SwCtrUvLthBhv
		13	0		
		12		SwCtrUvlo	
		11	1	SelSwCtrPWM[1]	SelSwCtrPWM[1]
		10	0	SelSwCtrPWM[0]	SelSwCtrPWM[0]
		9		SwCtrOneHundredDuty	SwCtrOneHundredDuty
		8			
		7			
		6	0	SwCtrFreqDiv2	SwCtrFreqDiv2
		5	0		
		4	0	SelFBRef[1]	SelFBRef[1]
		3	0	SelFBRef[0]	SelFBRef[0]
		2	0		
		1	0	SwCtrIlimit	
		0	0	SWCtrIlmitLth	

Switching regulator controller configuration register bits description:

- ClrSwCtrIlimLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear SWCtrIlmitLth bit.
- SwCtrUvLthBhv:
  - Toggle between two different behaviors that the switching regulator controller can have with respect to its UVLO event.
    - When this bit is written to “0” the switching regulator controller restarts without any external action.
    - When this bit is written to “1” the switching regulator controller will not restart until the SwCtrUvloLth bit in 0x03-ICStatus register is cleared.
- SwCtrUvlo:
  - This bit is read only.
  - It represents the switching regulator controller UVLO signal status.
- SelSwCtrPWM[1:0]:
  - These bits allow the selection of the duty cycle used by switching regulator controller. (See *Chapter 1.1.20*).
- SwCtrOneHundredDuty:
  - When this bit is written to “1”, switching regulator controller will use 100% duty cycle.
- SwCtrFreqDiv2:
  - When this bit is written to “1”, switching regulator controller will switch with a period doubled respect to the nominal one.
  - Any writing of this bit is ignored.
- SelFBRef[1:0]:
  - These bits allow the selection of the feedback reference voltage (VFBRef) used by switching regulator controller. (See *Chapter 1.1.20*).
- SwCtrIlimit:
  - This bit is read only.
  - It represents the instantaneous switching regulator controller current limit signal status.
- SwCtrIlmitLth:
  - This bit is read only.
  - It represents the latched SwCtrIlimit signal status.
- SwCtrEnable:
  - This bit allows the enabling and disabling of switching regulator controller. Particular care must be taken when disabling this regulator if it is a system regulator because it can cause unwanted system resets.

2.15 StdByMode: stand by mode register [0x18]

Table 16. Standby mode register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
001_1000	StdByMode	15	0		
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		EnStdByMode[3]
		2	0		EnStdByMode[2]
		1	0		EnStdByMode[1]
		0	0	EnStdByMode	EnStdByMode[0]

Stand by mode register bits description:

- EnStdByMode[3:0]:
  - Writing EnStdByMode [3:0]= “1001” will enable standby mode.
  - Any writing of EnStdByMode[3:0] different from “1001” will cause L6460 to exit from stand-by mode.
  - If EnStdByMode is read as “1” it means that L6460 stand by mode is enabled otherwise it is disabled.

2.16 Mtrs1_2Cfg: motors 1 & 2 configuration register [0x20]

Table 17. Standby mode register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality(2)	
				Read	Write
010_0000	Mtrs1_2Cfg	15	0		
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		Mtr1_2_Enable[3]
		2	0		Mtr1_2_Enable[2]
		1	0		Mtr1_2_Enable[1]
		0	0	Mtr1_2_Enable	Mtr1_2_Enable[0]

1. Once this register is written for the first time, the only events that can reset it to default values making it writable again are:
   - Power on reset event
   - Entering in “low power mode”
2. This register is writable once so first time this register is written the values will be loaded, all subsequent writes will be ignored.

Motors 1 & 2 configuration register bits description:

- Mtr1_2_Parallel:
  - If this bit is written to “1”, bridge 1 and 2 will work in parallel. In that case only bridge 1 configuration bits are taken in account to configure the resulting bridge.
- Mtr1_2_Enable[3:0]
  - Writing Mtr1_2_Enable[3:0]=B”1001” will enable the bridge 1 and bridge2.
  - Writing Mtr1_2_Enable[3:0]=B”0110” will disable bridge 1 and bridge2.
  - All writing of Mtr1_2_Enable[3:0] bits different from B”0110” or B”1001” will be ignored.
  - If Mtr1_2_Enable is read as “1” it means that bridge 1 and bridge2 bridges are enabled otherwise they are disabled.

2.17 Mtr1Cfg: motor 1 configuration register [0x21]

Table 18. Motor 1 configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_0001	Mtr1Cfg	15	0	Mtr1Table[1]	Mtr1Table[1]
		14	0	Mtr1Table[0]	Mtr1Table[0]
		13	0		
		12	0		
		11	1	Mtr1IlimitOffTimeB[1]	Mtr1IlimitOffTimeB[1]
		10	1	Mtr1IlimitOffTimeB[0]	Mtr1IlimitOffTimeB[0]
		9	0	Mtr1SideBILimSel[1]	Mtr1SideBILimSel[1]
		8	0	Mtr1SideBILimSel[0]	Mtr1SideBILimSel[0]
		7	0	Mtr1SelPWMSideB[1]	Mtr1SelPWMSideB[1]
		6	0	Mtr1SelPWMSideB[0]	Mtr1SelPWMSideB[0]
		5	1	Mtr1IlimitOffTimeA[1]	Mtr1IlimitOffTimeA[1]
		4	1	Mtr1IlimitOffTimeA[0]	Mtr1IlimitOffTimeA[0]
		3	0	Mtr1SideAILimSel[1]	Mtr1SideAILimSel[1]
		2	0	Mtr1SideAILimSel[0]	Mtr1SideAILimSel[0]
		1	0	Mtr1SelPWMSideA[1]	Mtr1SelPWMSideA[1]
		0	0	Mtr1SelPWMSideA[0]	Mtr1SelPWMSideA[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.

Motor 1 configuration register bits description:

- Mtr1Table[1:0]:
  - These bits allow the selection of the bridge configuration for bridge 1. (See *Chapter 1.1.5*).
  - These bits can be written only when Mtr1_2Enable bit in 0x20-Mtrs1_2Cfg register is at “0”. Once that bit is set to logic “1” (thus enabling bridge 1 and bridge 2) all following writings of Mtr1Table[1:0] bits will be ignored.
- Mtr1IlimitOffTimeB[1:0]:
  - If bridge 1 is NOT used as a full bridge, these bits select the off time after a current limit condition has been detected for side B of the half bridge. (See *Chapter 1.1.5*).
  - If bridge 1 is configured as a full bridge these bits are ignored.
- Mtr1IlimitOffTimeA[1:0]:
  - If bridge 1 is NOT used as a full bridge, these bits select the off time after a current limit condition has been detected for side A of the half bridge. (See *Chapter 1.1.5*).
  - If bridge 1 is configured as a full bridge the value of these bits are used for both sides.
- Mtr1SideBILimSel[1:0]:
  - These bits allow the selection of the current limitation for bridge 1 side B. (See *Chapter 1.1.5*).
  - If bridge 1 is used as a full bridge these bits are ignored and Mtr1SideAILimSel[1:0] are used for both sides.
- Mtr1SideAILimSel[1:0]:
  - These bits allow the selection of the current limitation for bridge 1 side A. (See *Chapter 1.1.5*).
  - If bridge 1 is used as a full bridge these bits are used for both sides A and B.
- Mtr1SelPWMSideB[1:0]:
  - These bits allow the selection of the PWM for side B of bridge 1 (See *Chapter 1.1.5*).
  - If bridge 1 is used as a full bridge, these bits are ignored.
- Mtr1SelPWMSideA[1:0]:
  - These bits allow the selection of the PWM for side A of bridge 1 (See *Chapter 1.1.5*).
  - If bridge 1 is used as a full bridge, these bits are used for both sides.

2.18 Mtr1Ctrl: motor 1 control register [0x22]

Table 19. Motor 1 control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_0010	Mtr1Ctrl	15	0	Mtr1CtrlSideB	Mtr1CtrlSideB
		14	0	Mtr1CtrlSideA	Mtr1CtrlSideA
		13	0		
		12	0		
		11	0		
		10	0		
		9	0	Mtr1PwmValue[9]	Mtr1PwmValue[9]
		8	0	Mtr1PwmValue[8]	Mtr1PwmValue[8]
		7	0	Mtr1PwmValue[7]	Mtr1PwmValue[7]
		6	0	Mtr1PwmValue[6]	Mtr1PwmValue[6]
		5	0	Mtr1PwmValue[5]	Mtr1PwmValue[5]
		4	0	Mtr1PwmValue[4]	Mtr1PwmValue[4]
		3	0	Mtr1PwmValue[3]	Mtr1PwmValue[3]
		2	0	Mtr1PwmValue[2]	Mtr1PwmValue[2]
		1	0	Mtr1PwmValue[1]	Mtr1PwmValue[1]
		0	0	Mtr1PwmValue[0]	Mtr1PwmValue[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Motor 1 control register bits description:

- Mtr1CtrlSideB:
  - This bit allows the selection of the direction for bridge 1 Side B.
- Mtr1CtrlSideA:
  - This bit allows the selection of the direction for bridge 1 Side A.
- Mtr1PwmValue[9:0]:
  - These bits allow the selection of the duty cycle of internal PWM generator for bridge 1. The resulting PWM signal will be at high level for a duration equal to: Value/(512*Fosc) were value is the decimal conversion of the Mtr1PwmValue[9:0] binary value. Any value higher than 512 will be set to 512.

2.19 Mtr1Limit: motor 1 current limit register [0x23]

Table 20. Motor 1 current limit register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_0011	Mtr1Limit	15	0		ClrMtr1IlimitLth
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0	Mtr1SideBIlimitLth	
		3	0		
		2	0		
		1	0		
		0	0	Mtr1SideAIlimitLth	

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.

Motor 1 current limit register bits description:

- ClrMtr1IlimitLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear both Mtr1SideBIlimitLth and Mtr1SideAIlimitLth bit.
- Mtr1SideBIlimitLth:
  - This bit is read only (writing to this bit is ignored).
  - It represents the latched output of current limit comparator for side B of bridge 1.
- Mtr1SideAIlimitLth:
  - This bit is read only (writing to this bit is ignored).
  - It represents the latched output of current limit comparator for side A of bridge 1.

2.20 Mtr2Cfg: motor 2 configuration register [0x24]

Table 21. Motor 2 configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_0100	Mtr2Cfg	15	0	Mtr2Table[1]	Mtr2Table[1]
		14	0	Mtr2Table[0]	Mtr2Table[0]
		13	0		
		12	0		
		11	1	Mtr2IlimitOffTimeB[1]	Mtr2IlimitOffTimeB[1]
		10	1	Mtr2IlimitOffTimeB[0]	Mtr2IlimitOffTimeB[0]
		9	0	Mtr2SideBILimSel[1]	Mtr2SideBILimSel[1]
		8	0	Mtr2SideBILimSel[0]	Mtr2SideBILimSel[0]
		7	0	Mtr2SelPWMSideB[1]	Mtr2SelPWMSideB[1]
		6	0	Mtr2SelPWMSideB[0]	Mtr2SelPWMSideB[0]
		5	1	Mtr2IlimitOffTimeA[1]	Mtr2IlimitOffTimeA[1]
		4	1	Mtr2IlimitOffTimeA[0]	Mtr2IlimitOffTimeA[0]
		3	0	Mtr2SideAILimSel[1]	Mtr2SideAILimSel[1]
		2	0	Mtr2SideAILimSel[0]	Mtr2SideAILimSel[0]
		1	0	Mtr2SelPWMSideA[1]	Mtr2SelPWMSideA[1]
		0	0	Mtr2SelPWMSideA[0]	Mtr2SelPWMSideA[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - ~ Software reset command in the 0x08-SoftResReg register.

Motor 2 configuration register bits description:

- Mtr2Table[1:0]:
  - These bits allow the selection of the bridge configuration for bridge 2. (See *Chapter 1.1.6*).
  - These bits can be written only when Mtr1_2Enable bit in 0x20-Mtrs1_2Cfg register is at “0”. Once that bit is set to logic “1” (thus enabling bridge 1 and bridge 2) all following writings of Mtr2Table[1:0] bits will be ignored.
- Mtr2IlimitOffTimeB[1:0]:
  - If bridge 2 is NOT used as a full bridge, these bits select the off time after a current limit condition has been detected for side B of the half bridge. (See *Chapter 1.1.6*).
  - If bridge 2 is configured as a full bridge these bits are ignored.
- Mtr2IlimitOffTimeA[1:0]:
  - If bridge 2 is NOT used as a full bridge, these bits select the off time after a current limit condition has been detected for side A of the half bridge. (See *Chapter 1.1.6*).
  - If bridge 2 is configured as a full bridge the value of these bits are used for both sides.
- Mtr2SideBILimSel[1:0]:
  - These bits allow the selection of the current limitation for bridge 2 side B. (See *Chapter 1.1.6*).
  - If bridge 2 is used as a full bridge these bits are ignored and Mtr2SideAILimSel[1:0] are used for both sides.
- Mtr2SideAILimSel[1:0]:
  - These bits allow the selection of the current limitation for bridge 2 side A. (See *Chapter 1.1.6*).
  - If Bridge 2 is used as a full bridge these bits are used for both sides A and B.
- Mtr2SelPWMSideB[1:0]:
  - These bits allow the selection of the PWM for side B of bridge 2. (See *Chapter 1.1.6*).
  - If bridge 2 is used as a full bridge, these bits are ignored.
- Mtr2SelPWMSideA[1:0]:
  - These bits allow the selection of the PWM for side A of bridge 2. (See *Chapter 1.1.6*).
  - If bridge 2 is used as a full bridge, these bits are used for both sides.

2.21 Mtr2Ctrl: motor 2 control register [0x25]

Table 22. Motor 2 control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_0101	Mtr2Ctrl	15	0	Mtr2CtrlSideB	Mtr2CtrlSideB
		14	0	Mtr2CtrlSideA	Mtr2CtrlSideA
		13	0		
		12	0		
		11	0		
		10	0		
		9	0	Mtr2PwmValue[9]	Mtr2PwmValue[9]
		8	0	Mtr2PwmValue[8]	Mtr2PwmValue[8]
		7	0	Mtr2PwmValue[7]	Mtr2PwmValue[7]
		6	0	Mtr2PwmValue[6]	Mtr2PwmValue[6]
		5	0	Mtr2PwmValue[5]	Mtr2PwmValue[5]
		4	0	Mtr2PwmValue[4]	Mtr2PwmValue[4]
		3	0	Mtr2PwmValue[3]	Mtr2PwmValue[3]
		2	0	Mtr2PwmValue[2]	Mtr2PwmValue[2]
		1	0	Mtr2PwmValue[1]	Mtr2PwmValue[1]
		0	0	Mtr2PwmValue[0]	Mtr2PwmValue[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - ~ Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Motor 2 control register bits description:

- Mtr2CtrlSideB:
  - This bit allows the selection of the direction for bridge 2 side B.
- Mtr2CtrlSideA:
  - This bit allows the selection of the direction for bridge 2 side A.
- Mtr2PwmValue[9:0]:
  - These bits allow the selection of the duty cycle of internal PWM generator for bridge 2. The resulting PWM signal will be at high level for a duration equal to: Value/(512*Fosc) were value is the decimal conversion of the Mtr2PwmValue[9:0] binary value. Any value higher than 512 will be set to 512.

2.22 Mtr2Limit: motor 2 current limit register [0x26]

Table 23. Motor 2 current limit register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_0110	Mtr2Limit	15	0		ClrMtr2IlimitLth
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0	Mtr2SideBIlimitLth	
		3	0		
		2	0		
		1	0		
		0	0	Mtr2SideAIlimitLth	

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.

Motor 2 current limit register bits description:

- ClrMtr2IlimitLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear both Mtr2SideBIlimitLth and Mtr2SideAIlimitLth bit.
- Mtr2SideBIlimitLth:
  - This bit is read only (writing to this bit is ignored).
  - It represents the latched output of current limit comparator for side b of bridge 2.
- Mtr2SideAIlimitLth:
  - This bit is read only (writing to this bit is ignored).
  - It represents the latched output of current limit comparator for side a of bridge 2.

2.23 Mtr3_4Cfg: motors 3 & 4 configurations register [0x28]

Table 24. Motors 3 & 4 configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality(2)	
				Read	Write
010_1000	Mtr3_4Cfg	15	0	Mtr3_4CfgTable[1]	Mtr3_4CfgTable[1]
		14	0	Mtr3_4CfgTable[0]	Mtr3_4CfgTable[0]
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		Mtr3_4_Enable[3]
		2	0		Mtr3_4_Enable[2]
		1	0		Mtr3_4_Enable[1]
		0	0	Mtr3_4_Enable	Mtr3_4_Enable[0]

1. Once this register is written for the first time, the only events that can reset it to default values making it writable again are:
   - Power on reset event
   - Entering in “Low Power mode”
2. This register is writable once so first time this register is written the values will be loaded, all subsequent writes will be ignored.

Bridges 3 & 4 configuration register bits description:

- Mtr3_4CfgTable[1:0]:
  - These bits select among bridge 3 & 4 type of operation (stepper driver, parallel bridge, single bridges). (See *Chapter 1.1.7*).
- Mtr3_4_Enable[3:0]
  - Writing Mtr3_4_Enable[3:0]=B”1001” will enable the bridge 3 and bridge 4.
  - Writing Mtr3_4_Enable[3:0]=B”0110” will disable bridge 3 and bridge 4.
  - All writing of Mtr3_4_Enable[3:0] bits different from B”0110” or B”1001” will be ignored.
  - If Mtr3_4_Enable is read as “1” it means that bridge 3 and bridge 4 are enabled otherwise they are disabled.

2.24 Mtr3Cfg: motor 3 configuration register [0x29]

Table 25. Motor 3 configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_1001	Mtr3Cfg	15	0	Mtr3Table[1]	Mtr3Table[1]
		14	0	Mtr3Table[0]	Mtr3Table[0]
		13	0		
		12	0		
		11	1	Mtr3IlimitOffTimeB[1]	Mtr3IlimitOffTimeB[1]
		10	1	Mtr3IlimitOffTimeB[0]	Mtr3IlimitOffTimeB[0]
		9	0		
		8	0		
		7	0	Mtr3SelPWMSideB[1]	Mtr3SelPWMSideB[1]
		6	0	Mtr3SelPWMSideB[0]	Mtr3SelPWMSideB[0]
		5	1	Mtr3IlimitOffTimeA[1]	Mtr3IlimitOffTimeA[1]
		4	1	Mtr3IlimitOffTimeA[0]	Mtr3IlimitOffTimeA[0]
		3	0		
		2	0		
		1	0	Mtr3SelPWMSideA[1]	Mtr3SelPWMSideA[1]
		0	0	Mtr3SelPWMSideA[0]	Mtr3SelPWMSideA[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.

Motor 3 configuration register bits description:

- Mtr3Table[1:0]:
  - These bits allow the selection of the bridge configuration for bridge 3 when it is NOT used as regulator. (See *Chapter 1.1.7*).
  - These bits can be written only when Mtr3_4Enable bit in 0x28-Mtrs3_4Cfg register is at “0”. Once that bit is set to logic “1” (thus enabling bridge 3 and bridge 4) all following writings of Mtr3Table[1:0] bits will be ignored.
- Mtr3IlimitOffTimeB[1:0]:
  - If bridge 3 is NOT used as a full bridge, these bits select the off time after a current limit condition has been detected for side B of the half bridge. (See *Chapter 1.1.7*).
  - If bridge 3 is configured as a full bridge these bits are ignored.
- Mtr3IlimitOffTimeA[1:0]:
  - If bridge 3 is NOT used as a full bridge, these bits select the off time after a current limit condition has been detected for side a of the half bridge. (See *Chapter 1.1.7*).
  - If bridge 3 is configured as a full bridge the value of these bits are used for both sides.
- Mtr3SelPWMSideB[1:0]:
  - These bits allow the selection of the PWM for side B of bridge 3. (See *Chapter 1.1.7*).
  - If bridge 3 is used as a full bridge, these bits are ignored.
- Mtr3SelPWMSideA[1:0]:
  - These bits allow the selection of the PWM for side A of bridge 3. (See *Chapter 1.1.7*).
  - If bridge 3 is used as a full bridge, these bits are used for both sides.

2.25 Mtr3Ctrl: motor 3 control register [0x2A]

Table 26. Motor 3 control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_1010	Mtr3Ctrl	15	0	Mtr3CtrlSideB	Mtr3CtrlSideB
		14	0	Mtr3CtrlSideA	Mtr3CtrlSideA
		13	0		
		12	0		
		11	0		
		10	0		
		9	0	Mtr3PwmValue[9]	Mtr3PwmValue[9]
		8	0	Mtr3PwmValue[8]	Mtr3PwmValue[8]
		7	0	Mtr3PwmValue[7]	Mtr3PwmValue[7]
		6	0	Mtr3PwmValue[6]	Mtr3PwmValue[6]
		5	0	Mtr3PwmValue[5]	Mtr3PwmValue[5]
		4	0	Mtr3PwmValue[4]	Mtr3PwmValue[4]
		3	0	Mtr3PwmValue[3]	Mtr3PwmValue[3]
		2	0	Mtr3PwmValue[2]	Mtr3PwmValue[2]
		1	0	Mtr3PwmValue[1]	Mtr3PwmValue[1]
		0	0	Mtr3PwmValue[0]	Mtr3PwmValue[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Motor 3 control register bits description:

- Mtr3CtrlSideB:
  - This bit allows the selection of the direction for bridge 3 side B.
- Mtr3CtrlSideA:
  - This bit allows the selection of the direction for bridge 3 side A.
- Mtr3PwmValue[9:0]:
  - These bits allow the selection of the duty cycle of internal PWM generator for bridge 3. The resulting PWM signal will be at high level for a duration equal to: value/(512*Fosc) were value is the decimal conversion of the Mtr3PwmValue[9:0] binary value. Any value higher than 512 will be set to 512.

2.26 Mtr3Limit: motor 3 current limit register [0x2B]

Table 27. Motor 1 current limit register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_1011	Mtr3Limit	15	0		ClrMtr3IlimitLth
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0	Mtr3SideBIlimitLth	
		3	0		
		2	0		
		1	0		
		0	0	Mtr3SideAIlimitLth	

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.

Motor 3 current limit register bits description:

- ClrMtr3IlimitLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear both Mtr3SideBIlimitLth and Mtr3SideAIlimitLth bit.
- Mtr3SideBIlimitLth:
  - This bit is read only (writing to this bit is ignored).
  - It represents the latched output of current limit comparator for side b of bridge 3.
- Mtr3SideAIlimitLth:
  - This bit is read only (writing to this bit is ignored).
  - It represents the latched output of current limit comparator for side a of bridge 3.

2.27 Mtr4Cfg: motor 4 configuration register [0x2C]

Table 28. Motor 4 configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality(2)	
				Read	Write
010_1100	Mtr4Cfg	15	0	Mtr4Table[1]	Mtr4Table[1]
		14	0	Mtr4Table[0]	Mtr4Table[0]
		13	0		
		12	0		
		11	1	Mtr4IlimToffSideB[1]	Mtr4IlimToffSideB[1]
		10	1	Mtr4IlimToffSideB[0]	Mtr4IlimToffSideB[0]
		9	0		
		8	0		
		7	0	Mtr4SelPWMSideB[1]	Mtr4SelPWMSideB[1]
		6	0	Mtr4SelPWMSideB[0]	Mtr4SelPWMSideB[0]
		5	1	Mtr4IlimToffSideA[1]	Mtr4IlimToffSideA[1]
		4	1	Mtr4IlimToffSideA[0]	Mtr4IlimToffSideA[0]
		3	0		
		2	0		
		1	0	Mtr4SelPWMSideA[1]	Mtr4SelPWMSideA[1]
		0	0	Mtr4Table[1]	Mtr4Table[1]

1. This register is used as motor configuration when bridge 3 & 4 are used in parallel. This register is ignored when Mtr3_4CfgTable[1:0] bits indicates stepper operation for bridge 3 & 4
2. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.

Motor 4 configuration register bits description:

- Mtr4Table[1:0]:
  - These bits allow the selection of the bridge configuration for bridge 4 when it is NOT used as regulator. (See *Chapter 1.1.8*).
  - These bits can be written only when Mtr3_4Enable bit in 0x28-Mtrs3_4Cfg register is at “0”. Once that bit is set to logic “1” (thus enabling bridge 3 and bridge 4) all following writings of Mtr4Table[1:0] bits will be ignored.
- Mtr4IlimitOffTimeB[1:0]:
  - If bridge 4 is NOT used as a full bridge, these bits select the off time after a current limit condition has been detected for side B of the half bridge. (See *Chapter 1.1.8*).
  - If bridge 4 is configured as a full bridge these bits are ignored.
- Mtr4IlimitOffTimeA[1:0]:
  - If bridge 4 is NOT used as a full bridge, these bits select the off time after a current limit condition has been detected for side A of the half bridge. (See *Chapter 1.1.8*).
  - If bridge 4 is configured as a full bridge the value of these bits are used for both sides.
- Mtr4SelPWMSideB[1:0]:
  - These bits allow the selection of the PWM for side B of bridge 4. (See *Chapter 1.1.8*).
  - If bridge 4 is used as a full bridge, these bits are ignored.
- Mtr4SelPWMSideA[1:0]:
  - These bits allow the selection of the PWM for side A of bridge 4. (See *Chapter 1.1.8*).
  - If bridge 4 is used as a full bridge, these bits are used for both sides.

2.28 Mtr4Ctrl: motor 4 control register [0x2D]

Table 29. Motor 4 control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_1101	Mtr4Ctrl	15	0	Mtr4CtrlSideB	Mtr4CtrlSideB
		14	0	Mtr4CtrlSideA	Mtr4CtrlSideA
		13	0		
		12	0		
		11	0		
		10	0		
		9	0	Mtr4PwmValue[9]	Mtr4PwmValue[9]
		8	0	Mtr4PwmValue[8]	Mtr4PwmValue[8]
		7	0	Mtr4PwmValue[7]	Mtr4PwmValue[7]
		6	0	Mtr4PwmValue[6]	Mtr4PwmValue[6]
		5	0	Mtr4PwmValue[5]	Mtr4PwmValue[5]
		4	0	Mtr4PwmValue[4]	Mtr4PwmValue[4]
		3	0	Mtr4PwmValue[3]	Mtr4PwmValue[3]
		2	0	Mtr4PwmValue[2]	Mtr4PwmValue[2]
		1	0	Mtr4PwmValue[1]	Mtr4PwmValue[1]
		0	0	Mtr4PwmValue[0]	Mtr4PwmValue[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Bridge 4 control register bits description:

- Mtr4CtrlSideB:
  - This bit allows the selection of the direction for bridge 4 side B.
- Mtr4CtrlSideA:
  - This bit allows the selection of the direction for bridge 4 side A.
- Mtr4PwmValue[9:0]:
  - These bits allow the selection of the duty cycle of internal PWM generator for bridge 4. The resulting PWM signal will be at high level for a duration equal to: value/(512*Fosc) were value is the decimal conversion of the Mtr4PwmValue[9:0] binary value. Any value higher than 512 will be set to 512.

2.29 Mtr4Limit: motor 4 current limit register [0x2E]

Table 30. Motor 4 current limit register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
010_1110	Mtr4Limit	15	0		ClrMtr4IlimitLth
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0	Mtr4SideBIlimitLth	
		3	0		
		2	0		
		1	0		
		0	0	Mtr4SideAIlimitLth	

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.

Motor 4 current limit register bits description:

- ClrMtr4IlimitLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear both Mtr4SideBIlimitLth and Mtr4SideAIlimitLth bit.
- Mtr4SideBIlimitLth:
  - This bit is read only (writing to this bit is ignored).
  - It represents the latched output of current limit comparator for side B of bridge 4.
- Mtr4SideAIlimitLth:
  - This bit is read only (writing to this bit is ignored).
  - It represents the latched output of current limit comparator for side A of bridge 4.

2.30 StpCfg1: stepper configuration 1 register [0x30]

Table 31. Stepper configuration 1 register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality(2)	
				Read	Write
011_0000	StpCfg1	15	0	ResetStep	
		14	0		
		13	1	StepOffTime[4]	StepOffTime[4]
		12	1	StepOffTime[3]	StepOffTime[3]
		11	1	StepOffTime[2]	StepOffTime[2]
		10	1	StepOffTime[1]	StepOffTime[1]
		9	1	StepOffTime[0]	StepOffTime[0]
		8	0	SeqMixedOnlyIn DecreasingPh	SeqMixedOnlyIn DecreasingPh
		7	0	StepBlkTime[1]	StepBlkTime[1]
		6	0	StepBlkTime[0]	StepBlkTime[0]
		5	0	SelStepRef	SelStepRef
		4	0	StepFromGpio	StepFromGpio
		3	0	StepCtrlMode[2]	StepCtrlMode[2]
		2	0	StepCtrlMode[1]	StepCtrlMode[1]
		1	0	StepCtrlMode[0]	StepCtrlMode[0]
		0	0	EnStepDrv	EnStepDrv

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.
2. The content of this register is ignored when bridge 3 & 4 are NOT configured as bipolar stepper motor driver.

Stepper configuration 1 register bits description:

- ResetStep:
  - This bit is write only.
  - Any writing to this bit is ignored when EnStepDrv is at logic level “0”.
  - If this bit is written to “1” (when EnStepDrv = “0”), it will force the stepper sequencer on initial position.
- StepOffTime[4:0]:
  - These bits allow the selection of the off time (from 2us to 64us) for stepper motor driver. (See *Chapter 1.1.18*).
- SeqMixedOnlyInDecreasingPh:
  - When using L6460 stepper sequencer, this bit allows the selection of mixed decay only to the phase that is reducing its current level.
- StepBlkTime[1:0]:
  - These bits allow the selection of the blanking time used to mask current spikes on rsense resistor. (See *Chapter 1.1.18*).
- SelStepRef:
  - This bit allows the selection of the reference voltage used for the rsense comparator. (See *Chapter 1.1.18*).
- StepFromGpio:
  - When this bit is set at “0”, the command to increase the sequencer steps is given by writing to “1” the StpCmd bit in the 0x33-StpCmd register.
  - When this bit is set at “1” the command to increase the sequencer steps is given by setting the GPIO12 pin at”1” for at least 1us.
- StepCtrlMode[2:0]:
  - These bits allow the selection of the functional mode for stepper motor driver. (See *Chapter 1.1.18*).
  - Each time these bits are changed with respect to their previous value, the sequencer state machine is reset and the stepping sequence position 0 is assumed.
- EnStepDrv:
  - This bit enables and disables the stepper motor driver outputs. It does not disable the sequencer that therefore could be advanced to the requested initial position without any output commutation.

2.31 StpCfg2: stepper configuration register 2 [0x31]

Table 32. Stepper configuration 2 register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality(2)	
				Read	Write
011_0001	StpCfg2	15	0	StepSeqPos[5]	
		14	0	StepSeqPos[4]	
		13	0	StepSeqPos[3]	
		12	0	StepSeqPos[2]	
		11	0	StepSeqPos[1]	
		10	0	StepSeqPos[0]	
		9	0	MixDecPhB[4]	MixDecPhB[4]
		8	0	MixDecPhB[3]	MixDecPhB[3]
		7	0	MixDecPhB[2]	MixDecPhB[2]
		6	0	MixDecPhB[1]	MixDecPhB[1]
		5	0	MixDecPhB[0]	MixDecPhB[0]
		4	0	MixDecPhA[4]	MixDecPhA[4]
		3	0	MixDecPhA[3]	MixDecPhA[3]
		2	0	MixDecPhA[2]	MixDecPhA[2]
		1	0	MixDecPhA[1]	MixDecPhA[1]
		0	0	MixDecPhA[0]	MixDecPhA[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.
2. The content of this register is ignored when bridge 3 & 4 are NOT configured as bipolar stepper motor driver.

Stepper Configuration 2 registers bits description:

- StepSeqPos[5:0]:
  - These bits are write only.
  - When stepper motor driver sequencer is active, these bits indicate one of the 64 possible positions of sequencer. When stepper motor driver sequencer is not active these bits have no meaning.
- MixDecPhB[4:0]:
  - These bits allow the selection (for the phase B) of the off time percentage that the stepper driver will spend in fast-decay mode. (See *Chapter 1.1.18*).
- MixDecPhA[4:0]:
  - These bits allow the selection (for the phase A) of the off time percentage that the stepper driver will spend in fast-decay mode. (See *Chapter 1.1.18*).

2.32 StpCtrl: stepper control register [0x32]

Table 33. Stepper control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality(2)	
				Read	Write
011_0010	StpCtrl	15	0	EnStepDrv	
		14	0	StepDir	StepDir
		13	0		
		12	0		
		11	0	DirPhB	DirPhB
		10	0		
		9	0	PhBDAC[3]	PhBDAC[3]
		8	0	PhBDAC[2]	PhBDAC[2]
		7	0	PhBDAC[1]	PhBDAC[1]
		6	0	PhBDAC[0]	PhBDAC[0]
		5	0	DirPhA	DirPhA
		4	0		
		3	0	PhADAC[3]	PhADAC[3]
		2	0	PhADAC[2]	PhADAC[2]
		1	0	PhADAC[1]	PhADAC[1]
		0	0	PhADAC[0]	PhADAC[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.
2. The content of this register is ignored when bridge 3 & 4 are NOT configured as bipolar stepper motor driver.

Stepper control register bits description:

- EnStepDrv.
  - This bit is read-only and repeats the status of the same bit in the 0x30-StpCfg1 register.
- StepDir:
  - This bit allows the selection of stepper motor driver direction when sequencer is active. (See *Chapter 1.1.18*).
  - This bit is ignored when stepper motor driver sequencer is NOT active.
- DirPhB:
  - This bit allows the selection of the direction of the current for stepper motor driver phase B. If this bit is written to “1” current is flowing out from phase B pin.
  - This bit is read-only when stepper motor driver sequencer is active.
- PhBDAC[3:0]:
  - These bits allow the selection of the current level for stepper motor driver phase B. (See *Chapter 1.1.18*).
  - The value written in these bits sets the module of maximum current level used in phase B when stepper motor driver sequencer is active and one among half step, full-step (1 or 2 phase on) mode is selected
  - These bits are read-only when stepper motor driver sequencer is active and one of micro-step modes (¼ step, ? step, and 1/16step) is selected. The values read in these bits represent the actual current level in phase B.
- DirPhA:
  - This bit allows the selection of the direction of the current for stepper motor driver phase A. If this bit is written to “1” current is flowing out from phase A pin.
  - This bit is read-only when stepper motor driver sequencer is active.
- PhADAC[3:0]:
  - These bits allow the selection of the current level for stepper motor driver phase A. (See *Chapter 1.1.18*).
  - The value written in these bits sets the module of maximum current level used in phase A when stepper motor driver sequencer is active and one among half step, full-step (1 or 2 phase on) mode is selected
  - These bits are read-only when stepper motor driver sequencer is active and one of micro-step modes (¼ step, ? step, and 1/16step) is selected. The values read in these bits represent the actual current level in phase A.

2.33 StpCmd: stepper step register [0x33]

Table 34. Stepper step register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
011_0011	StpCmd	15	0	-	StepCmd
		14	0	-	
		13	0	-	
		12	0	-	
		11	0	-	
		10	0	-	
		9	0	-	
		8	0	-	
		7	0	-	
		6	0	-	
		5	0	-	
		4	0	-	
		3	0	-	
		2	0	-	
		1	0	-	
		0	0	-	

Stepper Step register bits description:

- StepCmd:
  - This bit is write only.
  - Writing “1” in this bit when StepFromGpio = ”0” in 0x30-StpCfg1 register will cause the sequencer to move to the next step.

2.34 Aux1SwCfg: motor 3 AUX switching reg.1 config. register [0x35]

Table 35. Motor 3 auxiliary switching regulator 1 configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
011_0101	Aux1SwCfg	15	0		ClrAux1SwIlimLth
		14	0	Aux1UvLthBhv	Aux1UvLthBhv
		13	0		
		12	0		
		11	0	Aux1PWMTable[1]	Aux1PWMTable[1]
		10	1	Aux1PWMTable[0]	Aux1PWMTable[0]
		9	0	Aux1OneHundredDuty	Aux1OneHundredDuty
		8	0		
		7	0	SelFBRef[1]	SelFBRef[1]
		6	1	SelFBRef[0]	SelFBRef[0]
		5	0		
		4	0	Aux1SelLowSideBhv	Aux1SelLowSideBhv
		3	0	Aux1SwUvlo	
		2	0	Aux1SwIlimit	
		1	0	Aux1SwIlimitLth	
		0	0	Aux1SwEnable	Aux1SwEnable

Motor 3 auxiliary switching regulator 1 configuration register bits description:

- ClrAux1SwIlimLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear Aux1SwIlimitLth bit.
- Aux1UvLthBhv:
  - This bit is ignored if AUX1 is a system regulator.
  - If this bit is written to “0” it means that, in case of Uvlo event caused by Aux1 itself, the regulator will restart without any action by the user.
  - If this bit is written to “1” it means that, in case of Uvlo event caused by Aux1 itself, the regulator will remain off until the Aux1SwUvloLth bit in the 0x03-ICStatus register is reset.
- Aux1PWMTable[1:0]:
  - These bits allow the selection of the PWM duty cycle value. (See *Chapter 1.1.3*).
- Aux1OneHundredDuty:
  - If this bit is written to “1” Aux1 regulator will enter in 100% duty cycle mode.
- SelFBRef:
  - These bits allow the selection of the feedback reference voltage used from Aux1 regulator to select the feedback reference voltage. (See *Chapter 1.1.3*).
- Aux1SelLowSideBhv:
  - If this bit is written to “0” the low side power output of Aux1 regulator (in parallel with external Schottky diode) will be turned on for about 400ns after commutation from Ton to Toff. This will help to discharge the source capacitance of the high side power output.
- Aux1SwUvlo:
  - This bit is read only.
  - It represents the output status of the Aux1 regulator UVLO circuit.
- Aux1SwIlimit:
  - This bit is read only.
  - It represents the output status of the Aux1 regulator current limit circuit.
- Aux1SwIlimitLth:
  - This bit represents the latched output of the Aux1 regulator current limit circuit.
- Aux1SwEnable:
  - This bit allows the enabling and disabling of Aux1 regulator. Particular care must be taken when disabling this regulator if it is a system regulator because it can cause unwanted system resets.

2.35 Aux2SwCfg: motor 3 AUX switching reg. 2 config. register [0x36]

Table 36. Motor 3 auxiliary switching regulator 2 configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
011_0110	Aux2SwCfg	15	0	0	ClrAux2SwIlimLth
		14	0	Aux2UvLthBhv	Aux2UvLthBhv
		13	0		
		12	0		
		11	1	Aux2PWMTable[1]	Aux2PWMTable[1]
		10	0	Aux2PWMTable[0]	Aux2PWMTable[0]
		9	0	Aux2OneUndredDuty	Aux2OneUndredDuty
		8	0		
		7	1	SelFBRef[1]	SelFBRef[1]
		6	0	SelFBRef[0]	SelFBRef[0]
		5	0		
		4	0	Aux2SelLowSideBhv	Aux2SelLowSideBhv
		3	0	Aux2Uvlo	
		2	0	Aux2SwIlimit	
		1	0	Aux2SwIlimitLth	
		0	0	Aux2SwEnable	Aux2SwEnable

Motor 3 auxiliary switching regulator 2 configuration register bits description:

- ClrAux2SwIlimLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear Aux2SwIlimitLth bit.
- Aux2UvLthBhv:
  - This bit is ignored if AUX2 is a system regulator.
  - If this bit is written to “0” it means that, in case of Uvlo event caused by Aux2 itself, the regulator will restart without any action by the user.
  - If this bit is written to “1” it means that, in case of Uvlo event caused by Aux2 itself, the regulator will remain off until the Aux2SwUvloLth bit in the 0x03-ICStatus register is reset.
- Aux2PWMTable[1:0]:
  - These bits allow the selection of the PWM duty cycle value. (See *Chapter 1.1.3*).
- Aux2OneHundredDuty:
  - If this bit is written to “1” Aux2 regulator will enter in 100% duty cycle mode.
- SelFBRef:
  - These bits allow the selection of the feedback reference voltage used from Aux2 regulator to select the feedback reference voltage. (See *Chapter 1.1.3*).
- Aux2SelLowSideBhv:
  - If this bit is written to “0” the low side power output of Aux2 regulator (in parallel with external Schottky diode) will be turned on for about 400ns after commutation from Ton to Toff. This will help to discharge the source capacitance of the high side power output.
- Aux2SwUvlo:
  - This bit is read only.
  - It represents the output status of the Aux2 regulator UVLO circuit.
- Aux2SwIlimit:
  - This bit is read only.
  - It represents the output status of the Aux2 regulator Current limit circuit.
- Aux2SwIlimitLth:
  - This bit represents the latched output of the Aux2 regulator current limit circuit.
- Aux2SwEnable:
  - This bit allows the enabling and disabling of Aux2 regulator. Particular care must be taken when disabling this regulator if it is a system regulator because it can cause unwanted system resets.

2.36 Aux3SwCfg1: motor 4 AUX switching reg. 3 config. 1 register [0x37]

Table 37. Motor 4 auxiliary switching regulator 3 configuration 1 register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
011_0111	Aux3SwCfg1	15	0		
		14	0	Aux3UvLthBhv	Aux3UvLthBhv
		13	0		
		12	0		
		11	0	Aux3PWMTable[1]	Aux3PWMTable[1]
		10	1	Aux3PWMTable[0]	Aux3PWMTable[0]
		9	0	Aux3 OneHundredDuty	Aux3 OneHundredDuty
		8	0		
		7	0	SelCurrRef[1]	SelCurrRef[1]
		6	0	SelCurrRef[0]	SelCurrRef[0]
		5	0	SelFBRef[1]	SelFBRef[1]
		4	1	SelFBRef[0]	SelFBRef[0]
		3	0	Aux3BatteryCharge	Aux3BatteryCharge
		2	0		
		1	0	Aux3SelLowSideBhv	Aux3SelLowSideBhv
		0	0	Aux3SwEnable	Aux3SwEnable

Motor 4 auxiliary switching regulator 3 configuration register bits description:

- Aux3UvLthBhv:
  - This bit is ignored if AUX3 is a system regulator or it is configured as a battery charger.
  - If this bit is written to “0” it means that, in case of Uvlo event caused by Aux3 itself, the regulator will restart without any action by the user.
  - If this bit is written to “1” it means that, in case of Uvlo event caused by Aux3 itself, the regulator will remain off until the Aux3SwUvloLth bit in the 0x03-ICStatus register is reset.
- Aux3PWMTable[1:0]:
  - These bits allow the selection of the PWM duty cycle value. (See *Chapter 1.1.4*).
- Aux3OneHundredDuty:
  - If this bit is written to “1” Aux3 regulator will enter in 100% duty cycle mode.
  - respect the nominal one.
- SelCurrRef[1:0]:
  - These bits allow the selection of the feedback reference voltage used from Aux3 regulator to limit the current when in battery charger mode. (See *Chapter 1.1.4*).
- SelFBRef[1:0]:
  - These bits allow the selection of the feedback reference voltage used from Aux3 regulator to select the feedback reference voltage. (See *Chapter 1.1.4*).
- Aux3BatteryCharge:
  - If this bit is written to “1”, Aux3 regulator will enable battery charger functionality.
- Aux3SelLowSideBhv:
  - If this bit is written to “0” the low side power output of Aux3 regulator (in parallel with external Schottky diode) will be turned on for about 400ns after commutation from Ton to Toff. This will help to discharge the source capacitance of the high side power output.
- Aux3SwEnable:
  - This bit allows the enabling and disabling of Aux3 regulator. Particular care must be taken when disabling this regulator if it is a system regulator because it can cause unwanted system resets.

2.37 Aux3SwCfg2: motor 4 AUX switching reg. 3 config. 2 register [0x38]

Table 38. Motor 4 auxiliary switching regulator 3 configuration 2 register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
011_1000	Aux3SwCfg2	15	0	0	ClrAux3SwIlimLth
		14	-	Vloop3IsSys	
		13	0		
		12	-		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0	Aux3BatteryCharge	
		4	0	BattChrgIlimCmp	
		3	-	BattChrgIlimCmpLth	-
		2	-	Aux3SwIlimit	-
		1	0	Aux3SwIlimitLth	-
		0	0	Aux3Uvlo	

Motor 3 auxiliary switching regulator 2 configuration register bits description:

- ClrAux3SwIlimLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear Aux3SwIlimitLth and BattChrgIlimCmpLth bit.
- Vloop3IsSys:
  - This bit is read only.
  - If it is read as “1” it means that the switching regulator control loop (Vloop3) included into bridge 4 is a system regulator.
- Aux3BatteryCharge:
  - This bit is read only.
  - This bit is a replica of the same bit in the Aux3SwCfg1 register.
- BattChrgIlimCmp:
  - This bit is read only.
  - It represents the output status of the battery charger current comparator.
- BattChrgIlimCmpLth:
  - This bit represents the latched output status of the battery charger current comparator.
- Aux3SwIlimit:
  - This bit is read only.
  - It represents the output status of the auxiliary switching regulator 3 current limit circuit.
- Aux3SwIlimitLth:
  - This bit represents the latched output status of the auxiliary switching regulator 3 current limit circuit.
- Aux3Uvlo:
  - This bit is read only.
  - It represents the output status of the auxiliary switching regulator 3 UVLO circuit.

2.38 PwrCtrl: power mode control register [0x39]

Table 39. Power mode control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
011_1001	PwrCtrl	15	0		ClrAwakeLth
		14	0	AwakeLth	
		13	0	nAwake	
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		
		2	0		LowPwerMode[2]
		1	0		LowPwerMode[1]
		0	0		LowPwerMode[0]

1. The events that can reset the register to default values are:
   – Power on reset event.

Power mode control register bits description:

- ClrAwakeLth:
  – This bit is write only.
  – If this bit is written to “1” it will clear awakeLth bit.
- AwakeLth:
  – This bit is read only.
  – It represents the latch of the awake event signal.
- nAwake:
  – This bit is read only.
  – It represents the awake event signal.
- LowPwerMode[2:0]:
  – These bits are write only.
  – To enter in “Low power mode”, these bits must be written as LowPwerMode[2:0]=“110”.

2.39 CurrDacCtrl: current DAC control register [0x3C]

Table 40. Current DAC control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
011_1100	CurrDacCtrl	15	0	EnDac	EnDac
		14	0	EnDacScale	EnDacScale
		13	0		
		12	0	EnGpio8DigIn	EnGpio8DigIn
		11	0		
		10	0		
		9	0	DacRange[1]	DacRange[1]
		8	0	DacRange[0]	DacRange[0]
		7	0		
		6	0		
		5	0	DacValue[5]	DacValue[5]
		4	0	DacValue[4]	DacValue[4]
		3	0	DacValue[3]	DacValue[3]
		2	0	DacValue[2]	DacValue[2]
		1	0	DacValue[1]	DacValue[1]
		0	0	DacValue[0]	DacValue[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Currentr control register bits description:

- EnDac:
  - If this bit is written to “1” it will enable the current DAC.
- EnDacScale:
  - If this bit is written to “1” the sampling of the pin voltage will be done using the internal resistor divider.
  - If this bit is written to “0” the sampling of the pin voltage will be done on the pin without scaling its value but clamping the resulting voltage to 3.3 volts.
- EnGpio8DigIn:
  - If this bit is written to “1” it will enable the GPIO8 input schmitt trigger.
- DacRange[1:0]:
  - These bits allow the selection of the DAC current ranges. (See *Chapter 1.1.10*).
- DacValue[5:0]:
  - These bits allow the selection of the DAC current programmed value. (See *Chapter 1.1.10*).

2.40 AuxPwm1Ctrl: aux PWM gen. 1control register [0x40]

Table 41. General purpose PWM generator 1 control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
100_0000	AuxPwm1Ctrl	15	0		
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0	AuxPwm1Ctrl[9]	AuxPwm1Ctrl[9]
		8	0	AuxPwm1Ctrl [8]	AuxPwm1Ctrl [8]
		7	0	AuxPwm1Ctrl [7]	AuxPwm1Ctrl [7]
		6	0	AuxPwm1Ctrl [6]	AuxPwm1Ctrl [6]
		5	0	AuxPwm1Ctrl [5]	AuxPwm1Ctrl [5]
		4	0	AuxPwm1Ctrl [4]	AuxPwm1Ctrl [4]
		3	0	AuxPwm1Ctrl [3]	AuxPwm1Ctrl [3]
		2	0	AuxPwm1Ctrl [2]	AuxPwm1Ctrl [2]
		1	0	AuxPwm1Ctrl [1]	AuxPwm1Ctrl [1]
		0	0	AuxPwm1Ctrl [0]	AuxPwm1Ctrl [0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

General purpose PWM generator 1 control register bits description:

- AuxPwm1Ctrl[9:0]:
  - These bits allow the selection of the duty cycle value of PWM generator. (See *Chapter 1.1.2*).

2.41 AuxPwm2Ctrl: aux PWM gen. 2 control register [0x41]

Table 42. General purpose PWM generator 2 control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
100_0001	AuxPwm2Ctrl	15	0		
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0	AuxPwm2Ctrl[9]	AuxPwm2Ctrl[9]
		8	0	AuxPwm2Ctrl [8]	AuxPwm2Ctrl [8]
		7	0	AuxPwm2Ctrl [7]	AuxPwm2Ctrl [7]
		6	0	AuxPwm2Ctrl [6]	AuxPwm2Ctrl [6]
		5	0	AuxPwm2Ctrl [5]	AuxPwm2Ctrl [5]
		4	0	AuxPwm2Ctrl [4]	AuxPwm2Ctrl [4]
		3	0	AuxPwm2Ctrl [3]	AuxPwm2Ctrl [3]
		2	0	AuxPwm2Ctrl [2]	AuxPwm2Ctrl [2]
		1	0	AuxPwm2Ctrl [1]	AuxPwm2Ctrl [1]
		0	0	AuxPwm2Ctrl [0]	AuxPwm2Ctrl [0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

General purpose PWM generator 2 control register bits description:

- AuxPwm2Ctrl[9:0]:
  - These bits allow the selection of the duty cycle value of PWM generator. (See *Chapter 1.1.2*).

2.42 GpPwmBase: aux PWM gen. 3 time base register [0x42]

Table 43. General purpose PWM generator 3 time base register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
100_0010	GpPwmBase	15	0		
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0	GpPwmBase[6]	GpPwmBase[6]
		5	0	GpPwmBase[5]	GpPwmBase[5]
		4	0	GpPwmBase[4]	GpPwmBase[4]
		3	0	GpPwmBase[3]	GpPwmBase[3]
		2	0	GpPwmBase[2]	GpPwmBase[2]
		1	0	GpPwmBase[1]	GpPwmBase[1]
		0	0	GpPwmBase[0]	GpPwmBase[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

General purpose PWM generator 3 time base register bits description:

- GpPwm3Base[6:0]:
  - These bits allow the selection of the base clock for PWM generator 3. (See *Chapter 1.1.2*).

2.43 GpPwmCtrl: aux PWM gen. 3 control register [0x43]

Table 44. General purpose PWM generator 3 control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
100_0011	GpPwmCtrl	15	0	GpPwmHigh[7]	GpPwmHigh[7]
		14	0	GpPwmHigh[6]	GpPwmHigh[6]
		13	0	GpPwmHigh[5]	GpPwmHigh[5]
		12	0	GpPwmHigh[4]	GpPwmHigh[4]
		11	0	GpPwmHigh[3]	GpPwmHigh[3]
		10	0	GpPwmHigh[2]	GpPwmHigh[2]
		9	0	GpPwmHigh[1]	GpPwmHigh[1]
		8	0	GpPwmHigh[0]	GpPwmHigh[0]
		7	0	GpPwmLow[7]	GpPwmLow[7]
		6	0	GpPwmLow[6]	GpPwmLow[6]
		5	0	GpPwmLow[5]	GpPwmLow[5]
		4	0	GpPwmLow[4]	GpPwmLow[4]
		3	0	GpPwmLow[3]	GpPwmLow[3]
		2	0	GpPwmLow[2]	GpPwmLow[2]
		1	0	GpPwmLow[1]	GpPwmLow[1]
		0	0	GpPwmLow[0]	GpPwmLow[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

General purpose PWM generator 3 control register bits description:

- GpPwm3High[7:0]:
  - These bits allow the selection of the PWM generator high time. (See *Chapter 1.1.2*).
- GpPwm3Low[7:0]:
  - These bits allow the selection of the PWM generator low time. (See *Chapter 1.1.2*).

2.44 IntCtrlCfg: interrupt controller configuration register [0x46]

Table 45. Interrupt controller configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
100_0110	IntCtrlCfg	15	0		ClrIntCtrlLth
		14	0	IntCtrlLth	
		13	0	IntCtrlOut	
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0	IntCrtlPolarity	IntCrtlPolarity
		2	0	EnIntCtrlPulse	EnIntCtrlPulse
		1	0		
		0	0	EnIntCtrl	EnIntCtrl

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Interrupt controller configuration register bits description:

- ClrIntCtrlLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear IntCtrlLth bit.
- IntCtrlLth:
  - This bit is read only.
  - It represents the latched staus of IntCtrlOut bit.
- IntCtrlOut:
  - This bit is read only.
  - It represents the output signal status of Interrupt controller.
- IntCrtlPolarity:
  - If this bit is written to “0” it will set the active level of interrupt controller to active high.
  - If this bit is written to “1” it will set the active level of interrupt controller to active low.
- EnIntCtrlPulse:
  - If this bit is written to “1”, the interrupt controller will signal an interrupt event with a pulse on output. (See *Chapter 1.1.13*).
- EnIntCtrl:
  - If this bit is written to “1” it will enable the interrupt controller.

2.45 IntCtrlCtrl: interrupt controller control register [0x47]

Table 46. Interrupt controller control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
100_0111	IntCtrlCtrl	15	0	EnMtr1Fault	EnMtr1Fault
		14	0	EnMtr2Fault	EnMtr2Fault
		13	0	EnMtr3Fault	EnMtr3Fault
		12	0	EnMtr4Fault	EnMtr4Fault
		11	0	EnAWKLow	EnAWKLow
		10	0	EnSwRegCtrlIlim	EnSwRegCtrlIlim
		9	0	EnMainSwIlim	EnMainSwIlim
		8	0	EnLpwrSw1Ilim	EnLpwrSw1Ilim
		7	0	EnLpwrSw2Ilim	EnLpwrSw2Ilim
		6	0	EnWarm	EnWarm
		5	0	EnWatchDogWarn	EnWatchDogWarn
		4	0	EnWatchDog	EnWatchDog
		3	0	EnDigCmp	EnDigCmp
		2	0	EnADCDone1	EnADCDone1
		1	0	EnADCDone2	EnADCDone2
		0	0	EnVloop1Ilim	EnVloop1Ilim

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Interrupt controller control register bits description:

- EnMtr1Fault:
  - If this bit is written to “1” it will enable the interrupt request on bridge 1 fault detection.
- EnMtr2Fault:
  - If this bit is written to “1” it will enable the interrupt request on bridge 2 fault detection.
- EnMtr3Fault:
  - If this bit is written to “1” it will enable the interrupt request on bridge 3 fault detection.
- EnMtr4Fault:
  - If this bit is written to “1” it will enable the interrupt request on bridge 4 fault detection.
- EnAWKLow:
  - If this bit is written to “1” it will enable the interrupt request when nAWAKE pin is externally forced low.
- EnSwRegCtrlIlim:
  - If this bit is written to “1” it will enable the interrupt request when a current limit event is detected on switching regulator controller.
- EnMainSwIlim:
  - If this bit is written to “1” it will enable the interrupt request when a current limit event is detected on main switching regulator.
- EnLpwrSw1Ilim:
  - If this bit is written to “1” it will enable the interrupt request when a current limit event is detected on low power switch 1 (GPIO6).
- EnLpwrSw2Ilim:
  - If this bit is written to “1” it will enable the interrupt request when a current limit event is detected on low power switch 2. (GPIO7).
- EnWarm:
  - If this bit is written to “1” it will enable the interrupt request when a warming event is detected.
- EnWatchDogWarn:
  - If this bit is written to “1” it will enable the interrupt request when a watchdog warning event is detected.
- EnWatchDog:
  - If this bit is written to “1” it will enable the interrupt request when a watchdog event is detected (it will be signaled only if watchdog isn’t programmed to cause a reset).
- EnDigCmp:
  - If this bit is written to “1” it will enable the interrupt request when the digital comparator output is found high.
- EnADCDone1:
  - If this bit is written to “1” it will enable the interrupt request when ADC done bit is high on channel 1. This event is disabled if the related ADC channel is configured in continuous mode.
- EnADCDone2:

  - If this bit is written to “1” it will enable the interrupt request when ADC done bit is high on channel 2. This event is disabled if the related ADC channel is configured in continuous mode.

- EnVloop1Ilim:
  - If this bit is written to “1” it will enable the interrupt request when a current limit event is detected on auxiliary regulator 1.

2.46 DigCmpCfg: digital comparator configuration register [0x48]

Table 47. Digital comparator configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
100_1000	DigCmpCfg	15	0	EnDigCmp	EnDigCmp
		14	0	FilterCompare	FilterCompare
		13	0	DigCmpSelCh1[1]	CmpSelCh1[1]
		12	0	DigCmpSelCh1[0]	CmpSelCh1[0]
		11	0		
		10	0		
		9	0	DigCmpSelCh0[1]	CmpSelCh0[1]
		8	0	DigCmpSelCh0[0]	CmpSelCh0[0]
		7	0		
		6	0		
		5	0	DigCmpUpdate[1]	DigCmpUpdate[1]
		4	0	DigCmpUpdate[0]	DigCmpUpdate[0]
		3	0		
		2	0		
		1	0	SelCmpType[1]	SelCmpType[1]
		0	0	SelCmpType[0]	SelCmpType[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Digital comparator configuration register bits description:

- EnDigCmp:
  - If this bit is written to “1” it will enable the digital comparator operations.
- FilterCompare:
  - If this bit is written to “1”, the status of the digital comparator will be accepted only if it is confirmed for 3 rising edges of clock signal.
- DigCmpSelCh1[1:0]:
  - These bits allow the selection of the comparator input 1 data. (See *Chapter 1.1.11*).
- DigCmpSelCh0[1:0]:
  - These bits allow the selection of the comparator input 0 data. (See *Chapter 1.1.11*).
- DigCmpUpdate[1:0]:
  - These bits allow the selection of the update strategy of the comparator. (See *Chapter 1.1.11*).
- SelCmpType[1:0]:
  - These bits allow the selection of the comparison type performed by the digital comparator. (See *Chapter 1.1.11*).

2.47 DigCmpValue: digital comparator fixed value register [0x49]

Table 48. Digital comparator fixed value register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
100_1001	DigCmpValue	15	0		ClrDigCmpOutLth
		14	0	DigCmpOut	-
		13	0	DigCmpOutLth	
		12	0		
		11	0		
		10	0		
		9	0	DigCmpValue[9]	DigCmpValue[9]
		8	0	DigCmpValue[8]	DigCmpValue[8]
		7	0	DigCmpValue[7]	DigCmpValue[7]
		6	0	DigCmpValue[6]	DigCmpValue[6]
		5	0	DigCmpValue[5]	DigCmpValue[5]
		4	0	DigCmpValue[4]	DigCmpValue[4]
		3	0	DigCmpValue[3]	DigCmpValue[3]
		2	0	DigCmpValue[2]	DigCmpValue[2]
		1	0	DigCmpValue[1]	DigCmpValue[1]
		0	0	DigCmpValue[0]	DigCmpValue[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Digital comparator fixed value bits description:

- ClrDigCmpOutLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear DigCmpOutLth bit.
- DigCmpOut:
  - This bit is read only.
  - It represents the output signal status of the digital comparator circuit.
- DigCmpOutLth:
  - This bit is read only.
  - It represents the latched status of DigCmpOut bit.
- DigCmpValue[9:0]:
  - These bits allow the selection of the fixed value to be compared by digital comparator.

2.48 A2DControl: A2D system control register [0x50]

Table 49. A2D System control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_0000	A2DControl	15	0	A2DEnable	A2DEnable
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		
		2	0		
		1	0		
		0	0		

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

A2D system control register bits description:

- A2DEnable:
  - If this bit is written to “1” it will enable the A2D system.

2.49 A2DConfig0: channel 0 A2D configuration register [0x51]

Table 50. Channel 0 A2D configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_0001	A2DConfig0	15	0		A2DTrig0
		14	0	A2DCh0Waiting	
		13	0		
		12	0	A2DContinuous0	A2DContinuous0
		11	0	A2DType0	A2DType0
		10	0	A2DGpo0	A2DGpo0
		9	0		
		8	0	A2DChannel0[4]	A2DChannel0[4]
		7	0	A2DChannel0[3]	A2DChannel0[3]
		6	0	A2DChannel0[2]	A2DChannel0[2]
		5	0	A2DChannel0[1]	A2DChannel0[1]
		4	0	A2DChannel0[0]	A2DChannel0[0]
		3	0		
		2	0	A2DSample0[2]	A2DSample0[2]
		1	0	A2DSample0[1]	A2DSample0[1]
		0	0	A2DSample0[0]	A2DSample0[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Channel 0 A2D configuration register bits description:

- A2DTrig0:
  - This bit is write only.
  - Any writing in this bit is ignored when A2DContinuous0 = “1” or when A2DCh0Waiting = “1”.
  - If this bit is written to “1” (when A2DContinuous0 = “0”), it will trigger a conversion using the A2DChannel0[4:0] and A2DSample0[2:0] values.
- A2DCh0Waiting:
  - This bit is read only.
  - When A2DContinuous0 = “1” this bit is always read as “1”.
  - This bit is read as “1” if a conversion has been triggered on this channel and has not yet been completed.
- A2DContinuous0
  - If this bit is written to “1” the A/D converter is programmed to make continuous conversions.
- A2DType0:
  - This bit allows the selection between two possible A2D configurations:
    - If A2DType0 = “0” the A2D on channel 0 is configured as a 8 bit resolution converter.
    - If A2DType0 = “1” the A2D on channel 0 is configured as a 9 bit resolution converter.
  - Any writing in this bit is ignored when A2DContinuous0 = “1” or when A2DCh0Waiting = “1”.
- A2DGpo0:
  - If this bit is written to “1”, this “1” could be presented on the selected GPIO (See *Chapter 1.1.1*) allowing the possibility to signal, trough the GPIO, when channel 1 of the A/D converter is in use.
- A2DChannel0[4:0]:
  - These bits allow the selection of the analog multiplexer channel to be converted.
  - Any writing in these bits is ignored if A2DContinuous0 = “1” or A2DCh0Waiting = “1”.
- A2DSample0[2:0]:
  - These bits allow the selection of the sample time to be used for the conversion.
  - Any writing in these bits is ignored if A2DContinuous0 = “1” or A2DCh0Waiting = “1”.

2.50 A2DResult0: channel 0 A2D result register [0x52]

Table 51. Channel 0 A2D result register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_0010	A2DResult0	15	1	A2DDone0	-
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0	A2DResult0[8]	A2DResult0[8]
		7	0	A2DResult0[7]	A2DResult0[7]
		6	0	A2DResult0[6]	A2DResult0[6]
		5	0	A2DResult0[5]	A2DResult0[5]
		4	0	A2DResult0[4]	A2DResult0[4]
		3	0	A2DResult0[3]	A2DResult0[3]
		2	0	A2DResult0[2]	A2DResult0[2]
		1	0	A2DResult0[1]	A2DResult0[1]
		0	0	A2DResult0[0]	A2DResult0[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Channel 0 A2D result register bits description:

- A2DDone0:
  - This bit is read only.
  - This bit is “1” when a conversion has been completed.
- A2DResult0[8:0]:
  - These bits represent the result of the conversion.

2.51 A2DConfig1: channel 1 A2D configuration register [0x53]

Table 52. Channel 1 A2D configuration register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_0011	A2DConfig1	15	0		A2DTrig1
		14	0	A2DCh1Waiting	
		13	0		
		12	0	A2DContinuous1	A2DContinuous1
		11	0	A2DType1	A2DType1
		10	0	A2DGpo1	A2DGpo1
		9	0		
		8	0	A2DChannel1[4]	A2DChannel1[4]
		7	0	A2DChannel1[3]	A2DChannel1[3]
		6	0	A2DChannel1[2]	A2DChannel1[2]
		5	0	A2DChannel1[1]	A2DChannel1[1]
		4	0	A2DChannel1[0]	A2DChannel1[0]
		3	0		
		2	0	A2DSample1[2]	A2DSample1[2]
		1	0	A2DSample1[1]	A2DSample1[1]
		0	0	A2DSample1[0]	A2DSample1[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Channel 0 A2D configuration register bits description:

- A2DTrig1:
  - This bit is write only.
  - Any writing in this bit is ignored when A2DContinuous1 = “1” or when A2DCh1Waiting = “1”.
  - If this bit is written to “1” (when A2DContinuous1 = “0”), it will trigger a conversion using the A2DChannel1[4:0] and A2DSample1[2:0] values.
- A2DCh1Waiting:
  - This bit is read only.
  - When A2DContinuous0 = “1” this bit is always read as “1”.
  - This bit is read as “1” if a conversion has been triggered on this channel and has not yet been completed.
- A2DContinuous1
  - If this bit is written to “1” the A/D converter is programmed to make continuous conversions.
- A2DType1:
  - This bit allows the selection between two possible A2D configurations:
    - If A2DType1 = “0” the A2D on channel 1 is configured as a 8 bit resolution converter.
    - If A2DType1 = “1” the A2D on channel 1 is configured as a 9 bit resolution converter.
  - Any writing in this bit is ignored when A2DContinuous1 = “1” or when A2DCh1Waiting = “1”.
- A2DGpo1:
  - If this bit is written to “1”, this “1” could be presented on the selected GPIO (See *Chapter 1.1.1*) allowing the possibility to signal, trough the GPIO, when Channel 1 of the A/D converter is in use.
- A2DChannel1[4:0]:
  - These bits allow the selection of the analog multiplexer channel to be converted.
  - Any writing in these bits is ignored if A2DContinuous1 = “1” or A2DCh1Waiting = “1”.
- A2DSample1[2:0]:
  - These bits allow the selection of the sample time to be used for the conversion.
  - Any writing in these bits is ignored if A2DContinuous1 = “1” or A2DCh1Waiting = “1”.

2.52 A2DResult1: Channel 1 A2D result register

Table 53. Channel 1 A2D result register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_0100	A2DResult1	15	0	A2DDone1	-
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0	A2DResult1[8]	A2DResult1[8]
		7	0	A2DResult1[7]	A2DResult1[7]
		6	0	A2DResult1[6]	A2DResult1[6]
		5	0	A2DResult1[5]	A2DResult1[5]
		4	0	A2DResult1[4]	A2DResult1[4]
		3	0	A2DResult1[3]	A2DResult1[3]
		2	0	A2DResult1[2]	A2DResult1[2]
		1	0	A2DResult1[1]	A2DResult1[1]
		0	0	A2DResult1[0]	A2DResult1[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Channel 1 A2D result register bits description:

- A2DDone1:
  - This bit is read only.
  - This bit is “1” when a conversion has been completed.
- A2DResult1[8:0]:
  - These bits represent the result of the last A to D conversion.

2.53 GpioOutEnable: GPIO output enable register [0x58]

Table 54. GPIO output enable register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_1000	GpioOutEnable	15	0		
		14	0	GpioOutEnable[14]	GpioOutEnable[14]
		13	0	GpioOutEnable[13]	GpioOutEnable[13]
		12	0	GpioOutEnable[12]	GpioOutEnable[12]
		11	0	GpioOutEnable[11]	GpioOutEnable[11]
		10	0	GpioOutEnable[10]	GpioOutEnable[10]
		9	0	GpioOutEnable[9]	GpioOutEnable[9]
		8	0	GpioOutEnable[8]	GpioOutEnable[8]
		7	0	GpioOutEnable[7]	GpioOutEnable[7]
		6	0	GpioOutEnable[6]	GpioOutEnable[6]
		5	0	GpioOutEnable[5]	GpioOutEnable[5]
		4	0	GpioOutEnable[4]	GpioOutEnable[4]
		3	0	GpioOutEnable[3]	GpioOutEnable[3]
		2	0	GpioOutEnable[2]	GpioOutEnable[2]
		1	0	GpioOutEnable[1]	GpioOutEnable[1]
		0	0	GpioOutEnable[0]	GpioOutEnable[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

GPIO output enable bits description:

- GpioOutEnable[14:0]:
  - These bits allow the enabling of GPIO as output pins. (See *Chapter 1.1.12*).

2.54 0x59 GPIO control 1 register (GpioCtrl1)

Table 55. GPIO control 1 register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_0100	A2DResult1	15	0		
		14	0	Gpio14Mode[2]	Gpio14Mode[2]
		13	0	Gpio14Mode[1]	Gpio14Mode[1]
		12	0	Gpio14Mode[0]	Gpio14Mode[0]
		11	0	Gpio13Mode[2]	Gpio13Mode[2]
		10	0	Gpio13Mode[1]	Gpio13Mode[1]
		9	0	Gpio13Mode[0]	Gpio13Mode[0]
		8	0	Gpio12Mode[2]	Gpio12Mode[2]
		7	0	Gpio12Mode[1]	Gpio12Mode[1]
		6	0	Gpio12Mode[0]	Gpio12Mode[0]
		5	0	Gpio11Mode[2]	Gpio11Mode[2]
		4	0	Gpio11Mode[1]	Gpio11Mode[1]
		3	0	Gpio11Mode[0]	Gpio11Mode[0]
		2	0	Gpio10Mode[2]	Gpio10Mode[2]
		1	0	Gpio10Mode[1]	Gpio10Mode[1]
		0	0	Gpio10Mode[0]	Gpio10Mode[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

GPIO control 3 bits description:

- Gpio14Mode[2:0]:
  - These bits allow the selection of the GPIO[14] configuration. (See *Chapter 1.1.12*).
- Gpio13Mode[2:0]:
  - These bits allow the selection of the GPIO[13] configuration. (See *Chapter 1.1.12*).
- Gpio12Mode[2:0]:
  - These bits allow the selection of the GPIO[12] configuration. (See *Chapter 1.1.12*).
- Gpio11Mode[2:0]:
  - These bits allow the selection of the GPIO[11] configuration. (See *Chapter 1.1.12*).
- Gpio10Mode[2:0]:
  - These bits allow the selection of the GPIO[10] configuration. (See *Chapter 1.1.12*).

2.55 GpioCtrl2: GPIO control 2 register [0x5A]

Table 56. GPIO control 2 register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_1010	GpioCtrl2	15	0		
		14	0	Gpio9Mode[2]	Gpio9Mode[2]
		13	0	Gpio9Mode[1]	Gpio9Mode[1]
		12	0	Gpio9Mode[0]	Gpio9Mode[0]
		11	0	Gpio8Mode[2]	Gpio8Mode[2]
		10	0	Gpio8Mode[1]	Gpio8Mode[1]
		9	0	Gpio8Mode[0]	Gpio8Mode[0]
		8	0	Gpio7Mode[2]	Gpio7Mode[2]
		7	0	Gpio7Mode[1]	Gpio7Mode[1]
		6	0	Gpio7Mode[0]	Gpio7Mode[0]
		5	0	Gpio6Mode[2]	Gpio6Mode[2]
		4	0	Gpio6Mode[1]	Gpio6Mode[1]
		3	0	Gpio6Mode[0]	Gpio6Mode[0]
		2	0	Gpio5Mode[2]	Gpio5Mode[2]
		1	0	Gpio5Mode[1]	Gpio5Mode[1]
		0	0	Gpio5Mode[0]	Gpio5Mode[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

GPIO control 2 bits description:

- Gpio9Mode[2:0]:
  - These bits allow the selection of the GPIO[9] configuration. (See *Chapter 1.1.12*).
- Gpio8Mode[2:0]:
  - These bits allow the selection of the GPIO[8] configuration. (See *Chapter 1.1.12*).
- Gpio7Mode[2:0]:
  - These bits allow the selection of the GPIO7] configuration. (See *Chapter 1.1.12*).
- Gpio6Mode[2:0]:
  - These bits allow the selection of the GPIO[6] configuration. (See *Chapter 1.1.12*).
- Gpio5Mode[2:0]:
  - These bits allow the selection of the GPIO[5] configuration. (See *Chapter 1.1.12*).

2.56 GpioCtrl3: GPIO control 3 register [0x5B]

Table 57. GPIO control 3 register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
101_1011	GpioCtrl3	15	0		
		14	0	Gpio4Mode[2]	Gpio4Mode[2]
		13	0	Gpio4Mode[1]	Gpio4Mode[1]
		12	0	Gpio4Mode[0]	Gpio4Mode[0]
		11	0	Gpio3Mode[2]	Gpio3Mode[2]
		10	0	Gpio3Mode[1]	Gpio3Mode[1]
		9	0	Gpio3Mode[0]	Gpio3Mode[0]
		8	0	Gpio2Mode[2]	Gpio2Mode[2]
		7	0	Gpio2Mode[1]	Gpio2Mode[1]
		6	0	Gpio2Mode[0]	Gpio2Mode[0]
		5	0	Gpio1Mode[2]	Gpio1Mode[2]
		4	0	Gpio1Mode[1]	Gpio1Mode[1]
		3	0	Gpio1Mode[0]	Gpio1Mode[0]
		2	0	Gpio0Mode[2]	Gpio0Mode[2]
		1	0	Gpio0Mode[1]	Gpio0Mode[1]
		0	0	Gpio0Mode[0]	Gpio0Mode[0]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

GPIO control 3 bits description:

- Gpio4Mode[2:0]:
  - These bits allow the selection of the GPIO[4] configuration. (See *Chapter 1.1.12*).
- Gpio3Mode[2:0]:
  - These bits allow the selection of the GPIO[3] configuration. (See *Chapter 1.1.12*).
- Gpio2Mode[2:0]:
  - These bits allow the selection of the GPIO[2] configuration. (See *Chapter 1.1.12*).
- Gpio1Mode[2:0]:
  - These bits allow the selection of the GPIO[1] configuration. (See *Chapter 1.1.12*).
- Gpio0Mode[2:0]:
  - These bits allow the selection of the GPIO[0] configuration. (See *Chapter 1.1.12*).

2.57 GpioPadVal: GPIO pad value register [0x5C]

Table 58. GPIO pad value register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
101_0100	A2DResult1	15	0		-
		14	0	GpioPadValue[14]	-
		13	0	GpioPadValue[13]	-
		12	0	GpioPadValue[12]	-
		11	0	GpioPadValue[11]	-
		10	0	GpioPadValue[10]	-
		9	0	GpioPadValue[9]	-
		8	0	GpioPadValue[8]	-
		7	0	GpioPadValue[7]	-
		6	0	GpioPadValue[6]	-
		5	0	GpioPadValue[5]	-
		4	0	GpioPadValue[4]	-
		3	0	GpioPadValue[3]	-
		2	0	GpioPadValue[2]	-
		1	0	GpioPadValue[1]	-
		0	0	GpioPadValue[0]	-

GPIO pad value register bits description:

- GpioPadValue[14:0]:
  - These bits are read only.
  - They represent the logical value of the corresponding GPIO pin.

2.58 GpioOutVal: GPIO out value register [0x5D]

Table 59. GPIO out value register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
101_1101	GpioOutVal	15	0		
		14	0	GpioOutValue[14]	GpioOutValue[14]
		13	0	GpioOutValue[13]	GpioOutValue[13]
		12	0	GpioOutValue[12]	GpioOutValue[12]
		11	0	GpioOutValue[11]	GpioOutValue[11]
		10	0	GpioOutValue[10]	GpioOutValue[10]
		9	0	GpioOutValue[9]	GpioOutValue[9]
		8	0	GpioOutValue[8]	GpioOutValue[8]
		7	0	GpioOutValue[7]	GpioOutValue[7]
		6	0	GpioOutValue[6]	GpioOutValue[6]
		5	0	GpioOutValue[5]	GpioOutValue[5]
		4	0	GpioOutValue[4]	GpioOutValue[4]
		3	0	GpioOutValue[3]	GpioOutValue[3]
		2	0	GpioOutValue[2]	GpioOutValue[2]
		1	0	GpioOutValue[1]	GpioOutValue[1]
		0	0	GpioOutValue[0]	GpioOutValue[0]

GPIO out value register bits description:

- GpioOutValue[14:0]:
  - These bits set the value to be presented on GPIO outputs. (See *Chapter 1.1.12*).

2.59 LowVSwitchCtrl: low voltage switches control register [0x60]

Table 60. Low voltage switches control register

Address[6:0] (binary)	Register name	Bit number	Reset value(1)	Modality	
				Read	Write
110_0000	LowVSwitchCtrl	15	0	0	ClrLowVSwLth
		14	0	LowVSwIlimLth[2]	
		13	0	LowVSwIlim[2]	
		12	0	LowVSwIlimLth[1]	
		11	0	LowVSwIlim[1]	
		10	0		
		9	0		
		8	0		
		7	0		
		6	0		
		5	0		
		4	0		
		3	0		
		2	0		
		1	0	EnLowVSw[2]	EnLowVSw[2]
		0	0	EnLowVSw[1]	EnLowVSw[1]

1. The events that can reset the register to default values are:
   - Power on reset event.
   - Entering in “Low Power mode”.
   - Software reset command in the 0x08-SoftResReg register.
   - nRESET event.

Low voltage switches control bits description:

- ClrLowVSwLth:
  - This bit is write only.
  - If this bit is written to “1” it will clear LowVSwIlimLth[2:1] bits.
- LowVSwIlimLth[2]:
  - This bit is read only.
  - This bit represents the latched status of LowVSwIlim[2] bit.
- LowVSwIlim[2]:
  - This bit is read only.
  - This bit represents the output status of low voltage switch 2 current limit circuit.
- LowVSwIlimLth[1]:
  - This bit is read only.
  - This bit represents the latched status of LowVSwIlim[1] bit.
- LowVSwIlim[1]:
  - This bit is read only.
  - This bit represents the output status of low voltage switch 1 current limit circuit.
- EnLowVSw [2]:
  - If this bit is written to “1” it will enable the low voltage switch 2.
- EnLowVSw [1]:
  - If this bit is written to “1” it will enable the low voltage switch 1.

2.60 OpAmp1Ctrl: operational amplifier 1 control register [0x64]

Table 61. Operational amplifier 1 control register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality(1)	
				Read	Write
110_0100	OpAmp1Ctrl	15	0		
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0	Op1Ref[1]	Op1Ref[1]
		6	0	Op1Ref[0]	Op1Ref[0]
		5	0	Op1EnIntRef	Op1EnIntRef
		4	0	Op1BufConf	Op1BufConf
		3	0	Op1CompMode	Op1CompMode
		2	0	Op1EnMinusPin	Op1EnMinusPin
		1	0	Op1EnPlusPin	Op1EnPlusPin
		0	0	EnOp1	EnOp1

1. The operational amplifier 1 cannot be used when the device is configured as master because in this case L6460 uses GPIO[11] pin to control slaves devices. In this case the bit EnOp1 is forced at “0” and all writes to this bit will be ignored.

Operational amplifier 1 control bits description:

- Op1Ref[1:0]:
  - These bits allow the selection of the reference voltage to be selected for the non inverting pin of the operational amplifier. (See *Chapter 1.1.16*).
- Op1EnIntRef:
  - If this bit is written to “1” the non inverting input of the operational amplifier will be connected to the reference voltage selected by Op1Ref[1:0].
- Op1BufConf:
  - If this bit is written to “1” it will configure the operational amplifier as a buffer.
- Op1CompMode:
  - If this bit is written to “1” it will configure the operational amplifier in comparator mode.
- Op1EnMinusPin:
  - If this bit is written to “1” it will connect the operational amplifier inverting input to GPIO[10] pin.
- Op1EnPlusPin:
  - If this bit is written to “1” it will connect the operational amplifier non inverting input to GPIO[9] pin.
- EnOp1:
  - If this bit is written to “1” it will enable the operational amplifier 1.

2.61 OpAmp2Ctrl: operational amplifier 2 control register [0x65]

Table 62. Operational amplifier 2 control register

Address[6:0] (binary)	Register name	Bit number	Reset value	Modality	
				Read	Write
110_0101	OpAmp2Ctrl	15	0		
		14	0		
		13	0		
		12	0		
		11	0		
		10	0		
		9	0		
		8	0		
		7	0	Op2Ref[1]	Op2Ref[1]
		6	0	Op2Ref[0]	Op2Ref[0]
		5	0	Op2EnIntRef	Op2EnIntRef
		4	0	Op2BufConf	Op2BufConf
		3	0	Op2CompMode	Op2CompMode
		2	0	Op2EnMinusPin	Op2EnMinusPin
		1	0	Op2EnPlusPin	Op2EnPlusPin
		0	0	EnOp2	EnOp2

Operational amplifier 2 control bits description:

- Op2Ref[1:0]:
  - These bits allow the selection of the reference voltage to be selected for the non inverting pin of the operational amplifier. (See *Chapter 1.1.16*).
- Op2EnIntRef:
  - If this bit is written to “1” the non inverting input of the operational amplifier will be connected to the reference voltage selected by Op2Ref[1:0].
- Op2BufConf:
  - If this bit is written to “1” it will configure the operational amplifier as a buffer.
- Op2CompMode:
  - If this bit is written to “1” it will configure the operational amplifier in comparator mode.
- Op2EnMinusPin:
  - If this bit is written to “1” it will connect the operational amplifier inverting input to GPIO[12] pin.
- Op2EnPlusPin:
  - If this bit is written to “1” it will connect the operational amplifier non inverting input to GPIO[13] pin.
- EnOp2:
  - If this bit is written to “1” it will enable the operational amplifier 2.

3 Revision history

Table 63. Document revision history

Date	Revision	Changes
29-Jul-2010	1	Initial release.

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