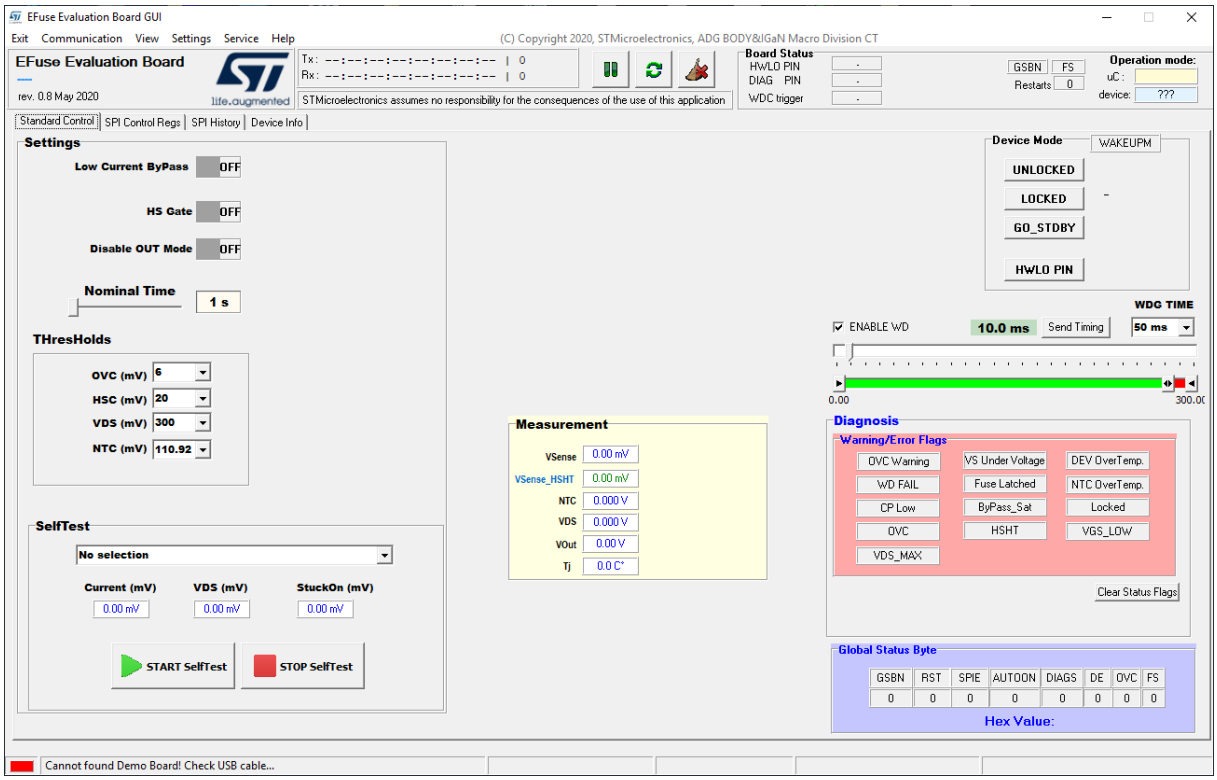
# Graphical user interface (GUI) for EV-VNF1048F

## Introduction

The STSW-EV-VNF1048F is the graphical user interface (GUI) dedicated to set and control the EV-VNF1048F using an EV-SPC582B programmed with a specific firmware able to create an advanced controller for a MOSFET in high side configuration, designed for the implementation of an intelligent high side switch for 12 V, 24 V and 48 V automotive applications.

**Figure 1. STSW-EV-VNF1048F graphical user interface**



# 1 Get software

Search on www.st.com, STSW-VNF1048 and in the “Tools & Software” section, get the software (GUI + Firmware) following the procedure.

# 2 Software installation

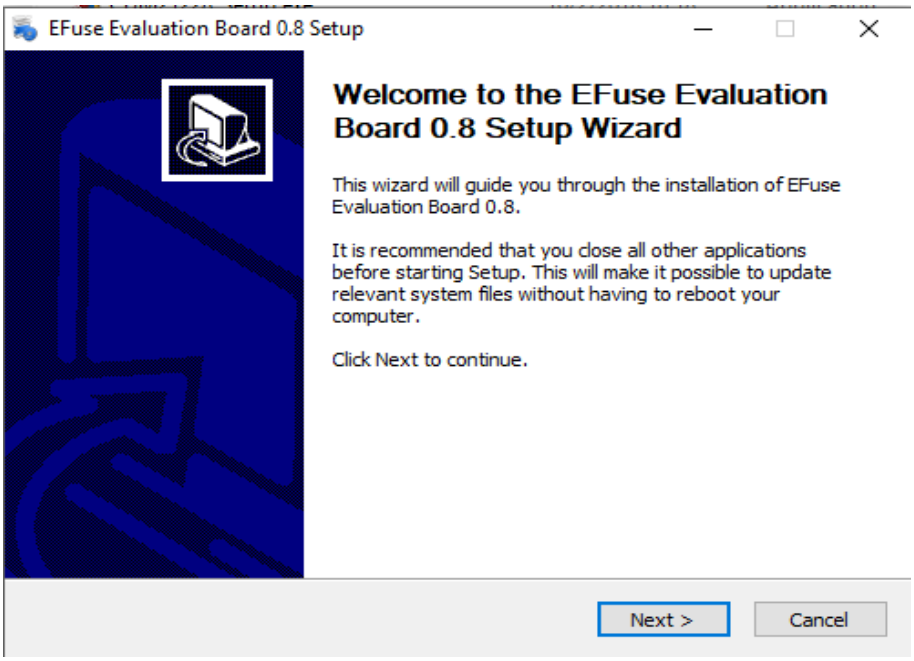
## 2.1 Firmware

Refer to the EV-SPC582B user manual.

## 2.2 GUI

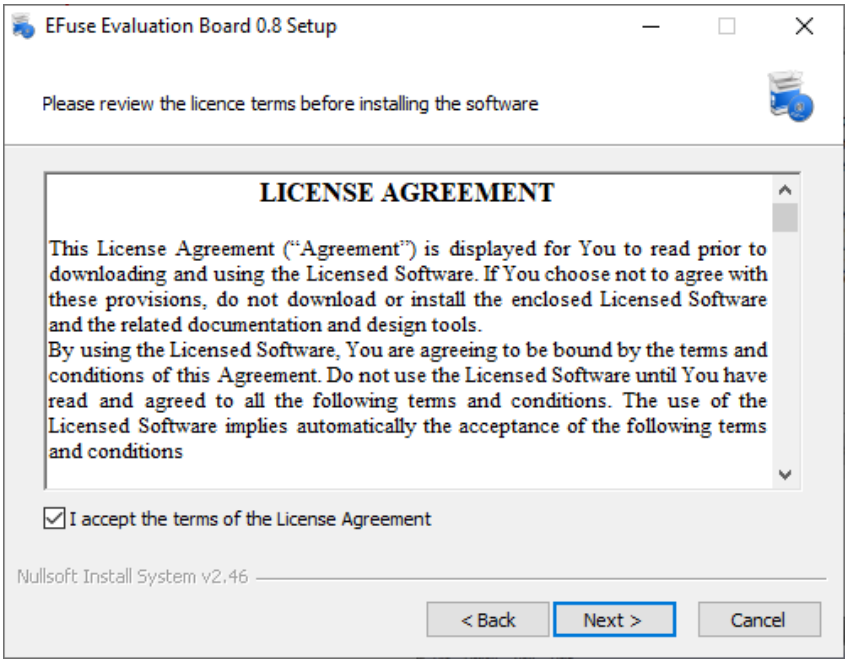
- Launch EFuse_Setup.exe

**Figure 2. Setup wizard**



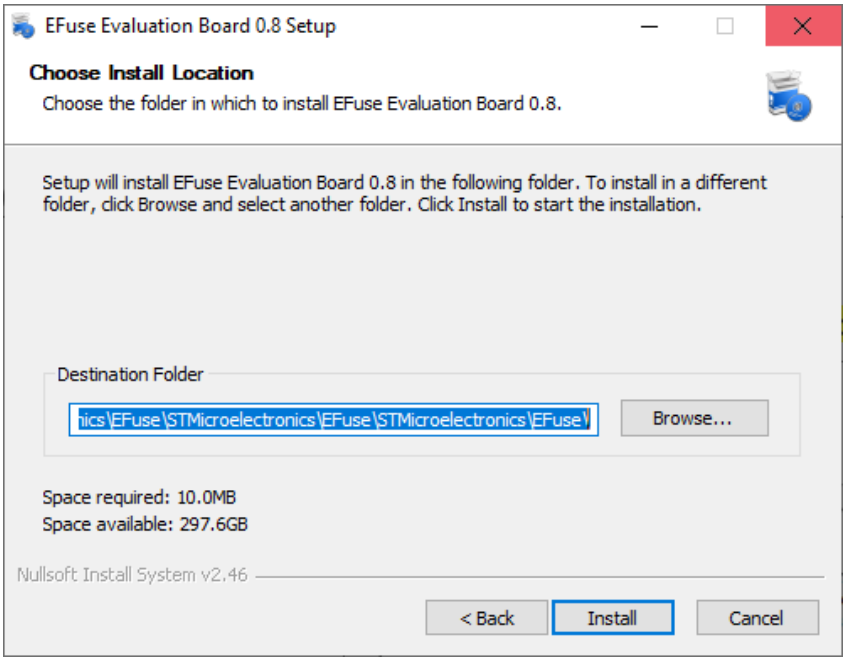

- Following step by step the wizard you will be able to install the GUI Efuse. To continue the installation you have to accept the terms of the license agreement:

Figure 3. **License agreement**



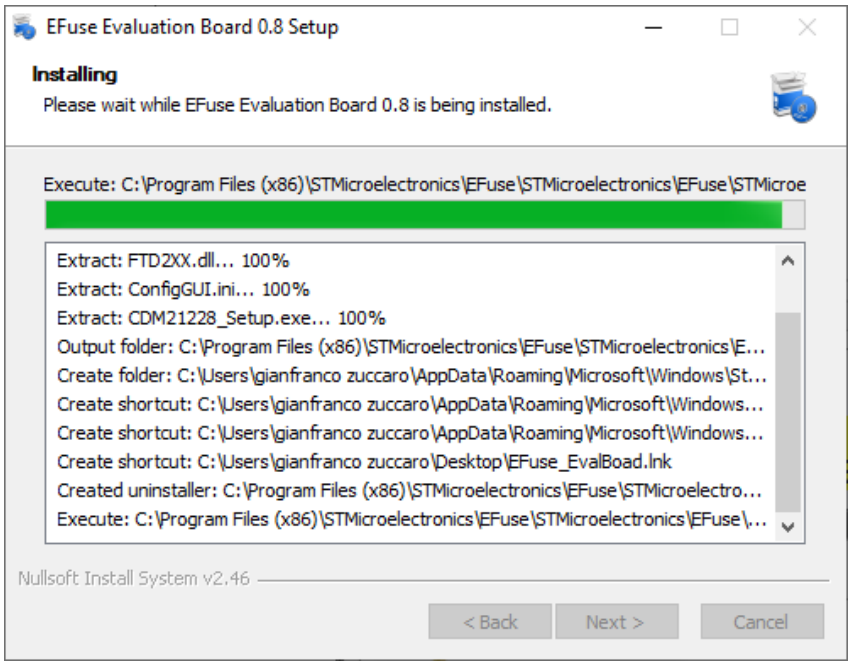

- Next you have to choose installation folder:

Figure 4. **Installation folder setup**




- The installation continues to the end:

Figure 5. **Copying files**




- Before ending the installation you will be proposed to install FTDI drivers. Skip this step if you want to install them at a different time (drivers could be obtained from the ftdichip website) or if they are already installed.

Figure 6. **FTDI installation (1/4)**

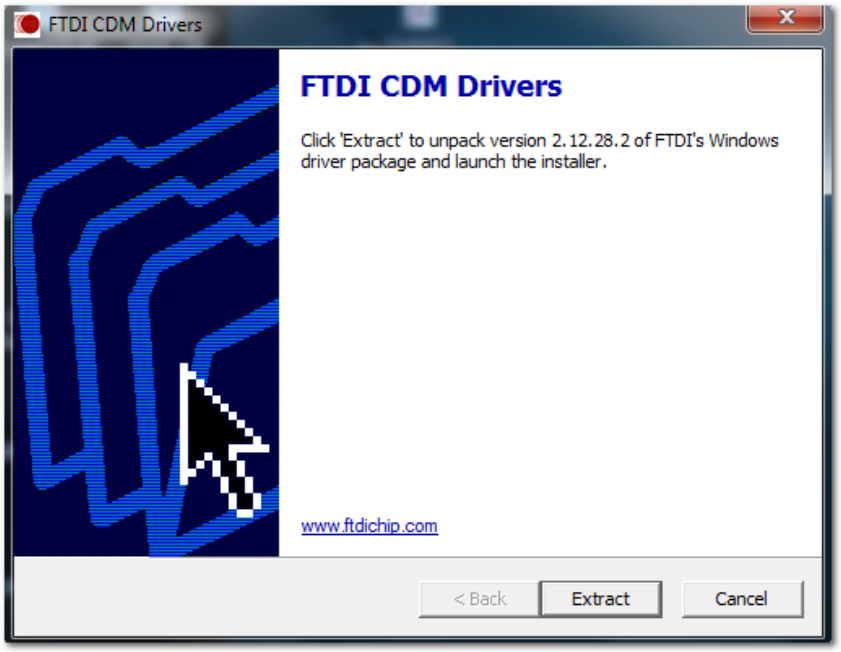


Figure 7. **FTDI installation (2/4)**

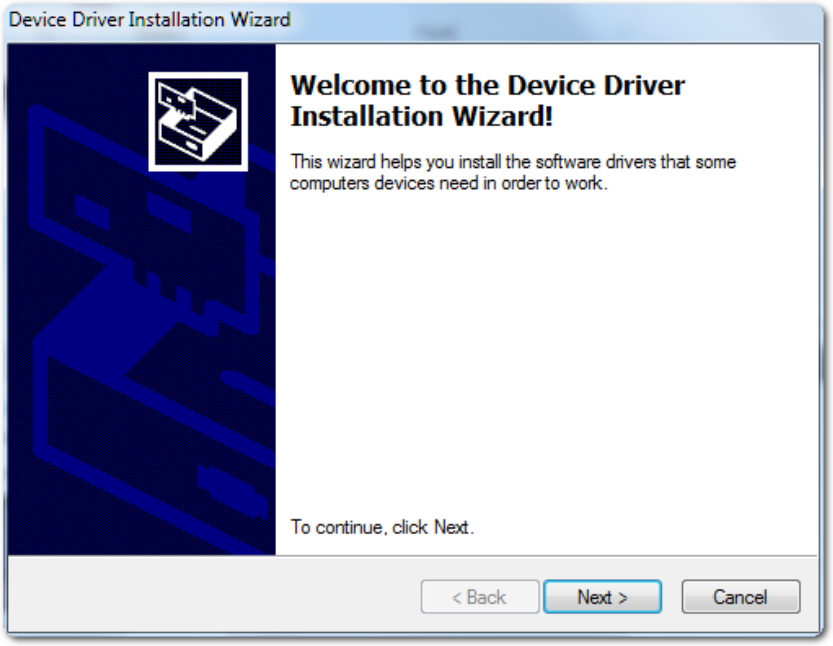
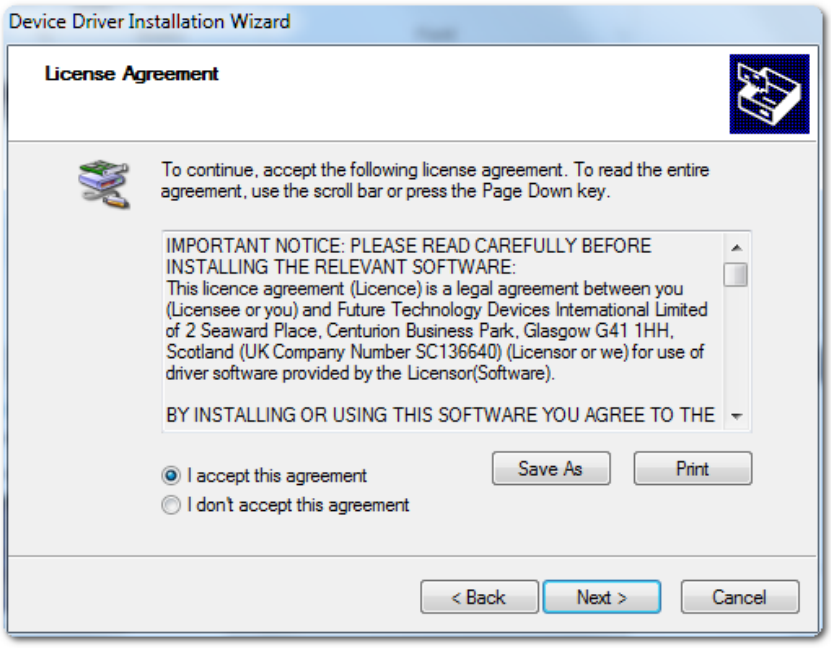
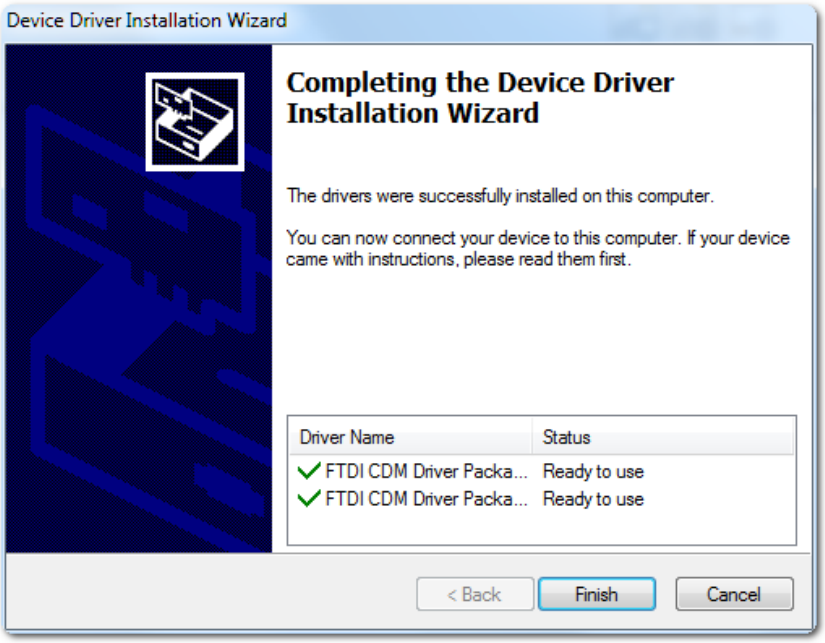



Figure 8. **FTDI installation (3/4)**




- To complete the FTDI installation the following dialog is shown to confirm the drivers were successfully installed.

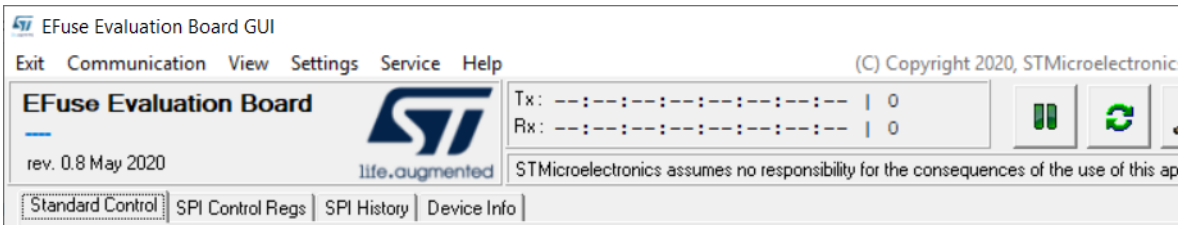
Figure 9. **FTDI installation (4/4)**



# 3 GUI description

The main form contains 4 tabs for device control

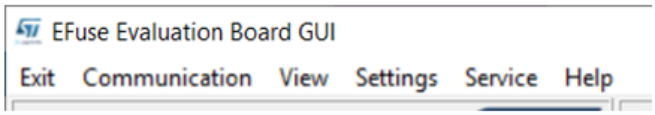
**Figure 10. Tabs for device control**




It is also embedded communication traffic monitor, showing communicated data between GUI and MCU.

## 3.1 Main menu

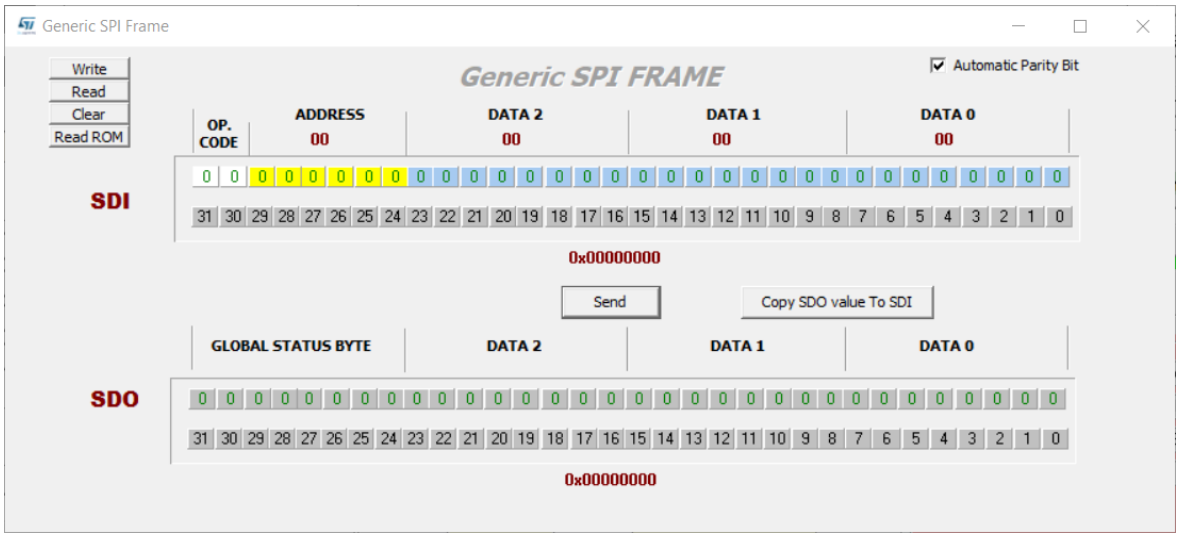
**Figure 11. Main menu**




It contains the following actions:

- Communication: possibility to Reset communication traffic and clear counters
- View: SPI registers overview
- Settings: allow to configure periodical refresh of registers
- Service: generic SPI frame allows to send a customizable SPI frame to device

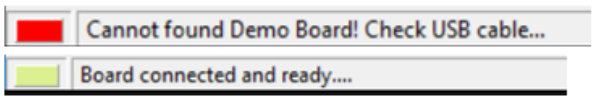
**Figure 12. Generic SPI frame**



## 3.2 Status strip

Icons show the interface status between FTDI and GUI.

**Figure 13. Status strip**

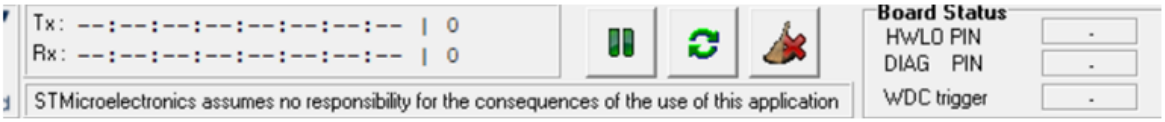



- board not connected
- normal application operation (communication between MCU and GUI correctly established)

## 3.3 Device diagnostic/communication

It shows SPI traffic detail (Tx and Rx).

**Figure 14. Diagnostic / communication panel**




Enable/Disable periodical reading of status registers and GSB

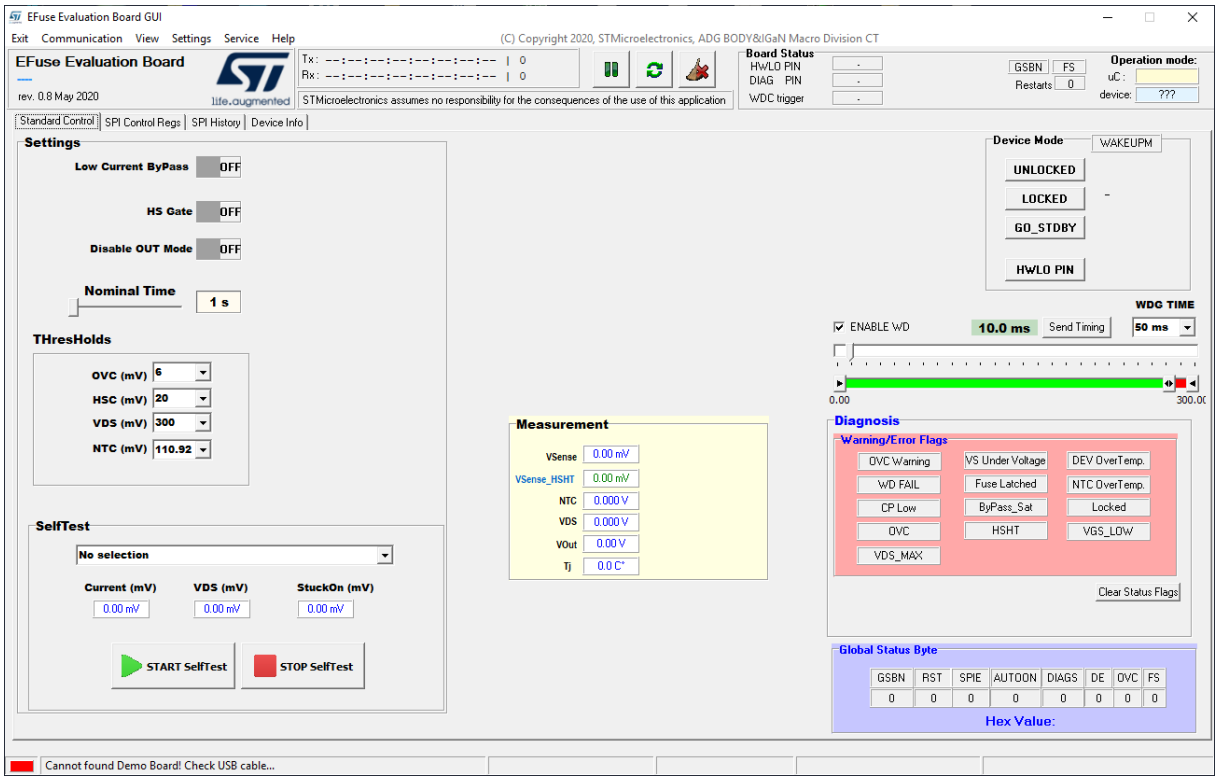
Refresh all registers (both control and status)

Clear all status registers

Board status section shows the status of the device pin HWLO and DIAG.

## 3.4 Standard control

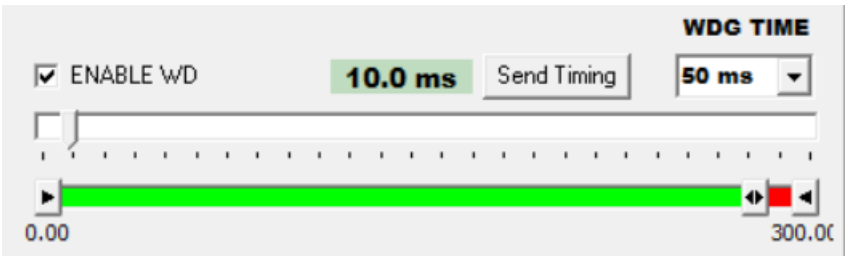
Figure 15. **Standard control**




This main tab shows the main device features, giving the possibility to apply different device modes, enable HS gate, execute self-test, set different thresholds and select diagnostic data to be periodically read and displayed or stopped.

### 3.4.1 Watchdog

Figure 16. **Watchdog**




Period for Watchdog (WD) serving is adjustable by item “WDG TIME”.

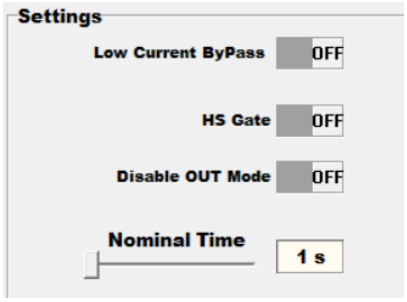
WD serving is applied by refreshing the WD_TRIG bit in one of the control registers.

Enabled WD – Enable/disable WD serving by refreshing the WD_TRIG bit

There is also the possibility to set the WD refresh time sent by MCU through a dedicated bar and button (“Send Timing”). This allows the testing of device WD timeout failure.

### 3.4.2 Settings

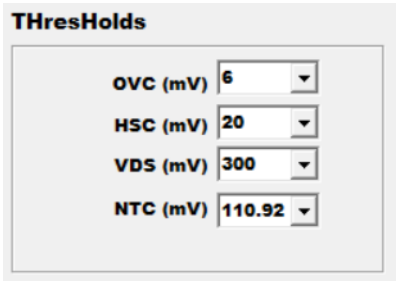
Figure 17. **Settings**




- **Low Current Bypass**:enables/disables the embedded P-channel Bypass setting bit 3 of the Control Registers 1
- **HS Gate**: enables/disables the external MOSFET setting bit 4 of Control Register 1
- **Disable OUT Mode**: configures the Watchdog behavior in Locked state setting bit 2 of Control Register 3
- **Nominal Time**: Configures the fuse nominal time setting bits from 23 to 16 of Control Register 2.

### 3.4.3 Threshold

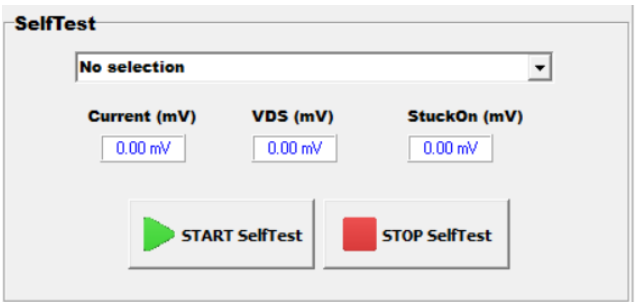
Figure 18. **Thresholds**




- **OVC**: Configures the value of Nominal Overcurrent Threshold setting bits from 15 to 11 of Control Register 2
- **HSC**: Configures the threshold for Hard Short Circuit Latch-off setting bits from 10 to 7 of Control Register 2
- **VDS**: Configures the threshold for External MOSFET desaturation shut-down setting bits from 6 to 2 of Control Register 2
- **NTC**: Configures a threshold for External MOSFET overtemperature shutdown via NTC setting bits from 8 to 5 of Control Register 3

### 3.4.4 Self-test

Figure 19. **Self-test**

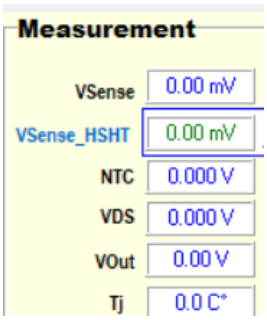



Allow to select Self-test to be executed (setting bit from 7 to 6 of Control Register 1) and to start and stop the test (setting bit 9 and bit 8 of Control Register 1).

A feedback about test result is also showed (value of Status register 5, 6, 7).

### 3.4.5 Measurements

Figure 20. **Measurements**




This section gives a status of the following status register:

- VSense: bits from 14 to 2 of Status Register 2
- Vsense_HSHT: bits from 11 to 2 of Status Register 8
- NTC: bits from 11 to 2 of Status Register 3
- VDS: bits from 22to 13 of Status Register 4
- VOut: bits from 11 to 2 of Status Register 4
- Tj: bits from 22 to 13 of Status Register 3

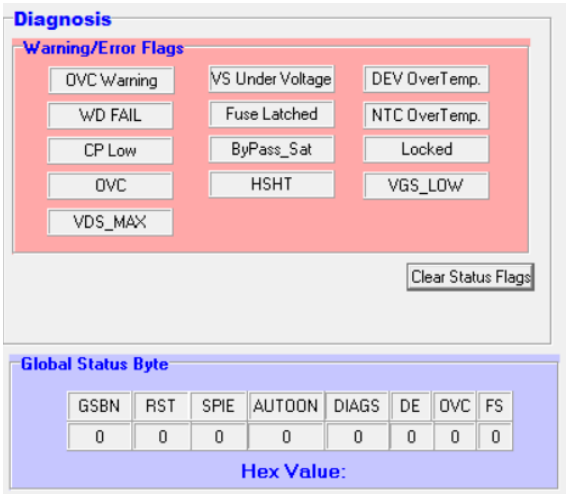
### 3.4.6 Log

Different set of registers to be periodically read from device.

### 3.4.7 Diagnosis

Diagnostic data are refreshed according to the diagnostic mode selected.

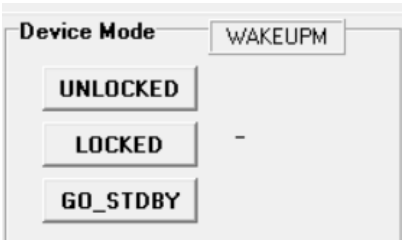
**Figure 21. Diagnosis**




"Clear Status Flag" button clears the bit of the related errors in the status register.

### 3.4.8 Device mode

**Figure 22. Device mode**




Device mode can be set by dedicated buttons.

**Figure 23. HWLO PIN button**

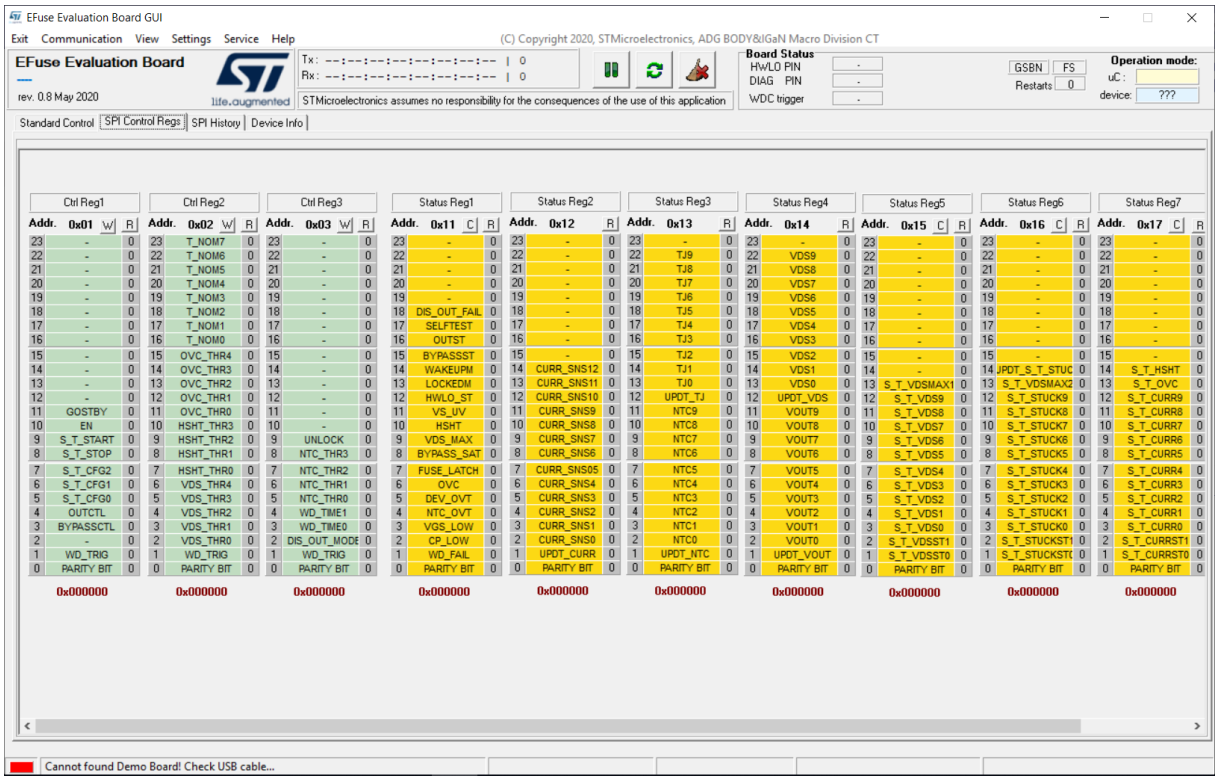

"HWLO PIN" button enables/disables device HWLO pin.

## 3.5 Registers access

The Tab “SPI Control Regs” contains the RAM control and status registers.
The Tab “Device Info” allows reading of the ROM device part.
Applicable controls for RAM registers:

1. Button R – read register content from device
2. Button W - store content of displayed register to device.
3. Button C - apply read&clear action on selected register
4. Mouse clicking on particular registry bits – change bit value for write operation (if possible).

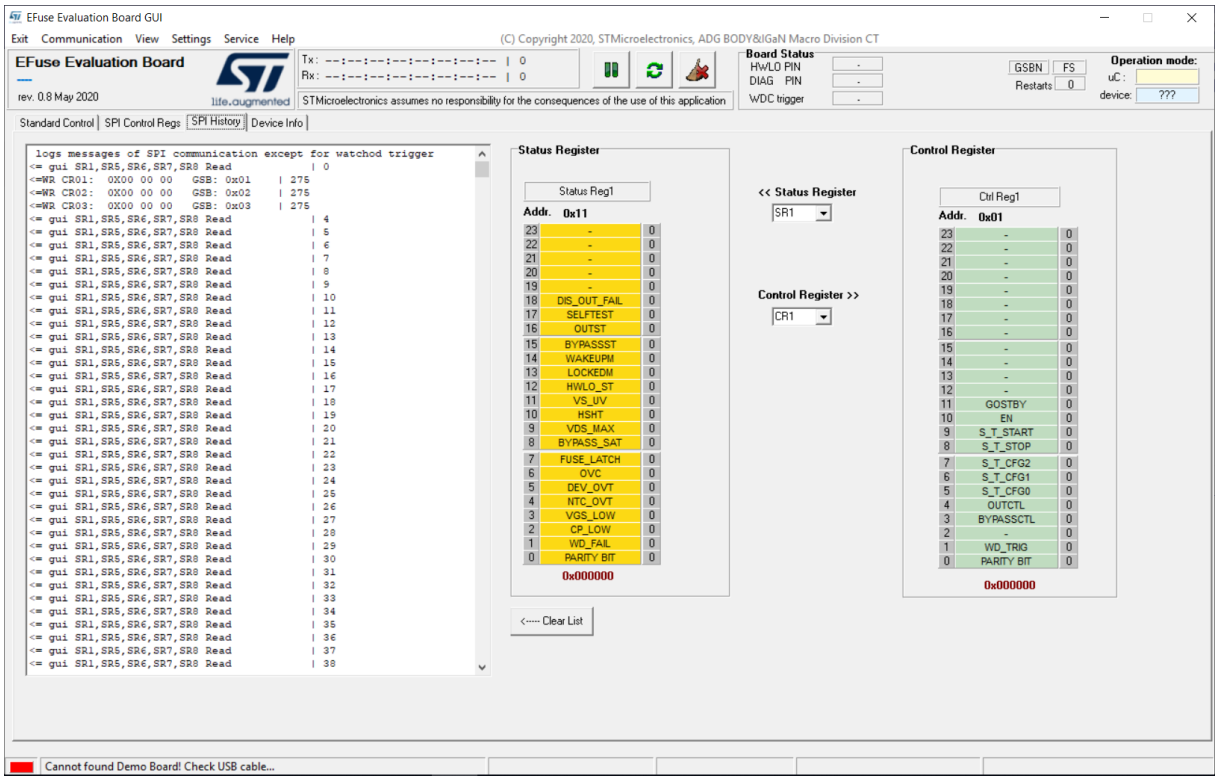
**Figure 24. SPI control register**



## 3.6 SPI history form

Display communications frames applied over GUI.

**Figure 25. SPI history form**



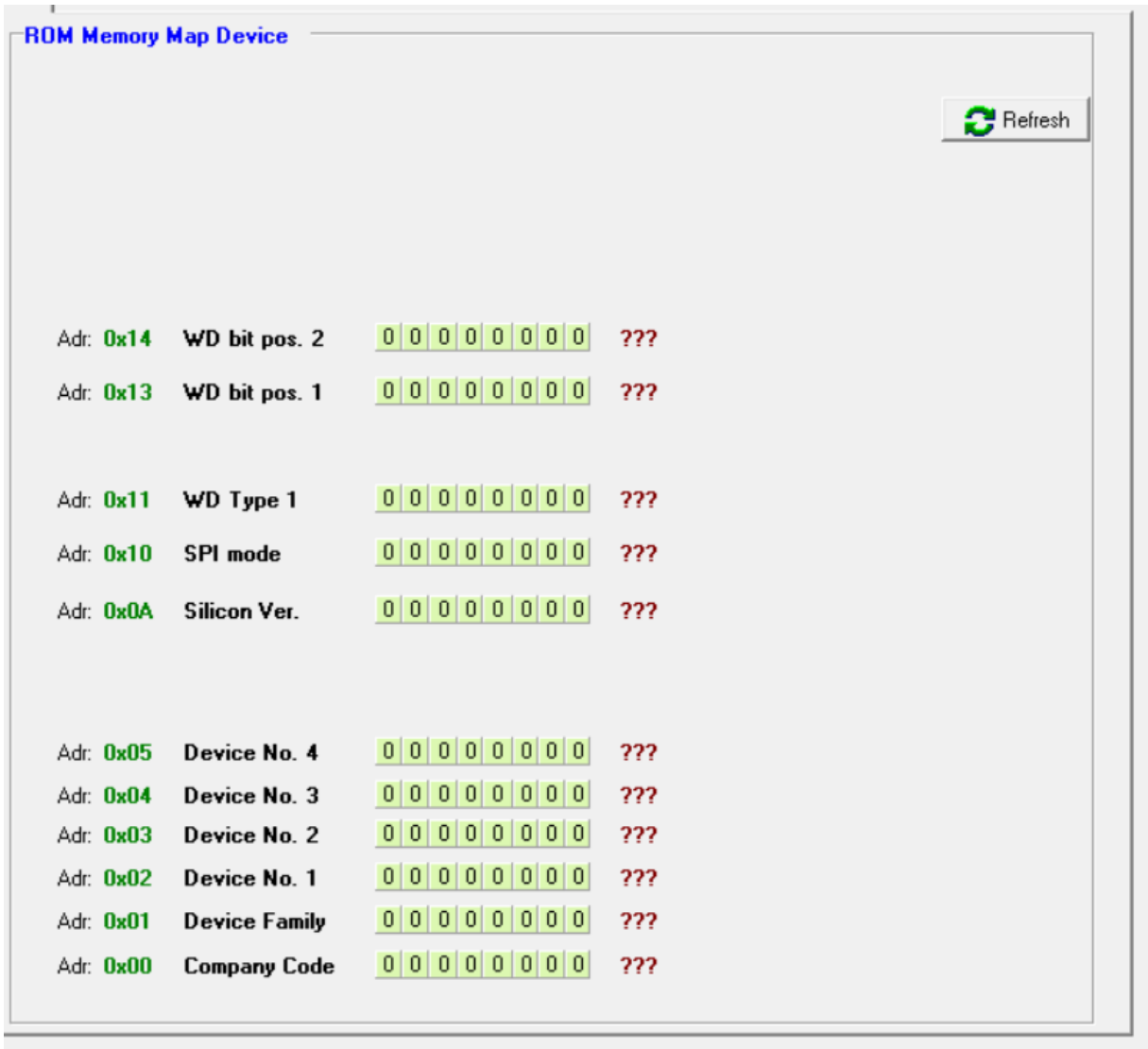

Button <----- Clear List erase all communication history from log window.

A control register and a status register can be selected for easy access.

## 3.7 Device Info

This form shows the device ROM and can be refreshed with the dedicated button.

Figure 26. **ROM memory map**



# Revision history

Table 1. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 28-Sep-2021 | 1 | Initial release. |

# Contents

# List of figures