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# **UM3044**

User manual

## Getting started with the testing platform of SiC MOSFETs for HiP247-4 packages

## **Introduction**

The [STDES-SICGP4](http://www.st.com/en/product/STDES-SICGP4?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044) is a testing platform reference design developed to test the high-speed switching performance of the ST's Silicon Carbide (SiC) MOSFETs. The platform implements a half-bridge configurations that supports HiP247-4 packages. By applying the appropriate digital signals and the correct input supplies, the board is able to generate the gate-driver commands to turn on/off the MOSFETs in the HB topology.

This platform allows testing the switching performance of the MOSFETs using the double-pulse test method. The [STDES-SICGP4](http://www.st.com/en/product/STDES-SICGP4?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044) is a fully assembled kit developed for performance evaluation only, not available for sale.



### **Figure 1. STDES-SICGP4 reference design**

## <span id="page-1-0"></span>**1 Getting started**

## **1.1 Safety precautions**



- **Warning:**  *The kit is not electrically isolated from the high-voltage supply DC input. • The evaluation kit is directly linked to the high DC voltage. No insulation is ensured between some accessible parts and the high DC voltage. • The high-side MOSFET source is switching, with reference to the common input voltage GND. All measurement equipment connected to this point must be isolated from the DC source before powering the board. It has to introduce a very low capacitance (<20 pF).*
	- *You can supply the kit only through a DC source. Take care about the correct polarity.*
- **Caution:** During assembly, testing, and operation, the evaluation kit poses several inherent hazards, including bare wires and hot surfaces.

All operations involving transportation, installation, use, and maintenance must be performed by skilled technical personnel who is familiar with the installation, use, and maintenance of power electronic systems.

#### **Work area safety**

- The work area must be clean and tidy.
- Do not work alone when the boards are powered.
- Protect the area against any unauthorized access by putting suitable barriers and signs.
- A system architecture that supplies power to the evaluation kit must be equipped with additional control and protective devices in accordance with the applicable safety requirements (that is, compliance with technical equipment and accident prevention rules).

#### **Electrical safety**

- Remove power supply from the evaluation kit and electrical loads before performing any electrical measurement.
- Arrange measurement setup, wiring, and configuration paying attention to high voltage sections.
- Once the setup is complete, power the kit.

**Danger:** *Do not touch the evaluation kit when it is powered or immediately after it has been disconnected from the voltage supply as several parts and power terminals containing potentially energized capacitors need time to discharge. Heat-sinks and transformers may still be very hot. The kit is not electrically isolated from the DC high voltage input.*

#### **Personal safety**

- Always wear suitable personal protective equipment, such as insulating gloves and safety glasses.
- Take adequate precautions and install the kit preventing accidental touch.
- Use protective shields, such as insulating box with interlocks.

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**Caution:** The kit is not equipped by EMI filter. Additionally, the fast switching of power MOSFETs can lead to high frequency oscillations, generating radiated noise.

The EMI conductive radiated emission can cross the standards limits.

#### **Conductive emissions**

To keep conductive emissions under the limit defined by EN55032, the additional EMI filter introducing attenuation in level 10 dB must be implemented.

#### **Radiated emission**

To keep EMI radiated emissions under the limit defined by EN55032, the shield introducing the attenuation of EMI noise about 40 dB in the range of 30 MHz to 100 MHz has to be applied.

#### **1.2 Overview**

The testing board contains a half bridge (HB) structure based on two high voltage SiC MOSFETs. The MOSFETs are controlled through isolated gate drivers, which are supplied via isolated DC-DC converters.

The system requires the connection of an external inductor, a source, a load, an auxiliary supply, and PWM signals. It can be used to test the operation in buck or boost configuration. You can use a low inductance shunt or assemble a coaxial shunt to measure the current through the low-side MOSFET. Thus, the board can be used as a tool for double pulse test (DPT).

The complete solution consists of several blocks: the main board, the drivers, and the DC-DC converters.



#### **Figure 2. STDES-SICGP4 block diagram**

#### **1.2.1 Main board**

The main board features two [SCTWA70N120G2V-4](https://www.st.com/en/product/SCTWA70N120G2V-4?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044) power SiC MOSFETs (Q1 and Q2), connected respectively, at the high and low side of a HB configuration.  $C_{IN}$  and  $C_{OUT}$  DC-Link foil capacitors work both as input and output capacitors, depending on the board usage in a Buck or a Boost topology. An external inductor (L) is connected between the HB center point and the  $C<sub>OUT</sub>$  capacitor.

The maximum voltage allowed on the power side is limited by both the MOSFETs and the capacitors rating. Normally the system embeds two [SCTWA70N120G2V-4](https://www.st.com/en/product/SCTWA70N120G2V-4?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044) SiC MOSFETs, able to withstand 1.2 kV, and two 1.2 kV foil capacitors, therefore the voltage must not exceed 1.0 kV.

The main board contains connectors to supply the signal side of the gate drivers and connections for PWM signals. The PWM signals have to be generated externally, for the high side and the low side separately.

<span id="page-3-0"></span>The board can be controlled through PWM signals for double pulse test. Consequently, the drain-source voltage drop and source current can be simply measured on the low side (Q2) MOSFET and used for switching energy calculation.

## **1.2.2 Driver boards**

The MOSFETs are controlled via gate drivers assembled on the separated subboards soldered to the main board. The STGAP2 rectangle in [Figure 2](#page-2-0) identifies the subboards. They embed a galvanic isolated gate driver [STGAP2HS](https://www.st.com/en/product/stgap2hs?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044) and the passive components around.

## **1.2.3 Isolated DC-DC converter**

The power part of the gate drivers is supplied through additional subboards stacked onto the driver board. These subboards contain an isolated SMPS that generates the supply voltage (positive and negative) for the gate driver.

The DC-DC converter is based on the fly-buck topology. The primary side converter is [L6986I](https://www.st.com/en/product/l6986i?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044).

The converter generates two output voltages. There is a discrete linear regulator behind each transformer winding. You can set the output voltage of the linear regulator through a resistor divider. This divider allows setting a custom gate voltage supply, depending on the tested MOSFETs.

## **1.3 Board connection**

## **1.3.1 Power terminals (J1-J6)**



#### **Figure 3. Position of connectors**

<span id="page-4-0"></span>There are the following power terminal connections:

- the DC bus between the high-side drain and the low-side source is connected to the J1 and J2 terminals (to the C3 capacitor)
- the J1 terminal is connected to the GND common power (PGND)
- the J2 terminal is connected to the HV bus line
- the J5 and J6 terminals are connected to the C6 capacitor
- the J5 terminal is connected to the GND power (PGND in the block diagram) and the J6 terminal is connected to the HV BUS line.

If the board works in buck mode, the voltage source is connected between the J2–J1 pins (J2 is connected to the positive source terminal and J1 is connected to the negative source terminal) and the J6–J5 terminals are connected to the load.

If the board is used in a boost mode, the J6–J5 terminals are connected to the voltage source (J6 is connected to the positive source and J5 is connected to the negative source terminal), while J2 and J1 terminals are connected to the load.

The J3–J4 terminals are dedicated to the connection of the power inductor.

### **1.3.2 Signal terminals (P1-P5)**

The signal side is dedicated to the connection of the auxiliary voltage (input), two PWM signals for MOSFET drivers (input), and shunt resistor sensing (output).

The auxiliary voltage and PWM signals can be connected to the board through the P1 header. The auxiliary voltage can be alternatively connected through P2 screw terminals. The PWM signals can be alternatively connected through the P3 and P4 SMA connectors.

The PWM signals can be generated through an oscillator or the MCU.

#### *Important: Avoid that both signals are set high at the same time.*

If the constant frequency is applied, both signals have to be complementary with the dead time.

You can apply a sense resistor between the source of the low-side MOSFET (Q2) and the power GND. There are two possible assembling options:

- a low inductance shunt, connected through the P5 connector MMCX
- a coaxial shunt, which is the BNC output

The shunt can be also shorted and not used. If a coaxial shunt is assembled, disassemble the low inductance shunt.

### **1.3.3 Connection summary**

#### **Table 1. Connectors and terminals**



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## **1.3.4 Typical connections**

The following figure shows the typical connection when the board is used in a buck converter mode (left side) or in a boost mode (right side).



### **Figure 4. Typical connection in buck (on the left) or boost mode (on the right)**

## **1.4 Maximum and minimum operating values**

For a safe operation, keep the voltages present on the terminals within the defined limits. The crossing of maximum values can damage the parts assembled on the PCB.

Using signal and auxiliary supply values out of the defined range can damage the board or cause it not to work properly.

Set the PWM logic level signals as defined in the table below.



#### **Table 2. Maximum and minimum values**

<span id="page-6-0"></span>

The maximum and minimum operating values refer to the original board MOSFETs. If you assemble MOSFETs with a lower  $V_{BDS}$ , adapt the limits for the J1, J2, J5, and J6 connectors.

*Important: Consider that the maximum value is valid also for the load. For instance, if the board works in the boost mode, the output voltage could reach the maximum value. Thus, you have to build an external limitation.*

#### **Table 3. PWM high and low levels: voltage ranges**



**Warning:** *• The DC supply has to be connected by respecting the signs applied on the board. The connection of a negative voltage can damage the board or parts of it. • The specification visible in [Table 2](#page-5-0) is valid for the original board. If the tested MOSFET is replaced with another device with a lower voltage, reduce the current or thermal rating maximum values of the original device [\(SCTWA70N120G2V-4\)](https://www.st.com/en/product/SCTWA70N120G2V-4?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044) accordingly.*

## **2 Testing the kit**

## **2.1 Test setup**

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To use the board, connect the external parts as shown in [Figure 4](#page-5-0).

Turn the power supplies off when they are connected to the board. Turn the first auxiliary supply on. Then, activate the PWM signal. Finally, turn on the power supply connected to the power connectors (J1 and J2 or J5 and J6).



## **2.2 Test equipment**

The auxiliary supply connected to P1 and P2 has to satisfy the following requirements:

- the supply voltage has to be within the specification defined in [Table 2](#page-5-0)
- an internal or external current limitation has to be implemented as per the level defined in [Table 2](#page-5-0)

The DC source that supplies the board input in buck or boost mode has to satisfy the following requirements:

• The requirements of the maximum voltage for J1 and J2 or J5 and J6 connectors specified in [Table 2](#page-5-0). The maximum voltage must not be crossed. Thus, if the DC source has a tolerance, the output voltage has to be set to the value lower or equal to the maximum value specified in [Table 2](#page-5-0)

The maximum input current must not cross the values specified in [Table 2.](#page-5-0) The current limitation has to be applied to limit the applied current. The current limiter can be implemented in the DC source or it can be an external component. If the current crosses the limit, turn off the DC source output.

• Reduce the current limit if the IRMSmax (see [Section 6](#page-12-0)) is lower than the maximum input current value defined in [Table 2.](#page-5-0)

• Protect the DC source output against overvoltage. If the DC source cannot guarantee this operation, apply an external surge suppressor to the input DC bus. If the protection allows any overvoltage spike, the total maximum DC voltage applied on the DC input must be set as the maximum DC voltage defined in [Table 2,](#page-5-0) reduced about the DC source voltage tolerance, and reduced about the possible voltage spike that the surge can generate.

Test the output electrical values. The load must integrate the protections listed below. Otherwise, implement these protections externally:

- The voltage on the output voltage must not cross the voltage value defined in [Table 2](#page-5-0) for J1 and J2 or J5 and J6 connectors. If the output voltage crosses the value specified in [Table 2,](#page-5-0) the in-built circuit or the externally applied circuit must sense the voltage and disconnect the input voltage DC source.
- Measure the output current through the load or through an external sensing circuit. If the output current crosses the limitation specified in [Table 2,](#page-5-0) disconnect the input DC voltage.

## **2.3 Test conditions**

While testing the board, the ambient temperature has to be within the thermal range specified in [Table 2](#page-5-0). Use a cover to protect the board in order to:

- avoid accidentally touching the board or the unisolated wires connected to the input, output, or inductor
- avoid accidentally touching the inductor
- protect against possible fire on the board
- protect against possible explosion of any components on the board

## <span id="page-8-0"></span>**2.4 Test inductor**

The inductor parameters applied to the J3 and J4 pins can be calculated by following the indications of [Section 6](#page-12-0) .

## <span id="page-9-0"></span>**3 DPT operation**

The double pulse test (DPT) allows measuring the turn on and off energy of the on-board low-side MOSFET. The simplest way is to connect input and output. It means the J6 and J2 connectors are connected through a short and low resistive wire. The test is provided on the low-side MOSFET (Q2).

The DPT operation requires the proper setting of the gate signal timing.

The signal for the high-side MOSFET is set to low. The low-side signal has to follow the timing shown in the following figure.



**Figure 5. DPT timing steps**

- 1.  $T_0$  period: both MOSFETs are turned off. The auxiliary and high power sources are connected.
- 2. T<sub>1</sub> period: low-side MSOFET is turned on. The high-side MOSFET is kept off. The inductor current rises up. At the end of the  $T_1$  period, the MOSFET current reaches the level used to test the MOSFET. The  $T_1$ duration allows programming the test current level.
- 3. T<sub>2</sub> period: if the current reaches the dedicated value, the  $T_2$  period starts from the low-side MOSFET turning off. The  $V_{DS}$  and  $I_S$  are measured during the transient for measurement of the  $E_{OFF}$  energy. The inductor current closes the loop through the high-side MOSFET. As the gate voltage of the high-side MOSFET is turned off, the current flows through the MOSFET body diode.
- 4.  $T_3$  period: at the beginning of the period, the low-side MOSFET is turned on. The V<sub>DS</sub> and I<sub>S</sub> are measured during the transient for measurement of the  $E_{ON}$  energy. This period finishes after the on energy inputs are collected.
- 5. T4 period: both MOSFETs are turned off. The inductor current flows through the high-side MOSFET body diode. The inductor slowly discharges. The period finished after the inductor current is 0 A.

## <span id="page-10-0"></span>**4 Shunt**

There are two options for the low-side MOSFET current measurement:

- Use the R22 resistor that is a low inductance shunt. The signal from this resistor is connected to the MMCX connector. It is referred to the source of the low-side MOSFET
- Use a coaxial shunt on the R13 position. In this case, disassemble R22

## **4.1 Coaxial shunt**

The coaxial shunt is not assembled in the original board. However, the PCB layout supports the use of this type of resistor.

The layout supports the version with a threaded case body with low-profile panel nuts (see R13 in [Section 8 Bill](#page-17-0) [of materials\)](#page-17-0).

This type of sense resistor is applicable to sense a fast transient signal that requires a bandwidth in the range of a hundred MHz. This is possible thanks to the coaxial shunt that has a marginal stray inductance.

To assemble a coaxial shunt, consider the following points:

- The board is originally assembled with the R22 resistor (low inductive SMD shunt). R22 is parallel to R13. The proper current sensing is possible only using one of these shunts. Therefore, if R13 is assembled, disassemble R22.
- The proper measurement considering the voltage sensing ( $V<sub>D-S</sub>$  and  $V<sub>G-S</sub>$ ) is referred to the source point of the transistor. Therefore, the coaxial shunt body, which is the grounding point, is connected to the source of the low-side MOSFET source. The middle point of the coaxial shunt is connected to the power GND of the board (power GND means that the GND is connected to the input and output capacitors and to the heat-sink). Connecting the coaxial shunt to the scope and connecting the voltage probe reference to the power GND at the same time cause the shorting of the coaxial shunt through the scope GND. Connect the voltage probe reference only to the source point of the low-side MOSFET.
- The connection of the coaxial shunt described in the previous point also causes the signal visible in the scope to be negative.
- The coaxial shunt body is close to the heat-sink. As the heat-sink is connected to the power GND, ensure that the GND of the coaxial cable connected to the coaxial shunt does not touch the heat-sink.
- When selecting the operating conditions, consider that the coaxial shunt has a limited average power dissipation.

# <span id="page-11-0"></span>**5 Gate driver supply voltage setting**

The driver isolated part is supplied via the isolated DC-DC converter. It is based on the fly-buck topology controlled through the [L6986I](https://www.st.com/en/product/l6986i?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044).

The converter generates two output voltages by two secondary windings. There is a discrete linear regulator behind each winding. You can set the output voltage of the linear regulator through a resistor divider. The voltage level connected to the VH pin of [STGAP2HS](https://www.st.com/en/product/stgap2hs?ecmp=tt9470_gl_link_feb2019&rt=um&id=UM3044) is set through the R2 and R3 resistors. The negative voltage connected to the VL pin of the gate driver is set through the R6 and R9 resistors.

The middle point of each divider is regulated to 2.5 V. The nominal setting of the gate voltage is +18 V/-3 V.

## **6 Inductor**

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The inductor is not embedded in the testing board. In the applied inductor:

- The inductance value has to be in the appropriate range
- The inductance value has not to drop below a certain level due to the operating current: that is, the inductor saturation current has to be high enough to avoid that the inductance drops below the minimum limit during the operation
- The inductor winding has to be rated to the applied voltages. It means it is rated to the voltage applied as the input and output protection.

The inductor value is defined through the following parameters:

- Inductance L (inductor inductance)
	- $-$  Saturation current  $I_{sat}$ : the current that makes the inductor to drop of about 20%
	- Maximum operating temperature
	- Maximum RMS current (IRMSmax): the current that causes the inductor thermal increase below the allowed operating temperature of the inductor for the maximum ambient temperature specified in [Table 2](#page-5-0)

## **6.1 Inductor value**

The inductor value has to guarantee that the pulse current does not saturate the inductor. The expected shortest duration of the MOSFET turn-on is considered 1 us. The inductor minimum value can be defined as:

$$
L_{\min} \ge \frac{t_{ON}V_{IN\_MAX}}{I_{MAX}}
$$

**Where** 

 $L_{\text{min}}$  is the inductance minimum value.

 $t_{ON}$  is the MOSFET turn on time. It is considered 1  $\mu$ s.

 $V_{IN-MAX}$  is the maximum input or output voltage (see [Table 2\)](#page-5-0).

I<sub>MAX</sub> is the maximum pulse inductor current. It is the lowest value among the pulse current defined for the input and for the output in [Table 2](#page-5-0) or Isat.

The maximum value of inductance is not limited.

# <span id="page-13-0"></span>**7 Schematic diagrams**



**Figure 6. STDES-SICGP4 main board circuit schematic - power section**

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### **Figure 7. STDES-SICGP4 main board circuit schematic - signal section**

<span id="page-14-0"></span>

ILS

#### **Figure 8. STDES-SICGP4 driver circuit schematic**

<span id="page-15-0"></span>





 $\overline{\text{VIN}}$ 

 $\frac{1}{\frac{1}{\text{GND}}}$ 

 $\frac{1}{\sin D}$ 

 $\overline{2}$  $\overline{4}$ 

Header 2x1

 $\frac{2}{1}$ 

Power



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### **Figure 9. STDES-SICGP4 DC-DC isolated converter circuit schematic**

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**Schematic diagrams Schematic diagramsUM3044**

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# <span id="page-17-0"></span>**8 Bill of materials**

## **Table 4. STDES-SICGP4 bill of materials**



## **Table 5. Main board bill of materials**



<span id="page-18-0"></span>

## **Table 6. Driver bill of materials**



### **Table 7. DC-DC converter bill of materials**





# <span id="page-20-0"></span>**Revision history**

## **Table 8. Document revision history**



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