

UM3077

User manual

Graphical user interface (GUI) for EV-L99LDLH32GEN

Introduction

The STSW-EVLDLH32GEN is the graphical user interface (GUI) dedicated to set and control the L99LDLH32 device assembled in the corresponding evaluation board EV-L99LDLH32GEN. The STSW-EVLDLH32GEN has been developed by using Visual Studio/C sharp and it works with the board EVAL-SPC582B programmed with a dedicated firmware.

alBoa arLED 2.3 Sep	rd tember 202	23	life.augr	mented Tx: 46:00 Rx: 46:00 STMicroele	2:01:00 2:01:03 ctronics a:	0:6C:00:00 8:6C:00:00 ssumes no resp):00:():00:(onsibility	00:FF 11 00:01 18 for the consequ	76 72 ences o	(Interpretention of the use of	II O 4	∳ Bo	ard Status WDC trigger	· ·	GSBN FS U	Deration mode: C:Re
ndard Co /M Set	ntrol Con	trol Reg rice [0,	s. PWM Control R	egs. Current Set Contr	ol Reg. Dil	N MAP & Config) Statu ols Dev	is Registers 1 ice [0,1]	Status R	legisters 2	Watch dog De	vice Info		>	BroadCast & UniCast	Frames
Dev	ice 1	- L9	9LDLH32												1	
Dev	ice 0	- L9	9LDLH32													
СН	PG MAP		DIN MAP	PWM Duty Cycle %	Hex	CURRENT	Hex		F/	AULTS		STATU	VLED	Operative Mode	Device STATUS:	Get Slave_ID
0	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT STATE	OL	SHT	OUT SHT GND		0.00 V	GO STBY	Active	Set Slave_ID 0 +
1	REGA	.00	001	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	DUT_SHT_GND		0.00 V	FAIL SAFE		
2	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	DUT_SHT_GND		0.00 V			
3	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	DUT_SHT_GND		0.00 V			
4	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V		PWM ALL	
5	REGA	.00	O ⁰¹	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V	ALL		1
6	REGA	.00	001	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V			
7	REGA	00)	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V		Global Status Byt	e 0x04
8	REGA	00	O ⁰¹	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V	7 6	5 4 3	2 1 0
9	REGA	•00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V	GSBN RST	SPIE FE2 FE1	DE GW FS
10	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V			
11	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V			4.
12	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V		Faults:	#
13	REGA	00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V	WDG Fa	al VS UV TW TSI	Clear Faults
14	REGA	•00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V	PG NO	TPREG	
15	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V			
16	REGA	.00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V			
17	REGA	.00	O ⁰¹	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	DUT_SHT_GND		0.00 V			
	REGA	00	O01	0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL	SHT	OUT_SHT_GND		0.00 V			
18																

Figure 1. STSW-EVLDLH32GEN graphical user interface



1 Get software

Search on www.st.com, STSW-EVLDLH32GEN and in the "Tools & Software" section. To get the software (GUI + Firmware) follow the procedure below.



2 Software installation

2.1 Firmware

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The board EVAL-SPC582B is programmed with a specific firmware.

2.2 GUI installation

The GUI installation has the following steps:

Launch SetupRearLed.exe



• Following step by step the wizard you are able to install the GUI RearLed. To continue the installation you have to accept the terms of the license agreement:

Figure 2. Setup wizard

Figure 3. License agreeme	nt
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Please review the licence terms before installin	g the software		
LICENSE AGREEMENT			
IMPORTANT-READ CAREFULLY: This for ST materials is made between you on entity by which you are employed or en LLA as "You" or "Licensee") and ST company incorporated under the laws of of this LLA through its Swiss branch loca 1228 Plan-les-Ouates, Geneva, Switzerlan mean any corporation, partnership, or o owns, is owned by, or is under common of ownership exists. For the purposes of	s Limited License A behalf of yourself, ngaged (collectively Microelectronics In the Netherlands act ated at 39, Chemin d ind (hereinafter "ST" other entity that, dir ownership with ST, f the foregoing, "c	Agreement or on beha y referred t internationa ing for the u Champ d). "Affiliat rectly or in for so long own", "ow	("LLA") alf of any to in this al NV, a purpose es Filles, es" shall idirectly, g as such med," or
☑ I accept the terms of the License Agreemer	nt		

Next you have to choose the installation folder:

Figure 4. Installation folder setup

Choose Install Location				1
Choose the folder in which to install RearLed Demo 2.0.				20
Setup will install RearLed Demo 2.0 in the following folder. To ins Browse and select another folder. Click Install to start the instal	stall in a d lation.	lifferen	t f <mark>old</mark> er,	<mark>c</mark> lick
Destination Folder				
Destination Folder		Brov	vse	
Destination Folder C:\Program Files (x86)\STMicroelectronics\RearLed Demo\		Brov	vse	
Destination Folder C:\Program Files (x86)\STMicroelectronics\RearLed Demo\ Space required: 16,8MB		Brov	vse	
Destination Folder C:\Program Files (x86)\STMicroelectronics\RearLed Demo\ Space required: 16.8MB Space available: 336.7GB		Brov	vse	
Destination Folder C:\Program Files (x86)\STMicroelectronics\RearLed Demo\ Space required: 16.8MB Space available: 336.7GB Isoft Install System v2.46		Brov	vse	



The installation continues till the end:

Figure 5. C	opying files			
RearLed Demo 2.0 Setup			ЦJ.	2
nstalling				-
Please wait while RearLed Demo 2.0 is being in	stalled.			6
Execute: C: \Program Files (x86) \STMicroelectr	onics \RearLed De	mo\CDM21228_	Setup.ex	2
Create shortcut: C:\Users\spizzond-adm\App	Data\Roaming\Mi	crosoft\Window	s\Start	
Create shortcut: C:\Users\spizzond-adm\Des	sktop RearLed Der	mo.lnk		
Skipped: FTD2XX.dll				_
Skipped: ConfigGUI.ini				1
Skipped: ASSP_VIP USB.zip				
Skipped: CDM21228_Setup.exe				
Create shortcut: C:\Users\spizzond-adm\App	Data Roaming Mi	crosoft\Window	s\Start	
Create shortcut: C:\Users\spizzond-adm\App	Data Roaming Mi	crosoft\Window	s\Start	
Created uninstaller: C:\Program Files (x86)\S	TMicroelectronics	RearLed Demo	uninst	e - 1
Execute: C:\Program Files (x86)\STMicroelec	tronics\RearLed D	emo\CDM21228	Setu	~
With the second se				
llsoft Install System v2.46				
	< Davis	Moset >	Con	
	< DBCK	Next>	Gan	CEI

Before ending the installation, it is proposed to install FTDI drivers. Skip this step if you want to install them at a different time (drivers could be obtained from the ftdichip website) or if they are already installed.

Figure 6. FTDI installation (1/4)



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Figure 8. FTDI installation (3/4)

Device Driver In	stallation Wizard
License Ag	reement
Ŵ	To continue, accept the following license agreement. To read the entire agreement, use the scroll bar or press the Page Down key.
	IMPORTANT NOTICE: PLEASE READ CAREFULLY BEFORE INSTALLING THE RELEVANT SOFTWARE: This licence agreement (Licence) is a legal agreement between you (Licensee or you) and Future Technology Devices International Limited of 2 Seaward Place, Centurion Business Park, Glasgow G41 1HH, Scotland (UK Company Number SC136640) (Licensor or we) for use of driver software provided by the Licensor(Software).
	BY INSTALLING OR USING THIS SOFTWARE YOU AGREE TO THE $\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \$
	 I accept this agreement I don't accept this agreement
	< Back Next > Cancel

 To complete the FTDI installation the following dialog box is shown to confirm that the drivers were successfully installed.

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Figure 9. FTDI installation (4/4)

Device Driver Installation Wiza	rd	Inc) and
	Completing the De Installation Wizard	evice Driver d
	The drivers were successfully in	stalled on this computer.
	You can now connect your devi came with instructions, please re	ice to this computer. If your device ead them first.
	Driver Name	Status
	✓ FTDI CDM Driver Packa ✓ FTDI CDM Driver Packa	Ready to use Ready to use
	< Back	Finish Cancel



3 GUI description

The main form contains four tabs for device control.

Figure 10. Tabs for device control

File Communication View Settin	gs Services He	elp (C) Copyright 2023, STMicroelectronics, ADG Low Voltage	ST IGaN Solutions	Macro Divisi	on	-		×
EvalBoard	57	Tx: 46:0C:01:00:6C:00:00:00:00:FF 1176 Rx: 46:0C:01:03:6C:00:00:00:00:00:1 1872		0 🏄	Board Status WDC trigger	GSBN FS Operation mode: Bestarts uC :	Relni	t
rev. 2.3 September 2023	life.augmented	STMicroelectronics assumes no responsibility for the consequences	of the use of this ap	plication				
Standard Control Control Regs. PWM	Control Regs. Curre	en t Set Control Reg. DIN MAP & Config Status Registers 1 Status	Registers 2 Watch	ndog Device	Info			

It is also embedded the communication traffic monitor, showing communicated data between GUI and MCU.

3.1 Main menu

Figure 11. Main menu

RearLed Evaluation Board GUI
 File Communication View Settings Services Help

It contains the following actions:

- Possibility to choose the communication interface
- View: SPI registers overview
- Settings: allow to configure periodical refresh of registers
- Service: generic SPI frame allows to send a customizable SPI frame to a specific device selected through a combo box

Figure 12. Generic SPI frame

🜆 Generic SP	I Frame					- 🗆 X
Device Dev	vice 0 🔻		Generic SPI	FRAME		
SDO	OP. CODE	ADDRESS	DATA 3	DATA 2	DATA 1	DATA 0
	39 38 37 0 0 0	7 36 35 34 33 3 0 0 0 0	32 31 30 29 28 27 26 25 24 0 0 0 0 0 0 0 0 0 0 0 0	23 22 21 20 19 18 17 16 0 0 0 0 0 0 0 0 0 0 0x000000000	15 14 13 12 11 10 9 8 0 0 0 0 0 0 0 0 0 0	7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0
SDI	GLOB4	AL STATUS BYTE	DATA 3	Send DATA 2	DATA 1	DATA 0
	39 38 3	37 36 35 34 33 0 0 0 0 0 0	32 31 30 29 28 27 26 25 2 0 0 0 0 0 0 0 0 0	4 23 22 21 20 19 18 17 1 0 0 0 0 0 0 0 0 0	6 15 14 13 12 11 10 9 8 0 0 0 0 0 0 0 0 0 0	7 6 5 4 3 2 1 0 0 0 0 0 0 0 0 0
				0x000000000		



3.2 Status strip

The icons show the interface status between FTDI and GUI.

Figure 13. Status strip Cannot found Demo Board! Check USB cable... Board connected and ready....

- board not connected
- normal application operation (communication between MCU and GUI correctly established)

3.3 Device diagnostic/communication

It shows SPI traffic detail (Tx and Rx).

Figure 14. Diagnostic/communication panel





Board status section shows the status of the device pin HWLO and DIAG.

If you choose one of the two communication buttons, described before, an pop-up menu appears where you can choose the FTDI or the serial port communication.



Figure 15. Interface configuration

💆 Select Inteface Co — 🗆 🗙	💯 Select Inteface Co — 🔲 🗙
	USB FTDI
SERIAL PORT	SERIAL PORT
	Config

By choosing the serial port option, another pop-up appears to configure the com port. Closing all the pop-up the connection starts automatically.

COM port: COM3		-	
Baud rate: COM3		500000	\$
Stop bits		Parity	
• 1 C 1,5	C 2	None	C Mark
Data hits		C Odd	C Space
C 4 C 5 C 6	C7 @ 8	C Even	
Flow control		J	
None	C DTR/RT	rs C	Xon/Xoff

Figure 16. Com port configuration



3.4 Standard control

Boar LED 3 Septe	r d ember 20.	23	life.cup	gmented	Tx: 46:0 Rx: 46:0 STMicroel	8:01:00 8:01:00 ectronics as	:00:00:0 :05:00:0 sumes no resp	0:00: 0:00: xonsibility	00:FF 11 00:01 17	1683 7817 Jences d	t if the use of	01 this application	×	WDC trigger [GSBN FS Operation mode: Restarts - UC:
ard Con	itrol Cor	ntrol Regi vice [0,1	. PwM Control	Regs. Currer	nt Set Cont	rol Reg. DIN	I MAP & Confi 1/0 Contr	g Statu ols Dev	us Registers 1 rice [0,1]	Status F	legisters 2	Watchdog De	vice Info		>	BroadCast & UniCast Frames
evi	ce O	- L99	LDLH32													
сн	PG MAP	DIN M/	P	P	WH Duty	Нех	CURRENT	Hex	FAULTS				STATU	VLED ^	Operative Mode	Device STATUS: Get Slave_ID 0
0	REGA		001		25.6 %	0xCD	1.0 mA	0x00	OUT_STATE	a	SHT	DUT_SHT_GND		0.00 V	GO STBY	Active Set Slave_ID 0 -
1 1	REGA	.00	001		7.5 %	0x08	1.0 mA	0x00	OUT_STATE	OL.	SHT	DUT_SHT_GND		0.00 V	FAIL SAFE	
2	REGA		O01		0.9 %	0x51	1.0 mA	0x00	OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V	L	
3 1	REGA	.00	O ⁰¹	Ē	-	-		-	OUT_STATE	a	SHT	DUT_SHT_GND		0.00 V		
4 1	REGA	.00	001						OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V		Pw/M ALL
5	REGA		001	Γ.	Send fra	me while tra	adving		OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V	ALL	J
6	REGA		O 01		0.0 %	0×00	1.0 mA	0x00	OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V		
7	REGA	.00	001		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V		Global Status Bute 0x04
8 8	REGA	.00	O 01		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	a	SHT	DUT_SHT_GND		0.00 V	7 6	5 4 3 2 1 0
9	REGA	.00	001		0.0 %	0×00	1.0 mA	0×00	OUT_STATE	α.	THE	DUT_SHT_GND		0.00 V	GSBN RST	SPIE FE2 FE1 DE GW FS
10	REGA		O01		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V		
11	REGA	.00	O 01		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	a	SHT	DUT_SHT_GND		0.00 V		
12	REGA	۰۵ ک	001		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V		Faults:
13	REGA	٥٥	O01		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL.	SHT	DUT_SHT_GND		0.00 V	WDGF	at VS UV TW TSD Dear Fault
14	REGA	00 ک	O01		0.0 %	0x00	1.0 mA	0×00	OUT_STATE	OL.	SHT	DUT_SHT_GND		0.00 V	PG NO	T PREG
15	REGA	۵۹	001		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V		
16	REGA	.00	O ⁰¹		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL.	SHT	DUT_SHT_GND		0.00 V		
17	REGA	<u>۵</u> 00	001		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL.	SHT	DUT_SHT_GND		0.00 V		
18	REGA		001		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	OL.	SHT	DUT_SHT_GND		0.00 V		
19	REGA	00 ک	O01		0.0 %	0x00	1.0 mA	0x00	OUT_STATE	α	SHT	DUT_SHT_GND		0.00 V		
	are a	00	0.01			1 0.00		1000		-		And the second second		· · · · · · · ·	1	

Figure 17. Standard control

This main tab shows the main device features, giving the possibility to apply different device modes, enable HS gate, execute self-test, set different thresholds and select diagnostic data to be periodically read and displayed or stopped.



3.4.1 Device control panel

0 REGA 0.0 0.0% 0x00 0.0% 0x19 OUT_STATE OL SHT DUT_SHT_GND I 1 REGA 0.00 0.0% 0x00 0.0% 0x19 OUT_STATE OL SHT DUT_SHT_GND I 2 REGA 0.00 0.0% 0x00 0.0% 0x19 OUT_STATE OL SHT DUT_SHT_GND I 3 REGA 0.00 0.0% 0x00 0.0% 0uT_STATE OL SHT DUT_SHT_GND I 4 REGA 0.00 0.0% 0x00 0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 5 REGA 0.00 0.0% 0x00 0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 6 REGA 0.00 0.0% 0x00 0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I I I I I </th <th>STATU</th> <th></th> <th></th> <th></th> <th>FAULTS</th> <th>Hex</th> <th>CURRENT</th> <th>Hex</th> <th>PWM Duty Cycle %</th> <th>AP</th> <th>DIN M</th> <th>PG MAP</th> <th>СН</th>	STATU				FAULTS	Hex	CURRENT	Hex	PWM Duty Cycle %	AP	DIN M	PG MAP	СН
1 REGA 0 0 0 0.0% 0x00 \$0.0mA 0x49 0UT_STATE 0. SHT DUT_SHT_GND 1 2 REGA 0 0 0 0.0% 0x00 \$0.0mA 0x49 0UT_STATE 0. SHT DUT_SHT_GND 1 3 REGA 0 0 0 0.0% 0x00 \$0.0mA 0x49 0UT_STATE 0. SHT DUT_SHT_GND 1 4 REGA 0 0 0.0% 0x00 \$0.0mA 0x49 0UT_STATE 0. SHT DUT_SHT_GND 1 5 REGA 0.0 0.0 0.0% 0x00 \$0.0mA 0x49 0UT_STATE 0. SHT DUT_SHT_GND 1 6 REGA 0.0 0.0 0.0% 0x00 \$0.0mA 0x49 0UT_STATE 0. SHT DUT_SHT_GND 1 7 REGA 0.0 0.0 0.0% 0x00 \$0.0mA 0x49 0UT_STATE 0. SHT DUT_SHT_GND 1 8		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	0
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4 REGA 0.00 0.00% 0x00 \$0.00A 0x49 OUT_STATE OL SHT DUT_SHT_GND I 5 REGA 0.00 0.01 0.00% 0x00 \$0.00A 0x49 OUT_STATE OL SHT DUT_SHT_GND I 6 REGA 0.00 0.01 0.00% 0x00 \$0.00A 0x49 OUT_STATE OL SHT DUT_SHT_GND I 7 REGA 0.00 0.01 0.00% 0x00 \$0.00A 0x49 OUT_STATE OL SHT DUT_SHT_GND I 8 REGA 0.00 0.01 0.00% 0x00 \$0.00A 0x19 OUT_STATE OL SHT DUT_SHT_GND I 9 REGA 0.00 0.01 0.00% 0x00 \$0.00A 0.01_STATE OL SHT DUT_SHT_GND I		DUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	O ⁰¹	00	REGA	3
5 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 6 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 7 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 8 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 9 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 10 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 11 REGA 0.00 0.01% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 12 REGA 0.00 <td></td> <td>OUT_SHT_GND</td> <td>SHT</td> <td>OL</td> <td>OUT_STATE</td> <td>0x49</td> <td>5.0 mA</td> <td>0x00</td> <td>0.0 %</td> <td>001</td> <td>● 00</td> <td>REGA</td> <td>4</td>		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	● 00	REGA	4
6 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 7 REGA 0.00 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 8 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 9 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 10 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 11 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 12 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 13 REGA 0.00		DUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	● 00	REGA	5
7 REGA 0.00 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 8 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 9 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 10 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 11 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 12 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 13 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 14 REGA 0.00<		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	6
8 REGA 0.00 0.00%		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	7
9 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 10 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 11 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 12 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 13 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 14 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 15 REGA 0.00 0.01 0.00% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 16 REGA		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	8
10 REGA 0 00 0 1 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 11 REGA 0 00 0 1 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 12 REGA 0 00 0 1 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 13 REGA 0 00 0 1 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 14 REGA 0 00 0 1 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 14 REGA 0 00 0 1 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 15 REGA 0 00 0 1 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 16 REGA		DUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	9
11 REGA 0 00 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [12 REGA 0 00 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [13 REGA 0 00 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [14 REGA 0 00 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [14 REGA 0 00 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [15 REGA 0 00 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [DUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	10
12 REGA 0 00 0 1 0.0 % 0x00 \$0.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 13 REGA 0 00 0 1 0.0 % 0x00 \$0.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 14 REGA 0 00 0 1 0.0 % 0x00 \$0.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 15 REGA 0 00 0 1 0.0 % 0x00 \$0.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 16 REGA 0 00 0 1 0.0 % 0x00 \$0.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 17 REGA 0 00 0 1 0.0 % 0x00 \$0.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 18 REGA 0 00 0 1 0.0 % 0x00 \$0.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 18		DUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	11
13 REGA 0.0 0.0 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 14 REGA 0.00 0.01 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 15 REGA 0.00 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 16 REGA 0.00 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 17 REGA 0.00 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 18 REGA 0.00 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 19 REGA 0.00 0.0% 0x00 \$.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I		DUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	● 00	REGA	12
14 REGA 0.0 0.0 \$0.0% 0x00 \$0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 15 REGA 0.00 0.0 \$0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 16 REGA 0.00 0.0 \$0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 17 REGA 0.00 0.0 \$0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 18 REGA 0.00 0.0 \$0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 18 REGA 0.00 0.0 \$0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1 19 REGA 0.00 0.0 \$0.0mA 0x49 OUT_STATE OL SHT DUT_SHT_GND 1		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	13
15 REGA 0.0 0.0		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	14
16 REGA ⁰ 0 ⁰		DUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	15
17 REGA © 00 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 18 REGA © 00 0 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I 19 REGA 000 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND I		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	O ⁰¹	● 00	REGA	16
18 REGA 00 01 0.0% 0x00 5.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	17
		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	00	REGA	18
0,0 % 0,0 % 0,0 MA 0,4 9 001_STATE OL SHI DUI_SHI_GND		OUT_SHT_GND	SHT	OL	OUT_STATE	0x49	5.0 mA	0x00	0.0 %	001	● 00	REGA	19
		STATU S I	STATU DUT_SHT_GND [DUT_SHT_GND [STATU SHT DUT_SHT_GND SHT DUT_SHT_GND	STATU OL SHT DUT_SHT_GND	FAULTS STATU S OUT_STATE OL SHT DUT_SHT_GND I OUT_STATE OL SHT DUT_SHT_GND I <td>Hex FAULTS STATU S 0x49 OUT_STATE OL SHT DUT_SHT_GND </td> <td>CURRENT Hex FAULTS STATU \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND </td> <td>HexCURRENTHexFAULTSSTATU0x00\$.0 mA0x49OUT_STATEOLSHTDUT_SHT_GND0x00\$.0 mA0x49</td> <td>PWM Duty Cycle % Hex CURRENT Hex FAULTS STATU S 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] [] [] [] <</td> <td>PWH Duty Cycle % Hex CURRENT Hex FAULTS STATU S 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND Image: constraints SHT DUT_SHT_GND Image: const</td> <td>DIN HAP PWM Duty Cycle % Hex CURRENT Hex FAULTS STATU S 0 0 0 1 0.0 % 0x0 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [0 0 0 1 0.0 % 0x0 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [<!--</td--><td>PG MAP DIN MAP PWM Duty Cycle % Hex CURRENT Hex FAULTS STATU S REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 <t< td=""></t<></td></td>	Hex FAULTS STATU S 0x49 OUT_STATE OL SHT DUT_SHT_GND	CURRENT Hex FAULTS STATU \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND	HexCURRENTHexFAULTSSTATU0x00\$.0 mA0x49OUT_STATEOLSHTDUT_SHT_GND0x00\$.0 mA0x49	PWM Duty Cycle % Hex CURRENT Hex FAULTS STATU S 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [] [] [] [] <	PWH Duty Cycle % Hex CURRENT Hex FAULTS STATU S 01 0.0 % 0x00 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND Image: constraints SHT DUT_SHT_GND Image: const	DIN HAP PWM Duty Cycle % Hex CURRENT Hex FAULTS STATU S 0 0 0 1 0.0 % 0x0 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [0 0 0 1 0.0 % 0x0 \$.0 mA 0x49 OUT_STATE OL SHT DUT_SHT_GND [</td <td>PG MAP DIN MAP PWM Duty Cycle % Hex CURRENT Hex FAULTS STATU S REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 <t< td=""></t<></td>	PG MAP DIN MAP PWM Duty Cycle % Hex CURRENT Hex FAULTS STATU S REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 REGA 0 0 0 1 0.0 % 0x00 5.0 mA 0x49 0UT_STATE 0.1 SHT DUT_SHT_GND 1 <t< td=""></t<>

Figure 18. Device control panel

This table reports all the channels of the selected device. For each channel you can set:

- DIN MAP
- Duty cycle
- Current

There is also diagnostic info:

- OL (Open load)
- SHT (Short to GND)
- SHT_VPRE (Short to VPreg)
- VLED (V indication)

3.4.2 Operative mode

Figure 19. Operative mode

	Device STATUS:	
ENABLE	berke stratos.	Get Slave_ID
GO STBY	Active	Set Slave_ID 0
FAIL SAFE		

To change device status use buttons ENABLE, GO STBY and FAIL SAFE. The device ID is managed using the buttons Get or Set Slave_ID.



3.4.3 Global status byte

Here is reported the GSB value of the device:

Figure 20. Global status byte



Figure 21. Faults



Here are reported the device warnings/errors:

- WDG fail (watchdog error)
- VS UV (undervoltage)
- TW (thermal warning)
- TSD (thermal shutdown)
- PG_NOT PREG (power not good for pre-regulator)



3.4.4 Add/Remove device form

+ - Get Device	mode 🗾	3		
Auto Scan				
Device 0	Normal 📢	UR7H Device 16	N/A	
Device 1	N/A	Device 17	N/A	
Device 2	N/A	Device 18	N/A	
Device 3	N/A	Device 19	N/A	
Device 4	N/A	Device 20	N/A	
Device 5	N/A	Device 21	N/A	
Device 6	N/A	Device 22	N/A	
Device 7	N/A	Device 23	N/A	
Device 8	N/A	Device 24	N/A	
Device 9	N/A	Device 25	N/A	
Device 10	N/A	Device 26	N/A	
Device 11	N/A	Device 27	N/A	
Device 12	N/A	Device 28	N/A	
Device 13	N/A	Device 29	N/A	
Device 14	N/A	Device 30	N/A	
Device 15	N/A	Device 31	N/A	

Figure 22. Add/Remove device form

- A new device can be added (+) or removed (-)
- Device status monitored until this checkbox "Autoscan" is checked
- Device status can be in 3 states:
 - 1. Green (normal mode)
 - 2. Red (failsafe mode)
 - 3. Yellow (standby mode)



- For each device it can be set (by right click):
 - 1. Device ID
 - 2. Type

•

- 3. Set device in normal, failsafe or standby mode
- 4. Send watchdog trigger
- 5. Read&Clear command

+ - Get Device	mode	€ 🖬			
🔽 Auto Scan					
Device 0	Normal	UR7H	Device 16	N/A	
Device 1	Norm	Set SlavelD		N/A	
Device 2	Norm	Set as UR7L		N/A	
Device 3	Norm	Set Device in .		N/A	
Device 4	Norm	Send WDG Tri		N/A	
Device 5	Norm	REad&Clear	J.	N/A	
Device 6	Normal	UR7H	Device 22	N/A	
Device 7	N/A		Device 23	N/A	
Device 8	N/A		Device 24	N/A	
Device 9	N/A		Device 25	N/A	
Device 10	N/A		Device 26	N/A	
Device 11	NZA		Device 27	N/A	
Device 12	N/A		Device 28	N/A	
Device 13	N/A		Device 29	N/A	
Device 14	N/A		Device 30	N/A	
Device 15	N/A		Device 31	N/A	

Figure 23. Device setting



3.5 Watchdog



Figure 24. Watchdog

Period for watchdog (WD) serving is adjustable by item "WDG TIME".

WD serving is applied by refreshing the WD_TRIG bit in one of the control registers.

Enabled WD-enable/disable WD serving by refreshing the WD_TRIG bit

There is also the possibility to set the WD refresh time sent by MCU through a dedicated bar and button ("Send Timing"). This allows the testing of device WD timeout failure.



3.6 Control register page



Figure 25. Control register page

This page displays the control registers for each device selected in the following combo box It is possible for each column to change the values and read or write new values by clicking the related buttons B or W.

Status register page 3.7

	1 -				Device 0	•	L99LDLH	32	1		,					
Standard Control Control	Regs. PWM Contro	I Regs. C	urrent Set Contro	Reg. D	IN MAP & Config Sta	atus F	Registers 1 Status Hegis	ters 2	Watchdog De	vice Info						
		Burst Re	ad									E	Burst Read			
				-1		-1.1	VALED ON DED	_	CTATUC 1		CTATUC O	-	CTATUS 2			
UUT_STATUS	SHI		UL		UUISHI_VPRE		VLEDUN RFR		STATUST		STATUS 2		STATUS 3		FIP_STATUS_T	FIP_STATUS_2
Addr. 0x27	Addr. 0x28		Addr. 0x29		Addr. 0x2A	_	Addr. 0x2B	A	ddr. 0x2C		Addr. 0x2D		Addr. 0x2E	_	Addr. 0x2F	Addr. 0x30
31 OUT_STATUS_CH31 1	31 SHT_CH31	0 3	0L_CH31	0	31 SHT_VPRE_CH31	0	31 VLEDON_RFR_CH31 0	31		0 31		0	31	0	31 0	31 FS_OUT_EN_CH31 0
30 OUT_STATUS_CH30 1	30 SHT_CH30	0 3	IO OL_CH30	0	30 SHT_VPRE_CH30	0	30 VLEDON_RFR_CH30 0	30		0 30		0	30	0	30 0	30 FS_OUT_EN_CH30 0
29 OUT_STATUS_CH29 1	29 SHT_CH29	0	19 OL_CH29	0	29 SHT_VPRE_CH29	0	29 VLEDON_RFR_CH29 0	29		0 29		0	29	0	29 0	29 FS_OUT_EN_CH29 0
28 OUT_STATUS_CH28 1	28 SHT_CH28	0	8 OL_CH28	0	28 SHT_VPRE_CH28	0	28 VLEDON_RFR_CH28 0	28	ті	0 28	NTC_ADC	0	28	0	28 0	28 FS_OUT_EN_CH28 0
27 OUT_STATUS_CH27 1	27 SHT_CH27	0	27 OL_CH27	0	27 SHT_VPRE_CH27	0	27 VLEDON_RFR_CH27 0	27		0 27		0	27	0	27 0	27 FS_OUT_EN_CH27 0
26 OUT_STATUS_CH26 1	26 SHT_CH26	0	CL_CH26	0	26 SHT_VPRE_CH26	0	26 VLEDON_RFR_CH26 0	26		0 26		0	26	0	26 0	26 FS_OUT_EN_CH26 0
25 OUT_STATUS_CH25 1	25 SHT_CH25	0	15 OL_CH25	0	25 SHT_VPRE_CH25	0	25 VLEDON_RFR_CH25 0	25		0 25		0	25	0	25 0	25 FS_OUT_EN_CH25 0
24 OUT_STATUS_CH24 1	24 SHT_CH24	0	4 OL_CH24	0	24 SHT_VPRE_CH24	0	24 VLEDON_RFR_CH24 0	24		0 24		0	24	0	24 0	24 FS_OUT_EN_CH24 0
23 OUT_STATUS_CH23 1	23 SHT_CH23	0	13 OL_CH23	0	23 SHT_VPRE_CH23	0	23 VLEDON_RFR_CH23 0	23		0 23		0	23	0	23 0	23 FS_OUT_EN_CH23 0
22 OUT_STATUS_CH22 1	22 SHT_CH22	0	2 OL_CH22	0	22 SHT_VPRE_CH22	0	22 VLEDON_RFR_CH22 0	22		0 22		0	22	0	22 0	22 FS_OUT_EN_CH22 0
21 OUT_STATUS_CH21 1	21 SHT_CH21	0	1 OL_CH21	0	21 SHT_VPRE_CH21	0	21 VLEDON_RFR_CH21 0	21		0 21		0	21	0	21 0	21 FS_OUT_EN_CH21 0
20 OUT_STATUS_CH20 1	20 SHT_CH20	0	0 OL_CH20	0	20 SHT_VPRE_CH20	0	20 VLEDON_RFR_CH2C 0	20		0 20	VLEDON_LOW	0	20	0	20 POR_DELAY 0	20 FS_OUT_EN_CH20 0
19 OUT_STATUS_CH19 1	19 SHT_CH19	0 1	19 OL_CH19	0	19 SHT_VPRE_CH19	0	19 VLEDON_RFR_CH19 0	19		0 19	_	0	19	0	19 0	19 FS_OUT_EN_CH19 0
18 OUT_STATUS_CH18 1	18 SHT_CH18	0 :	IS OL_CH18	0	18 SHT_VPRE_CH18	0	18 VLEDON_RFR_CH18 0	18		0 18		0	18	0	18 WD_CONF 0	18 FS_OUT_EN_CH18 0
17 OUT_STATUS_CH17 1	17 SHT_CH17	0 1	17 OL_CH17	0	17 SHT_VPRE_CH17	0	17 VLEDON_RFR_CH17 0	17		0 17		0	17 (REF_PRE_REG_M	A) 0	17 0	17 FS_OUT_EN_CH17 0
16 OUT_STATUS_CH16 1	16 SHT_CH16	0 :	IG OL_CH16	0	16 SHT_VPRE_CH16	0	16 VLEDON_RFR_CH16 0	16		0 16		0	16 DAC_RES_FAULT	0	16 PWM_FS_ALL_EN 0	16 FS_OUT_EN_CH16 0
15 OUT_STATUS_CH15 1	15 SHT_CH15	0 :	IS OL_CH15	0	15 SHT_VPRE_CH15	0	15 VLEDON_RFR_CH15 0	15		0 15		0	15 WD_FAIL	0	15 0	15 FS_OUT_EN_CH15 0
14 OUT_STATUS_CH14 1	14 SHT_CH14	0 :	14 OL_CH14	0	14 SHT_VPRE_CH14	0	14 VLEDON_RFR_CH14 0	14		0 14		0	14 VS_UV	0	14 0	14 FS_OUT_EN_CH14 0
13 OUT_STATUS_CH13 1	13 SHT_CH13	0 1	I3 OL_CH13	0	13 SHT_VPRE_CH13	0	13 VLEDON_RFR_CH13 0	13		0 13		0	13	0	13 0	13 FS_OUT_EN_CH13 0
12 OUT_STATUS_CH12 1	12 SHT_CH12	0 :	12 OL_CH12	0	12 SHT_VPRE_CH12	0	12 VLEDON_RFR_CH12 0	12	VPRE_REG	0 12		0	12 WD_STATUS	0	12 0	12 FS_OUT_EN_CH12 0
11 OUT_STATUS_CH11 1	11 SHT_CH11	0 1	11 OL_CH11	0	11 SHT_VPRE_CH11	0	11 VLEDON_RFR_CH11 0	11		0 11		0	11	0	11 0	11 FS_OUT_EN_CH11 0
10 OUT_STATUS_CH10 1	10 SHT_CH10	0 1	OL_CH10	0	10 SHT_VPRE_CH10	0	10 VLEDON_RFR_CH1C 0	10		0 10		0	10 DIN_STATUS	1	10 0	10 FS_OUT_EN_CH10 0
9 OUT_STATUS_CH9 1	9 SHT_CH9	0	9 OL_CH9	0	9 SHT_VPRE_CH9	0	9 VLEDON_RFR_CH9 0	9		0 9		0	9 NTC_FAULT	0	9 0	9 FS_OUT_EN_CH9 0
8 OUT_STATUS_CH8 1	8 SHT_CH8	0	8 OL_CH8	0	8 SHT_VPRE_CH8	0	8 VLEDON_RFR_CH8 0	8		0 8		0	8 NTC_DER_ACT	0	8 0	8 FS_OUT_EN_CH8 0
7 OUT_STATUS_CH7 1	7 SHT_CH7	0	7 OL_CH7	0	7 SHT_VPRE_CH7	0	7 VLEDON_RFR_CH7 0	7		0 7		0	7 OR_OL	0	7 0	7 FS_OUT_EN_CH7 0
6 OUT_STATUS_CH6 1	6 SHT_CH6	0	6 OL_CH6	0	6 SHT_VPRE_CH6	0	6 VLEDON_RFR_CH6 0	6		0 6		0	6 OR_SHT	0	6 0	6 FS_OUT_EN_CH6 0
5 OUT_STATUS_CH5 1	5 SHT_CH5	0	5 OL_CH5	0	5 SHT_VPRE_CH5	0	5 VLEDON_RFR_CH5 0	5		0 5		0	5 OR_OUT_STATUS	1	5 0	5 FS_OUT_EN_CH5 0
4 OUT_STATUS_CH4 1	4 SHT_CH4	0	4 OL_CH4	0	4 SHT_VPRE_CH4	0	4 VLEDON_RFR_CH4 0	4	VS	0 4		0	4 OR_OUTSHT_VPF	E O	4 WM_DUTY_ALL_AL	4 FS_OUT_EN_CH4 0
3 OUT_STATUS_CH3 1	3 SHT_CH3	0	3 OL_CH3	0	3 SHT_VPRE_CH3	0	3 VLEDON_RFR_CH3 0	3		0 3		0	3 TW	0	3 0	3 FS_OUT_EN_CH3 0
2 OUT_STATUS_CH2 1	2 SHT_CH2	0	2 OL_CH2	0	2 SHT_VPRE_CH2	0	2 VLEDON_RFR_CH2 0	2		0 2		0	2 TSD	0	2 0	2 FS_OUT_EN_CH2 0
1 OUT_STATUS_CH1 1	1 SHT_CH1	0	1 OL_CH1	0	1 SHT_VPRE_CH1	0	1 VLEDON_RFR_CH1 0	1		0 1		0	1	0	1 0	1 FS_OUT_EN_CH1 0
0 OUT_STATUS_CH0 1	0 SHT_CHO	0	0 OL_CHO	0	0 SHT_VPRE_CHO	0	0 VLEDON_RFR_CH0 0	0		0 0		0	0 PG_NOT_VPRE	1	0 0	0 FS_OUT_EN_CHO 0
OxFFFFFFFF	0x0000000	C	0x00000000	C	0x00000000 _		R 0x0000000		0x00000000		0x00000000		0x00000421	C	0x00000000	R 0x0000000

Figure 26. Status register page

This page displays the status registers for each device that you have selected in the following combo box

Device 0 💌

Burst Read It is possible to read 4 status registers at the same time by clicking "Burst Read" button

R C

, and it

is possible to read or clear some registers by clicking the related buttons



3.8 Device info

The form below shows the device ROM and can be refreshed with the dedicated button, and details about all the devices info stored in ROM:

- UR7H for L99LDLH32
- UR7L for L99LDLL16

Figure 27. ROM memory map

	Device 0 💌	L99LDLI	132		
Standard Control Control Regs. PW/M Control Regs. Current Set Control Reg. DIN	MAP & Config Statu	us Registers 1 Status Reg	isters 2 Watchdog Device In	fo]]	
DEVICE					
ROM Memory Map	Dev0 UR7H				
Adr. 0x3E	GSB Options	00000000	0x00	C Refresh	
Adr: 0x20 5	SPI CPHS test	01010101	0x55		
Adr. 0x16 V	₩D bit pos. 4	00000000	0x00		
Adr. 0x15 V	₩D bit pos. 3	0 0 0 0 0 0 0 0	0x00		
Adr. 0x14 V	₩D bit pos. 2	1 1 0 0 0 0 0 0	0xC0		
Adr. 0x13 V	₩D bit pos. 1	0 1 1 0 0 1 0 1	0x65		
Adr. 0x12	WD Type 2	0 0 0 0 0 0 0	0x00		
Adr. 0x11 V	WD Type 1	0 1 0 0 1 0 1 0	0x4A		
Adr: 0x10 5	SPI mode	0 1 0 0 0 0 0 0	0x40		
Adr. 0x0A S	Silicon Ver.	0 0 0 0 0 0 1 0	0x02		
Adr. 0x05 E	Device No. 4	0 1 0 0 1 0 0 0	0x48		
Adr. 0x04 E	Device No. 3	0 0 0 0 0 1 1 1	0x07		
Adr. 0x03 E	Device No. 2	0 1 0 1 0 0 1 0	0x52		
Adr. 0x02 E	Device No. 1	0 1 0 1 0 1 0 1	0x55		
Adr. 0x01 E	Device Family	00000010	0x02		
Adr: 0x00 0	Company Code	0 0 0 0 0 0 0	0x00		



3.9 BroadCast

The user can send a broadcast CAN frame to devices connected to the same chain setting current or duty cycle through the below dialog box.

	UniCast Frames
	Device index 0 💌
Single Read Single Read _Clear Single Write	TX-Addr TX-D3 TX-D2 TX-D1 TX-D0 11 h 22 h 33 h 44 h 55 h RX-GSB RX-D3 RX-D2 RX-D1 RX-D0 RX-D0 h
Burst Write	TX-Addr TX-D3 TX-D2 TX-D1 TX-D0 01 h 02 h 03 h 04 h 05 h TX-Addr TX-D3 TX-D2 TX-D1 TX-D0 TX-D0 11 h 12 h 13 h 14 h 15 h TX-Addr TX-D3 TX-D2 TX-D1 TX-D0 11 h 15 h TX-Addr TX-D3 TX-D2 TX-D1 TX-D0 12 h 23 h 24 h 25 h RX-GSB
Burst Read Addr 1Fh, 23h, 27h,	2Ch
TX-A Read 1F Rece	ddr TX-D3 TX-D2 TX-D1 TX-D0 h 00 h 00 h 00 h ived data (16 bytes)

Figure 28. BroadCast CAN frame



3.10 FTP programming dialog

The user can access the Non-volatile Memory (NVM) section of the selected device through the below dialog box. The user can read or write one or more memory sectors modifying single or multiple bytes.

FrmFTPFrame × Device index 0 💌 Key write, Key status (addr. 1Eh) CAN FTP CTM (apply 5V on CS pin or set CS EN bit) CS ENABLE Key write 000000CBA 00000000h => Key not accepted Key status 000000001 b >CTM Key accepted Key status 00000001 h FTP data Map - Read all FTP Read All FTP Write All 2 Write Address C Read Addr. 00h -Addr. Data Byte (hex values): FTP Write 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 DATA BYTE 15 0x80 DATA BYTE 14 0x00 DATA BYTE 13 0x00 DATA BYTE 12 0x00 1 0 1 0 ooh 01h 00 00 00 00 00 00 00 00 00 01 6C 01 01 6C 01 01 01 R W DATA BYTE 11 0x00 DATA BYTE 10 0x00 DATA BYTE 9 0x00 DATA BYTE 8 0x00 02h 00 00 00 00 00 00 00 00 01 6C 01 01 6C 01 01 01 W 03h 00 00 00 00 00 00 00 00 00 01 01 6C 01 01 6C 2B 01 R W DATA BYTE 7 0x00 DATA BYTE 6 0x00 DATA BYTE 5 0x00 DATA BYTE 4 0x00 04h 00 00 00 00 00 00 00 00 00 6C 01 01 6C 01 01 01 6C R W 05h RW DATA BYTE 3 0x00 DATA BYTE 2 0x00 DATA BYTE 1 0x00 DATA BYTE 0 0x00 06h RW 07h RW 08h RW RW 09h OAh RW OBh 00 00 00 00 00 00 00 00 00 00 00 C8 21 E0 0F EA 89 R W ODh RW 0Eh RW OFh RW

Figure 29. FTP programming dialog

Revision history

Table 1. Document revision history

Date	Revision	Changes
16-Sep-2022	1	Initial release.
25-Jun-2024	2	Updated Figure 1. STSW-EVLDLH32GEN graphical user interface, Figure 10. Tabs for device control, Section 3.1: Main menu, Section 3.3: Device diagnostic/communication, Figure 17. Standard control and Figure 25. Control register page.



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