How to integrate and configure the VD55G1 sensor

Introduction

This document is the user manual for the VD55G1 0.6 megapixel global shutter image sensor. It should be read in conjunction with the VD55G1 datasheet. The aim of this document is to provide further technical details about the VD55G1 and guidance on how to configure it for different applications.

Refer to the VD55G1 datasheet for information concerning the device functionalities and performances.

1 Acronyms and abbreviations

Table 1. Acronyms and abbreviations

Acronym/abbreviation	Definition
AE	auto exposure
AWU	auto wakeup
BCR	bus characteristic register
CCC	common command code
CE	chip enable
CSI	camera serial interface
DCR	device characteristic register
DMA	direct memory access
ECC	error correcting code
ENTDAA	enter dynamic address assignment
EOT	end of transmission
FOV	field of view
FW	firmware
FSM	firmware state machine
HAL	hardware abstraction layer
ID	identity / identification
ISL	intelligent status line
ISP	image signal processor
NVM	nonvolatile memory
OF	optical flow
PCB	printed circuit board
PLL	phase-locked loop
PWL	piece-wise linear
PWM	pulse-width modulation
RSTDAA	reset dynamic address assignment
ROI	region of interest
Rx	receiver
SCL	serial clock line
SDA	serial data line
SDR	single data rate
SNR	signal-to-noise ratio
Tx	transmitter
UI	user interface

2 Application schematic

Information on the application schematic and the layout recommendations are provided in the datasheet. This section explains the integration of the image sensor into an application from a hardware perspective.

2.1 Power supplies

To power on the device, all the external supplies (VCORE, VDDIO, and VANA) must be properly provided according to the device characteristics described in the Electrical characteristics section of the VD55G1 datasheet. Each supply should be in the operating range for a standard application configuration and compatible with the device power consumption (average and peak current).

2.2 Hardware reset (XSHUTDOWN)

The XSHUTDOWN pin mode manages the device chip state.

- At low level, the device is in power down state
- At high level, the device is active if all the power supplies are present

Refer to the device datasheets for the electrical specifications of the XSHUTDOWN pin.

2.3 Input clock

The device needs to be provided with an input clock to operate correctly. Refer to the Electrical characteristics section of the datasheet for the constraints of the input clock.

2.4 I2C interface

2.4.1 CCI protocol

The device is controlled via an I2C interface as defined by the MIPI CSI-2 specification (refer to *MIPI Alliance Standard for Camera Serial Interface 2).*

The device uses the CCI protocol over I2C. Details of this interface can be found in the device datasheet.

The value of the pull-up resistors, on the SDA and SCL signals, must be chosen to ensure the I2C bus constraints are met in fast mode+. If the device has to be used in fast mode, the correct pull-up resistors must be selected to support fast mode and fast mode+. The default configuration of the device is fast mode+. The switch to fast mode is only available in the software standby state.

2.4.2 Data alignment within registers

Registers larger than 8 bits wide are stored LSB (least significant byte) first, that is, the LSB is placed in the location with the lowest index (little endian).

Note: This ordering of multibyte registers is contrary to the recommended byte ordering detailed in the MIPI CSI-2 specification which states that multibyte registers should be stored MSB first.

2.5 MIPI CSI-2 transmitter interface

The VD55G1 device outputs a frame through a MIPI CSI-2 with the following characteristics:

- Data and clock polarity can be inverted

These configurations are detailed in Section 15: Output interface.

2.6 GPIO interface

The VD55G1 has four GPIOs which synchronize signals or act as in/out general purpose pins.

3 Control interface

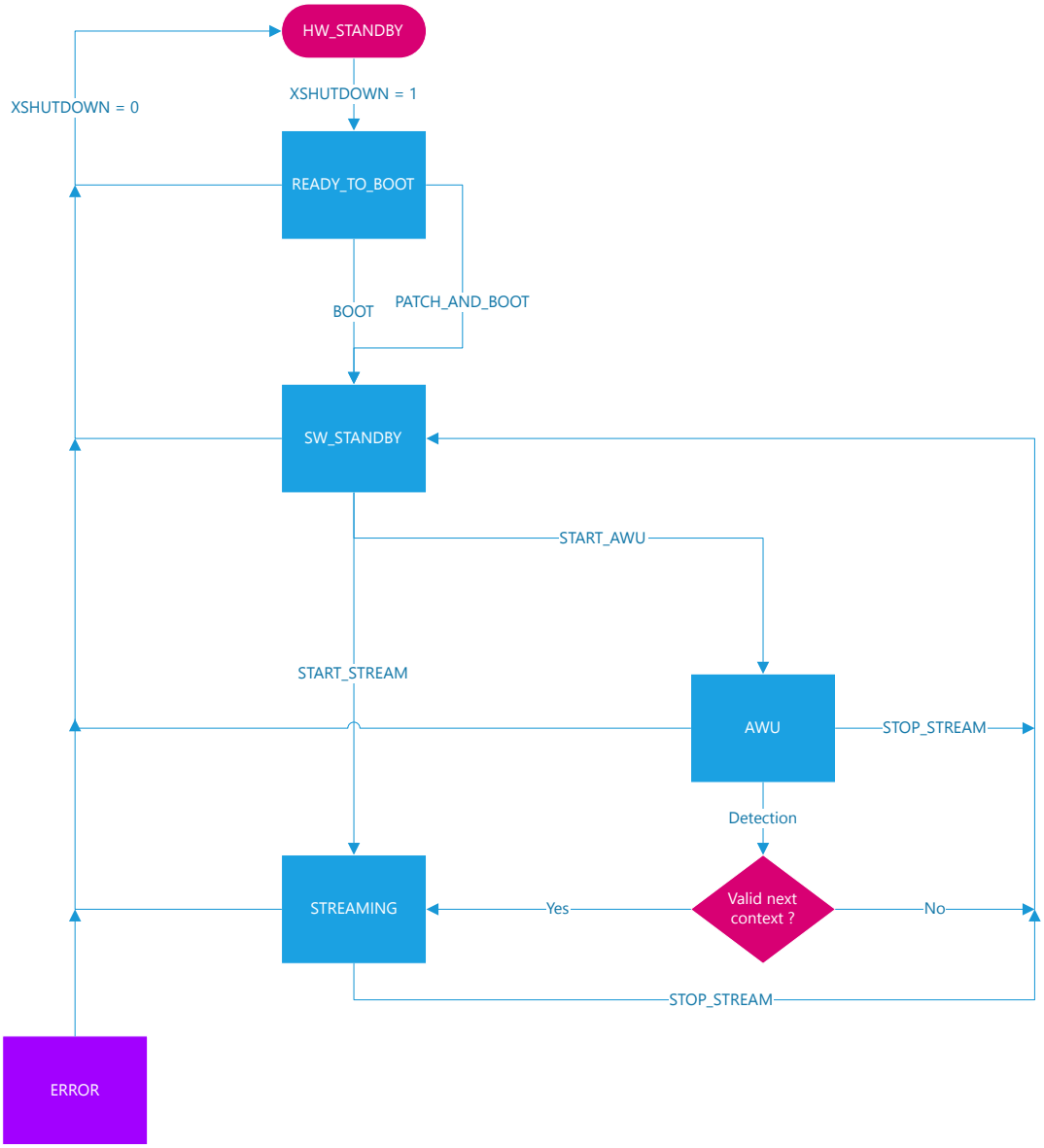
3.1 Register default value

The register default value depends on the device state. The default value, after device reset, may differ from the register default values observed once the firmware is in SW standby state.

The default values listed in this document are those observed in device SW standby state after the boot command is complete.

4 Firmware state machine

Figure 1. **Firmware state machine**



The SYSTEM_ FSM register in the STATUS group indicates the state of the device.

5 Steps from device power up to sensor streaming state

This section describes the steps to follow from device power up to sensor streaming state. A power-up sequence diagram is provided in the product datasheet.

5.1 Device power up sequence

To power on the device, all the external supplies (VCORE, VDDIO, VANA) must be properly provided according to the device characteristics described in the section Electrical characteristics of the datasheet. XSHUTDOWN must stay low. The device is in HW_STBY state.

5.2 Transition to READY-TO-BOOT

The CLKIN signal must be provided before the XSHUTDOWN pin can be set high. See the product datasheet for device signal specifications. The time between the release of the XSHUTDOWN pin and READY_TO_BOOT state depends on the external clock frequency due to firmware activity. The I2C interface is not operational before reaching the READY_TO_BOOT state. If the device answers an I2C request, it means the READY_TO_BOOT state has been reached.

5.3 READY_TO_BOOT

Once the device is in READY_TO_BOOT state, the host can configure I2C and must (with or without firmware patch) boot the sensor as follows:

1. Configure the I2C interface regarding the device address and I2C protocol to be used for read and write operations (see Section 11: I2C interface configuration).
2. Upload a firmware patch and boot. The firmware patch upload procedure is described in Section 9: Firmware patch
3. Issue a BOOT command to go to software standby state.

5.4 SW_STBY

From SW_STBY state, the host can perform the following actions:

- Configure the clock and PLL using the UI (see Section 12: Timings).
- Perform all static, dynamic, and context configurations such as synchronization, ISP, output image, exposure, gain, and context chain.
- Perform a thermal sensor read (see Section 16: Temperature)
- Read/write into the NVM memory (see Section 10: NVM).

Once these operations have been completed, the host must issue a START_STREAM command to go to streaming state, or START_AWU to initiate an auto wake-up session.

5.5 Streaming

In this state, the sensor streams frames depending on the host configuration previously set in standby state.

Alternatively, from the streaming state, the host can perform the following actions:

- Perform all “dynamic” configurations regarding image streaming through the dynamic or context register groups.
- Stop streaming by issuing a STOP_STREAM command. This makes the sensor go back to software standby state.

6 Steps to power down the device from sensor STREAMING state

This section describes how to power down the device starting from the sensor streaming state. A power down flow chart is available in the product datasheets. The power down steps are summarized as follows:

1. The host issues a STOP_STREAM command. This stops the current streaming and the device goes to standby state.
2. In SW_STBY state, the external clock signal, CLKIN, must be disabled and the XSHUTDOWN pin must be set to low. This sets the device to HW_STBY state.
3. Finally, the power supplies (VCORE, VDDIO, and VANA) can be driven down in any order. This turns the device off.

7 Commands management

The host sends commands through the UI by writing into different registers. An interrupt is raised to inform the firmware that a command has been issued, then the command is processed in the FSM. Once a command has been executed, the same register is cleared to indicate the command has been acknowledged. If a command is issued before the previous command has been acknowledged, the new command is ignored. If the command is not acknowledged, such status is updated in the ERROR_CODE register (Section 8: Error code).

8 Error code

If a command cannot be achieved or an error occurs during streaming, the device goes into an error state. In this case, the ERROR_CODE is different from 0x0000. The device must be rebooted.

9 Firmware patch

A firmware patch can be loaded in the READY_TO_BOOT state. To do so, perform the following actions:

1. Load the binary patch at address 0x2000.
2. Issue the PATCH_AND_BOOT command.

The firmware patch version is available in the STATUS register FWPATCH_REVISION.

10 NVM

Several 32-bit words are available in the NVM for customer use. Below is the procedure to program one or more consecutive words. The sensor must be in SW_STBY. This NVM is an OTP memory (one-time programmable).

- Write in the NVM mirror register group the needed values. Registers must be consecutive.
- Set the NVM_START_ADDRESS and NVM_NB_OF_WORD accordingly to specify what needs to be burnt.
  - The NVM_START_ADDRESS is the offset of the first byte to write in the NVM. To calculate this value, remove 0x640 from the targeted NVM register index. Example for the first customer area coordinates: NVM_START_ADDRESS = 0x7c = 0x6bc–0x640.
  - The NVM_NB_OF_WORD is the number of words to write in the NVM: 1 WORD = 4 bytes
- Issue an NVM_PROG command (see command registers).

An NVM_READ command can be run to reload values from the NVM in the NVM mirror registers.

This command also uses the values set in the NVM_START_ADDRESS and NVM_NB_OF_WORD.

The content of the NVM is automatically loaded at boot in the NVM mirror registers (see Appendix H.11: NVM_MIRROR registers).

The NVM customer area has a specific word: I2C_ADDRESS. This word controls the default I2C address at powerup. This feature is doubly protected as follows:

1. I2C address must be replicated in byte 0, byte 1 and byte 2
2. Security key 0xAA is set in byte 3 (MSB)

If the conditions are wrong, the I2C address is not updated.

I2C sequence example to write the first four words of the NVM

```
// Set NVM_NB_OF_WORDS
WriteAutoIncrement(0x0229, 0x3); // UI.SENSOR_SETTINGS.NVM_NB_OF_WORDS

//NVM address to write {0x7C}:
WriteAutoIncrement(0x022a, 0x7C); // UI.SENSOR_SETTINGS.NVM_START_ADDRESS

// Write 4 words
WriteAutoIncrement(0x06bC, 0x00, 0x02, 0x03, 0x04); // UI.NVM_MIRROR.CTM_AREA_0
WriteAutoIncrement(0x06bC, 0x05, 0x06, 0x07, 0x08); // UI.NVM_MIRROR.CTM_AREA_1
WriteAutoIncrement(0x06bC, 0x09, 0x0A, 0x0B, 0x0C); // UI.NVM_MIRROR.CTM_AREA_2
WriteAutoIncrement(0x06bC, 0x0D, 0x0E, 0x0F, 0x10); // UI.NVM_MIRROR.CTM_AREA_3

// Send NVM_PROG command
WriteByte(0x0201, 0x03); // UI.CMD.STBY

// Wait for command acknowledge
WaitValueEx(0x0201, 0x0); // UI.CMD.STBY.COMMAND
```

11 I2C interface configuration

The I2C default configuration is fast mode+ (which is compatible with fast mode).

The I2C control interface supports different slave IDs for read and write operations. By default, these addresses are either loaded from the NVM memory content (configured during device manufacturing test operations) or written to a default value by the firmware if the NVM is empty.

Without specific access, the I2C address does not change during device operations.

11.1 Temporary new address

Once the device is in standby state, the I2C address can be updated by the host controller. The update sequence is as follows:

1. Ensure the device is in SW_STBY state.
2. The host writes the new configuration into the DEVICE_ID bit fields of the DEVICE_COMMS_CTRL register.
3. The host issues an DEVICE_COMMS_UPDATE command from the STBY command register.

The new address is effective for the next I2C access until the device reboots (power down, power up).

```
// Write new address: 0x40 ( 7bit: 0x20 )
WriteAutoIncrement(0x0230, 0x40, 0x01); // UI.SENSOR_SETTINGS.DEVICE_COMMS_CTRL

// Send DEVICE_COMMS_UPDATE command
WriteAutoIncrement (0x0201, 0x05); // UI.CMD.STBY

// Wait for command acknowledge
WaitValueEx(11, 0x0201, 0x0, 0); // UI.CMD.STBY.COMMAND
```

11.2 Permanent new address

The new I2C address can be stored in the NVM by the host controller. The update sequence is as follows:

1. Ensure that the device is in SW STANDBY state.
2. The host writes the new configuration into the I2C_DEVICEID_(1/2/3) bit fields of the I2C_ADDRESS register of the NVM section.
3. The host writes the 0xAA key into the I2C_KEY bit field of the I2C_ADDRESS register of the NVM section.
4. The host initiates an NVM write of a single 32-bit word at offset 0x78 (0x6b8 - 0x640)
5. The host issues the NVM_PROG command from the STBY command register.

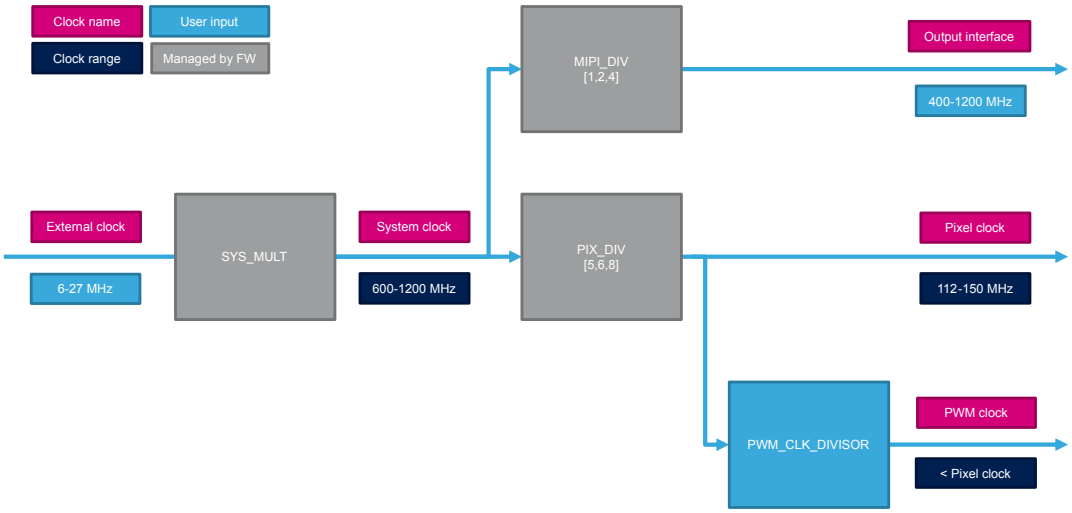
The new address is effective after the next device reboots (power down, power up).

```
// Set NVM_NB_OF_WORDS
WriteAutoIncrement(0x0229, 0x1); // UI.SENSOR_SETTINGS.NVM_NB_OF_WORDS

//NVM address to write {0x78}:
WriteAutoIncrement(0x022a, 0x78); // UI.SENSOR_SETTINGS.NVM_START_ADDRESS

// Write key and new address: 0x30 ( 7bit: 0x18 )
WriteAutoIncrement(0x06b8, 0x18, 0x18, 0x18, 0xaa); // UI.NVM_MIRROR.I2C_ADDRESS

// Send NVM_PROG command
WriteByte(0x0201, 0x03); // UI.CMD.STBY

// Wait for command acknowledge
WaitValueEx(0x0201, 0x0); // UI.CMD.STBY.COMMAND
```

12 Timings

12.1 Clock tree

Figure 2. **Clock tree**



12.2 External clock source frequency configuration

The device supports a range of external clock source frequencies. Refer to the product datasheet for information on the clock sources supported.

Once the device is in standby state, the host controller can update the external clock frequency configuration.

The new frequency configuration is used for internal PLL configurations. It is effective once the device is in streaming state, until the device reboots (power down, power up).

12.3 Output interface clock

The VD55G1 is dependent on this output interface. Line length should be adapted based on this clock speed (see Section 12.5: Line time for more details). If the requested BIT_RATE is not reachable, the firmware sets the closest, lowest, achievable frequency. The host can check the frequency in the status registers once the device is in streaming state.

The host can configure the output interface speed through the MIPI_DATA_RATE register. First the MIPI_DIV is automatically selected based on the following table.

Table 2. MIPI divider

Output interface speed (Mbps)	MIPI_DIV
[250-300]	4
]300-600]	2
]600-1200]	1

The SYS_MULT is computed with the following formula.

$$SYS\_MULT = \frac{MIPI\_DATA\_RATE}{EXT\_CLOCK \times MIPI\_DIV}$$

Based on this, the output interface clock is the following

$$OutputInterface = \frac{Externalclock \times SYS\_MULT}{MIPI\_DIV}$$

12.4 Pixel clock

The pixel clock is derived from the system clock based on the following table and formula to be in the range of 112-156 MHz.

Table 3. Pixel divider

System clock (MHz)	PIX_DIV
[600-780]	5
]780-900]	6
]900-1200]	8

$$Pixelclock = \frac{Externalclock \times SYS\_MULT}{PIX\_DIV}$$

12.5 Line time

Line time can be set using the LINE_LENGTH register.

Line time can be computed as follows:

$$time_{Line} = \frac{LINE\_LENGTH}{Pixelclock}$$

Use the following table to obtain the minimum LINE_LENGTH based on the ADC_MODE.

Table 4. Minimum line lengths

ADC_MODE	Line length
10 bits	1128
9 bits	978
Subtraction	1344

12.6 Frame rate

Frame rate can be set using the FRAME_LENGTH register.

Frame rate is computed as follows:

$$frame_{rate} = \frac{1}{line_{Time} * FRAME\_LENGTH}$$

FRAME_LENGTH cannot be reduced below a certain limit, depending on Y_HEIGHT.

$$FRAME\_LENGTH \geq Y_{HEIGHT} + 86$$

12.7 Examples of configuration

The following table list some examples of different configurations with the full resolution in 10 bits.

Table 5. Example configurations

EXT_CLOCK (MHz)	MIPI_DATA_RATE (Mbps)	MIPI_DIV	SYS_MULT	SYSTEM_PLL_CLK (MHz)	PIX_DIV	PIXEL_CLK (MHz)	Minimum line time (µs)	Maximum frame rate (fps)
12	402	2	67	402	6	134.0	22.24	57
12	648	1	54	648	5	129.6	13.8	92
12	744	1	62	744	5	148.8	12.2	105
12	840	1	70	840	6	140.0	10.64	119
12	1200	1	100	1200	8	150.0	7.52	168

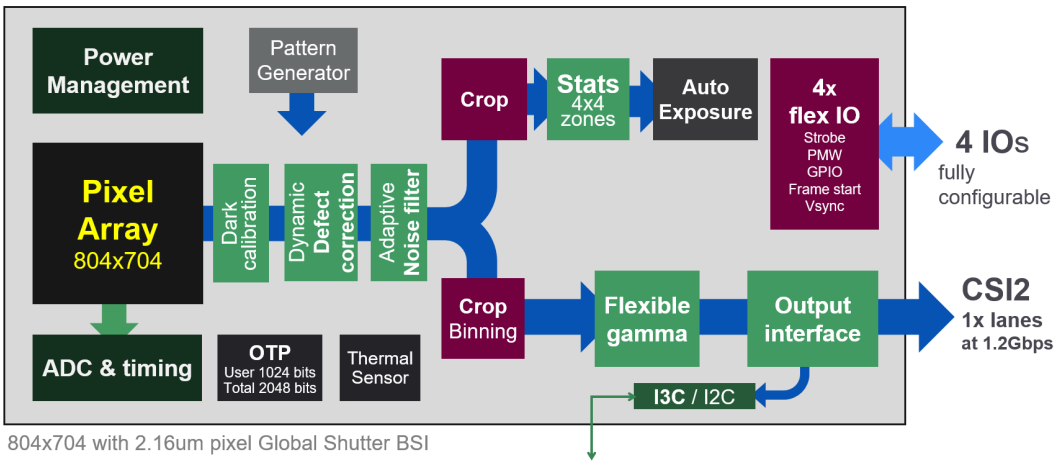
12.8 Synchronization modes

Using the register VT_CTRL, bit field SYNC_MODE, the device can be in master or slave mode. Two slave modes exist: external pulse or I2C command.

- MASTER
  - The device sends continuous frames
  - The frame rate is given by the FRAME_LENGTH register
- EXTERNAL_SYNC
  - The device starts to integrate a frame, then sends it each time the EXTERNAL_SYNC input pin is triggered.
  - Only GPIO_0 can be set as the EXTERNAL_SYNC pin
  - The maximum frame rate is defined by the FRAME_LENGTH register
- I2C_SYNC
  - The device starts to integrate a frame, then sends it at each VT_FSYNC_IN_I2C command. Command is acknowledged once the frame is sent.
  - The maximum frame rate is defined by the FRAME_LENGTH register

13 Video pipe

Figure 3. **Video pipe VD55G1**



13.1 Group parameter hold

The host can prevent the firmware from latching dynamic parameters (DYNAMIC and CONTEXT registers) from the UI registers. To do this, the host must set GROUP_PARAM_HOLD.HOLD = 1 (Enable). The UI parameters are updated when the host sets GROUP_PARAM_HOLD.HOLD = 0 (Disable). This allows the host to update the device with a complete new configuration without timing constraints. The only exceptions to this mechanism are the settings linked to the Binning/subsampling register (READOUT_CTRL).

13.2 Orientation

The device orientation can be set using the ORIENTATION register.

Figure 4. **Device orientation**

13.3 Pattern generator

The device can generate patterns for debugging purposes. Active pixel values are overridden when register PATGEN_CTRL is other than 0.

To use the pattern generator, the darklines must be deactivated by the darkcal average bypass (DARKCAL_CTRL.ENABLE= 0x2). And the pedestal must be set to 0.

13.4 Dark calibration

The device embeds an automatic dark calibration mechanism. The dark calibration target value can be set with the DARKCAL_PEDESTAL register which is a dynamic register. When the device outputs an 8-bit image, this value must be multiplied by 4 (that is, with the default value, the pedestal is 64 in 10-bit and 16 in 8-bit).

13.5 Defect correction and noise reduction

The device embeds the following:

- An automatic defect correction algorithm allowing defective pixels to be corrected.
- A noise reduction processing to increase image SNR.

The defect correction and noise reduction can be enabled or disabled with the DUSTER_CTRL register to match the application requirement and/or do a raw pixel analysis. The intensity of this correction can be managed by the DUSTER_DEF_COR_RATIO register.

13.6 Exposure

The exposure settings are either automatically controlled by the firmware (AEC) or directly controlled by the host (MANUAL). A third mode is to freeze the current settings of the AEC algorithm. When frozen, the auto exposure does not apply new exposure settings but continues to accumulate stats. The fifth mode is a bypass. In bypass mode, there is no exposure update nor statistic accumulation.

Whatever the mode, analog and digital gains are respectively limited to 8 and 32 by default.

13.6.1 Exposure mode control

The mode is controlled by the EXPOSURE_MODE register.

13.6.2 Manual exposure mode

Each context has its own manual exposure settings. Addresses below are provided for the CONTEXT 0 register group.

- Analog gain is controlled by the MANUAL_ANALOG_GAIN register. The gain is computed with the following formula:

$$analog\ gain = \left(\frac{32}{32 - MANUAL\_ANALOG\_GAIN}\right)$$

  The value of the register is in the range [0, 28], that means a gain from 1 to 8.
- Exposure time is controlled by the MANUAL_COARSE_EXPOSURE register. The value is expressed in line equivalent.
  The video timings are different according to the ADC conversion mode. The exposure time is also limited by the frame length. Therefore, the maximum exposure time is:

$$FRAME\_LENGTH - EXP\_COARSE\_INTG\_MARGIN$$

- The digital gain is controlled by the MANUAL_DIGITAL_GAIN register. The register is coded as fixed point 5.8.
- The value of the minimum integration time is five lines in 9 bits mode or four lines in 10 bits mode.

13.6.3 Automatic exposure mode

The registers to configure the automatic exposure control are in the DYNAMIC registers group.

In automatic mode, the AEC targets a level of luminance (in percentage of the saturation level that is, 100 is a saturated image). The AEC updates gains and exposure on a frame basis. Moreover, the AEC achieves luminance evaluation over a configurable area (ROI). See the next chapter for details.

The target is set by the AE_TARGET_PERCENTAGE register. The AEC mechanism tries to reach this target with the following formula.

$$exposure_{required} = \text{exposure}_{current} \times \frac{statistic_{\text{target}}}{statistic_{current}}$$

This equation can lead to brutal changes in the exposure. To smooth the exposure convergence, first a leaky then a step limit is put in place.

- The leaky (α parameter) adds some weight in the exposure history to smooth small exposure changes. It is controlled with the AE_LEAK_PROPORTION register.

$$exposure_{required} = exposure_{current} \times \left(1 - \alpha\left(1 - \frac{statistic_{\text{target}}}{statistic_{current}}\right)\right)$$

- The step limit avoids having significant steps with large exposure changes. It is controlled with the AE_STEP_PROPORTION register. For instance, it avoids doubling the exposure in 1 frame and have an overshoot of exposure. A value of 0 does not allow any change, a value of 1 allows any change.

Two modes of AEC are available. The mode is selected by bit[0] of AE_COMPILER_CONTROL register.

- 0 => Minimum gain. AEC sets minimum gains and prioritizes coarse integration
- 1 => Flicker free. AEC prioritizes integration time to be multiple of the flicker period

Two frequencies are available for the flicker free mode (see above). The frequency is selected by bit[1] of the AE_COMPILER_CONTROL register.

- 0 => 50 Hz
- 1 => 60 Hz

It is possible to force the initial values of the AEC output. This feature is controlled by bit[0] of AE_FORCE_COLDSTART register. If the feature is enabled, the AEC applies the following exposure settings at the next start streaming command:

- AE_COLDSTART_ COARSE_EXPOSURE register
- AE_COLDSTART_ ANALOG_GAIN register
- AE_COLDSTART_ DIGITAL_GAIN register

If the feature is disabled, the AEC applies the current values at the next start streaming command.

13.6.4 Auto exposure grid

The auto exposure is working on a 4x4 grid over the output image. Each bit of the EXPOSURE_STATS_ACTIVE_ZONE register corresponds to the activation of one of the zones.

By default, only active part of the grid is considered. This can be balanced with the EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT register.

The auto exposure will consider the following weights:

- Active grid: EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT
- Passive grid: 100 - EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT

13.6.5 Status of exposure settings

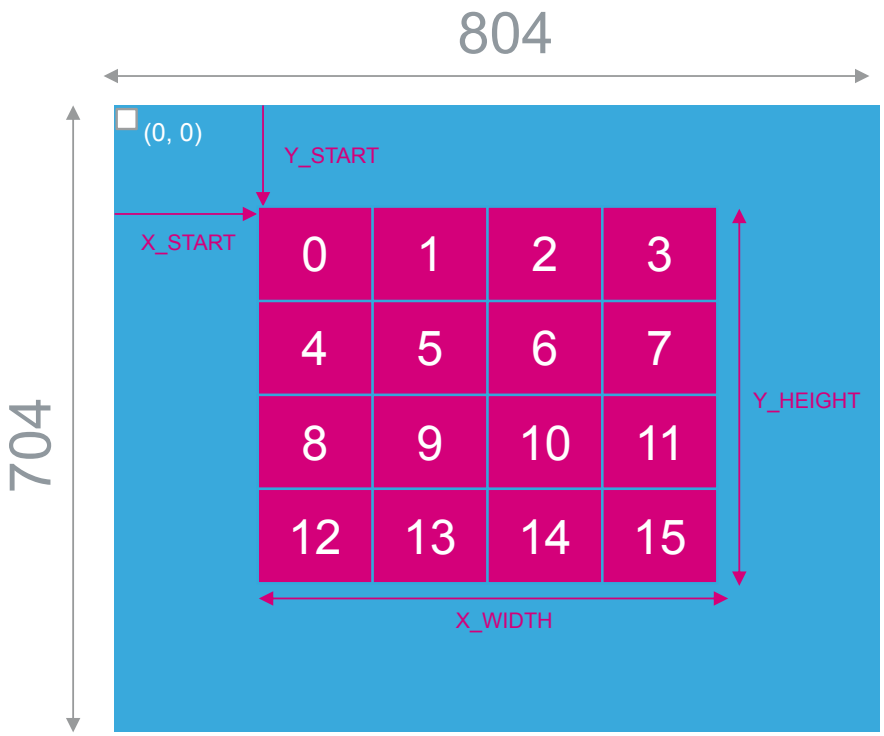
Whatever the exposure mode, the settings currently applied are available in the STATUS registers group.

- Exposure control mode is available in EXPOSURE_MODE register
- Coarse exposure time is available in APPLIED_COARSE_EXPOSURE register. The value is expressed in line equivalent.
- Analog gain is available in APPLIED_ANALOG_GAIN register
- Digital gain is available in APPLIED_DIGITAL_GAIN register
- Status of the AEC is available in AE_STATUS register

13.7 Frame resolution

The maximum output resolution is 804 x 704 pixels. This resolution can be reduced with X_WIDTH and Y_HEIGHT parameters in the context registers. The first pixel is defined with the X_START and Y_START registers.

Figure 5. Frame resolution



Once the field of view is defined with the X_WIDTH and Y_HEIGHT registers, a binning or subsampling can be applied to reduce the resolution and keep the same field of view. This is controlled by the READOUT_CTRL register.

Table 6. **Setting contraints when using decimation modes**

Mode	Decimation	x_start	y_start	x_width	y_height	x_out	y_out
NORMAL	1	2*N	2*N	804-4*N	704-4*N	4*N	4*N
SSAMP_X2	2	2+2*N	2+2*N	800-4*N	700-4*N	2*N	2*N
SSAMP_X4	4	6+4N	8+4*N	792-8*N	688-8*N	2*N	2*N
SSAMP_X8	8	18+16*N	24+16*N	768-32*N	656-32*N	4*N	4*N
DBIN_X2	2	6+2N	8+2*N	792-4*N	688-4*N	2*N	2*N
DBIN_X4	4	6+4N	8+4*N	792-8*N	688-8*N	2*N	2*N

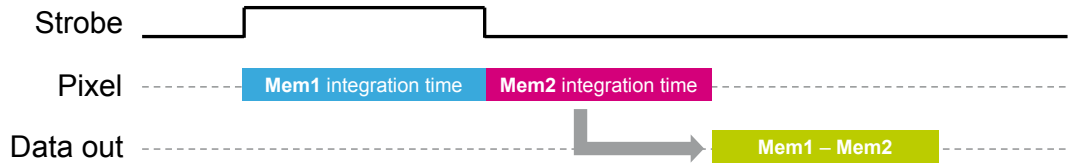
13.8 Subtraction

The VD55G1 can output a frame, which is the result of the subtraction of two subframes. These two subframes have the same integration time.

This mode is activated with the VT_MODE register and the integration time is controlled with the EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A register. A delay can be introduced between the two subframes for specific applications (like motion detection) with the VT_SUB_WAIT register.

When using the strobe mode with the VD55G1 GPIOs, only the first subframe will have the strobe active.

Figure 6. **Subtraction timing**



13.9 Frame masking

Specific use cases require to compute statistics but not to send the frame to the host. This mechanism can be enabled through the MASK_FRAME_CTRL register.

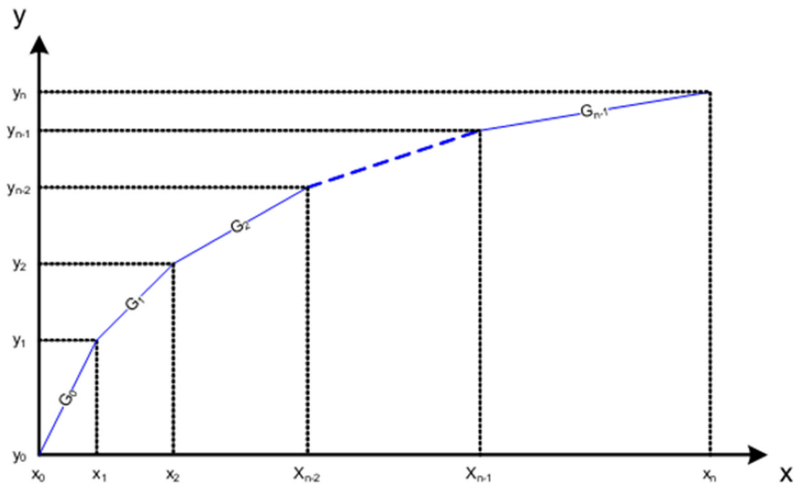
13.10 PWL

The role of the piece-wise linear module is to limit pixel dynamic to decrease data bandwidth before CSI-2 transmission.

The sensor has four PWL curves made of four segments. They have been computed to optimize image quality. The user can build, load, and exercise its own PWL compression. The PWL can be dynamically loaded.

The PWL curve is characterized by the start point coordinates (Xn,Yn) of each segment (called knee points) and the segment slope gradient (Gn).

Figure 7. **PWL compression example**



The PWL formula is: Y = Yn + (X – Xn) x Gn, for X in [Xn, Xn+1] where:

- X is the pixel input value
- Y is the pixel output value
- Xn the start point abscissa of the selected segment
- Yn the start point ordinate of the selected segment
- Gn is the gradient (slope) of the selected segment

The Xn coordinates are stored in the lower 16 bits of the field PWL_LUTX_ABSCISSA_n.

The Yn coordinates are stored in the lower 16 bits of the field PWL_LUTX_ORDINATE_n.

The Gn slope is stored in the upper 32 bits of the field PWL_LUTX_GRADIENT_n.

Gn is represented in normalized mantissa/exponent format with an implicit leading bit in the mantissa: Gn = (256+ Mantissa) * $2^{(Exponent - Bias)}$.

This leading bit (256) is not stored in the memory. Its default value is 256 except when both the LUT exponent and mantissa values are zero. This is a convention of the gradient zero coding.

The exponent is encoded in offset binary. It is represented with a bias value subtracted from the LUT exponent.

This representation is intended to minimize the width of the exponent value stored in the LUT.

The mantissa is an 8-bit field, and the exponent is a 4-bit field. The bias is a 6-bit field parameter constant for the whole shape, which is written in the field STREAM_STATICS.PWL_CTRL.EXPO_BIAS.

13.10.1 Programming of the custom curve

To enable the PWL use the register PWL_CTRL in statics registers.

The PWL selection is done by context with the register PWL_LUT_SEL.

There are two types of PWL: DEFAULT and USER.

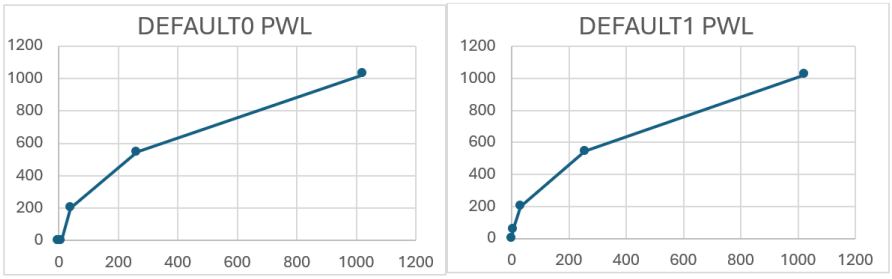
The two DEFAULT PWL are predefined as follows:

EXPO_BIAS = 10

Figure 8. Default PWL

DEFAULT0		
Abscissa	Ordinate	gradient
0	0	0
8	0	1168
40	200	653
264	548	320

DEFAULT1		
Abscissa	Ordinate	gradient
0	0	1440
4	52	1106
32	200	653
256	548	317



The two USER PWL are empty. They are filled by the user in stream statics.

- PWL_LUT_SEL.USER1
- PWL_LUT_SEL.USER2

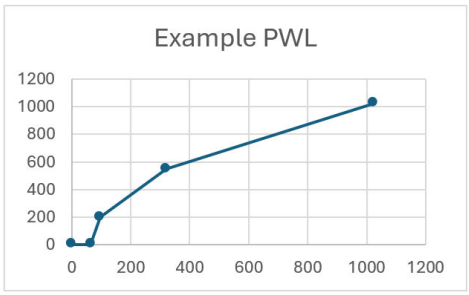
The calculation is based on the following rules:

- The first coordinates must be (0, 0).
- Output values are rounded to the nearest whole number.
- Output values are clipped to the maximum value of the curve.

The following is an example of PWL settings for a PWL curve with a pedestal of 64.

Figure 9. PWL example

Example: PWL curve with a pedestal of 64		
Abscissa	Ordinate	gradient
0	0	0
64	0	1168
96	200	653
320	548	346



14 Context management

Four contexts are available to change the settings during the streaming. The host configures the sequence to switch from one context to another one. The sensor sends X frames from one context, then switch to the Y context. X and Y are the values of the registers CONTEXT_REPEAT_COUNT_CTX[0,1,2,3] and CONTEXT_NEXT_CONTEXT.CTX[0,1,2,3].

The first frame output by the sensor is based on context 0 parameters. If CONTEXT_REPEAT_COUNT is set to 0, the sensor remains on the current context.

Note: The context loop can only be edited when not streaming.

The following values are available on the STATUS register group:

- FRAME_COUNTER
- CONTEXT_FRAME_COUNTER
- CONTEXT_REPEAT_COUNT
- CURRENT_CONTEXT
- NEXT_CONTEXT

15 Output interface

The output interface of the VD55G1 embeds a single lane MIPI DPHY interface. It supports up to 1.2 Gb/s of data rate.

Data are transferred through the CSI2 as follows:

- Status lines
- SMIA RAW10 or SMIA RAW8 image data

15.1 Configuration

All data (active image, ISL) can be output on different virtual channels and/or datatypes by using OIF_VC_CTRL and OIF_IMG_CTRL/OIF_ISL_CTRL registers. In some use cases, the content of a context is not sent but only used for the auto exposure convergence. To not output the frame context, use register MASK_FRAME_CTRL.

15.2 Frame format

The frame is made of status lines followed by the image content.

Figure 10. Image content

15.3 Status lines

Status lines are composed of 512 bytes. These bytes correspond to the values of the 512 first registers for the current frame. Some padding (0x0) is added to fit the active frame size.

If the image data is lower than 512, an additional status line is created. No more than 12 status lines can be sent.

Table 7. Example of status line for an image of 804 pixels in 10 bits.

Byte	0	1	2	3	4	5	...	513	...	1005
Register	0x31	0x47	0x35	0x53	0x10	0x10		—	—	—
Value	DEVICE_MODEL_ID				DEVICE_REVISION			0	0	0

15.4 Image data

Image data contain pixel values based on different crop and binning sets. Values can be coded on SMIA RAW10 or SMIA RAW8 depending on the register settings. Image width and height should be even. For SMIA RAW10 data, the image width should be a multiple of 4 pixels.

16 Temperature

The device embeds a thermal sensor. Temperature is read at each frame in streaming state or if a THSENS_READ command is sent when the device is in SW_STBY. The result is stored in the TEMPERATURE status register.

17 GPIOs

The VD55G1 has four configurable GPIOs. GPIO settings are part of the context register group and consequently they can differ from one context to another. Only GPIO_0 can be used to start frame synchronization that is, mode = 0xA:(VT_SLAVE_MODE).

GPIOs can be configured with the following modes.

- STROBE_MODE: envelop of the integration time
- PWM_STROBE: envelop of the integration time multiplied by the PWM
- PWM: continuous PWM
- GPIO_OUT: register control level
- VT_SLAVE_MODE: the input to trigger slave mode (only valid for GPIO 0)

PWM frequency is computed from the PWM_CLK_DIVIDER register with the following formula:

$$PWM_{frequency} = \frac{Pixel\_clock}{ClkDivider\_register + 1}$$

The low period duty cycle is computed from the PWM_DUTY_CYCLE register as follows:

$$Duty_{cycle} = \frac{16 - DutyCycle\mathrm{Re}\,gister}{16}$$

Appendix A Configuration for a standard streaming

This is the normal mode of operation.

Conditions:

- Fix resolution
- Fix strobe mode
- Automatic exposure

```
// UI.SENSOR_SETTINGS.EXT_CLOCK.VALUE / (val=12000000)
WriteAutoIncrement(0x0220, 0x0, 0x1b, 0xb7, 0x0);
// UI.SENSOR_SETTINGS.MIPI_DATA_RATE.VALUE / (val=1200000000)
WriteAutoIncrement(0x0224, 0x0, 0x8c, 0x86, 0x47);
// UI.STREAM_STATICS.LINE_LENGTH.VALUE / (val=1128)(7.52 us)
WriteAutoIncrement(0x0300, 0x68, 0x4);
// UI.STREAM_CTX0.EXPOSURE_MODE.MODE / (val=0)(AUTO)
WriteAutoIncrement(0x0500, 0x0);
// UI.STREAM_CTX0.FRAME_LENGTH.VALUE / (val=2659)(50 fps)
WriteAutoIncrement(0x050c, 0x63, 0xa, 0x0, 0x0);
// UI.STREAM_CTX0.GPIO_0_CTRL.Mode / (val=2)(STROBE)
WriteAutoIncrement(0x051d, 0x2);
```

Appendix B External subtraction background mode

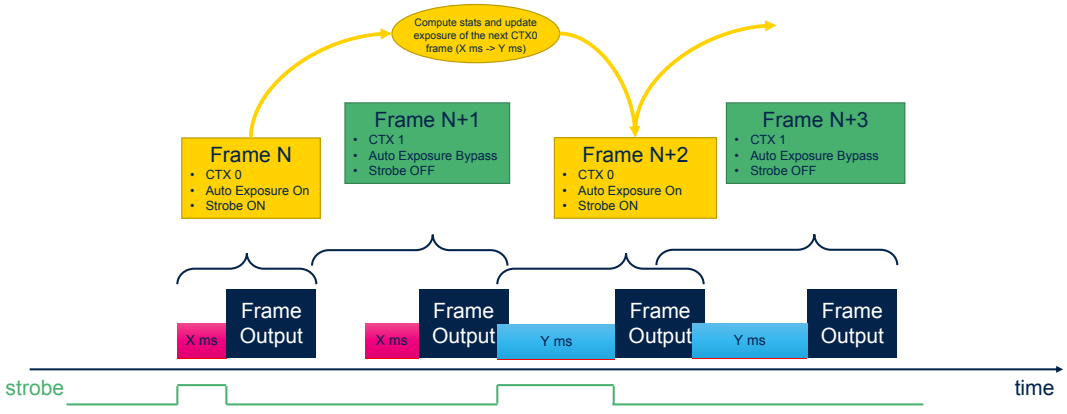
In this mode the sensor provides two consecutives frames to host: with and without active illumination. The sensor can automatically compute exposure or let the host do the job. Subtraction of frames is done by the host.

Conditions

- Strobe mode alternate between on and off
- Manual or automatic exposure

```
// UI.SENSOR_SETTINGS.EXT_CLOCK.VALUE / (val=12000000)
WriteAutoIncrement(0x0220, 0x0, 0x1b, 0xb7, 0x0);
// UI.SENSOR_SETTINGS.MIPI_DATA_RATE.VALUE / (val=1200000000)
WriteAutoIncrement(0x0224, 0x0, 0x8c, 0x86, 0x47);

// UI.STREAM_STATICS.LINE_LENGTH.VALUE / (val=1128)(7.52 us)
WriteAutoIncrement(0x0300, 0x68, 0x4);
// UI.STREAM_STATICS.EXPOSURE_USE_CASES.ENABLE_MULTI_CONTEXT / (val=1)
WriteAutoIncrement(0x0312, 0x4);
// UI.STREAM_STATICS.CONTEXT_NEXT_CONTEXT.CTX0 / (val=1)
// UI.STREAM_STATICS.CONTEXT_NEXT_CONTEXT.CTX1 / (val=0)
WriteAutoIncrement(0x03e4, 0x1, 0x11);
// UI.STREAM_STATICS.CONTEXT_REPEAT_COUNT_CTX0.VALUE / (val=1)
WriteAutoIncrement(0x03dc, 0x1, 0x0);
// UI.STREAM_STATICS.CONTEXT_REPEAT_COUNT_CTX1.VALUE / (val=1)
WriteAutoIncrement(0x03de, 0x1, 0x0);

// UI.STREAM_DYNAMICS.EXPOSURE_TARGET_PERCENTAGE_A.VALUE / (val=15)
WriteAutoIncrement(0x0486, 0xf);

// UI.STREAM_CTX0.EXPOSURE_MODE.MODE / (val=0)(AUTO)
WriteAutoIncrement(0x0500, 0x0);
// UI.STREAM_CTX0.FRAME_LENGTH.VALUE / (val=2659)(50 fps)
WriteAutoIncrement(0x050c, 0x63, 0xa, 0x0, 0x0);
// UI.STREAM_CTX0.GPIO_0_CTRL.Mode / (val=2)(STROBE)
WriteAutoIncrement(0x051d, 0x2);

// UI.STREAM_CTX1.EXPOSURE_MODE.MODE / (val=4)(BYPASS)
WriteAutoIncrement(0x0550, 0x4);
// UI.STREAM_CTX1.FRAME_LENGTH.VALUE / (val=2659)(50 fps)
WriteAutoIncrement(0x055c, 0x63, 0xa, 0x0, 0x0);
// UI.STREAM_CTX1.GPIO_0_CTRL.Mode / (val=5)(LOW)
WriteAutoIncrement(0x056d, 0x5);
```

Figure 11. Timing graph for external subtraction background mode



Appendix C Internal subtraction background mode

The purpose of this mode is to output a well exposed subtracted frame to the host. The subtraction is done in the sensor.

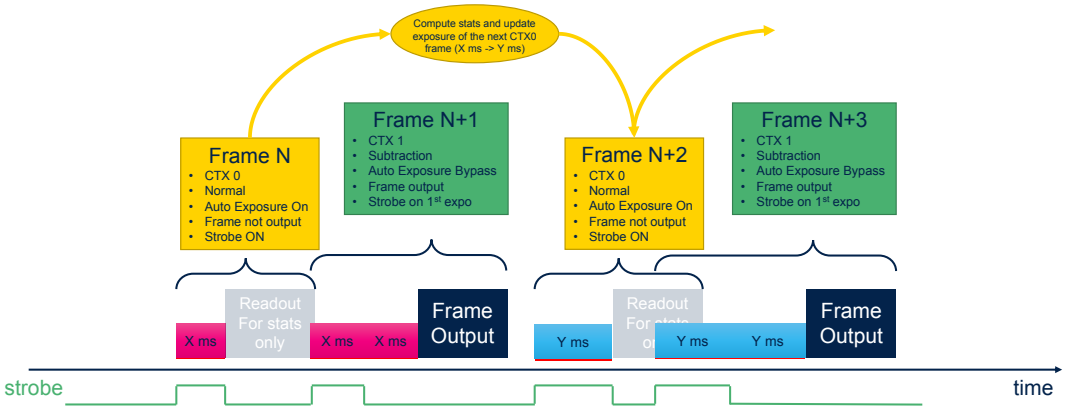
It is assumed that computing requested exposure time from a subtracted image is not manageable. Because of that, a normal frame is internally used to compute the requested exposure in subtraction mode.

Conditions:

- Strobe mode alternate between on and off on the subtracted image
- Manual or Automatic exposure

```
// UI.SENSOR_SETTINGS.EXT_CLOCK.VALUE / (val=12000000)
WriteAutoIncrement(0x0220, 0x0, 0x1b, 0xb7, 0x0);
// UI.SENSOR_SETTINGS.MIPI_DATA_RATE.VALUE / (val=1200000000)
WriteAutoIncrement(0x0224, 0x0, 0x8c, 0x86, 0x47);

// UI.STREAM_STATICS.LINE_LENGTH.VALUE / (val=1344)(8.96 us)
WriteAutoIncrement(0x0300, 0x40, 0x5);
// UI.STREAM_STATICS.EXPOSURE_USER_MAX_COARSE_INTEGRATION_LINES.VALUE / (val=446) (4ms  @ 8.9
6 us/ line)
WriteAutoIncrement(0x0372, 0xbe, 0x1);
// UI.STREAM_STATICS.EXPOSURE_USE_CASES.ENABLE_MULTI_CONTEXT / (val=1)
WriteAutoIncrement(0x0312, 0x4);
// UI.STREAM_STATICS.CONTEXT_NEXT_CONTEXT.CTX0 / (val=1)
// UI.STREAM_STATICS.CONTEXT_NEXT_CONTEXT.CTX1 / (val=0)
WriteAutoIncrement(0x03e4, 0x1, 0x11);
// UI.STREAM_STATICS.CONTEXT_REPEAT_COUNT_CTX0.VALUE / (val=1)
WriteAutoIncrement(0x03dc, 0x1, 0x0);
// UI.STREAM_STATICS.CONTEXT_REPEAT_COUNT_CTX1.VALUE / (val=1)
WriteAutoIncrement(0x03de, 0x1, 0x0);

// UI.STREAM_DYNAMICS.EXPOSURE_TARGET_PERCENTAGE_A.VALUE / (val=15)
WriteAutoIncrement(0x0486, 0xf);

// UI.STREAM_CTX0.EXPOSURE_MODE.MODE / (val=0)(AUTO)
WriteAutoIncrement(0x0500, 0x0);
// UI.STREAM_CTX0.FRAME_LENGTH.VALUE / (val=2232)(50 fps)
WriteAutoIncrement(0x050c, 0xb8, 0x8, 0x0, 0x0);
// UI.STREAM_CTX0.GPIO_0_CTRL.Mode / (val=2)(STROBE)
WriteAutoIncrement(0x051d, 0x2);
// UI.STREAM_CTX0.VT_MODE / (val=0)(NORMAL)
WriteAutoIncrement(0x0536, 0x00);
// UI.STREAM_CTX0.MASK_FRAME_CTRL / (val=1)(MASK FRAME)
WriteAutoIncrement(0x0537, 0x01);

// UI.STREAM_CTX1.EXPOSURE_MODE.MODE / (val=4) (BYPASS)
WriteAutoIncrement(0x0550, 0x4);
// UI.STREAM_CTX1.FRAME_LENGTH.VALUE / (val=2232)(50 fps)
WriteAutoIncrement(0x055c, 0xb8, 0x8, 0x0, 0x0);
// UI.STREAM_CTX1.GPIO_0_CTRL.Mode / (val=2)(STROBE)
WriteAutoIncrement(0x056d, 0x2);
// UI.STREAM_CTX1.VT_MODE / (val=1)(SUBTRACTION)
WriteAutoIncrement(0x0586, 0x01);
// UI.STREAM_CTX1.MASK_FRAME_CTRL / (val=0)(OUTPUT FRAME)
WriteAutoIncrement(0x0587, 0x00);
```

Figure 12. **Internal subtraction background mode**



Appendix D Multi ROI exposure

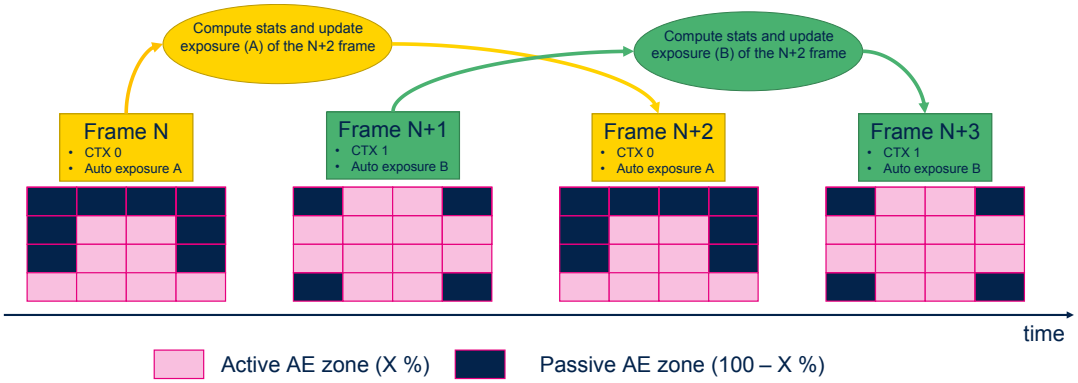
The purpose of this mode is to output even frames globally well expose and odd frames with exposure focusing on people.

Conditions:

- Double automatic exposure is enabled independently on even and odd frames
- Active AE zone are different between odd and even frames.
- Active and Passive AE zones are weighted differently

```
// UI.SENSOR_SETTINGS.EXT_CLOCK.VALUE / (val=12000000)
WriteAutoIncrement(0x0220, 0x0, 0x1b, 0xb7, 0x0);
// UI.SENSOR_SETTINGS.MIPI_DATA_RATE.VALUE / (val=1200000000)
WriteAutoIncrement(0x0224, 0x0, 0x8c, 0x86, 0x47);

// UI.STREAM_STATICS.LINE_LENGTH.VALUE / (val=1128)(7.52 us)
WriteAutoIncrement(0x0300, 0x68, 0x4);
// UI.STREAM_STATICS.EXPOSURE_USE_CASES.ENABLE_MULTI_CONTEXT / (val=1)
WriteAutoIncrement(0x0312, 0x4);
// UI.STREAM_STATICS.CONTEXT_NEXT_CONTEXT / (0->1, 1->0)
WriteAutoIncrement(0x03e4, 0x01, 0x11);
// UI.STREAM_STATICS.CONTEXT_REPEAT_COUNT_CTX0.VALUE / (val=1)
WriteAutoIncrement(0x03dc, 0x1, 0x0);
// UI.STREAM_STATICS.CONTEXT_REPEAT_COUNT_CTX1.VALUE / (val=1)
WriteAutoIncrement(0x03de, 0x1, 0x0);

// UI.STREAM_DYNAMICS.EXPOSURE_TARGET_PERCENTAGE_A.VALUE / (val=30)
WriteAutoIncrement(0x0486, 0x1e);
// UI.STREAM_DYNAMICS.EXPOSURE_TARGET_PERCENTAGE_B.VALUE / (val=30)
WriteAutoIncrement(0x0490, 0x1e);

// UI.STREAM_CTX0.EXPOSURE_MODE.MODE / (val=0) (AUTO)
WriteAutoIncrement(0x0500, 0x0);
// UI.STREAM_CTX0.FRAME_LENGTH.VALUE / (val=2232) (50 fps)
WriteAutoIncrement(0x050c, 0xb8, 0x8, 0x0, 0x0);
// UI.STREAM_CTX0.EXPOSURE_STATS_ACTIVE_ZONE.VALUE / (val=1647)
WriteAutoIncrement(0x0518, 0x6f, 0x6);
// UI.STREAM_CTX0.EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT.VALUE / (val=80)
WriteAutoIncrement(0x051a, 0x50);
// UI.STREAM_CTX0.GPIO_0_CTRL.Mode / (val=2)(STROBE)
WriteAutoIncrement(0x051d, 0x2);
// UI.STREAM_CTX0.EXPOSURE_INSTANCE.VALUE / (val=0)
WriteAutoIncrement(0x052d, 0x0);

// UI.STREAM_CTX1.EXPOSURE_MODE.MODE / (val=0) (AUTO)
WriteAutoIncrement(0x0550, 0x0);
// UI.STREAM_CTX1.FRAME_LENGTH.VALUE / (val=2232)(50 fps)
WriteAutoIncrement(0x055c, 0xb8, 0x8, 0x0, 0x0);
// UI.STREAM_CTX1.EXPOSURE_INSTANCE.VALUE / (val=1)
WriteAutoIncrement(0x057d, 0x1);
// UI.STREAM_CTX1.EXPOSURE_STATS_ACTIVE_ZONE.VALUE / (val=63888)
WriteAutoIncrement(0x0568, 0x90, 0xf9);
// UI.STREAM_CTX1.EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT.VALUE / (val=80)
WriteAutoIncrement(0x056a, 0x50);
// UI.STREAM_CTX1.GPIO_0_CTRL.Mode / (val=5)
WriteAutoIncrement(0x056d, 0x5);
// UI.STREAM_CTX1.EXPOSURE_INSTANCE.VALUE / (val=1)
WriteAutoIncrement(0x057d, 0x1);
```

Figure 13. **Timing graph for multi-ROI exposure**



Appendix E I3C image readout

In addition to retrieving pixels over the MIPI CSI interface, the VD55G1 can also read pixels over the I3C interface. These two features are mutually exclusive.

Reading pixels over the I3C involves using SDR mode when it is running at up to 12.5 Mbit per second. Up to 400 pixels per line can be read in RAW8 format.

The appendix below describes how to configure the VD55G1 to enable reading pixels over the I3C. The sensor operates in master mode and the I3C pixel readback is triggered at every line by an “IMAGE_READOUT” event of one of the sensor’s GPIOs.

Note that pixel readback is also possible with standard I²C fast plus mode. The maximum achievable frequency in I²C fast mode plus limits the number of pixels (several dozen) that can be retrieved.

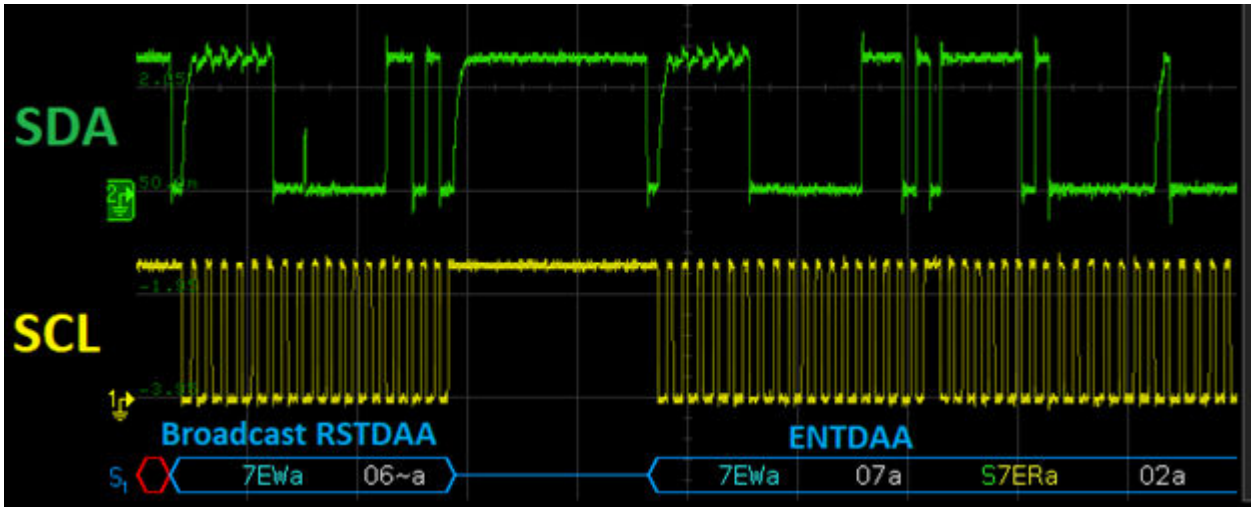
E.1 Enabling I3C communication with the VD55G1

I3C communication is initiated using the broadcast common command code (CCC) to enter a dynamic address assignment (ENTDAA). Such a sequence assigns a dedicated I3C address to the VD55G1.

The procedure below is based on an STM32N6 or STM32H5 example. It shows how to:

- Reset a dynamic address (using the broadcast CCC RSTDAA).
- Assign a dynamic address (using the broadcast CCC ENTDAA).
- Test the new I3C address communication (0x22 in the example).
- Set the I3C frequency to 12.5 MHz.

Figure 14. RSTDAA and ENTDAA entry sequences



Release the XSHUTDOWN pin to a high level. Then, make the dynamic address assignment. The sensor must have reached the READY_TO_BOOT state for the ENTDAA sequence to work properly.

If the 16-bit status register SYSTEM_FSM is pooled at address 0x1C, wait for the value 0x1 (READY_TO_BOOT) before proceeding to the assignment sequence. Note that you can apply an arbitrary delay instead of pooling this register. However, the duration from XSHUTDOWN pin release to READY_TO_BOOT state depends on the input clock frequency (typically 4 ms @ 12 MHz).

If the dynamic address assignment sequence occurs before READY_TO_BOOT state is reached, the reported provisioned ID, BCR, and DCR are inaccurate, and the dynamic assignment might fail.

Figure 15. **VD55G1 SYSTEM_FSM states**

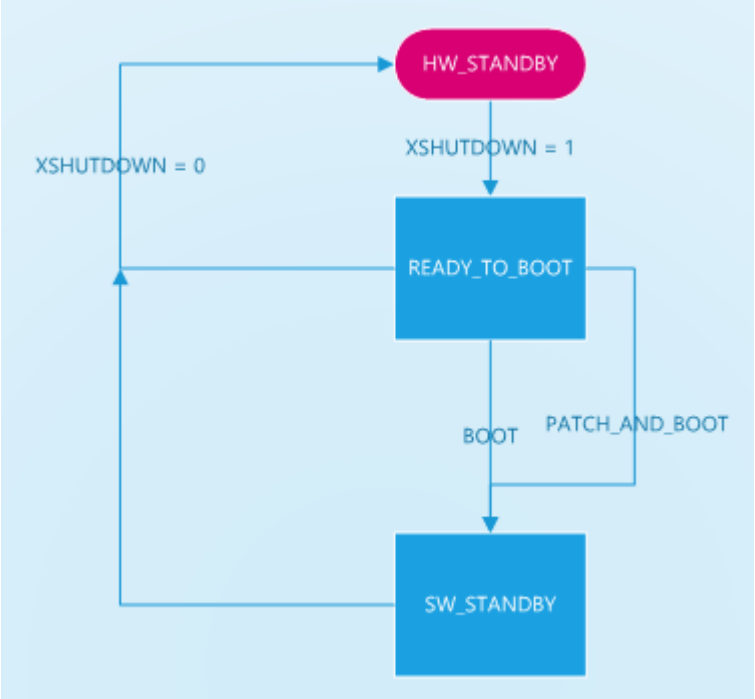
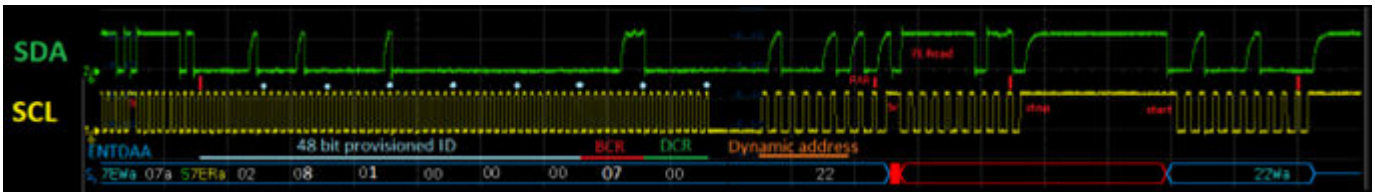


Figure 16. **Dynamic address assignment sequence**



The BCR register 0x07 = 0000 0111 provides the following information:

- Bits [7:6] = 00: The I3C target.
- Bit 5 = 0: No support of the optional advanced capabilities.
- Bit 4 = 0: Not a virtual target.
- Bit 3 = 0: The device always responds to the I3C bus commands.
- Bit 2 = 1: IBI payload enable.
- Bit 1 = 1: IBI request capable (depends on the hardware).
- Bit 0 = 1: Limitation on the maximum data speed.

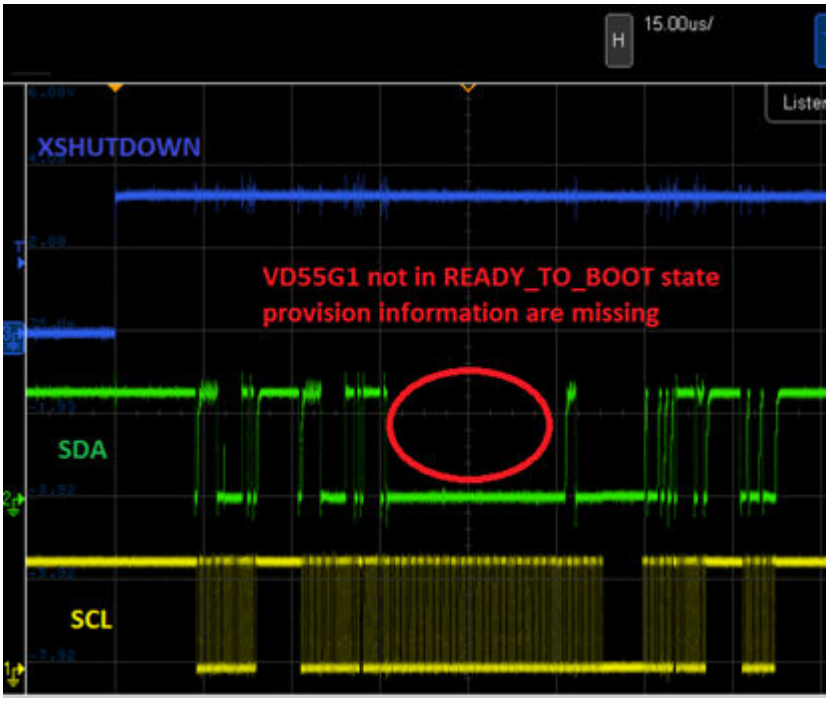
E.1.1 Sample code used for enabling I3C communication with the VD55G1

```
#define Broadcast_RSTDAA        0x06
#define I3C_BUSCLOCK_12MHZ      12500000
#define I2C_BUSCLOCK_1000KHZ    1000000
#define VD55G1_I2C_DYN_ADDR     0x44
#define VD55G1_I3C_READ_XSIZE   400
#define VD55G1_I3C_READ_YSIZE  (700/2)
#define IMAGE_READBACK_ADDRESS 0x2000
#define LINE_CLOCK_LENGTH_I3C 51000
#define FRAME_SIZE_I3C    (VD55G1_I3C_READ_YSIZE + 54 )
#define ANASUB_X2 3

uint8_t i3c_image[VD55G1_I3C_READ_XSIZE*VD55G1_I3C_READ_YSIZE];
uint8_t* p_buffer = (uint8_t*) i3c_image;
uint8_t  i3c_bus_busy = 0;

I3C_XferTypeDef Context_buffers;
uint32_t Control_Buffer[0x0f];
uint8_t TxBuffer[8];
uint8_t RxBuffer[VD55G1_I3C_READ_XSIZE];

I3C_PrivateTypeDef I2C_TxRx_Descriptor[2] = {
{VD55G1_I2C_ADDR>>1, {TxBuffer,8}, {NULL, 0U}, HAL_I3C_DIRECTION_WRITE},
{VD55G1_I2C_ADDR>>1, {NULL, 0U}, {RxBuffer, VD55G1_I3C_READ_XSIZE}, HAL_I3C_DIRECTION_READ},
};

void VD55G1_AssignDynamicAddress(void)
{

    Context_buffers.CtrlBuf.pBuffer = Control_Buffer;
    Context_buffers.CtrlBuf.Size    = 2;
    Context_buffers.TxBuf.pBuffer = TxBuffer;
    Context_buffers.TxBuf.Size      = 1;

    I3C_CCCTypeDef Broadcast_CCC ={0, Broadcast_RSTDAA, {NULL, 0}, LL_I3C_DIRECTION_WRITE};

    if (HAL_I3C_AddDescToFrame(&hbus_i3c1, &Broadcast_CCC,NULL, &Context_buffers, 1, I3C_BROA
DCAST_WITHOUT_DEFBYTE_RESTART) != HAL_OK)
        Error_Handler();

    if (HAL_I3C_Ctrl_TransmitCCC_IT(&hbus_i3c1, &Context_buffers) != HAL_OK)
        Error_Handler();
    while (HAL_I3C_GetState(&hbus_i3c1) != HAL_I3C_STATE_READY)
    {
    }

    if (HAL_I3C_Ctrl_DynAddrAssign_IT(&hbus_i3c1, I3C_ONLY_ENTDAA) != HAL_OK)
        Error_Handler();
    while (HAL_I3C_GetState(&hbus_i3c1) != HAL_I3C_STATE_READY)
        {
        }

    if (HAL_I3C_Ctrl_IsDeviceI3C_Ready(&hbus_i3c1, VD55G1_I2C_DYN_ADDR>>1, 3, 10) != HAL_OK)
        Error_Handler();

    I2C_TxRx_Descriptor[0].TargetAddr = VD55G1_I2C_DYN_ADDR>>1;
    I2C_TxRx_Descriptor[1].TargetAddr = VD55G1_I2C_DYN_ADDR>>1;

    if (I3C_Controller_BusCharacteristic_Config(&hbus_i3c1, I3C_BUSCLOCK_12MHZ, I2C_BUSCLOCK_
1000KHZ, 50, I3C_PURE_I3C_BUS) != 0)
        Error_Handler();
}

void HAL_I3C_TgtReqDynamicAddrCallback(I3C_HandleTypeDef *hi3c, uint64_t targetPayload)
{
  HAL_I3C_Ctrl_SetDynAddr(hi3c, VD55G1_I2C_DYN_ADDR>>1);
}
```

For more details, refer to the application note "AN5879 Introduction to I3C for STM32H5 series MCU". It is available on st.com.

E.1.2 Example of an ENTDAA response which is too early

Figure 17. Example of an ENTDAA response when the I3C configuration has been made too early



E.2 Streaming configuration

E.2.1 I3C readout duration

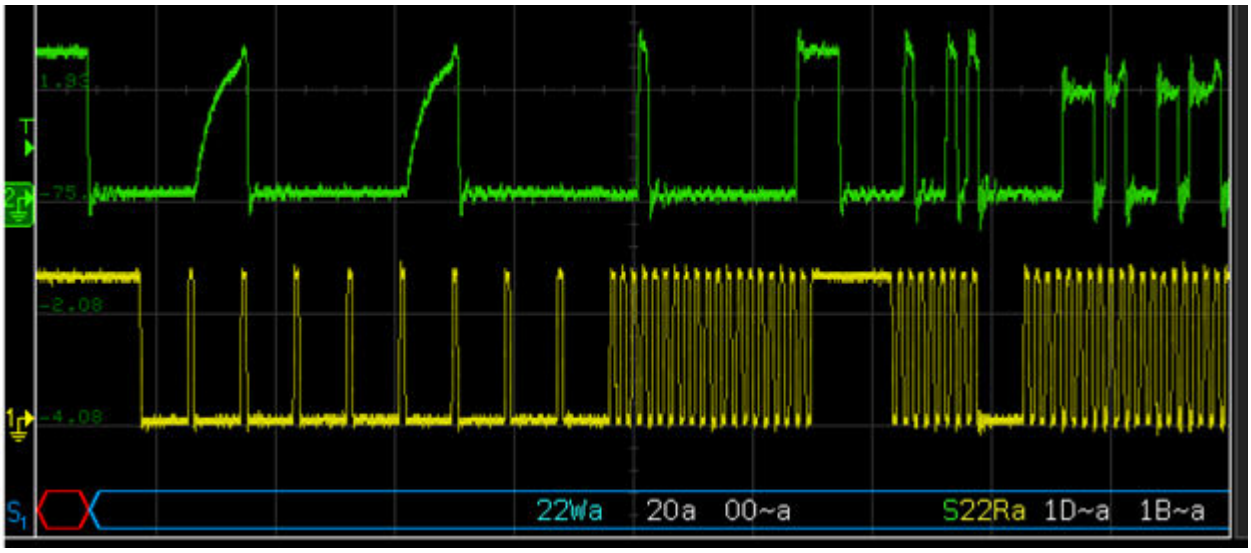
Considering a pixel requires nine clock cycles to be transmitted on an I3C bus that is running at 12.5 Mbit/s, a "minimum time" to capture 400 pixels is needed. As a quick rule of thumb, this minimum time is 288 µs (400*9*80 ns).

However, when we add the following mandatory bytes at the beginning of the I3C transfer:

- I3C broadcast address (0x7E) in slower open drain mode (optional).
- Device dynamic address (0x22) + write bit in slower open drain mode.
- Device register address (2 bytes + base address 0x2000) at the SDR frequency.
- Device dynamic address (0x22) + read bit at the SDR frequency.

The final I3C readout time is closer to 300 µs (see figure below).

Figure 18. Starting sequence of pixel I3C readout



Note that communication in open drain mode is made with the SCL high period below the 50 ns I²C glitch suppression filter.

E.2.2 Host management duration

In addition to the minimum required time to transfer data over the I3C bus, the host also needs to manage at least two events. They are the:

- GPIO “IMAGE_READOUT” event, which the sensor sends.
- "End of the I3C line pixel transfer" event, which is a firmware event.

The GPIO IMAGE_READOUT event:

- Initiates an I3C transfer by the host starting at the register address 0x2000.
- Prevents any other I²C/I3C communication attempts.
- Forbids any new IMAGE_READOUT event management during line pixel reading.

Without optimization, the duration of this event is slightly less than 30 µs using HALs on the STM32N6.

The end of the I3C line pixel transfer event:

- Manages the host capture memory pointer.
- Re-enables the I²C/I3C communication attempts when it is detected that the last line of the frame has been read.
- Re-enables the IMAGE_READOUT event management.

The duration of this event is slightly less than 2 µs on the STM32N6.

Clearly, management of these two events adds some additional time to the 300 µs previously counted. Consequently, 340 µs becomes a more realistic minimum line time.

Note: When the GPIO IMAGE_READOUT is high during an I3C pixel readout, it regularly generates some negative glitches. These glitches are less than 10 ns. They may be caught by the host system interrupt. It is better to prevent the host from reacting to such events by temporarily disabling the interrupt manager while the I3C readout is in progress.

E.2.3 Line length configuration

Line time is controlled via the register LINE_LENGTH. It is expressed in numbers of pixel clock cycles. LINE_TIME is dependent on the MIPI rate. Although the MIPI interface is not used in I3C pixel readout mode, its data rate value impacts line time. Consequently, this impacts the LINE_LENGTH value to be programmed. LINE_LENGTH is a 16-bit parameter. It cannot be greater than 65500. The table below provides some examples for defining line time. Note that 340 µs is considered as a minimum duration and not a target value.

Table 8. An example of line length settings

EXT_CLOCK (MHz)	MIPI_DATA_RATE (Mbps)	MIPI_DIV	SYS_PLL_CLOCK (MHz)	PIX_DIV	PIXEL CLOCK (MHz)	LINE_LENGTH for 340 µs
12	1200	1	1200	8	150.0	51000
12	1000	1	1000	8	125.0	42500
12	800	1	800	6	133.3	45333
12	640	1	640	5	128.0	43520
12	456	2	912	8	114.0	38760
12	420	2	840	6	140.0	47600

Note: The MIPI_DATA_RATE example at 456 Mbps is an interesting solution for systems where line time must be extremely stretched to allow the I3C readout sequence. Setting LINE_LENGTH to 65500 stretches the line time over 574 µs.

E.2.4 Image size configuration

Only lines up to 400 pixels can be read out over the I3C bus. But the host can read up to 704 lines in total.

To maintain a large FOV and preserve the form factor ratio of the image, use digital binning by two or analog subsampling by two.

Digital binning digitally combines every two pixels in horizontal and vertical directions to create the pixel output. This solution averages the pixel photoshot noise and improves the SNR without impacting the frame rate.

Analog subsampling retrieves every two pixels in horizontal and vertical directions from the image matrix prior to their entry into the digital image pipe. There is no noise improvement, but the frame rate can be almost doubled by the reduction of the FRAME_LENGTH parameter.

E.2.5 Frame length configuration

To achieve the maximum frame rate, the FRAME_LENGTH parameter must be set as low as possible.

FRAME_LENGTH is the sum of two numbers. It cannot be lower than the number of lines of the image. Alternatively, it cannot be lower than half the number of lines of the image when analog subsampling x2 is used. In both cases, add a minimum value of 54.

The frame rate cannot be above 7.3 fps when reading an image of 400x350 in analog subsampling x2.

E.2.6 Sensor configuration pseudocode

```
#define SKIP_HEADER  (1<<1)
#define ENABLE      1
#define DISABLE     0

write8(VD55G1_REG_GPIO0_CTRL, VD55G1_IMAGE_READOUT); // 0x51d 0xc
write16(VD55G1_REG_I3C_FRAME_READOUT_CTRL, (DISABLE<<2)| SKIP_HEADER | ENABLE ); // 0x324 3
write8(VD55G1_REG_ISL_ENABLE, DISABLE); // 0x326 0
write8(VD55G1_REG_VT_CTRL, 4); // 0x309 ADC 9 bit mode
write16(VD55G1_REG_FORMAT_CTRL, 8); // 0x30a RAW8

write16(VD55G1_REG_LINE_LENGTH, LINE_CLOCK_LENGTH); // 0x300

write16(VD55G1_REG_Y_START, 2); // 0x510
write16(VD55G1_REG_X_START, 2); // 0x514
write16(VD55G1_REG_Y_HEIGHT, VD55G1_I3C_READ_YSIZE*2); // 0x512
write16(VD55G1_REG_X_WIDTH, VD55G1_I3C_READ_XSIZE*2); // 0x516
write8(VD55G1_REG_READOUT_CTRL, ANASUB_X2); // 0x52e

write16(VD55G1_REG_FRAME_LENGTH, FRAME_SIZE_I3C); // 0x50c
write8(VD55G1_REG_STBY_CMD, 1); // 0x201 1
```

E.3 I3C operation

The VD55G1 informs the host when a line of pixels can be read. This information is selectable on the rising or falling edge event of one of the four GPIOs of the sensor. This is true only when the IMAGE_READOUT event has been configured.

When getting this event, the host has to launch the I3C read sequence to capture all the pixels of the line within the sensor line time.

The GPIO IMAGE_READOUT signal returns to idle state a few bytes before the end of the I3C readout sequence. But as explained in Appendix E.2.2: Host management duration, the GPIO IMAGE_READOUT event generates low level glitches all along the I3C readout sequence.

The pixel readout starts at the register address 0x2000.

If the I3C readout sequence takes too long, or if it starts with a latency and overlaps on the next line, the sensor is halted. The sensor then requires a full reconfiguration sequence. The same issue also happens with an incomplete I3C readout sequence (when retrieving fewer pixels than expected).

Do not interrupt the I3C pixel readout sequence with an extra I²C/I3C communication from the host to the sensor.

Preferably, use a full hardware mechanism such as an I3C read-back DMA transfer to minimize firmware actions and global latency.

Include a monitoring mechanism to ensure that I3C/I²C communication from the host to the sensor occurs only during the vertical blanking period. This is the period when there is no pixel read out activity. For example, communication from the host to the sensor is to update the exposure settings.

E.3.1 GPIO interrupt management

The following example code shows how to manage the GPIO IMAGE_READOUT and the end of each line capture. It is based on the HALs of the STM32N6. It implements a DMA mechanism and requires three channels to manage requests for the Rx, Tx, and controller.

This code example is based on the IMAGE_READOUT connected to an STM32 pin resource routed to EXTI10.

```
void EXTI10_IRQHandler(uint16_t GPIO_Pin)
{

TxBuffer[0]= IMAGE_READBACK_ADDRESS >> 8;
TxBuffer[1]= IMAGE_READBACK_ADDRESS & 0xff;
Context_buffers.CtrlBuf.pBuffer = Control_Buffer;
Context_buffers.CtrlBuf.Size  = 2 ;
Context_buffers.TxBuf.pBuffer = TxBuffer;
Context_buffers.RxBuf.pBuffer = i3c_image;

Context_buffers.TxBuf.Size = 2;
Context_buffers.RxBuf.Size = VD55G1_I3C_READ_XSIZE;
I2C_TxRx_Descriptor[0].TxBuf.Size = 2;
I2C_TxRx_Descriptor[1].RxBuf.Size = VD55G1_I3C_READ_XSIZE;

if (HAL_I3C_AddDescToFrame(&hbus_i3c1, NULL, &I2C_TxRx_Descriptor[0], &Context_buffers, 2, BU
S_RESTART) != HAL_OK)
  Error_Handler();
if (HAL_I3C_Ctrl_MultipleTransfer_DMA(&hbus_i3c1, &Context_buffers) != HAL_OK)
  Error_Handler()

I3c_bus_busy = 1;
HAL_NVIC_DisableIRQ(EXTI10_IRQn);
__HAL_GPIO_EXTI_CLEAR_IT(GPIO_PIN_10);
}
```

E.3.2 I3C end of capture management

```
void HAL_I3C_CtrlMultipleXferCpltCallback(I3C_HandleTypeDef *hi3c)
{
p_buffer = p_buffer + VD55G1_I3C_READ_YSIZE;

if (i3c_bus_busy ==1)
{
  if (p_buffer >= (i3c_image + (VD55G1_I3C_READ_XSIZE*VD55G1_I3C_READ_YSIZE)))
  {
    p_buffer = i3c_image;
    i3c_bus_busy = 0;
  }

  __HAL_GPIO_EXTI_CLEAR_IT(GPIO_PIN_10);
  HAL_NVIC_ClearPendingIRQ(EXTI10_IRQn);
  HAL_NVIC_EnableIRQ(EXTI10_IRQn);
  }
}
```

E.4 Snapshots of sequences

This section shows snapshots that include the channels below.

- Channel 0 (I3C EOT interrupt): The time the firmware spends in an interrupt that is generated by the end of the I3C receive burst.
- Channel 1 (EXTI10 interrupt): The time the firmware spends in an interrupt that is generated when the sensor receives a rising edge on the GPIO0 IMAGE_READOUT.
- Channel 2 (GPIO0): The GPIO0 signal is configured as the IMAGE READOUT. Not all transition details are shown.
- Channel 3 (SCL): The I3C SCL activity. Not all transition details are shown.
- Channel 4 (SDA): The I3C SDA activity. Not all transition details are shown.

In all snapshots, the sensor was configured to stream 16 lines (to ease readability).

E.4.1 Frame activity snapshots

Figure 19. Activity during a total frame

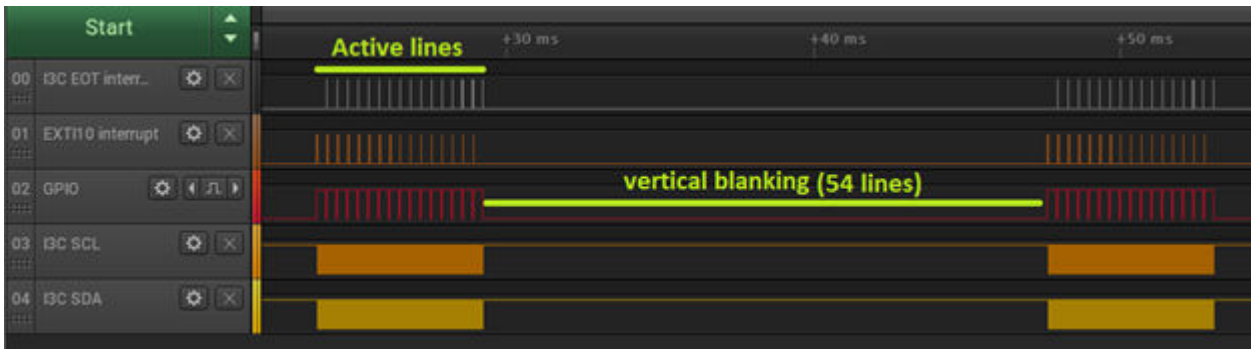
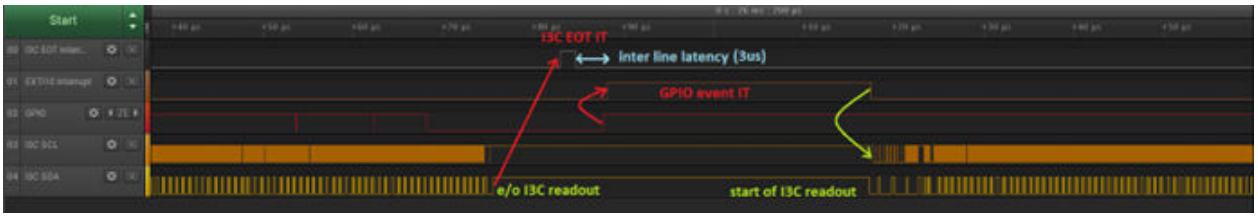


Figure 20. Zoom on the active line period

Figure 21. Zoom on horizontal blanking



E.4.2 GPIO IMAGE_READOUT details

Figure 22. **Regular pulses (glitches) in the IMAGE_READOUT signal**

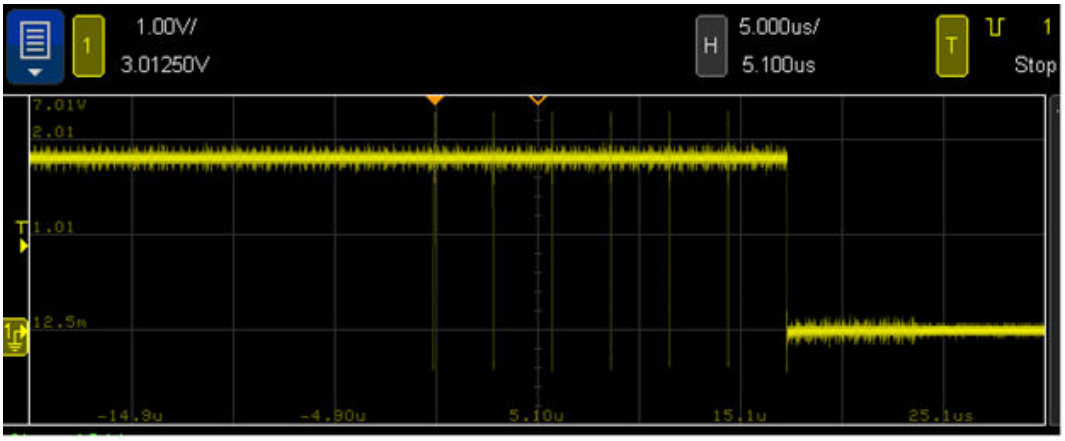
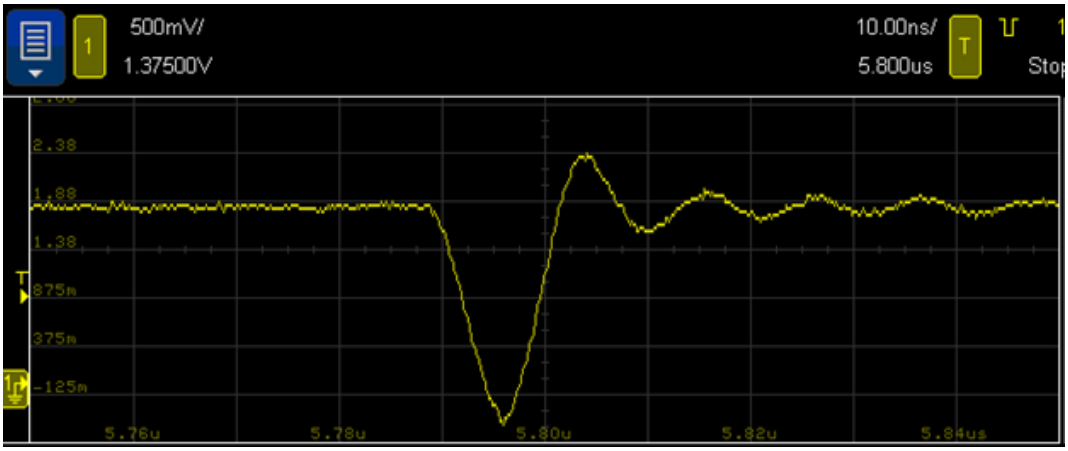


Figure 23. **Zoom on glitch**



Appendix F Spatial HDR mode

The following in an example script with TWO_EXPOSURE_HDR and autoexposure activated.

```
//SW_STBY
WriteAutoIncrement(0x0312, 0x02); // Activate TWO_EXPOSURE_HDR
WriteAutoIncrement(0x031c, 0x00, 0x00, 0x08, 0x00); //EXPOSURE_HDR_FIX_RATIO
WriteAutoIncrement(0x0486, 0x1e); // EXPOSURE_TARGET_PERCENTAGE_A
WriteAutoIncrement(0x0500, 0x02); // (val=0) / UI.STREAM_CTX0.EXPOSURE_MODE
```

F.1 TWO_EXPOSURE_HDR

Figure 24. TWO_EXPOSURE pixel schematic

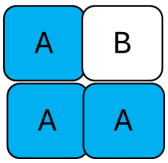


Figure 25. TWO_EXPOSURE timing

Manual exposure:
EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A: pixel integration time in line
EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B: pixel integration time in line

Note: The difference between the exposure values must be at least >4 to avoid issues with the image.

Autoexposition:
Pixel A is the long exposure.
EXPOSURE_HDR_FIX_RATIO
[15-31]: Exposure ratio multiplicator (multiplication of coarse exposure value only) between pixels B and A

Note: Setting EXPOSURE_HDR_FIX_RATIO to 0 creates issues on the image.

The gain for pixel A and pixel B is the same.

F.2 THREE_EXPOSURE_HDR

Figure 26. **THREE_EXPOSURE pixel schematic**

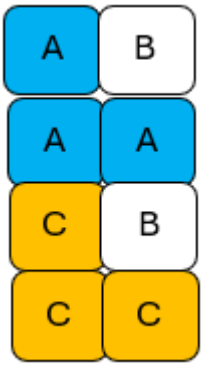


Figure 27. **THREE_EXPOSURE timing**

Manual exposure
EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A: pixel integration time in line
EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B: pixel integration time in line
EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C: pixel integration time in line

Note: The difference between the exposure values must be at least >4 to avoid image trouble.

EXPOSURE_HDR_FIX_RATIO

- [0-15]: Exposure ratio multiplicator (multiplication of coarse exposure value only) between pixels C and B
- [15-31]: Exposure ratio multiplicator (multiplication of coarse exposure value only) between pixels B and A

Note: Setting EXPOSURE_HDR_FIX_RATIO to 0 creates issues on the image.

The gain for pixels A, B, and C is the same.

F.3 TWO_EXPOSURE_LDR

The following is an example script
Manual exposition:
EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A: pixel integration time in line
EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B: pixel integration time in line

Note: The difference between the exposure values must be at least >4 to avoid image trouble.

Autoexposure:
Pixel A is the short exposure.
EXPOSURE_HDR_FIX_RATIO

- [15-31]: Exposure ratio multiplicator (multiplication of coarse exposure value only) between pixels B and A

Note: Setting EXPOSURE_HDR_FIX_RATIO to 0 creates issues on the image.

The gain for pixel A and pixel B is the same.

Appendix G Auto wake up

The VD55G1 can autonomously detect a change in the scene and trigger a decision to the host.

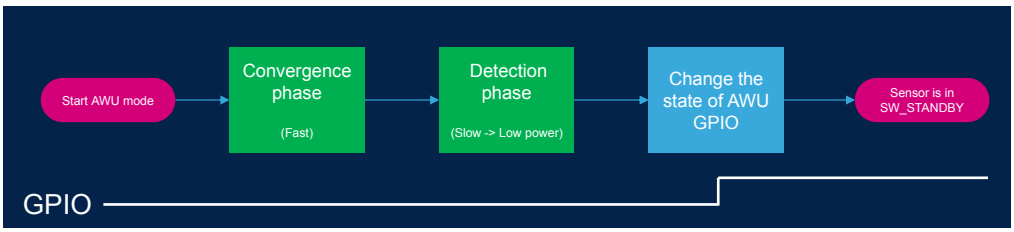
After a quick convergence phase (where the auto exposure and detection algorithm stabilize) the sensor switch to a low frame rate and wait for an event.

The event is a quick change in the exposure on the monitored part of the grid.

Once the event is detected, the sensor can:

- Stop streaming
- Raise any GPIO

Figure 28. Auto wake up flow



Convergence phase

This phase assumes that the scene is not changing.

1. Stabilization of the auto exposure.
2. Compute a reference level μ_{ref} and a reference standard deviation σ_{ref} for each zone of the grid based on the pixel accumulation (sum of the pixel values).

$$N = count_{pixel}$$

$$accumulation_{norm} = accumulation_{pixel} - pedestal \times N$$

$$\mu_{ref} = \frac{1}{N}\sum_{n=0}^{N-1} accumulation_{norm}\left(n\right)$$

$$\sigma_{ref} = \sqrt{\frac{1}{N}\sum_{n=0}^{N-1}\left(accumulation_{norm}(n) - \mu_{ref}\right)^2}$$

Detection phase

1. For any zone if $\left(\left|\mu_{last} - \mu_{ref}\right| > K \times \sigma_{ref}\right)$ then a change is detected.
   - μ_{last} is the last reference level computed in the same manner of μ_{ref} on the current frame
   - The K value is defined by register STREAM_STATICS.AWU_DETECTION_THRESHOLD
2. If enough zones have changed the AWU is triggered. The zone number is defined by register STREAM_STATICS.AWU_CTRL. NO_OF_ZONE_TO_WAKEUP
3. If there is no change detected, exposure and reference level are adjusted

$$accumulation_{norm} = \left(accumulation_{pixel} - pedestal \times count_{pixel}\right) \times \frac{exposure(init)}{exposure(last)}$$

When the host issues a START_AWU in the STBY command register, the sensor uses the context 3 streaming configuration. The only exception to that is the STREAM_STATICS.FRAME_LENGTH_FOR_CONVERGENCE register in the static group register. See the example for more details.

```
// UI.SENSOR_SETTINGS.EXT_CLOCK.VALUE / (val=12000000)
WriteAutoIncrement(0x0220, 0x0, 0x1b, 0xb7, 0x0);
 // UI.SENSOR_SETTINGS.MIPI_DATA_RATE.VALUE / (val=1200000000)
WriteAutoIncrement(0x0224, 0x0, 0x8c, 0x86, 0x47);
 // UI.STREAM_STATICS.LINE_LENGTH.VALUE / (val=1128)
WriteAutoIncrement(0x0300, 0x68, 0x4);

 // UI.STREAM_STATICS.AWU_DETECTION_THRESHOLD.INTEGER / (val=6)
WriteAutoIncrement(0x0370, 0x0, 0x6);
 // UI.STREAM_STATICS.AWU_CTRL / (val=4418)
WriteAutoIncrement(0x036c, 0x42, 0x11, 0x0, 0x0);
 // UI.STREAM_STATICS.EXPOSURE_USER_MAX_COARSE_INTEGRATION_LINES.VALUE / (val=446)
WriteAutoIncrement(0x0372, 0xbe, 0x1);
 // UI.STREAM_STATICS.AWU_CTRL.FRAME_LENGTH_FOR_CONVERGENCE / (val=2216)
WriteAutoIncrement(0x036c, 0x42, 0x11, 0xa8, 0x8);
 // UI.STREAM_STATICS.EXPOSURE_USE_CASES.ENABLE_MULTI_CONTEXT / (val=0)
WriteAutoIncrement(0x0312, 0x0);
 // UI.STREAM_STATICS.CONTEXT_NEXT_CONTEXT.CTX0 / (val=0)
WriteAutoIncrement(0x03e4, 0x10, 0x11);
 // UI.STREAM_STATICS.CONTEXT_NEXT_CONTEXT.CTX3 / (val=255)
WriteAutoIncrement(0x03e4, 0x10, 0xf1);
 // UI.STREAM_STATICS.CONTEXT_REPEAT_COUNT_CTX0.VALUE / (val=0)
WriteAutoIncrement(0x03dc, 0x0, 0x0);
 // UI.STREAM_STATICS.CONTEXT_REPEAT_COUNT_CTX3.VALUE / (val=0)
WriteAutoIncrement(0x03e2, 0x0, 0x0);

 // UI.STREAM_CTX0.EXPOSURE_MODE.MODE / (val=0)
WriteAutoIncrement(0x0500, 0x0);
 // UI.STREAM_CTX0.FRAME_LENGTH.VALUE / (val=2216)
WriteAutoIncrement(0x050c, 0xa8, 0x8, 0x0, 0x0);
 // UI.STREAM_CTX0.GPIO_0_CTRL.Mode / (val=2)
WriteAutoIncrement(0x051d, 0x2);
 // UI.STREAM_CTX0.GPIO_1_CTRL.Mode / (val=5)
WriteAutoIncrement(0x051e, 0x5);
 // UI.STREAM_CTX0.MASK_FRAME_CTRL / (val=0)
WriteAutoIncrement(0x0537, 0x00);

 // UI.STREAM_CTX3.FRAME_LENGTH.VALUE / (val=26595)
WriteAutoIncrement(0x05fc, 0xe3, 0x67, 0x0, 0x0);
 // UI.STREAM_CTX3.GPIO_0_CTRL.Mode / (val=2)
WriteAutoIncrement(0x060d, 0x2);
 // UI.STREAM_CTX3.GPIO_1_CTRL.Mode / (val=13)
WriteAutoIncrement(0x060e, 0xd);
 // UI.STREAM_CTX3.MASK_FRAME_CTRL / (val=1)
WriteAutoIncrement(0x0627, 0x01);
```

Appendix H Register map and description

H.1 Address blocks summary

Table 9. **UI address blocks**

Block base address	Address block name	Range	Description
0x0000	STATUS	0x200	Device status
0x0200	CMD	0x4	Commands to control the device
0x0220	SENSOR_SETTINGS	0x14	General settings of the device
0x0300	STREAM_STATICS	0x128	Static configuration for streaming
0x0480	STREAM_DYNAMICS	0x80	Dynamic configuration for streaming
0x0500	STREAM_CTX0	0x50	Used to control the dynamic settings of the sensor. The sensor can be configured to automatically switch between these settings from frame to frame
0x0550	STREAM_CTX1	0x50	
0x05A0	STREAM_CTX2	0x50	
0x05F0	STREAM_CTX3	0x50	
0x0640	NVM_MIRROR	0x100	Buffer for NVM operations

H.2 STATUS registers

H.2.1 STATUS register summary

Table 10. **STATUS register list**

Address	Register name	Description
0x0000	DEVICE_MODEL_ID	Device identification
0x0004	DEVICE_REVISION	Device revision
0x0006	WARNING_CODE	Warning detected by the firmware
0x0008	ROM_REVISION	ROM code revision
0x000C	UI_REVISION	Revision of the UI to use
0x000E	OPTICAL_REVISION	Optical revision of the device
0x0010	ERROR_CODE	Error detected by the firmware
0x0012	FWPATCH_REVISION	Firmware patch in used
0x0014	VTIMING_RD_REVISION	Read-Pattern Vtiming revision
0x0018	VTIMING_GR_REVISION	Global Reset-Pattern Vtiming revision
0x001A	VTIMING_GT_REVISION	Global Transfer-Sequence Vtiming revision
0x001C	SYSTEM_FSM	Sensor system FSM status
0x001E	NVM	NVM status
0x0028	EXT_CLOCK	Integer part of the external clock frequency in Hz
0x002C	SYSTEM_PLL_CLK	PLL output frequency in Hz
0x0030	PIXEL_CLK	Pixel clock frequency in Hz
0x0034	MCU_CLK	MCU clock frequency in Hz
0x0038	CLK_PLL_MULT	PLL multiplier value
0x0039	CLK_ERROR	Error detected in the clock tree
0x003A	I2C_ADDRESS	Address used for I2C/I3C
0x003C	TEMPERATURE	Last temperature measured with the thermal sensor
0x003E	FRAME_RATE	Frame rate
0x0040	FRAME_COUNTER	Global frame counter
0x0042	CONTEXT_FRAME_COUNTER	Context frame counter
0x0044	CONTEXT_REPEAT_COUNT	Number of frames for the context in use
0x0046	CURRENT_CONTEXT	Current context
0x0047	NEXT_CONTEXT	The next context to be streamed after a RepeatCount number of frames are streamed out
0x0048	ORIENTATION	Image orientation
0x004A	VT_CTRL	Video timing controls
0x004B	FORMAT_CTRL	Frame output format control
0x004C	OIF_CTRL	Configuration of the output interface
0x004E	OIF_VC_CTRL	Virtual channel
0x004F	OIF_IMG_CTRL	Data type for the image data
0x0050	OIF_ISL_CTRL	Data type for ISL
0x0051	PLL_STATUS	PLL status
0x0052	PATGEN_CTRL	Pattern generator control

Address	Register name	Description
0x0054	VT_COARSE_EXP_LINES_A	Applied coarse integration lines A
0x0056	VT_ANALOG_GAIN	Applied analog gain
0x0058	ISP_DIGITAL_GAIN_CH0	Digital gain, applied from the exposure algorithm channel 0
0x0060	EXPOSURE_MODE	Exposure mode control
0x0061	EXPOSURE_STATUS_A	Status of the auto exposure A
0x0062	EXPOSURE_MEAN_ENERGY_A	Mean energy of the input image for the auto exposure A
0x0064	LINE_LENGTH	Applied line length
0x0066	ISP_EXPOSURE_DIGITAL_GAIN	Digital gain, computed by the exposure in automatic mode
0x0068	FRAME_LENGTH	Applied frame length
0x006C	X_START	Image X start from the video timing
0x006E	X_END	Image X end from the video timing
0x0070	Y_START	Image Y start from the video timing
0x0072	Y_END	Image Y end from the video timing
0x0074	X_SIZE	Image X size
0x0076	Y_SIZE	Image Y size
0x0078	READOUT_CTRL	Streaming readout mode control
0x007A	WAIT_DELAY	Wait time before the next frame, and blanking in lines
0x007C	EXPOSURE_COARSE_EXP_LINES_B	Coarse exposure time in lines
0x007E	EXPOSURE_COARSE_EXP_LINES_C	Coarse exposure time in lines
0x0080	EXPOSURE_MEAN_ENERGY_B	Mean energy of the input image
0x0082	EXPOSURE_LIMITS_MINIMUM_COARSE_LINES	Minimum coarse integration in lines
0x0084	EXPOSURE_LIMITS_MAXIMUM_COARSE_LINES	Maximum coarse integration in lines
0x0090	USER	This register is a marker
0x0091	GPIO_0_CTRL	Input GPIO value if input mode is used
0x0092	GPIO_1_CTRL	Input GPIO value if input mode is used
0x0093	GPIO_2_CTRL	Input GPIO value if input mode is used
0x0094	GPIO_3_CTRL	Input GPIO value if input mode is used
0x0095	DARKCAL_CTRL	Darck calibration configuration
0x0096	DARKCAL_PEDESTAL	Pedestal value used in the DDC block
0x00A8	DARKCAL_STATS_CH0	Channel 0 statistics
0x00AC	DARKCAL_STATS_CH1	Channel 1 statistics
0x00B0	DARKCAL_STATS_CH2	Channel 2 statistics
0x00B4	DARKCAL_STATS_CH3	Channel 3 statistics
0x00B8	STARTUP_TIME	Time for start up
0x00BC	BOOT_TIME	Time for boot
0x00E8	EXPOSURE_COARSE_EXP_LINES_A	Coarse exposure time in lines
0x00EA	EXPOSURE_ANALOG_GAIN	Analog gain used
0x00EC	EXPOSURE_DIGITAL_GAIN_CH0	Digital gain, applied from the exposure algorithm channel 0
0x00F4	PATCH_TIME	Time to run the patch command
0x0104	VT_SUBTRACTION_CTRL	Delay between the integration lines
0x0106	STREAMING_FSM	FSM streaming status

Address	Register name	Description
0x0107	LOW_POWER_MODE_FEASIBLE	Low power mode feasability
0x0128	VT_COARSE_EXP_LINES_B	Coarse exposure time in lines
0x012A	VT_COARSE_EXP_LINES_C	Coarse exposure time in lines
0x012C	EXPOSURE_USE_CASES	Auto exposure configuration
0x012D	EXPOSURE_STATUS_B	Auto exposure B status
0x012E	EXPOSURE_GROUP_TOKEN	Exposure token status
0x012F	FSM_AWU_STATE	AWU FSM status
0x0130	CHANNEL_STAT_MEAN_ENERGY_ACC0	Mean energy of the accumulator 0
0x0132	CHANNEL_STAT_MEAN_ENERGY_ACC1	Mean energy of accumulator 1
0x0134	CHANNEL_STAT_MEAN_ENERGY_ACC2	Mean energy of accumulator 2
0x0136	DARK_LINES_COUNT	Number of dark lines streamed
0x0137	PWL	PWL status
0x0138	DEFCOR_STATUS	Number of defects corrected by DEFCOR
0x0140	MANUFACTURER_ID	Manufacturer's ID
0x0143	AWU_LEARN_DEFINITIVE	True when the reference levels and standard deviations for the current frame can be trusted
0x0144	AWU_STATUS	Status of the auto wake up
0x0148	VT_SUB_WAIT	Delay between two integrations in VT subtraction mode
0x014C	VT_SUB_DIGITAL_OFFSET	Offset for VT-SUB
0x014E	VT_MODE	Mode of the video timing
0x014F	CHANNEL_STATS_STATE_FOR_EXPOSURE	Channel stat IP status
0x0154	VT_START_TIME	VT start time
0x0158	VT_STOP_TIME	VT stop time
0x0170	EXPOSURE_PENDING_INTG_ABSORBED	Flag set when pending exposure is absorbed
0x0171	EXPOSURE_ACTIVE_INSTANCE	Exposure instance used for the actual frame
0x0174	EXPOSURE_COARSE_INTG_MARGIN	Coarse exposure integration margin
0x0176	EXPOSURE_NON_OVERLAP_LIMIT	Nonoverlap exposure limit
0x0178	LOW_POWER_INTER_FRAME_COMPUTED	Time between frames in LP mode
0x0180	LOW_POWER_LONGEST_EXPOSURE_SELECTED	Longest exposure selected in LP mode
0x0182	EXPOSURE_MAX_COARSE_LINES_VT_SUB_A	Maximum coarse integration in lines for VT-SUB mode A
0x0184	EXPOSURE_MAX_COARSE_LINES_VT_SUB_B	Maximum coarse integration in lines for VT-SUB mode B
0x0186	EXPOSURE_MAX_COARSE_LINES_VT_MULTI	Maximum coarse integration in lines for VT-multi-exposure mode

H.2.2 DEVICE_MODEL_ID

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x0000

Type: RO

Reset: 0x5335 4731

Description: Device identification

[31:0]	**VALUE:** VD55G1 device name

H.2.3 DEVICE_REVISION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOP_DIE								BOTTOM_DIE							
RO								RO							

Address: 0x0004

Type: RO

Reset: 0x0202

Description: Device revision

[15:8]	**TOP_DIE:** Top die mask code (HW)
[7:0]	**BOTTOM_DIE:** Bottom die mask code (HW)

H.2.4 WARNING_CODE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0006

Type: RO

Reset: 0x0000

Description: Warning detected by the firmware

[15:0] **VALUE:** Warning codes

-0x0000: DEFINES_NO_SYSTEM_ERROR
-0x0001: DEFINES_SYSTEM_ERROR_ERR0
-0x0002: DEFINES_MCU_ITC_INIT_IRQ
-0x0100: CRM_ERROR_PLL_SYS_LOCK_TIMEOUT
-0x0101: CRM_ERROR_PLL_DAC_LOCK_TIMEOUT
-0x0102: CRM_ERROR_DAC_MULT_DIV
-0x0103: CRM_ERROR_DPHY_ESC_RANGE
-0x0104: CRM_ERROR_THSENS_RANGE
-0x0105: CRM_ERROR_EXT_CLK_RANGE
-0x0106: CRM_ERROR_HOST_CLK_RANGE
-0x0107: CRM_ERROR_PLL_MULT_RANGE
-0x0108: CRM_ERROR_COUNTER_CLK_FREQ
-0x0109: CRM_ERROR_PIXEL_CLK_FREQ
-0x0200: DEFINES_THSENS_TIMEOUT_ERROR
-0x0201: DEFINES_THSENS_DATAREADY_ERROR
-0x0202: DEFINES_THSENS_TEMP_125_ERROR
-0x0203: DEFINES_THSENS_TEMP_135_ERROR
-0x0300: DPHYTX_BASE_ERROR
-0x0400: XP70PATCH_ERROR_PATCH_CODE_TOO_LARGE
-0x0401: XP70PATCH_ERROR_TOO_MANY_PATCHES
-0x0402: XP70PATCH_ERROR_TOO_MANY_HOOKS
-0x0403: XP70PATCH_ERROR_BAD_CRC
-0x0404: XP70PATCH_ERROR_BAD_PATCH_ADDR
-0x0405: XP70PATCH_ERROR_BAD_MD5SUM
-0x0500: EXCEPTIONS_ERROR_PROTECT
-0x0501: EXCEPTIONS_ERROR_OPCODE
-0x0502: EXCEPTIONS_ERROR_GPRSIZE
-0x0503: EXCEPTIONS_ERROR_PMISALIGN
-0x0504: EXCEPTIONS_ERROR_POUTOFMEM
-0x0505: EXCEPTIONS_ERROR_PEXECUTE
-0x0506: EXCEPTIONS_ERROR_DMISALIGN
-0x0507: EXCEPTIONS_ERROR_DOUTOFMEM
-0x0508: EXCEPTIONS_ERROR_DREAD
-0x0509: EXCEPTIONS_ERROR_DWRITE
-0x050A: EXCEPTIONS_ERROR_PSYSERR
-0x050B: EXCEPTIONS_ERROR_OVERFLOW
-0x050C: EXCEPTIONS_ERROR_UNKNOWN
-0x0600: CRCCCITT_BASE_ERROR
-0x0700: MULTICROPPER_BASE_ERROR
-0x0800: DEFINES_I3C_PAD_COMMS_DRIVE_ERROR
-0x0A00: DEFINES_VTIMING_LONG_COARSE_MAX_ERROR
-0x0A01: DEFINES_VTIMING_LONG_COARSE_MIN_ERROR
-0x0A02: DEFINES_VTIMING_LONG_COARSE_IR_MAX_ERROR
-0x0A03: DEFINES_VTIMING_LONG_COARSE_IR_MIN_ERROR
-0x0A04: DEFINES_VTIMING_BAD_FRAME_LENGTH_ERROR

-0x0A05: DEFINES_VTIMING_ISB_LONG_PIPE_OVERFLOW
-0x0A06: DEFINES_VTIMING_Y_SIZE_SS_ERROR
-0x0A07: DEFINES_VTIMING_X_SIZE_SS_ERROR
-0x0A08: DEFINES_VTIMING_BGISON_LOW
-0x0A09: DEFINES_VTIMING_BGISON_HIGH
-0x0A0A: DEFINES_VTIMING_TOKEN_NOT_FOUND_ERROR
-0x0B00: DEFINES_ISP_SDR_FIFO_FULL_ERROR
-0x0B01: DEFINES_ISP_ISLGEN_INVALID_CFG_ERROR
-0x0B02: DEFINES_ISP_ISLGEN_MEMORY_LOCKED_ERROR
-0x0B03: DEFINES_ISP_ISLGEN_MISSED_TRIGGER_ERROR
-0x0B04: DEFINES_ISP_ISLGEN_TOO_MANY_ENTRIES_ERROR
-0x0B05: DEFINES_ISP_MULTICROP_NO_ROI_ERROR
-0x0B06: DEFINES_ISP_ISB2IDP_LINEBLANKING_ERROR
-0x0B07: DEFINES_ISP_CHANNELSTATS_CHANNEL_INDEX_ERROR
-0x0B08: DEFINES_ISP_CHANNELSTATS_ROI_ERROR
-0x0B09: DEFINES_ISP_CHANNELSTATS_STATS_OV_ERROR
-0x0B0A: DEFINES_ISP_PATGEN_ERROR_INVALID_PATTERN
-0x0B0B: DEFINES_ISP_X_Y_ERROR_INVALID_XY_CONFIG
-0x0B0C: DEFINES_ISP_CHANNELSTATS_PATTERN_ERROR
-0x0B0D: DEFINES_ISP_EXPOSURE_USE_CASE_ERROR
-0x0C00: DEFINES_OIF_CSI_LANE_DESYNC_ERROR
-0x0C01: DEFINES_OIF_CSI_PKT_TOO_LONG_ERROR
-0x0C02: DEFINES_OIF_CSI_PKT_TOO_SHORT_ERROR
-0x0C03: DEFINES_OIF_CSI_UNDERFLOW_ERROR
-0x0C04: DEFINES_OIF_MERGER_EXT_SYNC_MISSED_ERROR
-0x0C05: DEFINES_OIF_ISB2T1_UNDERFLOW
-0x0C06: DEFINES_OIF_I3CRDOUT_CONFIG_ERROR
-0x0C07: DEFINES_OIF_I3CRDOUT_IBI_ERROR
-0x0D00: DEFINES_GENERIC_BAD_PARAM_NVM_CTRL

H.2.5 ROM_REVISION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				MAJOR_REVISION				MINOR_REVISION				MICRO_REVISION			
-				RO				RO				RO			

Address: 0x0008

Type: RO

Reset: 0x0252

Description: ROM code revision

[11:8]	**MAJOR_REVISION:** Major ROM code revision
[7:4]	**MINOR_REVISION:** Minor ROM code revision
[3:0]	**MICRO_REVISION:** Micro ROM code revision

H.2.6 UI_REVISION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAJOR_REVISION								MINOR_REVISION							
RO								RO							

Address: 0x000C

Type: RO

Reset: 0x0249

Description: Revision of the UI to use

[15:8]	**MAJOR_REVISION:** Major UI revision
[7:0]	**MINOR_REVISION:** Minor UI revision

H.2.7 OPTICAL_REVISION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x000E

Type: RO

Reset: 0x0000

Description: Optical revision of the device

[15:0]	**VALUE:** Optical revision

H.2.8 ERROR_CODE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0010

Type: RO

Reset: 0x0000

Description: Error detected by the firmware

[15:0] **VALUE:** Error code

-0x0000: DEFINES_NO_SYSTEM_ERROR
-0x0001: DEFINES_SYSTEM_ERROR_ERR0
-0x0002: DEFINES_MCU_ITC_INIT_IRQ
-0x0100: CRM_ERROR_PLL_SYS_LOCK_TIMEOUT
-0x0101: CRM_ERROR_PLL_DAC_LOCK_TIMEOUT
-0x0102: CRM_ERROR_DAC_MULT_DIV
-0x0103: CRM_ERROR_DPHY_ESC_RANGE
-0x0104: CRM_ERROR_THSENS_RANGE
-0x0105: CRM_ERROR_EXT_CLK_RANGE
-0x0106: CRM_ERROR_HOST_CLK_RANGE
-0x0107: CRM_ERROR_PLL_MULT_RANGE
-0x0108: CRM_ERROR_COUNTER_CLK_FREQ
-0x0109: CRM_ERROR_PIXEL_CLK_FREQ
-0x0200: DEFINES_THSENS_TIMEOUT_ERROR
-0x0201: DEFINES_THSENS_DATAREADY_ERROR
-0x0202: DEFINES_THSENS_TEMP_125_ERROR
-0x0203: DEFINES_THSENS_TEMP_135_ERROR
-0x0300: DPHYTX_BASE_ERROR
-0x0400: XP70PATCH_ERROR_PATCH_CODE_TOO_LARGE
-0x0401: XP70PATCH_ERROR_TOO_MANY_PATCHES
-0x0402: XP70PATCH_ERROR_TOO_MANY_HOOKS
-0x0403: XP70PATCH_ERROR_BAD_CRC
-0x0404: XP70PATCH_ERROR_BAD_PATCH_ADDR
-0x0405: XP70PATCH_ERROR_BAD_MD5SUM
-0x0500: EXCEPTIONS_ERROR_PROTECT
-0x0501: EXCEPTIONS_ERROR_OPCODE
-0x0502: EXCEPTIONS_ERROR_GPRSIZE
-0x0503: EXCEPTIONS_ERROR_PMISALIGN
-0x0504: EXCEPTIONS_ERROR_POUTOFMEM
-0x0505: EXCEPTIONS_ERROR_PEXECUTE
-0x0506: EXCEPTIONS_ERROR_DMISALIGN
-0x0507: EXCEPTIONS_ERROR_DOUTOFMEM
-0x0508: EXCEPTIONS_ERROR_DREAD
-0x0509: EXCEPTIONS_ERROR_DWRITE
-0x050A: EXCEPTIONS_ERROR_PSYSERR
-0x050B: EXCEPTIONS_ERROR_OVERFLOW
-0x050C: EXCEPTIONS_ERROR_UNKNOWN
-0x0600: CRCCCITT_BASE_ERROR
-0x0700: MULTICROPPER_BASE_ERROR
-0x0800: DEFINES_I3C_PAD_COMMS_DRIVE_ERROR
-0x0A00: DEFINES_VTIMING_LONG_COARSE_MAX_ERROR
-0x0A01: DEFINES_VTIMING_LONG_COARSE_MIN_ERROR
-0x0A02: DEFINES_VTIMING_LONG_COARSE_IR_MAX_ERROR
-0x0A03: DEFINES_VTIMING_LONG_COARSE_IR_MIN_ERROR
-0x0A04: DEFINES_VTIMING_BAD_FRAME_LENGTH_ERROR

-0x0A05: DEFINES_VTIMING_ISB_LONG_PIPE_OVERFLOW
-0x0A06: DEFINES_VTIMING_Y_SIZE_SS_ERROR
-0x0A07: DEFINES_VTIMING_X_SIZE_SS_ERROR
-0x0A08: DEFINES_VTIMING_BGISON_LOW
-0x0A09: DEFINES_VTIMING_BGISON_HIGH
-0x0A0A: DEFINES_VTIMING_TOKEN_NOT_FOUND_ERROR
-0x0B00: DEFINES_ISP_SDR_FIFO_FULL_ERROR
-0x0B01: DEFINES_ISP_ISLGEN_INVALID_CFG_ERROR
-0x0B02: DEFINES_ISP_ISLGEN_MEMORY_LOCKED_ERROR
-0x0B03: DEFINES_ISP_ISLGEN_MISSED_TRIGGER_ERROR
-0x0B04: DEFINES_ISP_ISLGEN_TOO_MANY_ENTRIES_ERROR
-0x0B05: DEFINES_ISP_MULTICROP_NO_ROI_ERROR
-0x0B06: DEFINES_ISP_ISB2IDP_LINEBLANKING_ERROR
-0x0B07: DEFINES_ISP_CHANNELSTATS_CHANNEL_INDEX_ERROR
-0x0B08: DEFINES_ISP_CHANNELSTATS_ROI_ERROR
-0x0B09: DEFINES_ISP_CHANNELSTATS_STATS_OV_ERROR
-0x0B0A: DEFINES_ISP_PATGEN_ERROR_INVALID_PATTERN
-0x0B0B: DEFINES_ISP_X_Y_ERROR_INVALID_XY_CONFIG
-0x0B0C: DEFINES_ISP_CHANNELSTATS_PATTERN_ERROR
-0x0B0D: DEFINES_ISP_EXPOSURE_USE_CASE_ERROR
-0x0C00: DEFINES_OIF_CSI_LANE_DESYNC_ERROR
-0x0C01: DEFINES_OIF_CSI_PKT_TOO_LONG_ERROR
-0x0C02: DEFINES_OIF_CSI_PKT_TOO_SHORT_ERROR
-0x0C03: DEFINES_OIF_CSI_UNDERFLOW_ERROR
-0x0C04: DEFINES_OIF_MERGER_EXT_SYNC_MISSED_ERROR
-0x0C05: DEFINES_OIF_ISB2T1_UNDERFLOW
-0x0C06: DEFINES_OIF_I3CRDOUT_CONFIG_ERROR
-0x0C07: DEFINES_OIF_I3CRDOUT_IBI_ERROR
-0x0D00: DEFINES_GENERIC_BAD_PARAM_NVM_CTRL

H.2.9 FWPATCH_REVISION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAJOR_REVISION								MINOR_REVISION							
RO								RO							

Address: 0x0012

Type: RO

Reset: 0x0000

Description: Firmware patch in used

[15:8]	**MAJOR_REVISION:** Major FWP revision
[7:0]	**MINOR_REVISION:** Minor FWP revision

H.2.10 VTIMING_RD_REVISION

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTRAM_UPDATED	RESERVED							LDEC								RESERVED								PATTERN							
RO	-							RO								-								RO							

Address: 0x0014

Type: RO

Reset: 0x0000 0000

Description: Read-Pattern Vtiming revision

[31]	**VTRAM_UPDATED:** VTRAM update status in case of a manual update
[23:16]	**LDEC:** Line decoder timing version
[7:0]	**PATTERN:** RD pattern timing version

H.2.11 VTIMING_GR_REVISION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PATTERN							
-								RO							

Address: 0x0018

Type: RO

Reset: 0x0000

Description: Global Reset-Pattern Vtiming revision

[7:0]	**PATTERN:** GR pattern timing version

H.2.12 VTIMING_GT_REVISION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PATTERN							
-								RO							

Address: 0x001A

Type: RO

Reset: 0x0000

Description: Global Transfer-Sequence Vtiming revision

[7:0]	**PATTERN:** GT pattern timing version

H.2.13 SYSTEM_FSM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				VALUE							
-				-				RO							

Address: 0x001C

Type: RO

Reset: 0x0001

Description: Sensor system FSM status

[7:0] **VALUE:** Sensor system FSM status

-0x00: HW_STBY
-0x01: READY_TO_BOOT
-0x02: SW_STBY
-0x03: STREAMING
-0x04: STREAMING_AWU_MODE
-0xAA: FW_STALL
-0xFF: ERROR

H.2.14 NVM

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DRIVER_FSM		ECC_ERROR	RESERVED	READ_FAIL	READ_OK	PROG_FAIL	PROG_OK
-								RO		RO	-	RO	RO	RO	RO

Address: 0x001E

Type: RO

Reset: 0x0000

Description: NVM status

[7:6]	**DRIVER_FSM:** NVM driver FSM -0x00: IDLE -0x01: PROG_OP -0x02: READ_OP -0x03: ERROR
[5]	**ECC_ERROR:** ECC error detection -0x0: NO_ERROR -0x1: ECC_ERROR
[3]	**READ_FAIL:** Error during a read operation
[2]	**READ_OK:** Successful read operation
[1]	**PROG_FAIL:** Error during a program operation
[0]	**PROG_OK:** Successful program operation

H.2.15 EXT_CLOCK

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x0028

Type: RO

Reset: 0x0000 0000

Description: Integer part of the external clock frequency in Hz

[31:0]	**VALUE:** Integer part of the external clock frequency in Hz

H.2.16 SYSTEM_PLL_CLK

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x002C

Type: RO

Reset: 0x0000 0000

Description: PLL output frequency in Hz

[31:0]	**VALUE:** PLL output frequency in Hz

H.2.17 PIXEL_CLK

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x0030

Type: RO

Reset: 0x0000 0000

Description: Pixel clock frequency in Hz

[31:0]	**VALUE:** Pixel clock frequency in Hz

H.2.18 MCU_CLK

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x0034

Type: RO

Reset: 0x0000 0000

Description: MCU clock frequency in Hz

[31:0]	**VALUE:** MCU clock frequency in Hz

H.2.19 CLK_PLL_MULT

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0038

Type: RO

Reset: 0x00

Description: PLL multiplier value

[7:0]	**VALUE:** PLL multiplier value

H.2.20 CLK_ERROR

7	6	5	4	3	2	1	0
CLK_ERR_THSENS	CLK_ERR_ESC	CLK_ERR_NVM	CLK_ERR_HOST	CLK_ERR_CPNEG	CLK_ERR_CPPOS	CLK_ERR_COUNTER	CLK_ERR_PIX
RO	RO	RO	RO	RO	RO	RO	RO

Address: 0x0039

Type: RO

Reset: 0x00

Description: Error detected in the clock tree

[7]	**CLK_ERR_THSENS:** Bit 7: CLK_ERR_THSENS = 0 if 125 kHz ≤ CLK_ERR_THSENS ≤ 250 kHz
[6]	**CLK_ERR_ESC:** Bit 6: CLK_ERR_ESC = 0 if CLK_ERR_ESC ≤ 20 MHz
[5]	**CLK_ERR_NVM:** Bit 5: CLK_ERR_NVM = 0 if 10 MHz ≤ CLK_ERR_NVM ≤ 67 MHz. All other situations = 1
[4]	**CLK_ERR_HOST:** Bit 4, CLK_ERR_HOST = 0 if CLK_ERR_HOST ≤ 175 MHz. All other situations = 1.
[3]	**CLK_ERR_CPNEG:** Bit 3, CLK_ERR_CPNEG = 0 if 150 MHz ≤ CLK_ERR_CPNEG ≤ 161 MHz. All other situations = 1.
[2]	**CLK_ERR_CPPOS:** Bit 2, CLK_ERR_CPPOS = 0 if 400 MHz ≤ CLK_ERR_CPPOS ≤ 500 MHz. All other situations = 1
[1]	**CLK_ERR_COUNTER:** Bit 1, CLK_ERR_COUNTER = 0 if CLK_ERR_COUNTER ≤ 400 MHz. All other situations = 1.
[0]	**CLK_ERR_PIX:** Bit 0, CLK_ERR_PIX = 0 if CLK_ERR_COUNTER/CLK_ERR_PIX ≥ 8/3. All other situations = 1.

H.2.21 I2C_ADDRESS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_ID															RESERVED
RO															-

Address: 0x003A

Type: RO

Reset: 0x0020

Description: Address used for I2C/I3C

[15:1]	**DEVICE_ID:** Device I3C address

H.2.22 TEMPERATURE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH_DEGREE_INT															
RO															

Address: 0x003C

Type: RO

Reset: 0x0000

Description: Last temperature measured with the thermal sensor

[15:0]	**TH_DEGREE_INT:** Temperature in Celcius

H.2.23 FRAME_RATE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x003E

Type: RO

Reset: 0x0000

Description: Frame rate

[15:0]	**VALUE:** Frame rate (in 12.4 fixed point format)

H.2.24 FRAME_COUNTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0040

Type: RO

Reset: 0x0000

Description: Global frame counter

[15:0]	**VALUE:** Frame counter over all contexts

H.2.25 CONTEXT_FRAME_COUNTER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0042

Type: RO

Reset: 0x0000

Description: Context frame counter

[15:0]	**VALUE:** Frame counter for the context in use

H.2.26 CONTEXT_REPEAT_COUNT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0044

Type: RO

Reset: 0x0000

Description: Number of frames for the context in use

[15:0]	**VALUE:** Number of frames for the context in use

H.2.27 CURRENT_CONTEXT

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0046

Type: RO

Reset: 0x00

Description: Current context

[7:0]	**VALUE:** Current context

H.2.28 NEXT_CONTEXT

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0047

Type: RO

Reset: 0x00

Description: The next context to be streamed after a RepeatCount number of frames are streamed out

[7:0]	**VALUE:** The next context to be streamed after a RepeatCount number of frames are streamed out. If this register carries a value > 3, the FW performs a stop streaming operation, after streaming the frames equal to the number stipulated in the RepeatCount register.

H.2.29 ORIENTATION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MODE	
-														RO	

Address: 0x0048

Type: RO

Reset: 0x0000

Description: Image orientation

[1:0]	**MODE:** Image orientation mode control -0x0: = no flip -0x1: = X flip -0x2: = Y flip -0x3: = XY flip

H.2.30 VT_CTRL

7	6	5	4	3	2	1	0
RESERVED					ADC_MODE	SYNC_MODE	
-					RO	RO	

Address: 0x004A

Type: RO

Reset: 0x00

Description: Video timing controls

[2]	**ADC_MODE:** Video timing ADC mode 9 or 10 bits -0x0: = standard mode with 10 bits -0x1: = fast mode with 9 bits
[1:0]	**SYNC_MODE:** Video timing synchronization mode -0x0: = master mode -0x1: = streaming on EXTSYNC pulses -0x2: = streaming on I3C pulses

H.2.31 FORMAT_CTRL

7	6	5	4	3	2	1	0
RESERVED					OUT_FORMAT		
-					RO		

Address: 0x004B

Type: RO

Reset: 0x00

Description: Frame output format control

[4:0]	**OUT_FORMAT:** Frame output format control -0x8: RAW8 -0xA: RAW10

H.2.32 OIF_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DATALANE0_SWAP	RESERVED		CLKLANE_SWAP	RESERVED		
-									RO	-		RO	-		

Address: 0x004C

Type: RO

Reset: 0x0000

Description: Configuration of the output interface

[6] **DATALANE0_SWAP:** Lane swapping

-0x0: NO_SWAP
-0x1: LANE_SWAP

[3] **CLKLANE_SWAP:** Clock lane swapping

-0x0: NO_SWAP
-0x1: LANE_SWAP

H.2.33 OIF_VC_CTRL

7	6	5	4	3	2	1	0
RESERVED				ISL		ACTIVE_PIX	
-				RO		RO	

Address: 0x004E

Type: RO

Reset: 0x00

Description: Virtual channel

[3:2]	**ISL:** Virtual channel selection for ISL
[1:0]	**ACTIVE_PIX:** Virtual channel selection for image

H.2.34 OIF_IMG_CTRL

7	6	5	4	3	2	1	0
RESERVED				DATA_TYPE			
-				RO			

Address: 0x004F

Type: RO

Reset: 0x00

Description: Data type for the image data

[5:0]	**DATA_TYPE:** Data type selection aligned with RAW format

H.2.35 OIF_ISL_CTRL

7	6	5	4	3	2	1	0
RESERVED				DATA_TYPE			
-				RO			

Address: 0x0050

Type: RO

Reset: 0x00

Description: Data type for ISL

[5:0]	**DATA_TYPE:** Data type selection

H.2.36 PLL_STATUS

7	6	5	4	3	2	1	0
RESERVED					SYSTEM_CLOCK_EXT_VS_PLL	PLL_LOCK	
-					RO	RO	

Address: 0x0051

Type: RO

Reset: 0x00

Description: PLL status

[2]	**SYSTEM_CLOCK_EXT_VS_PLL:** System clock driven by -0x0: EXTERNAL -0x1: PLL
[1:0]	**PLL_LOCK:** PLL lock status -0x0: UNLOCK -0x1: WAITING_FOR_LOCK -0x2: LOCK

H.2.37 PATGEN_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						TYPE						RESERVED		ENABLE	
-						RO						-		RO	

Address: 0x0052

Type: RO

Reset: 0x0000

Description: Pattern generator control

[9:4]	**TYPE:** -0x22: = diagonal grayscale -0x28: = pseudo random
[1:0]	**ENABLE:** Patgen configuration -0x00: BYPASS -0x01: PATGEN_NORMAL

H.2.38 VT_COARSE_EXP_LINES_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0054

Type: RO

Reset: 0x0000

Description: Applied coarse integration lines A

[15:0]	**VALUE:** Coarse integration lines A

H.2.39 VT_ANALOG_GAIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											VALUE				
-											RO				

Address: 0x0056

Type: RO

Reset: 0x0000

Description: Applied analog gain

[4:0] **VALUE:**

-0x00: AnalogGain_AGAIN_1
-0x01: AnalogGain_AGAIN_1_03
-0x02: AnalogGain_AGAIN_1_07
-0x03: AnalogGain_AGAIN_1_1
-0x04: AnalogGain_AGAIN_1_14
-0x05: AnalogGain_AGAIN_1_19
-0x06: AnalogGain_AGAIN_1_23
-0x07: AnalogGain_AGAIN_1_28
-0x08: AnalogGain_AGAIN_1_33
-0x09: AnalogGain_AGAIN_1_39
-0x0A: AnalogGain_AGAIN_1_45
-0x0B: AnalogGain_AGAIN_1_52
-0x0C: AnalogGain_AGAIN_1_6
-0x0D: AnalogGain_AGAIN_1_68
-0x0E: AnalogGain_AGAIN_1_78
-0x0F: AnalogGain_AGAIN_1_88
-0x10: AnalogGain_AGAIN_2
-0x11: AnalogGain_AGAIN_2_13
-0x12: AnalogGain_AGAIN_2_29
-0x13: AnalogGain_AGAIN_2_46
-0x14: AnalogGain_AGAIN_2_67
-0x15: AnalogGain_AGAIN_2_91
-0x16: AnalogGain_AGAIN_3_2
-0x17: AnalogGain_AGAIN_3_56
-0x18: AnalogGain_AGAIN_4
-0x19: AnalogGain_AGAIN_4_57
-0x1A: AnalogGain_AGAIN_5_33
-0x1B: AnalogGain_AGAIN_6_4
-0x1C: AnalogGain_AGAIN_8

H.2.40 ISP_DIGITAL_GAIN_CH0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RO								RO							

Address: 0x0058

Type: RO

Reset: 0x0000

Description: Digital gain, applied from the exposure algorithm channel 0

[15:8]	**INTEGER:** Digital gain, applied from the exposure algorithm channel 0. Note that the integer part is in 5.8 fixed point format.
[7:0]	**FRACT:** Digital gain, applied from the exposure algorithm channel 0. Note that the fractional part is in 5.8 fixed point format.

H.2.41 EXPOSURE_MODE

7	6	5	4	3	2	1	0
RESERVED					MODE		
-					RO		

Address: 0x0060

Type: RO

Reset: 0x00

Description: Exposure mode control

[2:0] **MODE:** Exposure mode control

-0x0: = automatic mode
-0x1: = freeze AE with currentt settings
-0x2: = manual setting mode
-0x4: BYPASS

H.2.42 EXPOSURE_STATUS_A

7	6	5	4	3	2	1	0
			RESERVED				STATUS
			-				RO

Address: 0x0061

Type: RO

Reset: 0x00

Description: Status of the auto exposure A

[0] **STATUS:**

-0x0: UNSTABLE
-0x1: STABLE

H.2.43 EXPOSURE_MEAN_ENERGY_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RO								RO							

Address: 0x0062

Type: RO

Reset: 0x0000

Description: Mean energy of the input image for the auto exposure A

[15:8]	**INTEGER:** Mean energy of the input image (integer part)
[7:0]	**FRACT:** Mean energy of the input image (fractional part)

H.2.44 LINE_LENGTH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0064

Type: RO

Reset: 0x0000

Description: Applied line length

[15:0]	**VALUE:** Line length output from the sensor (including the line blanking)

H.2.45 ISP_EXPOSURE_DIGITAL_GAIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RO								RO							

Address: 0x0066

Type: RO

Reset: 0x0000

Description: Digital gain, computed by the exposure in automatic mode

[15:8]	**INTEGER:** Digital gain, computed by the exposure in automatic mode. This gain does not include white balance gains. It represents only the integer part of the gain in fixed point format.
[7:0]	**FRACT:** Digital gain, computed by the exposure in automatic mode. This gain does not include white balance gains. It represents only the fractional part of the gain in fixed point format.

H.2.46 FRAME_LENGTH

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x0068

Type: RO

Reset: 0x0000 0000

Description: Applied frame length

[31:0]	**VALUE:** Frame length as programmed in the sensor

H.2.47 X_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x006C

Type: RO

Reset: 0x0000

Description: Image X start from the video timing

[15:0]	**VALUE:** Image X start from the video timing

H.2.48 X_END

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x006E

Type: RO

Reset: 0x0000

Description: Image X end from the video timing

[15:0]	**VALUE:** Image X end from the video timing

H.2.49 Y_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0070

Type: RO

Reset: 0x0000

Description: Image Y start from the video timing

[15:0]	**VALUE:** Image Y start from the video timing

H.2.50 Y_END

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0072

Type: RO

Reset: 0x0000

Description: Image Y end from the video timing

[15:0]	**VALUE:** Image Y end from the video timing

H.2.51 X_SIZE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0074

Type: RO

Reset: 0x0000

Description: Image X size

[15:0]	**VALUE:** Image X size

H.2.52 Y_SIZE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0076

Type: RO

Reset: 0x0000

Description: Image Y size

[15:0]	**VALUE:** Image Y size

H.2.53 READOUT_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													CFG		
-													RO		

Address: 0x0078

Type: RO

Reset: 0x0000

Description: Streaming readout mode control

[2:0] **CFG:** Streaming readout mode control

-0x00: = normal streaming
-0x01: = digital binning x2
-0x02: = digital binning x4
-0x03: = subsampling x2
-0x04: = subsampling x4
-0x05: = subsampling x8
-0x06: = XY binning x2

H.2.54 WAIT_DELAY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x007A

Type: RO

Reset: 0x0000

Description: Wait time before the next frame, and blanking in lines

[15:0]	**VALUE:** Wait time before the next frame, and blanking in lines

H.2.55 EXPOSURE_COARSE_EXP_LINES_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x007C

Type: RO

Reset: 0x0000

Description: Coarse exposure time in lines

[15:0]	**VALUE:** Coarse exposure time in lines

H.2.56 EXPOSURE_COARSE_EXP_LINES_C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x007E

Type: RO

Reset: 0x0000

Description: Coarse exposure time in lines

[15:0]	**VALUE:** Coarse exposure time in lines

H.2.57 EXPOSURE_MEAN_ENERGY_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RO								RO							

Address: 0x0080

Type: RO

Reset: 0x0000

Description: Mean energy of the input image

[15:8]	**INTEGER:** Mean energy of the input image (integer part)
[7:0]	**FRACT:** Mean energy of the input image (fractional part)

H.2.58 EXPOSURE_LIMITS_MINIMUM_COARSE_LINES

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0082

Type: RO

Reset: 0x0000

Description: Minimum coarse integration in lines

[15:0]	**VALUE:** Minimum coarse integration in lines

H.2.59 EXPOSURE_LIMITS_MAXIMUM_COARSE_LINES

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0084

Type: RO

Reset: 0x0000

Description: Maximum coarse integration in lines

[15:0]	**VALUE:** Maximum coarse integration in lines

H.2.60 USER

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0090

Type: RO

Reset: 0x00

Description: This register is a marker

[7:0]	**VALUE:** This register is a marker

H.2.61 GPIO_0_CTRL

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0091

Type: RO

Reset: 0x00

Description: Input GPIO value if input mode is used

[7:0]	**VALUE:** Input GPIO value if input mode is used

H.2.62 GPIO_1_CTRL

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0092

Type: RO

Reset: 0x00

Description: Input GPIO value if input mode is used

[7:0]	**VALUE:** Input GPIO value if input mode is used

H.2.63 GPIO_2_CTRL

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0093

Type: RO

Reset: 0x00

Description: Input GPIO value if input mode is used

[7:0]	**VALUE:** Input GPIO value if input mode is used

H.2.64 GPIO_3_CTRL

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0094

Type: RO

Reset: 0x00

Description: Input GPIO value if input mode is used

[7:0]	**VALUE:** Input GPIO value if input mode is used

H.2.65 DARKCAL_CTRL

7	6	5	4	3	2	1	0
RESERVED	NOISE_MASK_BASED_ON_DGAIN	LEAKYNESS				ENABLE	
-	RO	RO				RO	

Address: 0x0095

Type: RO

Reset: 0x00

Description: Darck calibration configuration

[6]	**NOISE_MASK_BASED_ON_DGAIN:** Noise mask based on digital gain -0x0: FALSE -0x1: TRUE
[5:2]	**LEAKYNESS:** Antecedents of the leaky accumulation process
[1:0]	**ENABLE:** DarkCal mode control -0x0: = disable DarkCal -0x1: = enable DarkCal in automatic mode -0x2: = bypass the DarkCal average -0x3: = use the DarkCal average for all channels

H.2.66 DARKCAL_PEDESTAL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						VALUE									
-						RO									

Address: 0x0096

Type: RO

Reset: 0x0000

Description: Pedestal value used in the DDC block

[9:0]	**VALUE:** Pedestal value used in the DDC block

H.2.67 DARKCAL_STATS_CH0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														INTEGER											FRACT						
-														RO											RO						

Address: 0x00A8

Type: RO

Reset: 0x0000 0000

Description: Channel 0 statistics

[17:7]	**INTEGER:** Channel 0 statistics (integer part)
[6:0]	**FRACT:** Channel 0 statistics (fractional part)

H.2.68 DARKCAL_STATS_CH1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														INTEGER											FRACT						
-														RO											RO						

Address: 0x00AC

Type: RO

Reset: 0x0000 0000

Description: Channel 1 statistics

[17:7]	**INTEGER:** Channel 1 statistics (integer part)
[6:0]	**FRACT:** Channel 1 statistics (fractional part)

H.2.69 DARKCAL_STATS_CH2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														INTEGER											FRACT						
-														RO											RO						

Address: 0x00B0

Type: RO

Reset: 0x0000 0000

Description: Channel 2 statistics

[17:7]	**INTEGER:** Channel 2 statistics (integer part)
[6:0]	**FRACT:** Channel 2 statistics (fractional part)

H.2.70 DARKCAL_STATS_CH3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														INTEGER											FRACT						
-														RO											RO						

Address: 0x00B4

Type: RO

Reset: 0x0000 0000

Description: Channel 3 statistics

[17:7]	**INTEGER:** Channel 3 statistics (integer part)
[6:0]	**FRACT:** Channel 3 statistics (fractional part)

H.2.71 STARTUP_TIME

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x00B8

Type: RO

Reset: 0x0000 0000

Description: Time for start up

[31:0]	**VALUE:** Time for start up

H.2.72 BOOT_TIME

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x00BC

Type: RO

Reset: 0x0000 0000

Description: Time for boot

[31:0]	**VALUE:** Time for boot

H.2.73 EXPOSURE_COARSE_EXP_LINES_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x00E8

Type: RO

Reset: 0x0000

Description: Coarse exposure time in lines

[15:0]	**VALUE:** Coarse exposure time in lines

H.2.74 EXPOSURE_ANALOG_GAIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											VALUE				
-											RO				

Address: 0x00EA

Type: RO

Reset: 0x0000

Description: Analog gain used

[4:0] **VALUE:**

-0x00: AnalogGain_AGAIN_1
-0x01: AnalogGain_AGAIN_1_03
-0x02: AnalogGain_AGAIN_1_07
-0x03: AnalogGain_AGAIN_1_1
-0x04: AnalogGain_AGAIN_1_14
-0x05: AnalogGain_AGAIN_1_19
-0x06: AnalogGain_AGAIN_1_23
-0x07: AnalogGain_AGAIN_1_28
-0x08: AnalogGain_AGAIN_1_33
-0x09: AnalogGain_AGAIN_1_39
-0x0A: AnalogGain_AGAIN_1_45
-0x0B: AnalogGain_AGAIN_1_52
-0x0C: AnalogGain_AGAIN_1_6
-0x0D: AnalogGain_AGAIN_1_68
-0x0E: AnalogGain_AGAIN_1_78
-0x0F: AnalogGain_AGAIN_1_88
-0x10: AnalogGain_AGAIN_2
-0x11: AnalogGain_AGAIN_2_13
-0x12: AnalogGain_AGAIN_2_29
-0x13: AnalogGain_AGAIN_2_46
-0x14: AnalogGain_AGAIN_2_67
-0x15: AnalogGain_AGAIN_2_91
-0x16: AnalogGain_AGAIN_3_2
-0x17: AnalogGain_AGAIN_3_56
-0x18: AnalogGain_AGAIN_4
-0x19: AnalogGain_AGAIN_4_57
-0x1A: AnalogGain_AGAIN_5_33
-0x1B: AnalogGain_AGAIN_6_4
-0x1C: AnalogGain_AGAIN_8

H.2.75 EXPOSURE_DIGITAL_GAIN_CH0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RO								RO							

Address: 0x00EC

Type: RO

Reset: 0x0000

Description: Digital gain, applied from the exposure algorithm channel 0

[15:8]	**INTEGER:** Digital gain, applied from the exposure algorithm channel 0. Note that the integer part is in 5.8 fixed point format.
[7:0]	**FRACT:** Digital gain, applied from the exposure algorithm channel 0. Note that the fractional part is in 5.8 fixed point format.

H.2.76 PATCH_TIME

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x00F4

Type: RO

Reset: 0x0000 0000

Description: Time to run the patch command

[31:0]	**VALUE:** Time to run the patch command

H.2.77 VT_SUBTRACTION_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								DELAY							
-								RO							

Address: 0x0104

Type: RO

Reset: 0x0000

Description: Delay between the integration lines

[14:0]	**DELAY:** Delay between the integration lines (in lines)

H.2.78 STREAMING_FSM

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0106

Type: RO

Reset: 0x00

Description: FSM streaming status

[7:0] **VALUE:** FSM streaming status

-0x00: STBY
-0x01: START_STREAM
-0x02: SOF_TASK
-0x03: DARK_TASK
-0x04: EOF_TASK
-0x05: ITPOINT_TASK
-0x06: LATCH_TASK
-0x07: FRAME_BLANKING
-0x08: WAKEUP_TASK
-0x09: START_INTEGRATION_COUNTER
-0x0A: START_INTEGRATION
-0x0B: STOP_STREAM
-0x0C: WAITING_TRIG
-0x0D: CHANNEL_STAT_TASK
-0x0E: STATS_PROCESSING_TASK
-0x0F: EXPOSURE_A_RUN_TASK
-0x10: EXPOSURE_B_RUN_TASK
-0x20: STREAMING
-0x21: CONTEXT_CHANGE_FOR_EXPOSURE
-0x22: CONTEXT_CHANGE_FOR_SOC
-0x23: CONTEXT_RUNNING
-0x24: STREAMING_ENTER_LOW_POWER
-0x25: STREAMING_LOW_POWER
-0x26: STREAMING_EXIT_LOW_POWER
-0x27: LOW_POWER_ENTER
-0x28: LOW_POWER
-0x29: MCU_WAKEUP
-0x2A: WAITING_FOR_VT_START
-0x2B: STREAMING_STOP_DPHY_DOWN_BEGINS
-0x2C: STREAMING_STOP_DPHY_DOWN_COMPLETED
-0x2D: STREAMING_START_DPHY_UP_BEGINS
-0x2E: STREAMING_START_DPHY_UP_COMPLETED
-0x2F: MCU_IDLE
-0x30: MCU_RUNNING
-0x31: PRE_LATCH_PROG_IZR2_TASK

H.2.79 LOW_POWER_MODE_FEASIBLE

7	6	5	4	3	2	1	0
			RESERVED				VALUE
			-				RO

Address: 0x0107

Type: RO

Reset: 0x00

Description: Low power mode feasability

[0] **VALUE:** Low power mode feasability

-0x0: FALSE
-0x1: TRUE

H.2.80 VT_COARSE_EXP_LINES_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0128

Type: RO

Reset: 0x0000

Description: Coarse exposure time in lines

[15:0]	**VALUE:** Coarse exposure time in lines

H.2.81 VT_COARSE_EXP_LINES_C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x012A

Type: RO

Reset: 0x0000

Description: Coarse exposure time in lines

[15:0]	**VALUE:** Coarse exposure time in lines

H.2.82 EXPOSURE_USE_CASES

7	6	5	4	3	2	1	0
RESERVED					ENABLE_MULTI_CONTEXT	MODE	
-					RO	RO	

Address: 0x012C

Type: RO

Reset: 0x00

Description: Auto exposure configuration

[2]	**ENABLE_MULTI_CONTEXT:** Different ROI statistics per context -0x0: FALSE -0x1: TRUE
[1:0]	**MODE:** Select exposure use cases in terms of exposure count and HDR -0x0: SINGLE_EXPOSURE_LDR -0x1: TWO_EXPOSURE_LDR -0x2: TWO_EXPOSURE_HDR -0x3: THREE_EXPOSURE_HDR

H.2.83 EXPOSURE_STATUS_B

7	6	5	4	3	2	1	0
			RESERVED				STATUS
			-				RO

Address: 0x012D

Type: RO

Reset: 0x00

Description: Auto exposure B status

[0] **STATUS:**

-0x0: UNSTABLE
-0x1: STABLE

H.2.84 EXPOSURE_GROUP_TOKEN

7	6	5	4	3	2	1	0
PROGRAMMED				STATUS			
RO				RO			

Address: 0x012E

Type: RO

Reset: 0x00

Description: Exposure token status

[7:4]	**PROGRAMMED:** Programmed value going to the exposure group token registers
[3:0]	**STATUS:** Received value coming from the exposure group token registers

H.2.85 FSM_AWU_STATE

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x012F

Type: RO

Reset: 0x00

Description: AWU FSM status

[7:0] **VALUE:** AWU FSM status

-0x00: AWU_OFF
-0x01: AWU_CONVERGENCE_RUNNING
-0x02: AWU_CONVERGENCE_DONE
-0x03: AWU_DETECTION_RUNNING
-0xAA: AWU_DETECTION_DONE
-0xFF: AWU_ERROR

H.2.86 CHANNEL_STAT_MEAN_ENERGY_ACC0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RO								RO							

Address: 0x0130

Type: RO

Reset: 0x0000

Description: Mean energy of the accumulator 0

[15:8]	**INTEGER:** Mean energy of the fractional part for accumulator 0
[7:0]	**FRACT:** Mean energy of the integer part for accumulator 0

H.2.87 CHANNEL_STAT_MEAN_ENERGY_ACC1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RO								RO							

Address: 0x0132

Type: RO

Reset: 0x0000

Description: Mean energy of accumulator 1

[15:8]	**INTEGER:** Mean energy fractional part for accumulator 1
[7:0]	**FRACT:** Mean energy of the integer part for accumulator 1

H.2.88 CHANNEL_STAT_MEAN_ENERGY_ACC2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RO								RO							

Address: 0x0134

Type: RO

Reset: 0x0000

Description: Mean energy of accumulator 2

[15:8]	**INTEGER:** Mean energy of the fractional part for accumulator 2
[7:0]	**FRACT:** Mean energy of the integer part for accumulator 2

H.2.89 DARK_LINES_COUNT

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0136

Type: RO

Reset: 0x00

Description: Number of dark lines streamed

[7:0]	**VALUE:** Number of dark lines streamed

H.2.90 PWL

7	6	5	4	3	2	1	0
RESERVED					LUT_SEL		ENABLE
-					RO		RO

Address: 0x0137

Type: RO

Reset: 0x00

Description: PWL status

[2:1] **LUT_SEL:** PWL status

-0x0: DEFAULT0
-0x1: DEFAULT1
-0x2: USER0
-0x3: USER1

[0] **ENABLE:**

-0x0: DISABLE
-0x1: ENABLE

H.2.91 DEFCOR_STATUS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NO_OF_DEFECTS_CORRECTED																															
RO																															

Address: 0x0138

Type: RO

Reset: 0x0000 0000

Description: Number of defects corrected by DEFCOR

[31:0]	**NO_OF_DEFECTS_CORRECTED:** Number of defects corrected by DEFCOR

H.2.92 MANUFACTURER_ID

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0140

Type: RO

Reset: 0x0104

Description: Manufacturer's ID

[15:0]	**VALUE:** Manufacturer's ID

H.2.93 AWU_LEARN_DEFINITIVE

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x0143

Type: RO

Reset: 0x00

Description: True when the reference levels and standard deviations for the current frame can be trusted

[7:0]	**VALUE:** True when the reference levels and standard deviations for the current frame can be trusted

H.2.94 AWU_STATUS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															DETECTION	ZONE_DETECTION															
-															RO	RO															

Address: 0x0144

Type: RO

Reset: 0x0000 0000

Description: Status of the auto wake up

[16]	**DETECTION:** Global detection status -0x0: NONE_DETECTED -0x1: MOTION_DETECTED
[15:0]	**ZONE_DETECTION:** Detection per zone

H.2.95 VT_SUB_WAIT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			VT_SUB_WAIT_PIXELS													VT_SUB_WAIT_LINES															
-			RO													RO															

Address: 0x0148

Type: RO

Reset: 0x0000 0000

Description: Delay between two integrations in VT subtraction mode

[28:16]	**VT_SUB_WAIT_PIXELS:** Delay in pixels (13 bits) between two integrations in VT subtraction mode
[15:0]	**VT_SUB_WAIT_LINES:** Delay in lines between two integrations in VT subtraction mode

H.2.96 VT_SUB_DIGITAL_OFFSET

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						DIGITAL_OFFSET									
-						RO									

Address: 0x014C

Type: RO

Reset: 0x0000

Description: Offset for VT-SUB

[9:0]	**DIGITAL_OFFSET:** Offset for VT-SUB, which is 512: power(2, bitwidth-1)

H.2.97 VT_MODE

7	6	5	4	3	2	1	0
			RESERVED				MODE
			-				RO

Address: 0x014E

Type: RO

Reset: 0x00

Description: Mode of the video timing

[0] **MODE:** Mode

-0x0: MULTI_EXPO
-0x1: VT_SUB

H.2.98 CHANNEL_STATS_STATE_FOR_EXPOSURE

7	6	5	4	3	2	1	0
VALUE							
RO							

Address: 0x014F

Type: RO

Reset: 0x00

Description: Channel stat IP status

[7:0] **VALUE:** Status

-0x0: NONE
-0x1: FIRST_FRAME
-0x2: READY_TO_PROCESS
-0x3: SKIPPED
-0x4: COMPLETE

H.2.99 VT_START_TIME

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x0154

Type: RO

Reset: 0x0000 0000

Description: VT start time

[31:0]	**VALUE:** VT start time

H.2.100 VT_STOP_TIME

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x0158

Type: RO

Reset: 0x0000 0000

Description: VT stop time

[31:0]	**VALUE:** VT stop time

H.2.101 EXPOSURE_PENDING_INTG_ABSORBED

7	6	5	4	3	2	1	0
RESERVED							VALUE
-							RO

Address: 0x0170

Type: RO

Reset: 0x00

Description: Flag set when pending exposure is absorbed

[0]	**VALUE:** Flag set when pending exposure is absorbed

H.2.102 EXPOSURE_ACTIVE_INSTANCE

7	6	5	4	3	2	1	0
RESERVED							VALUE
-							RO

Address: 0x0171

Type: RO

Reset: 0x00

Description: Exposure instance used for the actual frame

[0] **VALUE:**

-0x0: EXPOSURE_A
-0x1: EXPOSURE_B

H.2.103 EXPOSURE_COARSE_INTG_MARGIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0174

Type: RO

Reset: 0x0000

Description: Coarse exposure integration margin

[15:0]	**VALUE:** Coarse exposure integration margin

H.2.104 EXPOSURE_NON_OVERLAP_LIMIT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0176

Type: RO

Reset: 0x0000

Description: Nonoverlap exposure limit

[15:0]	**VALUE:** Nonoverlap exposure limit

H.2.105 LOW_POWER_INTER_FRAME_COMPUTED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RO																															

Address: 0x0178

Type: RO

Reset: 0x0000 0000

Description: Time between frames in LP mode

[31:0]	**VALUE:** Time between frames in LP mode

H.2.106 LOW_POWER_LONGEST_EXPOSURE_SELECTED

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0180

Type: RO

Reset: 0x0000

Description: Longest exposure selected in LP mode

[15:0]	**VALUE:** Longest exposure selected in LP mode

H.2.107 EXPOSURE_MAX_COARSE_LINES_VT_SUB_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0182

Type: RO

Reset: 0x0000

Description: Maximum coarse integration in lines for VT-SUB mode A

[15:0]	**VALUE:** Maximum coarse integration in lines for VT-SUB mode (A)

H.2.108 EXPOSURE_MAX_COARSE_LINES_VT_SUB_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0184

Type: RO

Reset: 0x0000

Description: Maximum coarse integration in lines for VT-SUB mode B

[15:0]	**VALUE:** Maximum coarse integration in lines for VT-SUB mode (B)

H.2.109 EXPOSURE_MAX_COARSE_LINES_VT_MULTI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RO															

Address: 0x0186

Type: RO

Reset: 0x0000

Description: Maximum coarse integration in lines for VT-multi-exposure mode

[15:0]	**VALUE:** Maximum coarse integration in lines for VT-multi-exposure mode

H.3 CMD registers

H.3.1 CMD register summary

Table 11. **CMD register list**

Address	Register name	Description
0x0200	BOOT	Register to send command in BOOT state
0x0201	STBY	Register to send command in STBY state
0x0202	STREAMING	Register to send command in STREAMING state

H.3.2 BOOT

7	6	5	4	3	2	1	0
RESERVED						COMMAND	
-						RW	

Address: 0x0200

Type: RW

Reset: 0x00

Description: Register to send command in BOOT state

[1:0] **COMMAND:** List of commands available in BOOT state

-0x0: CMD_ACK
-0x1: BOOT
-0x2: PATCH_AND_BOOT
-0x3: DEVICE_COMMS_UPDATE

H.3.3 STBY

7	6	5	4	3	2	1	0
RESERVED				COMMAND			
-				RW			

Address: 0x0201

Type: RW

Reset: 0x00

Description: Register to send command in STBY state

[3:0] **COMMAND:** List of commands available in STBY state:

-0x0: CMD_ACK
-0x1: START_STREAM
-0x2: NVM_READ
-0x3: NVM_PROG
-0x4: THSENS_READ
-0x5: DEVICE_COMMS_UPDATE
-0x6: START_VTRAM_UPDATE
-0x7: END_VTRAM_UPDATE
-0x8: START_AWU

H.3.4 STREAMING

7	6	5	4	3	2	1	0
RESERVED				COMMAND			
-				RW			

Address: 0x0202

Type: RW

Reset: 0x00

Description: Register to send command in STREAMING state

[3:0] **COMMAND:** List of commands available in STREAMING state:

-0x0: CMD_ACK
-0x1: STOP_STREAM
-0x2: VT_FSYNC_IN_I3C

H.4 SENSOR_SETTINGS registers

H.4.1 SENSOR_SETTINGS register summary

Table 12. SENSOR_SETTINGS register list

Address	Register name	Description
0x0220	EXT_CLOCK	External clock frequency in Hz
0x0224	MIPI_DATA_RATE	PLL MIPI clock frequency in Hz
0x0229	NVM_NB_OF_WORDS	Number of 32-bit words to read/write in burst mode
0x022A	NVM_START_ADDRESS	Start address in NVM for read/write burst operation
0x0230	DEVICE_COMMS_CTRL	I2C and I3C controls

H.4.2 EXT_CLOCK

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0220

Type: RW

Reset: 0x00B7 1B00

Description: External clock frequency in Hz

[31:0]	**VALUE:** External clock frequency in Hz

H.4.3 MIPI_DATA_RATE

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0224

Type: RW

Reset: 0x4786 8C00

Description: PLL MIPI clock frequency in Hz

[31:0]	**VALUE:** PLL MIPI clock frequency in Hz

H.4.4 NVM_NB_OF_WORDS

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x0229

Type: RW

Reset: 0x00

Description: Number of 32-bit words to read/write in burst mode

[7:0]	**VALUE:** Number of 32-bit words to read/write in burst mode

H.4.5 NVM_START_ADDRESS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							VALUE								
-							RW								

Address: 0x022A

Type: RW

Reset: 0x0000

Description: Start address in NVM for read/write burst operation

[8:0]	**VALUE:** Start address in NVM for read/write burst operation

H.4.6 DEVICE_COMMS_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED					DRIVE			DEVICE_ID							RESERVED
-					RW			RW							-

Address: 0x0230

Type: RW

Reset: 0x0120

Description: I2C and I3C controls

[10:8]	**DRIVE:** Drive configurations for I2C/I3C pads
[7:1]	**DEVICE_ID:** Device I2C address

H.5 STREAM_STATICS registers

H.5.1 STREAM_STATICS register summary

Table 13. **STREAM_STATICS register list**

Address	Register name	Description
0x0300	LINE_LENGTH	Line length configuration
0x0302	ORIENTATION	Image orientation mode control
0x0304	PATGEN_CTRL	Patgen configuration
0x0308	EXPOSURE_FORCE_COLDSTART	Force the exposure to start from for the auto exposure
0x0309	VT_CTRL	ADC modes & Synchronization modes
0x030A	FORMAT_CTRL	Select frame output format between RAW8 and RAW10
0x030C	OIF_CTRL	Control of CSI polarity inversion for data lane and clock lane
0x030E	OIF_VC_CTRL	Virtual channel selection
0x030F	OIF_IMG_CTRL	CSI data type selection for RAW Image format
0x0310	OIF_ISL_CTRL	CSI data type selection for status lines
0x0311	OIF_ULPM	Enable/disable Ultra-Low Power Mode
0x0312	EXPOSURE_USE_CASES	Auto exposure use case
0x0313	EXPOSURE_PRIORITY_LONG_VS_SHORT	Auto exposure priority
0x0314	EXPOSURE_LOG_LEAKY	Enable logarithm log
0x0315	EXPOSURE_MIN_LINES_BW_DIFF_EXPOSURES	Minimum difference exposure when using double exposure mechanism
0x0316	EXPOSURE_LIMITS_AG_MIN	Minimum analog gain
0x0317	EXPOSURE_LIMITS_AG_MAX	Maximum analog gain
0x0318	EXPOSURE_LIMITS_DG_MIN	Minimum digital gain
0x031A	EXPOSURE_LIMITS_DG_MAX	Maximum digital gain
0x031C	EXPOSURE_HDR_FIX_RATIO	HDR ratio when in HDr auto exposure mode
0x0324	I3C_FRAME_READOUT_CTRL	I3C readout configuration
0x0326	ISL_ENABLE	Control of the ISL output
0x0327	ISL_PKT_EQ_ACTIVELINE	Padding of the ISL to the image array
0x0328	FSYNC_IN_DELAY	Delay of the start integration when in slave mode
0x032A	DARKCAL_CTRL	Control of the dark calibration
0x032B	PWL_CTRL	Control of the PWL
0x032C	PWL_LUT0_ABSCISSA_0	Abscissa 0
0x032E	PWL_LUT0_ABSCISSA_1	Abscissa 1
0x0330	PWL_LUT0_ABSCISSA_2	Abscissa 2
0x0332	PWL_LUT0_ABSCISSA_3	Abscissa 3
0x0334	PWL_LUT0_ORDINATE_0	Ordinate 0
0x0336	PWL_LUT0_ORDINATE_1	Ordinate 1
0x0338	PWL_LUT0_ORDINATE_2	Ordinate 2
0x033A	PWL_LUT0_ORDINATE_3	Ordinate 3
0x033C	PWL_LUT0_GRADIENT_0	Gradient 0
0x0340	PWL_LUT0_GRADIENT_1	Gradient 1

Address	Register name	Description
0x0344	PWL_LUT0_GRADIENT_2	Gradient 2
0x0348	PWL_LUT0_GRADIENT_3	Gradient 3
0x034C	PWL_LUT1_ABSCISSA_0	Abscissa 0
0x034E	PWL_LUT1_ABSCISSA_1	Abscissa 1
0x0350	PWL_LUT1_ABSCISSA_2	Abscissa 2
0x0352	PWL_LUT1_ABSCISSA_3	Abscissa 3
0x0354	PWL_LUT1_ORDINATE_0	Ordinate 0
0x0356	PWL_LUT1_ORDINATE_1	Ordinate 1
0x0358	PWL_LUT1_ORDINATE_2	Ordinate 2
0x035A	PWL_LUT1_ORDINATE_3	Ordinate 3
0x035C	PWL_LUT1_GRADIENT_0	Gradient 0
0x0360	PWL_LUT1_GRADIENT_1	Gradient 1
0x0364	PWL_LUT1_GRADIENT_2	Gradient 2
0x0368	PWL_LUT1_GRADIENT_3	Gradient 3
0x036C	AWU_CTRL	Auto wake up controls
0x0370	AWU_DETECTION_THRESHOLD	Auto wake up detection threshold
0x0372	EXPOSURE_USER_MAX_COARSE_INTEGRATION_LINES	Maximum integration time
0x0374	EXPOSURE_COLDSTART_EXPOSURE_TIME_US_A	Cold start for the auto exposure instance A
0x0378	EXPOSURE_COLDSTART_EXPOSURE_TIME_US_B	Cold start for the auto exposure instance B
0x037C	EXPOSURE_COARSE_INTG_MARGIN	Margin of the integration time compare to the frame length
0x0380	EXPOSURE_MINIMUM_COARSE_LINES	Minimum integration time
0x0384	AWU_IPS_CTRL	Auto wake up controls
0x0386	EXPOSURE_OVER_EXPOSURE_IN_FLICKER_FREE_IN_EV_A	Allowed excess exposure in flicker free in EV for A
0x0388	EXPOSURE_OVER_EXPOSURE_IN_FLICKER_FREE_IN_EV_B	Allowed excess exposure in flicker free in EV for B
0x038A	EXPOSURE_COMPILATION_PROBLEM_THRESHOLD_RATIO	Compilation problem threshold ration
0x03AC	DARKCAL_NOISE_MASK	Noise generator configuration
0x03AE	DUSTER_CTRL	Defect correction and noise reduction controls
0x03DC	CONTEXT_REPEAT_COUNT_CTX0	Number of frame to be output from context 0
0x03DE	CONTEXT_REPEAT_COUNT_CTX1	Number of frame to be output from context 1
0x03E0	CONTEXT_REPEAT_COUNT_CTX2	Number of frame to be output from context 2
0x03E2	CONTEXT_REPEAT_COUNT_CTX3	Number of frame to be output from context 3
0x03E4	CONTEXT_NEXT_CONTEXT	Context chaining
0x03E6	VT_SUB_DIGITAL_OFFSET	Offset for the subtraction
0x03E8	VT_SUB_WAIT	Delay between 2 frames in subtraction mode

H.5.2 LINE_LENGTH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0300

Type: RW

Reset: 0x0468

Description: Line length configuration

[15:0]	**VALUE:** Line length configuration

H.5.3 ORIENTATION

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														MODE	
-														RW	

Address: 0x0302

Type: RW

Reset: 0x0000

Description: Image orientation mode control

[1:0] **MODE:** Image orientation mode control

-0x00: = no flip
-0x01: = X flip
-0x02: = Y flip
-0x03: = XY flip

H.5.4 PATGEN_CTRL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																						TYPE						RESERVED		ENABLE	
-																						RW						-		RW	

Address: 0x0304

Type: RW

Reset: 0x0000 0220

Description: Patgen configuration

[9:4]	**TYPE:** -0x22: = diagonal grayscale -0x28: = pseudo random
[1:0]	**ENABLE:** Patgen configuration -0x00: BYPASS -0x01: PATGEN

H.5.5 EXPOSURE_FORCE_COLDSTART

7	6	5	4	3	2	1	0
RESERVED							VALUE
-							RW

Address: 0x0308

Type: RW

Reset: 0x00

Description: Force the exposure to start from for the auto exposure

[0] **VALUE:** Force the exposure to start from for the auto exposure

-0x0: FALSE
-0x1: TRUE

H.5.6 VT_CTRL

7	6	5	4	3	2	1	0
RESERVED					ADC_MODE	SYNC_MODE	
-					RW	RW	

Address: 0x0309

Type: RW

Reset: 0x00

Description: ADC modes & Synchronization modes

[2]	**ADC_MODE:** Video timing ADC mode 9 or 10 bits -0x0: = standard mode with 10 bits -0x1: = fast mode with 9 bits
[1:0]	**SYNC_MODE:** Video timing synchronization mode -0x00: = master mode -0x01: = streaming on EXTSYNC pulses -0x02: = streaming on I3C pulses

H.5.7 FORMAT_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											OUT_FORMAT				
-											RW				

Address: 0x030A

Type: RW

Reset: 0x000A

Description: Select frame output format between RAW8 and RAW10

[4:0]	**OUT_FORMAT:** Frame output format control -0x8: RAW8 -0xA: RAW10

H.5.8 OIF_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									DATALANE0_SWAP	RESERVED		CLKLANE_SWAP	RESERVED		
-									RW	-		RW	-		

Address: 0x030C

Type: RW

Reset: 0x0000

Description: Control of CSI polarity inversion for data lane and clock lane

[6] **DATALANE0_SWAP:** CSI lane 0 swapping

-0x0: NO_SWAP
-0x1: LANE_SWAP

[3] **CLKLANE_SWAP:** CSI clock lane swapping

-0x0: NO_SWAP
-0x1: LANE_SWAP

H.5.9 OIF_VC_CTRL

7	6	5	4	3	2	1	0
RESERVED				ISL		ACTIVE_PIX	
-				RW		RW	

Address: 0x030E

Type: RW

Reset: 0x00

Description: Virtual channel selection

[3:2]	**ISL:** Virtual channel selection for ISL
[1:0]	**ACTIVE_PIX:** Virtual channel selection for the output image

H.5.10 OIF_IMG_CTRL

7	6	5	4	3	2	1	0
RESERVED				DATA_TYPE			
-				RW			

Address: 0x030F

Type: RW

Reset: 0x2B

Description: CSI data type selection for RAW Image format

[5:0]	**DATA_TYPE:** Data type selection for RAW Image format

H.5.11 OIF_ISL_CTRL

7	6	5	4	3	2	1	0
RESERVED				DATA_TYPE			
-				RW			

Address: 0x0310

Type: RW

Reset: 0x12

Description: CSI data type selection for status lines

[5:0]	**DATA_TYPE:** Data type selection for status lines

H.5.12 OIF_ULPM

7	6	5	4	3	2	1	0
			RESERVED				ENABLE
			-				RW

Address: 0x0311

Type: RW

Reset: 0x00

Description: Enable/disable Ultra-Low Power Mode

[0] **ENABLE:** ULPM enable

-0x0: DISABLE
-0x1: ENABLE

H.5.13 EXPOSURE_USE_CASES

7	6	5	4	3	2	1	0
RESERVED					ENABLE_MULTI_CONTEXT	MODE	
-					RW	RW	

Address: 0x0312

Type: RW

Reset: 0x00

Description: Auto exposure use case

[2]	**ENABLE_MULTI_CONTEXT:** Different ROI statistics per context -0x0: FALSE -0x1: TRUE
[1:0]	**MODE:** Select exposure use cases in terms of exposure count and HDR -0x0: SINGLE_EXPOSURE_LDR -0x1: TWO_EXPOSURE_LDR -0x2: TWO_EXPOSURE_HDR -0x3: THREE_EXPOSURE_HDR

H.5.14 EXPOSURE_PRIORITY_LONG_VS_SHORT

7	6	5	4	3	2	1	0
RESERVED							VALUE
-							RW

Address: 0x0313

Type: RW

Reset: 0x00

Description: Auto exposure priority

[0]	**VALUE:** This register gives priority to either the long or short exposure. The prioritized exposure is calculated first. The nonprioritized exposure is calculated second, based on the calculation of the prioritized exposure. -0x0: SHORT_EXPO -0x1: LONG_EXPO

H.5.15 EXPOSURE_LOG_LEAKY

7	6	5	4	3	2	1	0
			RESERVED				ENABLE
			-				RW

Address: 0x0314

Type: RW

Reset: 0x01

Description: Enable logarithm log

[0] **ENABLE:**

-0x0: FALSE
-0x1: TRUE

H.5.16 EXPOSURE_MIN_LINES_BW_DIFF_EXPOSURES

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x0315

Type: RW

Reset: 0x05

Description: Minimum difference exposure when using double exposure mechanism

[7:0]	**VALUE:** Accommodate design limitation of minimum lines, between different exposures, in multi-exposure cases (two exposures must be separated by some minimum constraints).

H.5.17 EXPOSURE_LIMITS_AG_MIN

7	6	5	4	3	2	1	0
RESERVED					VALUE		
-					RW		

Address: 0x0316

Type: RW

Reset: 0x00

Description: Minimum analog gain

[4:0] **VALUE:**

-0x00: AnalogGain_AGAIN_1
-0x01: AnalogGain_AGAIN_1_03
-0x02: AnalogGain_AGAIN_1_07
-0x03: AnalogGain_AGAIN_1_1
-0x04: AnalogGain_AGAIN_1_14
-0x05: AnalogGain_AGAIN_1_19
-0x06: AnalogGain_AGAIN_1_23
-0x07: AnalogGain_AGAIN_1_28
-0x08: AnalogGain_AGAIN_1_33
-0x09: AnalogGain_AGAIN_1_39
-0x0A: AnalogGain_AGAIN_1_45
-0x0B: AnalogGain_AGAIN_1_52
-0x0C: AnalogGain_AGAIN_1_6
-0x0D: AnalogGain_AGAIN_1_68
-0x0E: AnalogGain_AGAIN_1_78
-0x0F: AnalogGain_AGAIN_1_88
-0x10: AnalogGain_AGAIN_2
-0x11: AnalogGain_AGAIN_2_13
-0x12: AnalogGain_AGAIN_2_29
-0x13: AnalogGain_AGAIN_2_46
-0x14: AnalogGain_AGAIN_2_67
-0x15: AnalogGain_AGAIN_2_91
-0x16: AnalogGain_AGAIN_3_2
-0x17: AnalogGain_AGAIN_3_56
-0x18: AnalogGain_AGAIN_4
-0x19: AnalogGain_AGAIN_4_5714
-0x1A: AnalogGain_AGAIN_5_3333
-0x1B: AnalogGain_AGAIN_6_4
-0x1C: AnalogGain_AGAIN_8_0

H.5.18 EXPOSURE_LIMITS_AG_MAX

7	6	5	4	3	2	1	0
RESERVED			VALUE				
-			RW				

Address: 0x0317

Type: RW

Reset: 0x1C

Description: Maximum analog gain

[4:0] **VALUE:**

-0x00: AnalogGain_AGAIN_1
-0x01: AnalogGain_AGAIN_1_03
-0x02: AnalogGain_AGAIN_1_07
-0x03: AnalogGain_AGAIN_1_1
-0x04: AnalogGain_AGAIN_1_14
-0x05: AnalogGain_AGAIN_1_19
-0x06: AnalogGain_AGAIN_1_23
-0x07: AnalogGain_AGAIN_1_28
-0x08: AnalogGain_AGAIN_1_33
-0x09: AnalogGain_AGAIN_1_39
-0x0A: AnalogGain_AGAIN_1_45
-0x0B: AnalogGain_AGAIN_1_52
-0x0C: AnalogGain_AGAIN_1_6
-0x0D: AnalogGain_AGAIN_1_68
-0x0E: AnalogGain_AGAIN_1_78
-0x0F: AnalogGain_AGAIN_1_88
-0x10: AnalogGain_AGAIN_2
-0x11: AnalogGain_AGAIN_2_13
-0x12: AnalogGain_AGAIN_2_29
-0x13: AnalogGain_AGAIN_2_46
-0x14: AnalogGain_AGAIN_2_67
-0x15: AnalogGain_AGAIN_2_91
-0x16: AnalogGain_AGAIN_3_2
-0x17: AnalogGain_AGAIN_3_56
-0x18: AnalogGain_AGAIN_4
-0x19: AnalogGain_AGAIN_4_5714
-0x1A: AnalogGain_AGAIN_5_3333
-0x1B: AnalogGain_AGAIN_6_4
-0x1C: AnalogGain_AGAIN_8_0

H.5.19 EXPOSURE_LIMITS_DG_MIN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0318

Type: RW

Reset: 0x0100

Description: Minimum digital gain

[15:8]	**INTEGER:** Exposure limits of the digital gain minimum (integer part)
[7:0]	**FRACT:** Exposure limits of the digital gain minimum (fractional part)

H.5.20 EXPOSURE_LIMITS_DG_MAX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x031A

Type: RW

Reset: 0x1FFF

Description: Maximum digital gain

[15:8]	**INTEGER:** Exposure limits of the digital gain maximum (integer part)
[7:0]	**FRACT:** Exposure limits of the digital gain maximum (fractional part)

H.5.21 EXPOSURE_HDR_FIX_RATIO

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LONG_TO_MEDIUM																MEDIUM_TO_SHORT															
RW																RW															

Address: 0x031C

Type: RW

Reset: 0x0008 0008

Description: HDR ratio when in HDr auto exposure mode

[31:16]	**LONG_TO_MEDIUM:** HDR gain for exposure_RGB_2 with respect to exposure_RGB_1
[15:0]	**MEDIUM_TO_SHORT:** HDR gain for exposure_RGB_3 with respect to exposure_RGB_1

H.5.22 I3C_FRAME_READOUT_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	I3C_PAYLOAD_SIZE									GPIO_THRESHOLD_MODE			INTERRUPT_MODE_TO_HOST	I3C_READOUT_SKIP_HEADER	ENABLE
-	RW									RW			RW	RW	RW

Address: 0x0324

Type: RW

Reset: 0x0002

Description: I3C readout configuration

[14:6]	**I3C_PAYLOAD_SIZE:** Number of bytes per read transaction (if 0, use the current output image width). The value must be a module of 4.
[5:3]	**GPIO_THRESHOLD_MODE:** GPIO threshold operating mode -0x0: DEFAULT -0x1: MODE1 -0x2: MODE2 -0x3: MODE3 -0x4: MODE4
[2]	**INTERRUPT_MODE_TO_HOST:** -0x0: GPIO -0x1: I3C_SLAVE_IBI
[1]	**I3C_READOUT_SKIP_HEADER:** Skip the SOF/EOF while sending data -0x0: = skip header is disabled -0x1: = skip header is enabled
[0]	**ENABLE:** I3C frame readout control -0x0: = I3C frame readout is disabled -0x1: = I3C frame readout is enabled

H.5.23 ISL_ENABLE

7	6	5	4	3	2	1	0
			RESERVED				VALUE
			-				RW

Address: 0x0326

Type: RW

Reset: 0x01

Description: Control of the ISL output

[0] **VALUE:** Output ISL

-0x0: Disable
-0x1: Enable

H.5.24 ISL_PKT_EQ_ACTIVELINE

7	6	5	4	3	2	1	0
ENABLE							
RW							

Address: 0x0327

Type: RW

Reset: 0x01

Description: Padding of the ISL to the image array

[7:0]	**ENABLE:**	
		-0x0: DISABLED -0x1: ENABLED

H.5.25 FSYNC_IN_DELAY

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0328

Type: RW

Reset: 0x0000

Description: Delay of the start integration when in slave mode

[15:0]	**VALUE:** Tunable slave mode delay in lines

H.5.26 DARKCAL_CTRL

7	6	5	4	3	2	1	0
RESERVED	NOISE_MASK_BASED_ON_DGAIN	LEAKYNESS				ENABLE	
-	RW	RW				RW	

Address: 0x032A

Type: RW

Reset: 0x41

Description: Control of the dark calibration

[6]	**NOISE_MASK_BASED_ON_DGAIN:** Noise mask based on digital gain -0x0: FALSE -0x1: TRUE
[5:2]	**LEAKYNESS:** Antecedent of the leaky accumulation process
[1:0]	**ENABLE:** DarkCal mode control -0x0: = disable DarkCal -0x1: = enable DarkCal in automatic mode -0x2: = bypass the DarkCal average -0x3: = use the Darkcal average for all channels

H.5.27 PWL_CTRL

7	6	5	4	3	2	1	0
			EXPO_BIAS				ENABLE
			RW				RW

Address: 0x032B

Type: RW

Reset: 0x00

Description: Control of the PWL

[7:1]	**EXPO_BIAS:** PWL_VALUE
[0]	**ENABLE:** -0x0: DISABLE -0x1: ENABLE

H.5.28 PWL_LUT0_ABSCISSA_0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x032C

Type: RW

Reset: 0x0000

Description: Abscissa 0

[15:0]	**VALUE:** Abscissa 0

H.5.29 PWL_LUT0_ABSCISSA_1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x032E

Type: RW

Reset: 0x0000

Description: Abscissa 1

[15:0]	**VALUE:** Abscissa 1

H.5.30 PWL_LUT0_ABSCISSA_2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0330

Type: RW

Reset: 0x0000

Description: Abscissa 2

[15:0]	**VALUE:** Abscissa 2

H.5.31 PWL_LUT0_ABSCISSA_3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0332

Type: RW

Reset: 0x0000

Description: Abscissa 3

[15:0]	**VALUE:** Abscissa 3

H.5.32 PWL_LUT0_ORDINATE_0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0334

Type: RW

Reset: 0x0000

Description: Ordinate 0

[15:0]	**VALUE:** Ordinate 0

H.5.33 PWL_LUT0_ORDINATE_1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0336

Type: RW

Reset: 0x0000

Description: Ordinate 1

[15:0]	**VALUE:** Ordinate 1

H.5.34 PWL_LUT0_ORDINATE_2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0338

Type: RW

Reset: 0x0000

Description: Ordinate 2

[15:0]	**VALUE:** Ordinate 2

H.5.35 PWL_LUT0_ORDINATE_3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x033A

Type: RW

Reset: 0x0000

Description: Ordinate 3

[15:0]	**VALUE:** Ordinate 3

H.5.36 PWL_LUT0_GRADIENT_0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x033C

Type: RW

Reset: 0x0000 0000

Description: Gradient 0

[31:0]	**VALUE:** Gradient 0

H.5.37 PWL_LUT0_GRADIENT_1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0340

Type: RW

Reset: 0x0000 0000

Description: Gradient 1

[31:0]	**VALUE:** Gradient 1

H.5.38 PWL_LUT0_GRADIENT_2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0344

Type: RW

Reset: 0x0000 0000

Description: Gradient 2

[31:0]	**VALUE:** Gradient 2

H.5.39 PWL_LUT0_GRADIENT_3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0348

Type: RW

Reset: 0x0000 0000

Description: Gradient 3

[31:0]	**VALUE:** Gradient 3

H.5.40 PWL_LUT1_ABSCISSA_0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x034C

Type: RW

Reset: 0x0000

Description: Abscissa 0

[15:0]	**VALUE:** Abscissa 0

H.5.41 PWL_LUT1_ABSCISSA_1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x034E

Type: RW

Reset: 0x0000

Description: Abscissa 1

[15:0]	**VALUE:** Abscissa 1

H.5.42 PWL_LUT1_ABSCISSA_2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0350

Type: RW

Reset: 0x0000

Description: Abscissa 2

[15:0]	**VALUE:** Abscissa 2

H.5.43 PWL_LUT1_ABSCISSA_3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0352

Type: RW

Reset: 0x0000

Description: Abscissa 3

[15:0]	**VALUE:** Abscissa 3

H.5.44 PWL_LUT1_ORDINATE_0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0354

Type: RW

Reset: 0x0000

Description: Ordinate 0

[15:0]	**VALUE:** Ordinate 0

H.5.45 PWL_LUT1_ORDINATE_1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0356

Type: RW

Reset: 0x0000

Description: Ordinate 1

[15:0]	**VALUE:** Ordinate 1

H.5.46 PWL_LUT1_ORDINATE_2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0358

Type: RW

Reset: 0x0000

Description: Ordinate 2

[15:0]	**VALUE:** Ordinate 2

H.5.47 PWL_LUT1_ORDINATE_3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x035A

Type: RW

Reset: 0x0000

Description: Ordinate 3

[15:0]	**VALUE:** Ordinate 3

H.5.48 PWL_LUT1_GRADIENT_0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x035C

Type: RW

Reset: 0x0000 0000

Description: Gradient 0

[31:0]	**VALUE:** Gradient 0

H.5.49 PWL_LUT1_GRADIENT_1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0360

Type: RW

Reset: 0x0000 0000

Description: Gradient 1

[31:0]	**VALUE:** Gradient 1

H.5.50 PWL_LUT1_GRADIENT_2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0364

Type: RW

Reset: 0x0000 0000

Description: Gradient 2

[31:0]	**VALUE:** Gradient 2

H.5.51 PWL_LUT1_GRADIENT_3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0368

Type: RW

Reset: 0x0000 0000

Description: Gradient 3

[31:0]	**VALUE:** Gradient 3

H.5.52 AWU_CTRL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRAME_LENGTH_FOR_CONVERGENCE																NO_OF_ZONE_TO_WAKEUP					INTERRUPT_MODE_TO_HOST	DETECT_BYPASS_ON_EXP_CHANGE	DETECT_COMPUTE_ZSCORE	DETECT_COMPARISON_MODE		DETECT_DECISION_MODE		LEARNING_MODE		RESET	BYPASS
RW																RW					RW	RW	RW	RW		RW		RW		RW	RW

Address: 0x036C

Type: RW

Reset: 0x0316 0942

Description: Auto wake up controls

[31:16]	**FRAME_LENGTH_FOR_CONVERGENCE:** Frame length of AWU first convergence cycle
[15:11]	**NO_OF_ZONE_TO_WAKEUP:** Number of zones needed to detect movement
[10]	**INTERRUPT_MODE_TO_HOST:** -0x0: GPIO -0x1: I3C_SLAVE_IBI
[9]	**DETECT_BYPASS_ON_EXP_CHANGE:** Bypass detection when the current exposure is different from the previous one -0x0: FALSE -0x1: TRUE
[8]	**DETECT_COMPUTE_ZSCORE:** Compute Z-scores -0x0: FALSE -0x1: TRUE
[7:6]	**DETECT_COMPARISON_MODE:** -0x0: BYPASS -0x1: ZSCORE
[5:4]	**DETECT_DECISION_MODE:** -0x0: GLOBAL
[3:2]	**LEARNING_MODE:** Choice of learning algorithm -0x00: TEMPORAL_AVERAGE_LEAKY -0x01: TEMPORAL_AVERAGE_WINDOW
[1]	**RESET:** -0x0: DISABLE -0x1: ENABLE
[0]	**BYPASS:** -0x0: DISABLE -0x1: ENABLE

H.5.53 AWU_DETECTION_THRESHOLD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0370

Type: RW

Reset: 0x0600

Description: Auto wake up detection threshold

[15:8]	**INTEGER:** Integer
[7:0]	**FRACT:** Fractional

H.5.54 EXPOSURE_USER_MAX_COARSE_INTEGRATION_LINES

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0372

Type: RW

Reset: 0x7FFF

Description: Maximum integration time

[15:0]	**VALUE:** User maximum coarse integration [15 bits maximum]

H.5.55 EXPOSURE_COLDSTART_EXPOSURE_TIME_US_A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0374

Type: RW

Reset: 0x0000 07D0

Description: Cold start for the auto exposure instance A

[31:0]	**VALUE:** Coarse exposure time in microseconds for the first exposure

H.5.56 EXPOSURE_COLDSTART_EXPOSURE_TIME_US_B

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0378

Type: RW

Reset: 0x0000 07D0

Description: Cold start for the auto exposure instance B

[31:0]	**VALUE:** Coarse exposure time in microseconds for the second exposure

H.5.57 EXPOSURE_COARSE_INTG_MARGIN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_10BIT																ADC_9BIT															
RW																RW															

Address: 0x037C

Type: RW

Reset: 0x0039 0039

Description: Margin of the integration time compare to the frame length

[31:16]	**ADC_10BIT:** Coarse integration exposure margin for the 10-bit ADC
[15:0]	**ADC_9BIT:** Coarse integration exposure margin for the 9-bit ADC

H.5.58 EXPOSURE_MINIMUM_COARSE_LINES

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_10BIT																ADC_9BIT															
RW																RW															

Address: 0x0380

Type: RW

Reset: 0x0004 0005

Description: Minimum integration time

[31:16]	**ADC_10BIT:** Minimum exposure in 10-bit mode
[15:0]	**ADC_9BIT:** Minimum exposure in 9-bit mode

H.5.59 AWU_IPS_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													DDC_BYPASS_DARKAVG	DUSTER_BYPASS	HDEFCOR_BYPASS
-													RW	RW	RW

Address: 0x0384

Type: RW

Reset: 0x0007

Description: Auto wake up controls

[2] **DDC_BYPASS_DARKAVG:** DARKCAL_BYPASS_DARKAVG

-0x0: DISABLE
-0x1: ENABLE

[1] **DUSTER_BYPASS:** DUSTER control

-0x0: DISABLE
-0x1: ENABLE

[0] **HDEFCOR_BYPASS:** HDEFCOR control

-0x0: DISABLE
-0x1: ENABLE

H.5.60 EXPOSURE_OVER_EXPOSURE_IN_FLICKER_FREE_IN_EV_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0386

Type: RW

Reset: 0x0000

Description: Allowed excess exposure in flicker free in EV for A

[15:8]	**INTEGER:** Allowed excess exposure in flicker free in EV for A
[7:0]	**FRACT:** Allowed excess exposure in flicker free in EV for A

H.5.61 EXPOSURE_OVER_EXPOSURE_IN_FLICKER_FREE_IN_EV_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0388

Type: RW

Reset: 0x0000

Description: Allowed excess exposure in flicker free in EV for B

[15:8]	**INTEGER:** Allowed excess exposure in flicker free in EV for B
[7:0]	**FRACT:** Allowed excess exposure in flicker free in EV for B

H.5.62 EXPOSURE_COMPILATION_PROBLEM_THRESHOLD_RATIO

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						INTEGER		FRACT							
-						RW		RW							

Address: 0x038A

Type: RW

Reset: 0x0133

Description: Compilation problem threshold ration

[9:8]	**INTEGER:** Compilation problem threshold ration (integer part)
[7:0]	**FRACT:** Compilation problem threshold ration (fractional part)

H.5.63 DARKCAL_NOISE_MASK

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								VALUE							
-								RW							

Address: 0x03AC

Type: RW

Reset: 0x007F

Description: Noise generator configuration

[7:0]	**VALUE:** Noise generator configuration registers

H.5.64 DUSTER_CTRL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										NOISE_CORRECTION	RING_ENABLE	GAUSSIAN_MONO5X5_ENABLE	DYN_ENABLE		ENABLE
-										RW	RW	RW	RW		RW

Address: 0x03AE

Type: RW

Reset: 0x0013

Description: Defect correction and noise reduction controls

[5] **NOISE_CORRECTION:** Enable/Disable the noise correction

-0x0: DISABLE
-0x1: ENABLE

[4] **RING_ENABLE:** Duster ring correction control

-0x0: = disable duster ring correction
-0x1: = enable duster ring correction

[3] **GAUSSIAN_MONO5X5_ENABLE:** Selection of the size of the filter for the noise reduction

-0x0: = use 3x3 filter
-0x1: = use 5x5 filter

[2:1] **DYN_ENABLE:** Selection of the configuration for pixel defect correction

-0x0: = disable duster dynamic correction
-0x1: = duster corrects singlets and couplets
-0x2: = duster corrects only couplets

[0] **ENABLE:** Duster mode control

-0x0: = fully disable duster
-0x1: = enable duster modules

H.5.65 CONTEXT_REPEAT_COUNT_CTX0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x03DC

Type: RW

Reset: 0x0000

Description: Number of frame to be output from context 0

[15:0]	**VALUE:** Number of frames per context

H.5.66 CONTEXT_REPEAT_COUNT_CTX1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x03DE

Type: RW

Reset: 0x0000

Description: Number of frame to be output from context 1

[15:0]	**VALUE:** Number of frames per context

H.5.67 CONTEXT_REPEAT_COUNT_CTX2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x03E0

Type: RW

Reset: 0x0000

Description: Number of frame to be output from context 2

[15:0]	**VALUE:** Number of frames per context

H.5.68 CONTEXT_REPEAT_COUNT_CTX3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x03E2

Type: RW

Reset: 0x0000

Description: Number of frame to be output from context 3

[15:0]	**VALUE:** Number of frames per context

H.5.69 CONTEXT_NEXT_CONTEXT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTX3				CTX2				CTX1				CTX0			
RW				RW				RW				RW			

Address: 0x03E4

Type: RW

Reset: 0x1111

Description: Context chaining

[15:12]	**CTX3:** Next context target, if > 3, stop streaming occurs after a repeat count
[11:8]	**CTX2:** Next context target, if > 3, stop streaming occurs after a repeat count
[7:4]	**CTX1:** Next context target, if > 3, stop streaming occurs after a repeat count
[3:0]	**CTX0:** Next context target, if > 3, stop streaming occurs after a repeat count

H.5.70 VT_SUB_DIGITAL_OFFSET

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						DIGITAL_OFFSET									
-						RW									

Address: 0x03E6

Type: RW

Reset: 0x0200

Description: Offset for the subtraction

[9:0]	**DIGITAL_OFFSET:** Offset for VT-SUB which is 512: power(2, bitwidth-1)

H.5.71 VT_SUB_WAIT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED			VT_SUB_WAIT_PIXELS													VT_SUB_WAIT_LINES															
-			RW													RW															

Address: 0x03E8

Type: RW

Reset: 0x0000 0000

Description: Delay between 2 frames in subtraction mode

[28:16]	**VT_SUB_WAIT_PIXELS:** Delay in pixels (13 bits) between two integrations in VT subtraction mode
[15:0]	**VT_SUB_WAIT_LINES:** Delay in lines between two integrations in VT subtraction mode

H.6 STREAM_DYNAMICS registers

H.6.1 STREAM_DYNAMICS register summary

Table 14. STREAM_DYNAMICS register list

Address	Register name	Description
0x0481	GROUP_PARAM_HOLD	Holds the application of the dynamic parameters
0x0482	EXPOSURE_COMPILER_CONTROL_A	Controls the auto exposure A
0x0484	EXPOSURE_COMPENSATION_A	Exposure compensation for the auto exposure A
0x0486	EXPOSURE_TARGET_PERCENTAGE_A	Target of the auto exposure A
0x0488	EXPOSURE_STEP_PROPORTION_A	Maximum step of the auto exposure A
0x048A	EXPOSURE_LEAK_PROPORTION_A	Leak proportion of the auto exposure A
0x048C	EXPOSURE_COMPILER_CONTROL_B	Controls the auto exposure B
0x048E	EXPOSURE_COMPENSATION_B	Exposure compensation for the auto exposure B
0x0490	EXPOSURE_TARGET_PERCENTAGE_B	Target of the auto exposure B
0x0492	EXPOSURE_STEP_PROPORTION_B	Maximum step of the auto exposure B
0x0494	EXPOSURE_LEAK_PROPORTION_B	Leak proportion of the auto exposure B
0x049C	EXPOSURE_MIN_STEP	Minimum exposure step to change exposure
0x049E	EXPOSURE_MAX_STEP	Maximum exposure step
0x04A0	EXPOSURE_FLICKER_TOLERANCE_PERCENT	Tolerance of the auto exposure when aligned to the flicker frequency
0x0496	DUSTER_DEF_COR_RATIO	Manages the intensity of the defective pixel correction

H.6.2 GROUP_PARAM_HOLD

7	6	5	4	3	2	1	0
RESERVED							HOLD
-							RW

Address: 0x0481

Type: RW

Reset: 0x00

Description: Hold the application of the dynamic parameters

[0]	**HOLD:** Hold the application of dynamic parameters

H.6.3 EXPOSURE_COMPILER_CONTROL_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														FLICKER_FREQUENCY	MODE
-														RW	RW

Address: 0x0482

Type: RW

Reset: 0x0000

Description: Controls of the auto exposure A

[1] **FLICKER_FREQUENCY:**

-0x0: DEF_50Hz
-0x1: DEF_60Hz

[0] **MODE:**

-0x0: MINIMUM_GAIN
-0x1: FLICKER_FREE

H.6.4 EXPOSURE_COMPENSATION_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0484

Type: RW

Reset: 0x0000

Description: Exposure compensation for the auto exposure A

[15:8]	**INTEGER:** Change the target exposure in stops by increasing or decreasing the integer part of this value
[7:0]	**FRACT:** Change the target exposure in stops by increasing or decreasing the fractional part of this value

H.6.5 EXPOSURE_TARGET_PERCENTAGE_A

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x0486

Type: RW

Reset: 0x1B

Description: Target of the auto exposure A

[7:0]	**VALUE:** This is the target in percent which the exposure algorithm tries to achieve in integers

H.6.6 EXPOSURE_STEP_PROPORTION_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0488

Type: RW

Reset: 0x0080

Description: Maximum step of the auto exposure A

[15:8]	**INTEGER:** Fixed point step proportion (8.8)
[7:0]	**FRACT:** Fixed point step proportion (8.8)

H.6.7 EXPOSURE_LEAK_PROPORTION_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x048A

Type: RW

Reset: 0x1F40

Description: Leak proportion of the auto exposure A

[15]	**INTEGER:** Fixed point step proportion (1.15)
[14:0]	**FRACT:** Fixed point step proportion (1.15)

H.6.8 EXPOSURE_COMPILER_CONTROL_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED														FLICKER_FREQUENCY	MODE
-														RW	RW

Address: 0x048C

Type: RW

Reset: 0x0000

Description: Controls of the auto exposure B

[1] **FLICKER_FREQUENCY:**

-0x0: DEF_50Hz
-0x1: DEF_60Hz

[0] **MODE:**

-0x0: MINIMUM_GAIN
-0x1: FLICKER_FREE

H.6.9 EXPOSURE_COMPENSATION_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x048E

Type: RW

Reset: 0x0000

Description: Exposure compensation for the auto exposure B

[15:8]	**INTEGER:** Change the target exposure in stops by increasing or decreasing this value
[7:0]	**FRACT:** Change the target exposure in stops by increasing or decreasing this value

H.6.10 EXPOSURE_TARGET_PERCENTAGE_B

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x0490

Type: RW

Reset: 0x1B

Description: Target of the auto exposure B

[7:0]	**VALUE:** This is the target in percent which the exposure algorithm tries to achieve in integers

H.6.11 EXPOSURE_STEP_PROPORTION_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0492

Type: RW

Reset: 0x0080

Description: Maximum step of the auto exposure B

[15:8]	**INTEGER:** Fixed point step proportion (8.8)
[7:0]	**FRACT:** Fixed point step proportion (8.8)

H.6.12 EXPOSURE_LEAK_PROPORTION_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0494

Type: RW

Reset: 0x1F40

Description: Leak proportion of the auto exposure B

[15]	**INTEGER:** Fixed point step proportion (1.15)
[14:0]	**FRACT:** Fixed point step proportion (1.15)

H.6.13 EXPOSURE_MIN_STEP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x049C

Type: RW

Reset: 0x0002

Description: Minimum exposure step to change exposure

[15:8]	**INTEGER:** Minimum step of integer part
[7:0]	**FRACT:** Minimum step of fractional part

H.6.14 EXPOSURE_MAX_STEP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x049E

Type: RW

Reset: 0x0400

Description: Maximum exposure step

[15:8]	**INTEGER:** Maximum step of integer part
[7:0]	**FRACT:** Maximum step of fractional part

H.6.15 EXPOSURE_FLICKER_TOLERANCE_PERCENT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x04A0

Type: RW

Reset: 0x0500

Description: Tolerance of the auto exposure when aligned to the flicker frequency

[15:8]	**INTEGER:** Tolerance percent of integer part
[7:0]	**FRACT:** Tolerance percent of fractional part

H.6.16 DUSTER_DEF_COR_RATIO

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x0496

Type: RW

Reset: 0x64

Description: Manages the intensity of the defective pixel correction.

[7:0]	**VALUE:** Manages the intensity of the defective pixel correction. The default value is 100%. Higher values increase the correction. Lower values decrease the correction.

H.7 STREAM_CTX0 registers

H.7.1 STREAM_CTX0 register summary

Table 15. **STREAM_CTX0 register list**

Address	Register name	Description
0x0500	EXPOSURE_MODE	Exposure mode control
0x0501	EXPOSURE_MANUAL_ANALOG_GAIN	Manual analog gain
0x0502	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A	Manual coarse exposure
0x0504	EXPOSURE_MANUAL_DIGITAL_GAIN_CH0	Manual digital gain
0x050C	FRAME_LENGTH	Length of the frame
0x0510	Y_START	Y start for image output
0x0512	Y_HEIGHT	Y height for image output
0x0514	X_START	X start for image output
0x0516	X_WIDTH	X wIdth for image output
0x0518	EXPOSURE_STATS_ACTIVE_ZONE	Active zones for the auto exposure statistique computation
0x051A	EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT	Statistics zone weight
0x051B	USER	Marker used by host
0x051D	GPIO_0_CTRL	Control of the GPIO 0
0x051E	GPIO_1_CTRL	Control of the GPIO 1
0x051F	GPIO_2_CTRL	Control of the GPIO 2
0x0520	GPIO_3_CTRL	Control of the GPIO 3
0x0521	VSYNC_START_DELAY	Capabilty to shift the start of the VSYNC
0x0522	VSYNC_END_DELAY	Capabilty to shift the end of the VSYNC
0x0523	STROBE_START_DELAY	Capabilty to shift the start of the STROBE
0x0524	STROBE_END_DELAY	Capabilty to shift the end of the STROBE
0x0526	DARKCAL_PEDESTAL	Pedestal to be applied
0x0528	PWM_CTRL	Controls of the PWM
0x052C	PWL_LUTSEL	Control of the PWL
0x052D	EXPOSURE_INSTANCE	Instance of exposure to be used in this context
0x052E	READOUT_CTRL	Decimation control
0x0530	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B	Manual exposure for the second exposure
0x0532	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C	Manual exposure for the third exposure
0x0536	VT_MODE	Subtraction control
0x0537	MASK_FRAME_CTRL	Control to mask frames

H.7.2 EXPOSURE_MODE

7	6	5	4	3	2	1	0
RESERVED					MODE		
-					RW		

Address: 0x0500

Type: RW

Reset: 0x02

Description: Exposure mode control

[2:0] **MODE:** Exposure mode control

-0x0: = automatic mode
-0x1: = freeze AE with current settings
-0x2: = manual setting mode
-0x4: BYPASS

H.7.3 EXPOSURE_MANUAL_ANALOG_GAIN

7	6	5	4	3	2	1	0
RESERVED			VALUE				
-			RW				

Address: 0x0501

Type: RW

Reset: 0x00

Description: Manual analog gain

[4:0] **VALUE:**

-0x00: AnalogGain_AGAIN_1
-0x01: AnalogGain_AGAIN_1_03
-0x02: AnalogGain_AGAIN_1_07
-0x03: AnalogGain_AGAIN_1_1
-0x04: AnalogGain_AGAIN_1_14
-0x05: AnalogGain_AGAIN_1_19
-0x06: AnalogGain_AGAIN_1_23
-0x07: AnalogGain_AGAIN_1_28
-0x08: AnalogGain_AGAIN_1_33
-0x09: AnalogGain_AGAIN_1_39
-0x0A: AnalogGain_AGAIN_1_45
-0x0B: AnalogGain_AGAIN_1_52
-0x0C: AnalogGain_AGAIN_1_6
-0x0D: AnalogGain_AGAIN_1_68
-0x0E: AnalogGain_AGAIN_1_78
-0x0F: AnalogGain_AGAIN_1_88
-0x10: AnalogGain_AGAIN_2
-0x11: AnalogGain_AGAIN_2_13
-0x12: AnalogGain_AGAIN_2_29
-0x13: AnalogGain_AGAIN_2_46
-0x14: AnalogGain_AGAIN_2_67
-0x15: AnalogGain_AGAIN_2_91
-0x16: AnalogGain_AGAIN_3_2
-0x17: AnalogGain_AGAIN_3_56
-0x18: AnalogGain_AGAIN_4
-0x19: AnalogGain_AGAIN_4_5714
-0x1A: AnalogGain_AGAIN_5_3333
-0x1B: AnalogGain_AGAIN_6_4
-0x1C: AnalogGain_AGAIN_8_0

H.7.4 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0502

Type: RW

Reset: 0x0032

Description: Manual coarse exposure

[15:0]	**VALUE:** Coarse exposure time in lines

H.7.5 EXPOSURE_MANUAL_DIGITAL_GAIN_CH0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0504

Type: RW

Reset: 0x0100

Description: Manual digital gain

[15:8]	**INTEGER:** Digital gain (integer part) for channel 0 in manual mode
[7:0]	**FRACT:** Digital gain (fractional part) for channel 0 in manual mode

H.7.6 FRAME_LENGTH

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x050C

Type: RW

Reset: 0x0000 0316

Description: Length of the frame

[31:0]	**VALUE:** Length of the frame (including blanking in lines)

H.7.7 Y_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0510

Type: RW

Reset: 0x0000

Description: Y start for image output

[15:0]	**VALUE:** Y start for image output

H.7.8 Y_HEIGHT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0512

Type: RW

Reset: 0x02C0

Description: Y height for image output

[15:0]	**VALUE:** Y height for image output

H.7.9 X_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0514

Type: RW

Reset: 0x0000

Description: X start for image output

[15:0]	**VALUE:** X start for image output

H.7.10 X_WIDTH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0516

Type: RW

Reset: 0x0324

Description: X wIdth for image output

[15:0]	**VALUE:** X width for image output

H.7.11 EXPOSURE_STATS_ACTIVE_ZONE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0518

Type: RW

Reset: 0xFFFF

Description: Active zones for the auto exposure statistique computation

[15:0]	**VALUE:** Active zones for the auto exposure statistique computation

H.7.12 EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x051A

Type: RW

Reset: 0x64

Description: Statistics zone weight

[7:0]	**VALUE:** Statistics zone weight

H.7.13 USER

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x051B

Type: RW

Reset: 0x00

Description: Marker used by host

[7:0]	**VALUE:** Marker used by host

H.7.14 GPIO_0_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x051D

Type: RW

Reset: 0x01

Description: Control of the GPIO 0

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xA: VT_SLAVE_MODE -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.7.15 GPIO_1_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x051E

Type: RW

Reset: 0x02

Description: Control of the GPIO 1

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.7.16 GPIO_2_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x051F

Type: RW

Reset: 0x06

Description: Control of the GPIO 2

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.7.17 GPIO_3_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x0520

Type: RW

Reset: 0x02

Description: Control of the GPIO 3

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.7.18 VSYNC_START_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0521

Type: RW

Reset: 0x00

Description: Capabilty to shift the start of the VSYNC

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.7.19 VSYNC_END_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0522

Type: RW

Reset: 0x00

Description: Capabilty to shift the end of the VSYNC

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.7.20 STROBE_START_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0523

Type: RW

Reset: 0x00

Description: Capabilty to shift the start of the STROBE

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.7.21 STROBE_END_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0524

Type: RW

Reset: 0x00

Description: Capabilty to shift the end of the STROBE

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.7.22 PWM_CTRL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLkDivisor																RESERVED												DutyCycle			
RW																-												RW			

Address: 0x0528

Type: RW

Reset: 0x0064 0007

Description: Controls of the PWM

[31:16]	**CLkDivisor:** Number of pulses to send out
[3:0]	**DutyCycle:** Duty cycle in percent

H.7.23 PWL_LUTSEL

7	6	5	4	3	2	1	0
RESERVED						LUT_SEL	
-						RW	

Address: 0x052C

Type: RW

Reset: 0x00

Description: Control of the PWL

[1:0] **LUT_SEL:** Piecewise linear transformation look up table

-0x0: DEFAULT0
-0x1: DEFAULT1
-0x2: USER0
-0x3: USER1

H.7.24 EXPOSURE_INSTANCE

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x052D

Type: RW

Reset: 0x00

Description: Instance of exposure to be used in this context

[7:0] **VALUE:** Instance

-0x0: INSTANCE_A
-0x1: INSTANCE_B

H.7.25 READOUT_CTRL

7	6	5	4	3	2	1	0
RESERVED					CFG		
-					RW		

Address: 0x052E

Type: RW

Reset: 0x00

Description: Decimation control

[2:0] **CFG:** Streaming readout mode control

-0x00: = normal streaming
-0x01: = digital binning x2
-0x02: = digital binning x4
-0x03: = subsampling x2
-0x04: = subsampling x4
-0x05: = subsampling x8
-0x06: = XY binning x2

H.7.26 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0530

Type: RW

Reset: 0x0032

Description: Manual exposure for the second exposure

[15:0]	**VALUE:** Manual exposure for visible medium

H.7.27 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0532

Type: RW

Reset: 0x0032

Description: Manual exposure for the third exposure

[15:0]	**VALUE:** Manual exposure for visible short

H.7.28 VT_MODE

7	6	5	4	3	2	1	0
			RESERVED				MODE
			-				RW

Address: 0x0536

Type: RW

Reset: 0x00

Description: Subtraction control

[0] **MODE:** Mode

-0x0: MULTI_EXPO
-0x1: VT_SUB

H.7.29 MASK_FRAME_CTRL

7	6	5	4	3	2	1	0
			RESERVED				MASK
			-				RW

Address: 0x0537

Type: RW

Reset: 0x00

Description: Control to mask frames

[0] **MASK:** Enable/Disable

-0x0: DISABLE
-0x1: ENABLE

H.8 STREAM_CTX1 registers

H.8.1 STREAM_CTX1 register summary

Table 16. **STREAM_CTX1 register list**

Address	Register name	Description
0x0550	EXPOSURE_MODE	Exposure mode control
0x0551	EXPOSURE_MANUAL_ANALOG_GAIN	Manual analog gain
0x0552	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A	Manual coarse exposure
0x0554	EXPOSURE_MANUAL_DIGITAL_GAIN_CH0	Manual digital gain
0x055C	FRAME_LENGTH	Length of the frame
0x0560	Y_START	Y start for image output
0x0562	Y_HEIGHT	Y height for image output
0x0564	X_START	X start for image output
0x0566	X_WIDTH	X wIdth for image output
0x0568	EXPOSURE_STATS_ACTIVE_ZONE	Active zones for the auto exposure statistique computation
0x056A	EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT	Statistics zone weight
0x056B	USER	Marker used by host
0x056D	GPIO_0_CTRL	Control of the GPIO 0
0x056E	GPIO_1_CTRL	Control of the GPIO 1
0x056F	GPIO_2_CTRL	Control of the GPIO 2
0x0570	GPIO_3_CTRL	Control of the GPIO 3
0x0571	VSYNC_START_DELAY	Capabilty to shift the start of the VSYNC
0x0572	VSYNC_END_DELAY	Capabilty to shift the end of the VSYNC
0x0573	STROBE_START_DELAY	Capabilty to shift the start of the STROBE
0x0574	STROBE_END_DELAY	Capabilty to shift the end of the STROBE
0x0576	DARKCAL_PEDESTAL	Pedestal to be applied
0x0578	PWM_CTRL	Controls of the PWM
0x057C	PWL_LUTSEL	Control of the PWL
0x057D	EXPOSURE_INSTANCE	Instance of exposure to be used in this context
0x057E	READOUT_CTRL	Decimation control
0x0580	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B	Manual exposure for the second exposure
0x0582	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C	Manual exposure for the third exposure
0x0586	VT_MODE	Subtraction control
0x0587	MASK_FRAME_CTRL	Control to mask frames

H.8.2 EXPOSURE_MODE

7	6	5	4	3	2	1	0
RESERVED					MODE		
-					RW		

Address: 0x0550

Type: RW

Reset: 0x02

Description: Exposure mode control

[2:0] **MODE:** Exposure mode control

-0x0: = automatic mode
-0x1: = freeze AE with current settings
-0x2: = manual setting mode
-0x4: BYPASS

H.8.3 EXPOSURE_MANUAL_ANALOG_GAIN

7	6	5	4	3	2	1	0
RESERVED			VALUE				
-			RW				

Address: 0x0551

Type: RW

Reset: 0x00

Description: Manual analog gain

[4:0] **VALUE:**

-0x00: AnalogGain_AGAIN_1
-0x01: AnalogGain_AGAIN_1_03
-0x02: AnalogGain_AGAIN_1_07
-0x03: AnalogGain_AGAIN_1_1
-0x04: AnalogGain_AGAIN_1_14
-0x05: AnalogGain_AGAIN_1_19
-0x06: AnalogGain_AGAIN_1_23
-0x07: AnalogGain_AGAIN_1_28
-0x08: AnalogGain_AGAIN_1_33
-0x09: AnalogGain_AGAIN_1_39
-0x0A: AnalogGain_AGAIN_1_45
-0x0B: AnalogGain_AGAIN_1_52
-0x0C: AnalogGain_AGAIN_1_6
-0x0D: AnalogGain_AGAIN_1_68
-0x0E: AnalogGain_AGAIN_1_78
-0x0F: AnalogGain_AGAIN_1_88
-0x10: AnalogGain_AGAIN_2
-0x11: AnalogGain_AGAIN_2_13
-0x12: AnalogGain_AGAIN_2_29
-0x13: AnalogGain_AGAIN_2_46
-0x14: AnalogGain_AGAIN_2_67
-0x15: AnalogGain_AGAIN_2_91
-0x16: AnalogGain_AGAIN_3_2
-0x17: AnalogGain_AGAIN_3_56
-0x18: AnalogGain_AGAIN_4
-0x19: AnalogGain_AGAIN_4_5714
-0x1A: AnalogGain_AGAIN_5_3333
-0x1B: AnalogGain_AGAIN_6_4
-0x1C: AnalogGain_AGAIN_8_0

H.8.4 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0552

Type: RW

Reset: 0x0032

Description: Manual coarse exposure

[15:0]	**VALUE:** Coarse exposure time in lines

H.8.5 EXPOSURE_MANUAL_DIGITAL_GAIN_CH0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x0554

Type: RW

Reset: 0x0100

Description: Manual digital gain

[15:8]	**INTEGER:** Digital gain (integer part) for channel 0 in manual mode
[7:0]	**FRACT:** Digital gain (fractional part) for channel 0 in manual mode

H.8.6 FRAME_LENGTH

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x055C

Type: RW

Reset: 0x0000 0316

Description: Length of the frame

[31:0]	**VALUE:** Length of the frame (including blanking in lines)

H.8.7 Y_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0560

Type: RW

Reset: 0x0000

Description: Y start for image output

[15:0]	**VALUE:** Y start for image output

H.8.8 Y_HEIGHT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0562

Type: RW

Reset: 0x02C0

Description: Y height for image output

[15:0]	**VALUE:** Y height for image output

H.8.9 X_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0564

Type: RW

Reset: 0x0000

Description: X start for image output

[15:0]	**VALUE:** X start for image output

H.8.10 X_WIDTH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0566

Type: RW

Reset: 0x0324

Description: X wIdth for image output

[15:0]	**VALUE:** X width for image output

H.8.11 EXPOSURE_STATS_ACTIVE_ZONE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0568

Type: RW

Reset: 0xFFFF

Description: Active zones for the auto exposure statistique computation

[15:0]	**VALUE:** Active zones for the auto exposure statistique computation

H.8.12 EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x056A

Type: RW

Reset: 0x64

Description: Statistics zone weight

[7:0]	**VALUE:** Statistics zone weight

H.8.13 USER

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x056B

Type: RW

Reset: 0x00

Description: Marker used by host

[7:0]	**VALUE:** Marker used by host

H.8.14 GPIO_0_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x056D

Type: RW

Reset: 0x01

Description: Control of the GPIO 0

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xA: VT_SLAVE_MODE -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.8.15 GPIO_1_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x056E

Type: RW

Reset: 0x02

Description: Control of the GPIO 1

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.8.16 GPIO_2_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x056F

Type: RW

Reset: 0x06

Description: Control of the GPIO 2

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.8.17 GPIO_3_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x0570

Type: RW

Reset: 0x02

Description: Control of the GPIO 3

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.8.18 VSYNC_START_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0571

Type: RW

Reset: 0x00

Description: Capabilty to shift the start of the VSYNC

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.8.19 VSYNC_END_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0572

Type: RW

Reset: 0x00

Description: Capabilty to shift the end of the VSYNC

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.8.20 STROBE_START_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0573

Type: RW

Reset: 0x00

Description: Capabilty to shift the start of the STROBE

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.8.21 STROBE_END_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0574

Type: RW

Reset: 0x00

Description: Capabilty to shift the end of the STROBE

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.8.22 DARKCAL_PEDESTAL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0576

Type: RW

Reset: 0x0008

Description: Pedestal to be applied

[15:0]	**VALUE:** DarkCal pedestal

H.8.23 PWM_CTRL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLkDivisor																RESERVED												DutyCycle			
RW																-												RW			

Address: 0x0578

Type: RW

Reset: 0x0064 0007

Description: Controls of the PWM

[31:16]	**CLkDivisor:** Number of pulses to send out
[3:0]	**DutyCycle:** Duty cycle in percent

H.8.24 PWL_LUTSEL

7	6	5	4	3	2	1	0
RESERVED						LUT_SEL	
-						RW	

Address: 0x057C

Type: RW

Reset: 0x00

Description: Control of the PWL

[1:0] **LUT_SEL:** Piecewise linear transformation look up table

-0x0: DEFAULT0
-0x1: DEFAULT1
-0x2: USER0
-0x3: USER1

H.8.25 EXPOSURE_INSTANCE

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x057D

Type: RW

Reset: 0x00

Description: Instance of exposure to be used in this context

[7:0] **VALUE:** Instance

-0x0: INSTANCE_A
-0x1: INSTANCE_B

H.8.26 READOUT_CTRL

7	6	5	4	3	2	1	0
RESERVED					CFG		
-					RW		

Address: 0x057E

Type: RW

Reset: 0x00

Description: Decimation control

[2:0] **CFG:** Streaming readout mode control

-0x00: = normal streaming
-0x01: = digital binning x2
-0x02: = digital binning x4
-0x03: = subsampling x2
-0x04: = subsampling x4
-0x05: = subsampling x8
-0x06: = XY binning x2

H.8.27 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0580

Type: RW

Reset: 0x0032

Description: Manual exposure for the second exposure

[15:0]	**VALUE:** Manual exposure for visible medium

H.8.28 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0582

Type: RW

Reset: 0x0032

Description: Manual exposure for the third exposure

[15:0]	**VALUE:** Manual exposure for visible short

H.8.29 VT_MODE

7	6	5	4	3	2	1	0
			RESERVED				MODE
			-				RW

Address: 0x0586

Type: RW

Reset: 0x00

Description: Subtraction control

[0] **MODE:** Mode

-0x0: MULTI_EXPO
-0x1: VT_SUB

H.8.30 MASK_FRAME_CTRL

7	6	5	4	3	2	1	0
			RESERVED				MASK
			-				RW

Address: 0x0587

Type: RW

Reset: 0x00

Description: Control to mask frames

[0] **MASK:** Enable/Disable

-0x0: DISABLE
-0x1: ENABLE

H.9 STREAM_CTX2 registers

H.9.1 STREAM_CTX2 register summary

Table 17. **STREAM_CTX2 register list**

Address	Register name	Description
0x05A0	EXPOSURE_MODE	Exposure mode control
0x05A1	EXPOSURE_MANUAL_ANALOG_GAIN	Manual analog gain
0x05A2	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A	Manual coarse exposure
0x05A4	EXPOSURE_MANUAL_DIGITAL_GAIN_CH0	Manual digital gain
0x05AC	FRAME_LENGTH	Length of the frame
0x05B0	Y_START	Y start for image output
0x05B2	Y_HEIGHT	Y height for image output
0x05B4	X_START	X start for image output
0x05B6	X_WIDTH	X wIdth for image output
0x05B8	EXPOSURE_STATS_ACTIVE_ZONE	Active zones for the auto exposure statistique computation
0x05BA	EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT	Statistics zone weight
0x05BB	USER	Marker used by host
0x05BD	GPIO_0_CTRL	Control of the GPIO 0
0x05BE	GPIO_1_CTRL	Control of the GPIO 1
0x05BF	GPIO_2_CTRL	Control of the GPIO 2
0x05C0	GPIO_3_CTRL	Control of the GPIO 3
0x05C1	VSYNC_START_DELAY	Capabilty to shift the start of the VSYNC
0x05C2	VSYNC_END_DELAY	Capabilty to shift the end of the VSYNC
0x05C3	STROBE_START_DELAY	Capabilty to shift the start of the STROBE
0x05C4	STROBE_END_DELAY	Capabilty to shift the end of the STROBE
0x05C6	DARKCAL_PEDESTAL	Pedestal to be applied
0x05C8	PWM_CTRL	Controls of the PWM
0x05CC	PWL_LUTSEL	Control of the PWL
0x05CD	EXPOSURE_INSTANCE	Instance of exposure to be used in this context
0x05CE	READOUT_CTRL	Decimation control
0x05D0	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B	Manual exposure for the second exposure
0x05D2	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C	Manual exposure for the third exposure
0x05D6	VT_MODE	Subtraction control
0x05D7	MASK_FRAME_CTRL	Control to mask frames

H.9.2 EXPOSURE_MODE

7	6	5	4	3	2	1	0
RESERVED					MODE		
-					RW		

Address: 0x05A0

Type: RW

Reset: 0x02

Description: Exposure mode control

[2:0] **MODE:** Exposure mode control

-0x0: = automatic mode
-0x1: = freeze AE with current settings
-0x2: = manual setting mode
-0x4: BYPASS

H.9.3 EXPOSURE_MANUAL_ANALOG_GAIN

7	6	5	4	3	2	1	0
RESERVED			VALUE				
-			RW				

Address: 0x05A1

Type: RW

Reset: 0x00

Description: Manual analog gain

[4:0] **VALUE:**

-0x00: AnalogGain_AGAIN_1
-0x01: AnalogGain_AGAIN_1_03
-0x02: AnalogGain_AGAIN_1_07
-0x03: AnalogGain_AGAIN_1_1
-0x04: AnalogGain_AGAIN_1_14
-0x05: AnalogGain_AGAIN_1_19
-0x06: AnalogGain_AGAIN_1_23
-0x07: AnalogGain_AGAIN_1_28
-0x08: AnalogGain_AGAIN_1_33
-0x09: AnalogGain_AGAIN_1_39
-0x0A: AnalogGain_AGAIN_1_45
-0x0B: AnalogGain_AGAIN_1_52
-0x0C: AnalogGain_AGAIN_1_6
-0x0D: AnalogGain_AGAIN_1_68
-0x0E: AnalogGain_AGAIN_1_78
-0x0F: AnalogGain_AGAIN_1_88
-0x10: AnalogGain_AGAIN_2
-0x11: AnalogGain_AGAIN_2_13
-0x12: AnalogGain_AGAIN_2_29
-0x13: AnalogGain_AGAIN_2_46
-0x14: AnalogGain_AGAIN_2_67
-0x15: AnalogGain_AGAIN_2_91
-0x16: AnalogGain_AGAIN_3_2
-0x17: AnalogGain_AGAIN_3_56
-0x18: AnalogGain_AGAIN_4
-0x19: AnalogGain_AGAIN_4_5714
-0x1A: AnalogGain_AGAIN_5_3333
-0x1B: AnalogGain_AGAIN_6_4
-0x1C: AnalogGain_AGAIN_8_0

H.9.4 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05A2

Type: RW

Reset: 0x0032

Description: Manual coarse exposure

[15:0]	**VALUE:** Coarse exposure time in lines

H.9.5 EXPOSURE_MANUAL_DIGITAL_GAIN_CH0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x05A4

Type: RW

Reset: 0x0100

Description: Manual digital gain

[15:8]	**INTEGER:** Digital gain (integer part) for channel 0 in manual mode
[7:0]	**FRACT:** Digital gain (fractional part) for channel 0 in manual mode

H.9.6 FRAME_LENGTH

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x05AC

Type: RW

Reset: 0x0000 0316

Description: Length of the frame

[31:0]	**VALUE:** Length of the frame (including blanking in lines)

H.9.7 Y_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05B0

Type: RW

Reset: 0x0000

Description: Y start for image output

[15:0]	**VALUE:** Y start for image output

H.9.8 Y_HEIGHT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05B2

Type: RW

Reset: 0x02C0

Description: Y height for image output

[15:0]	**VALUE:** Y height for image output

H.9.9 X_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05B4

Type: RW

Reset: 0x0000

Description: X start for image output

[15:0]	**VALUE:** X start for image output

H.9.10 X_WIDTH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05B6

Type: RW

Reset: 0x0324

Description: X wIdth for image output

[15:0]	**VALUE:** X width for image output

H.9.11 EXPOSURE_STATS_ACTIVE_ZONE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05B8

Type: RW

Reset: 0xFFFF

Description: Active zones for the auto exposure statistique computation

[15:0]	**VALUE:** Active zones for the auto exposure statistique computation

H.9.12 EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x05BA

Type: RW

Reset: 0x64

Description: Statistics zone weight

[7:0]	**VALUE:** Statistics zone weight

H.9.13 USER

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x05BB

Type: RW

Reset: 0x00

Description: Marker used by host

[7:0]	**VALUE:** Marker used by host

H.9.14 GPIO_0_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x05BD

Type: RW

Reset: 0x01

Description: Control of the GPIO 0

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xA: VT_SLAVE_MODE -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.9.15 GPIO_1_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x05BE

Type: RW

Reset: 0x02

Description: Control of the GPIO 1

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.9.16 GPIO_2_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x05BF

Type: RW

Reset: 0x06

Description: Control of the GPIO 2

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.9.17 GPIO_3_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x05C0

Type: RW

Reset: 0x02

Description: Control of the GPIO 3

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.9.18 VSYNC_START_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x05C1

Type: RW

Reset: 0x00

Description: Capabilty to shift the start of the VSYNC

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.9.19 VSYNC_END_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x05C2

Type: RW

Reset: 0x00

Description: Capabilty to shift the end of the VSYNC

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.9.20 STROBE_START_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x05C3

Type: RW

Reset: 0x00

Description: Capabilty to shift the start of the STROBE

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.9.21 STROBE_END_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x05C4

Type: RW

Reset: 0x00

Description: Capabilty to shift the end of the STROBE

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.9.22 DARKCAL_PEDESTAL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05C6

Type: RW

Reset: 0x0008

Description: Pedestal to be applied

[15:0]	**VALUE:** DarkCal pedestal

H.9.23 PWM_CTRL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLkDivisor																RESERVED												DutyCycle			
RW																-												RW			

Address: 0x05C8

Type: RW

Reset: 0x0064 0007

Description: Controls of the PWM

[31:16]	**CLkDivisor:** Number of pulses to send out
[3:0]	**DutyCycle:** Duty cycle in percent

H.9.24 PWL_LUTSEL

7	6	5	4	3	2	1	0
RESERVED						LUT_SEL	
-						RW	

Address: 0x05CC

Type: RW

Reset: 0x00

Description: Control of the PWL

[1:0]	**LUT_SEL:** Piecewise linear transformation look up table -0x0: DEFAULT0 -0x1: DEFAULT1 -0x2: USER0 -0x3: USER1

H.9.25 EXPOSURE_INSTANCE

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x05CD

Type: RW

Reset: 0x00

Description: Instance of exposure to be used in this context

[7:0]	**VALUE:** Instance -0x0: INSTANCE_A -0x1: INSTANCE_B

H.9.26 READOUT_CTRL

7	6	5	4	3	2	1	0
RESERVED					CFG		
-					RW		

Address: 0x05CE

Type: RW

Reset: 0x00

Description: Decimation control

[2:0] **CFG:** Streaming readout mode control

-0x00: = normal streaming
-0x01: = digital binning x2
-0x02: = digital binning x4
-0x03: = subsampling x2
-0x04: = subsampling x4
-0x05: = subsampling x8
-0x06: = XY binning x2

H.9.27 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05D0

Type: RW

Reset: 0x0032

Description: Manual exposure for the second exposure

[15:0]	**VALUE:** Manual exposure for visible medium

H.9.28 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05D2

Type: RW

Reset: 0x0032

Description: Manual exposure for the third exposure

[15:0]	**VALUE:** Manual exposure for visible short

H.9.29 VT_MODE

7	6	5	4	3	2	1	0
			RESERVED				MODE
			-				RW

Address: 0x05D6

Type: RW

Reset: 0x00

Description: Subtraction control

[0] **MODE:** Mode

-0x0: MULTI_EXPO
-0x1: VT_SUB

H.9.30 MASK_FRAME_CTRL

7	6	5	4	3	2	1	0
			RESERVED				MASK
			-				RW

Address: 0x05D7

Type: RW

Reset: 0x00

Description: Control to mask frames

[0]	**MASK:** Enable/Disable -0x0: DISABLE -0x1: ENABLE

H.10 STREAM_CTX3 registers

H.10.1 STREAM_CTX3 register summary

Table 18. **STREAM_CTX3 register list**

Address	Register name	Description
0x05F0	EXPOSURE_MODE	Exposure mode control
0x05F1	EXPOSURE_MANUAL_ANALOG_GAIN	Manual analog gain
0x05F2	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A	Manual coarse exposure
0x05F4	EXPOSURE_MANUAL_DIGITAL_GAIN_CH0	Manual digital gain
0x05FC	FRAME_LENGTH	Length of the frame
0x0600	Y_START	Y start for image output
0x0602	Y_HEIGHT	Y height for image output
0x0604	X_START	X start for image output
0x0606	X_WIDTH	X wIdth for image output
0x0608	EXPOSURE_STATS_ACTIVE_ZONE	Active zones for the auto exposure statistique computation
0x060A	EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT	Statistics zone weight
0x060B	USER	Marker used by host
0x060D	GPIO_0_CTRL	Control of the GPIO 0
0x060E	GPIO_1_CTRL	Control of the GPIO 1
0x060F	GPIO_2_CTRL	Control of the GPIO 2
0x0610	GPIO_3_CTRL	Control of the GPIO 3
0x0611	VSYNC_START_DELAY	Capabilty to shift the start of the VSYNC
0x0612	VSYNC_END_DELAY	Capabilty to shift the end of the VSYNC
0x0613	STROBE_START_DELAY	Capabilty to shift the start of the STROBE
0x0614	STROBE_END_DELAY	Capabilty to shift the end of the STROBE
0x0616	DARKCAL_PEDESTAL	Pedestal to be applied
0x0618	PWM_CTRL	Controls of the PWM
0x061C	PWL_LUTSEL	Control of the PWL
0x061D	EXPOSURE_INSTANCE	Instance of exposure to be used in this context
0x061E	READOUT_CTRL	Decimation control
0x0620	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B	Manual exposure for the second exposure
0x0622	EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C	Manual exposure for the third exposure
0x0626	VT_MODE	Subtraction control
0x0627	MASK_FRAME_CTRL	Control to mask frames

H.10.2 EXPOSURE_MODE

7	6	5	4	3	2	1	0
RESERVED					MODE		
-					RW		

Address: 0x05F0

Type: RW

Reset: 0x02

Description: Exposure mode control

[2:0] **MODE:** Exposure mode control

-0x0: = automatic mode
-0x1: = freeze AE with current settings
-0x2: = manual setting mode
-0x4: BYPASS

H.10.3 EXPOSURE_MANUAL_ANALOG_GAIN

7	6	5	4	3	2	1	0
RESERVED			VALUE				
-			RW				

Address: 0x05F1

Type: RW

Reset: 0x00

Description: Manual analog gain

[4:0] **VALUE:**

-0x00: AnalogGain_AGAIN_1
-0x01: AnalogGain_AGAIN_1_03
-0x02: AnalogGain_AGAIN_1_07
-0x03: AnalogGain_AGAIN_1_1
-0x04: AnalogGain_AGAIN_1_14
-0x05: AnalogGain_AGAIN_1_19
-0x06: AnalogGain_AGAIN_1_23
-0x07: AnalogGain_AGAIN_1_28
-0x08: AnalogGain_AGAIN_1_33
-0x09: AnalogGain_AGAIN_1_39
-0x0A: AnalogGain_AGAIN_1_45
-0x0B: AnalogGain_AGAIN_1_52
-0x0C: AnalogGain_AGAIN_1_6
-0x0D: AnalogGain_AGAIN_1_68
-0x0E: AnalogGain_AGAIN_1_78
-0x0F: AnalogGain_AGAIN_1_88
-0x10: AnalogGain_AGAIN_2
-0x11: AnalogGain_AGAIN_2_13
-0x12: AnalogGain_AGAIN_2_29
-0x13: AnalogGain_AGAIN_2_46
-0x14: AnalogGain_AGAIN_2_67
-0x15: AnalogGain_AGAIN_2_91
-0x16: AnalogGain_AGAIN_3_2
-0x17: AnalogGain_AGAIN_3_56
-0x18: AnalogGain_AGAIN_4
-0x19: AnalogGain_AGAIN_4_5714
-0x1A: AnalogGain_AGAIN_5_3333
-0x1B: AnalogGain_AGAIN_6_4
-0x1C: AnalogGain_AGAIN_8_0

H.10.4 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x05F2

Type: RW

Reset: 0x0032

Description: Manual coarse exposure

[15:0]	**VALUE:** Coarse exposure time in lines

H.10.5 EXPOSURE_MANUAL_DIGITAL_GAIN_CH0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEGER								FRACT							
RW								RW							

Address: 0x05F4

Type: RW

Reset: 0x0100

Description: Manual digital gain

[15:8]	**INTEGER:** Digital gain (integer part) for channel 0 in manual mode
[7:0]	**FRACT:** Digital gain (fractional part) for channel 0 in manual mode

H.10.6 FRAME_LENGTH

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x05FC

Type: RW

Reset: 0x0000 0316

Description: Length of the frame

[31:0]	**VALUE:** Length of the frame (including blanking in lines)

H.10.7 Y_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0600

Type: RW

Reset: 0x0000

Description: Y start for image output

[15:0]	**VALUE:** Y start for image output

H.10.8 Y_HEIGHT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0602

Type: RW

Reset: 0x02C0

Description: Y height for image output

[15:0]	**VALUE:** Y height for image output

H.10.9 X_START

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0604

Type: RW

Reset: 0x0000

Description: X start for image output

[15:0]	**VALUE:** X start for image output

H.10.10 X_WIDTH

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0606

Type: RW

Reset: 0x0324

Description: X wIdth for image output

[15:0]	**VALUE:** X width for image output

H.10.11 EXPOSURE_STATS_ACTIVE_ZONE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0608

Type: RW

Reset: 0xFFFF

Description: Active zones for the auto exposure statistique computation

[15:0]	**VALUE:** Active zones for the auto exposure statistique computation

H.10.12 EXPOSURE_STATS_ACTIVE_ZONE_WEIGHT

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x060A

Type: RW

Reset: 0x64

Description: Statistics zone weight

[7:0]	**VALUE:** Statistics zone weight

H.10.13 USER

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x060B

Type: RW

Reset: 0x00

Description: Marker used by host

[7:0]	**VALUE:** Marker used by host

H.10.14 GPIO_0_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x060D

Type: RW

Reset: 0x01

Description: Control of the GPIO 0

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xA: VT_SLAVE_MODE -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.10.15 GPIO_1_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x060E

Type: RW

Reset: 0x02

Description: Control of the GPIO 1

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.10.16 GPIO_2_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x060F

Type: RW

Reset: 0x06

Description: Control of the GPIO 2

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.10.17 GPIO_3_CTRL

7	6	5	4	3	2	1	0
RESERVED		Polarity	VALUE	Mode			
-		RW	RW	RW			

Address: 0x0610

Type: RW

Reset: 0x02

Description: Control of the GPIO 3

[5]	**Polarity:** Polarity value -0x0: NO_INVERSION -0x1: INVERTED
[4]	**VALUE:** GPIO value -0x0: GPIO_LOW -0x1: GPIO_HIGH
[3:0]	**Mode:** GPIO mode -0x0: FSYNC_OUT -0x1: GPIO_IN -0x2: STROBE -0x3: PWM_STROBE -0x4: PWM -0x5: GPIO_OUT -0x6: VSYNC_OUT_MODE0 -0x7: VSYNC_OUT_MODE1 -0x8: VSYNC_OUT_MODE2 -0x9: EVENT_TRACKER -0xC: IMAGE_READOUT -0xD: AWU_DETECTION

H.10.18 VSYNC_START_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0611

Type: RW

Reset: 0x00

Description: Capabilty to shift the start of the VSYNC

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.10.19 VSYNC_END_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0612

Type: RW

Reset: 0x00

Description: Capabilty to shift the end of the VSYNC

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.10.20 STROBE_START_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0613

Type: RW

Reset: 0x00

Description: Capabilty to shift the start of the STROBE

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.10.21 STROBE_END_DELAY

7	6	5	4	3	2	1	0
DELAY_L							
RW							

Address: 0x0614

Type: RW

Reset: 0x00

Description: Capabilty to shift the end of the STROBE

[7:0]	**DELAY_L:** Signed value of the delay to apply in lines

H.10.22 DARKCAL_PEDESTAL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0616

Type: RW

Reset: 0x0008

Description: Pedestal to be applied

[15:0]	**VALUE:** DarkCal pedestal

H.10.23 PWM_CTRL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLkDivisor																RESERVED												DutyCycle			
RW																-												RW			

Address: 0x0618

Type: RW

Reset: 0x0064 0007

Description: Controls of the PWM

[31:16]	**CLkDivisor:** Number of pulses to send out
[3:0]	**DutyCycle:** Duty cycle in percent

H.10.24 PWL_LUTSEL

7	6	5	4	3	2	1	0
RESERVED						LUT_SEL	
-						RW	

Address: 0x061C

Type: RW

Reset: 0x00

Description: Control of the PWL

[1:0] **LUT_SEL:** Piecewise linear transformation look up table

-0x0: DEFAULT0
-0x1: DEFAULT1
-0x2: USER0
-0x3: USER1

H.10.25 EXPOSURE_INSTANCE

7	6	5	4	3	2	1	0
VALUE							
RW							

Address: 0x061D

Type: RW

Reset: 0x00

Description: Instance of exposure to be used in this context

[7:0]	**VALUE:** Instance -0x0: INSTANCE_A -0x1: INSTANCE_B

H.10.26 READOUT_CTRL

7	6	5	4	3	2	1	0
RESERVED					CFG		
-					RW		

Address: 0x061E

Type: RW

Reset: 0x00

Description: Decimation control

[2:0]	**CFG:** Streaming readout mode control -0x00: = normal streaming -0x01: = digital binning x2 -0x02: = digital binning x4 -0x03: = subsampling x2 -0x04: = subsampling x4 -0x05: = subsampling x8 -0x06: = XY binning x2

H.10.27 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0620

Type: RW

Reset: 0x0032

Description: Manual exposure for the second exposure

[15:0]	**VALUE:** Manual exposure for visible medium

H.10.28 EXPOSURE_MANUAL_COARSE_EXPOSURE_LINES_C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE															
RW															

Address: 0x0622

Type: RW

Reset: 0x0032

Description: Manual exposure for the third exposure

[15:0]	**VALUE:** Manual exposure for visible short

H.10.29 VT_MODE

7	6	5	4	3	2	1	0
			RESERVED				MODE
			-				RW

Address: 0x0626

Type: RW

Reset: 0x00

Description: Subtraction control

[0] **MODE:** Mode

-0x0: MULTI_EXPO
-0x1: VT_SUB

H.10.30 MASK_FRAME_CTRL

7	6	5	4	3	2	1	0
			RESERVED				MASK
			-				RW

Address: 0x0627

Type: RW

Reset: 0x00

Description: Control to mask frames

[0]	**MASK:** Enable/Disable -0x0: DISABLE -0x1: ENABLE

H.11 NVM_MIRROR registers

H.11.1 NVM_MIRROR register summary

Table 19. **NVM_MIRROR register list**

Address	Register name	Description
0x0648	ENG1	ENG1 register
0x064C	ENG2	ENG2 register
0x069C	I3C	I3C register
0x06B8	I2C_ADDRESS	I2C_ADDRESS register
0x06BC	CTM_AREA_n [32]	CTM_AREA_n register

H.11.2 ENG1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x0648

Type: RW

Reset: 0x0000 0000

[31:0]	**VALUE:** First word of the unique part traceability

H.11.3 ENG2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x064C

Type: RW

Reset: 0x0000 0000

[31:0]	**VALUE:** Second word of the unique part traceability

H.11.4 I3C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE		RESERVED																						PRODUCT_CODE							
RW		-																						RW							

Address: 0x069C

Type: RW

Reset: 0x0000 0000

[31:30]	**VALUE:**
[7:0]	**PRODUCT_CODE:**

H.11.5 I2C_ADDRESS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2C_KEY								RESERVED	I2C_DEVICEID_3							RESERVED	I2C_DEVICEID_2							RESERVED	I2C_DEVICEID_1						
RW								-	RW							-	RW							-	RW						

Address: 0x06B8

Type: RW

Reset: 0x0000 0000

[31:24]	**I2C_KEY:** if I2C key = 0xAA, update I2C address
[22:16]	**I2C_DEVICEID_3:** Device I2C address
[14:8]	**I2C_DEVICEID_2:** Device I2C address
[6:0]	**I2C_DEVICEID_1:** Device I2C address

H.11.6 CTM_AREA_n [32]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VALUE																															
RW																															

Address: 0x06BC

Type: RW

Reset: 0x0000 0000

[31:0]	**VALUE:** Customer area

Revision history

Table 20. **Document revision history**

Date	Version	Changes
10-Jul-2024	1	Initial release
18-Sep-2024	2	Section 5.4: SW_STBY: Corrected spelling of "START_STREAMING" to "START_STREAM". Section 10: NVM: Added a sentence about the OTP. Corrected the cross reference to Appendix H.11: NVM_MIRROR registers. Updated Table 5. Example configurations. Section 13.5: Defect correction and noise reduction: Added a sentence about the DUSTER_DEF_COR_RATIO register. Section 13.6: Exposure: Updated the amount (8 and 32 respectively) by which the analog and digital gains are limited. Updated the code in Appendix B: External subtraction background mode. Updated Figure 25. TWO_EXPOSURE timing. Updated Figure 27. THREE_EXPOSURE timing. Updated Figure 28. Auto wake up flow. Updated Table 9. UI address blocks. Added the register DUSTER_DEF_COR_RATIO. Removed the register ANALOG_READOUT_SETTINGS.

Contents