Testing platform of SiC MOSFET for packages HU3PAK

Introduction

The board is a testing platform focused on SiC MOSFETs. The platform contains a half-bridge structure that supports HU3PAK packages. By connecting input digital signals and supplying drivers, it allows the generation of appropriate gate driver signals for the turn ON/OFF of MOSFETs in the half-bridge structure. This board allows for testing the switching performance of MOSFETs, for instance, using the double pulse test method.

Figure 1. STDES-SICGPHU3 board

1 Getting started

1.1 Safety precautions

Danger: *There is a danger of serious personal injury, property damage or death due to electrical shock and burn hazards if the kit or components are improperly used or installed incorrectly.*

Warning:

- *The kit is not electrically isolated from the high-voltage supply DC input.*
- *The evaluation board is directly linked to the high DC voltage. No insulation is ensured between some accessible parts and the high DC voltage.*
- *The high side MOSFET source is switching referring to the common input voltage GND. All measurement equipment connected to this point must be isolated from the DC source before powering the board and it has to introduce very low capacitance (<20 pF).*
- *The board is possible to supply only by DC source. Take care about correct polarity.*

Caution: During assembly, testing, and operation, the evaluation board poses several inherent hazards, including bare wires and hot surfaces.

All operations involving transportation, installation, use, and maintenance must be performed by skilled technical personnel who are familiar with the installation, use, and maintenance of power electronic systems.

Work area safety

- The work area must be clean and tidy
- Do not work alone when boards are powered
- Protect the area against any unauthorized access by putting suitable barriers and signs
- A system architecture that supplies power to the evaluation board must be equipped with additional control and protective devices in accordance with the applicable safety requirements (i.e., compliance with technical equipment and accident prevention rules)

Electrical safety

- Remove the power supply from the evaluation board and electrical loads before preparing any electrical measurement
- Arrange measurement setup, wiring, and configuration paying attention to high voltage sections
- Once the setup is complete, power the board

Danger:

Danger: *Do not touch the evaluation board when it is powered or immediately after it has been disconnected from the voltage supply as several parts and power terminals containing potentially energized capacitors need time to discharge, and heat-sinks and transformers may still be very hot.*

The kit is not electrically isolated from the DC high voltage input.

Personal safety

- Always wear suitable personal protective equipment, such as insulating gloves and safety glasses
- Take adequate precautions and install the board to prevent accidental touch
- Use protective shields, such as insulating boxes with interlocks

Caution: The board is not equipped by an EMI filter. Additionally, the fast switching of power MOSFETs can leads to high frequency oscillations generating radiated noise.

The EMI conductive and radiated emission can cross the standards limits according to assembled MOSFETs and application. To keep them within limits additional filters and shielding must be implemented.

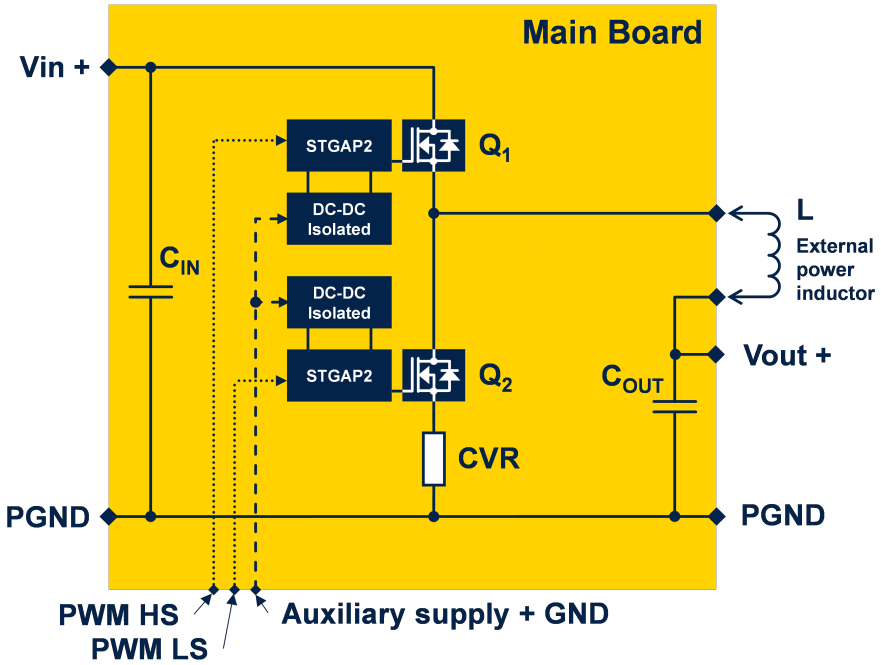
1.2 Overview

The testing board contains a half-bridge (HB) structure based on two high-voltage SiC MOSFETs. The MOSFETs are controlled by isolated gate drivers, which are supplied by isolated DC-DC converters.

The system requires the connection of an external inductor, source, load, auxiliary supply, and PWM signals. It can be used for testing the operation in buck or boost configuration. It is possible to use a low inductance shunt or to assemble a coaxial shunt to measure current through the low-side MOSFET. In this perspective, the board can be used as a tool for double pulse test (DPT).

The complete solution consists of several blocks, including the main board, drivers, and DC-DC converters. The principal block diagram is displayed in Section 1.2: Overview, and the detailed schematic of each part is displayed in .

Figure 2. Principal block diagram



Main board

The main board contains the power MOSFETs connected in a HB structure, where Q1 is the high side and Q2 is the low side. There are blocking foil capacitors and MLCCs, with one capacitor connected over the HB and the second capacitor connected between one inductor output and power GND. They work as input and output capacitors depending on the board's use, whether it is used in a buck or boost configuration. The middle point of the HB is connected to a terminal for inductor connection, and the second terminal for the inductor is connected to the foil capacitor. The maximum voltage of the power part is limited by the used MOSFETs and foil capacitors, with nominally assembled 1.2 kV MOSFETs and 1.2 kV foil capacitors, therefore the voltage must not exceed 1.2 kV. However, due to safety margins, the maximum working voltage is 1 kV. During operation, special focus on any voltage overshooting over both MOSFETs is recommended.

The main board contains connectors to supply the signal side of gate drivers and a connection for PWM signals. The PWM signals are connected to the input of gate drivers, and they have to be generated externally for the high side and low side separately.

The evaluation board can be used for different purposes, but the major reason for its development is MOSFET switching performance testing. The board can be controlled by PWM signals to provide a double pulse test, allowing for the measurement of the drain-source voltage drop and source current on the low side (Q2) MOSFET, which can be used for switching energy calculation.

Driver boards

The MOSFETs are controlled via gate drivers assembled on separate sub boards that are soldered to the main board. The sub boards are indicated by STGAP2 rectangular in the block diagram and contain isolated gate driver STGAP2SICSC and passive components around. The gate driver boards are assembled on the main board.

Isolated DC-DC converter

The power part of gate drivers is supplied by additional sub boards stacked on the driver board. This subboard contains an isolated SMPS that generates supply voltage (positive and negative) for the gate driver. The DC-DC converter is based on fly-buck topology, with the primary side converter being A6986I.

The converter generates two output voltages, and there is a discrete linear regulator behind each transformer. The output voltage of the linear regulator can be set by a resistor divider, allowing for the setting of a custom gate voltage supply depending on the tested MOSFETs.

1.3 Board connection

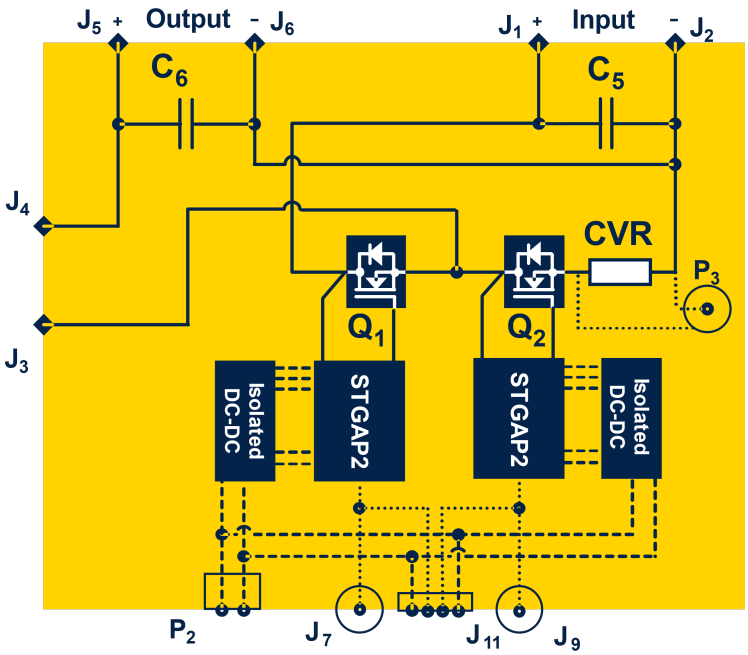
Power terminals J1 - J6

The principal diagram showing position of connectors on the real test board is visible in Figure 3. There are three couples of power terminals. The DC bus between HS Drain and low side Source is connected to terminals J1 and J2 (to capacitor C5). Terminal J2 is connected to common power GND (PGND), the terminal J1 is connected to HV bus line. The terminals J5 and J6 are connected to capacitor C6. It is applied between one terminal of inductor and power GND. The terminal J6 is connected to power GND (PGND in block diagram) and the terminal J5 is connected to HV BUS line.

If the board works in buck mode voltage source is connected between pins J1 - J2 (J1 is connected to positive source terminal and the J2 is connected to negative source terminal) and the terminals J5 - J6 are connected to the load. If the board is used in a boost mode, the terminals J5 - J6 are connected to voltage source (J5 is connected to positive source and the J6 is connected to negative source terminal) and terminal J2 and J1 are connected to the load.

The terminals J3 - J4 are dedicated for connection of the power inductor.

Figure 3. Position of connectors



Signal terminals J7, J9, J11

The auxiliary voltage and PWM signals can be connected to the board by header J11. Auxiliary voltage can be alternatively connected by screw terminals P2. The PWM signals can be alternatively connected through SMA connectors J7 and J11.

PWM signals can be generated by oscillator or MCU. It is important to avoid both signals are set HIGH at the same time. If the constant frequency is applied both signal has to be complementary with dead time.

There is possible to apply sense resistor between Source of low side MOSFET (Q2) and power GND. There are two possible assembling options.

- Low inductance shunt. It is sensed by MMCX connector P5

- Coaxial shunt. It has BNC output

The shunt can be also shorted and not used. In case coaxial shunt is assembled the Low inductance shunt has be disassembled.

Connection summary

All the connectors and terminals are listed in the table below:

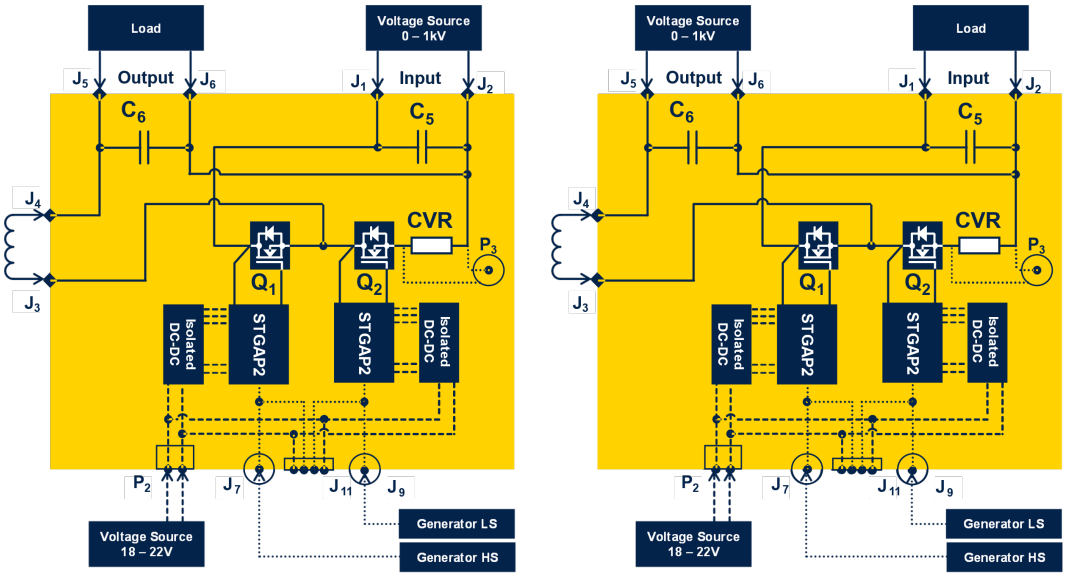
Table 1. Connectors list

Name	Pin	Label	Description
J1	1	J1	Source voltage or load. Use source if buck converter mode operation is used. Use load in case boost or DPT mode operation is used. J1 positive, J2 negative terminal.
J2	1	J2	
J3	1	J3	Inductor terminal
J4	1	J4	
J5	1	J5	Source voltage or load. Use load if buck converter mode operation is used. Use source in case boost or DPT mode operation is used. J5 positive, J6 negative terminal.
J6	1	J6	
J11	1	J11	Auxiliary supply positive terminal
	2	J11	PWM digital input for high side MOSFET driver
	3	J11	PWM digital input for low side MOSFET driver
	4	J11	GND for auxiliary supply and PWM signals
P2	1	P2	GND for auxiliary supply
	2	P2	Auxiliary supply positive terminal
J7	1	J7	PWM digital input for high side MOSFET driver, SMA coaxial connector
J8	1	J8	PWM digital input for high side MOSFET driver, 2.54mm pin header
J9	1	J9	PWM digital input for low side MOSFET driver, SMA coaxial connector
J10	1	J10	PWM digital input for low side MOSFET driver, 2.54mm pin header
P3	1	P3	Power shunt (R22) connection, MMCX coaxial connector

1.4 Typical connections

The Figure 4 shows connection is case the board is used in buck converter mode (left side) and in a boost mode (right side).

Figure 4. Typical connection in buck (left) or boost mode (right)



1.5 Maximum and operating values

To ensure safe operation, the voltages present on the terminals have to be within defined limits. Crossing the maximum values can lead to damage of parts assembled on the PCB. Using signal and auxiliary supply values out of the defined range can cause board damage or the board will not work correctly.

The maximum and minimum operating values are listed in Section 1.5, which refers to the originally applied MOSFETs. In case MOSFETs with lower Vbds are assembled, the limits for connectors J1, J2, J5, and J6 have to be adapted. It is important to consider that the maximum value is also valid for the load. For instance, in case the board works in boost mode, the output voltage could reach the maximum value. It is important to implement limitations externally to ensure safe operation.

Table 2. Maximum and minimum values

Connector	Description	Min.	Max.
J2 - J1,	DC bus over HB (input in buck mode)	0	1000V
J6 - J5	Inductor to GND (output in buck mode)	0	1000V
P2, J11 - pins(1 - 4)	Auxiliary supply voltage range	18V	22V
P2, J11 - pins(1 - 4)	Auxiliary supply input current	0	100mA
J7-10 J11 - pins(3 - 4) J11 - pins(2 - 4)	PWM - voltage range	0	3.3V
-	Ambient temperature	10°C	30°C

The PWM logic level signals has to be set regarding the Section 1.5.

Table 3. PWM – logic High and Low – voltage range

Description	Min.	Max.
PWM High level	2.2V	3.3V
PWM Low level	1.1V	3.3V

Warning: *The DC supply has to be connected respecting signs applied on the Board. Connection of negative voltage can lead to destruction of the board or some part of the board*

The specification visible in Section 1.5 is valid for original board. In case the tested MOSFET will have lower voltage, current or thermal rating, the maximum values has to be reduced accordantly.

1.6 Testing set-up

The using of the board requires to connect external parts as shown in Figure 4. Typical connection in buck (left) or boost mode (right). The power supplies has to be turned OFF when they are connected to the board. First, turn ON auxiliary supply. Then activate PWM signal and the power supply connected to power connectors (J1, J2 or J5, J6) turn ON last.

Warning:

- *Apply cover above the board to protect again possible issue*
- *Do not touch the power board when the power supply is applied*
- *Use isolated connection between power source and the board*
- *Use DC power source either with built in protections against overvoltage and overcurrent or use external protections on the input path*
- *Use DC load either with built in protections against overvoltage and overcurrent or use external protections on the input path*
- *There is no isolation and to use it connected to external DC voltage is possible only if the board itself and the external equipment is enclosure in the protective area (for instance closed box) avoiding any electrical risk*

1.6.1 Testing equipment

Auxiliary supply connected to J11 or to P2 has to satisfy the following requirements:

- The supply voltage has to be within the specification defined in Table 2
- There has to be implemented either internal or external current limitation to the level defined in Table 2

The DC source supplying the input of the board (independently if the board is working in BUCK or in BOOST mode) has to satisfy the following features:

- Requirements of maximum voltage for connectors J1, J2 respectively J5, J6 are specified in the Table 2. The maximum voltage must not be crossed. It means in case the DC source has tolerance or overshoot, the output voltage has to be set to the value lower or equal to the maximum value specified in the Table 2 reduced about this
- The current limitation has to be applied according to the assembled MOSFETs and intended application (Buck or boost). The current limiter can be implemented either in the DC source or it can be an external component. In case the current is crossing the limit the DC source output has to be turned OFF, not limited to constant-current supply
- The DC source output has to be protected against any overvoltage. If this operation is not possible to guarantee by the DC source itself, the external surge suppressor has to be applied on the input DC bus. If the protection allows any overvoltage spike, the total maximum DC voltage applied on the DC input must be set as the maximum DC voltage defined in Table 2 reduced about DC source voltage tolerance and reduced about possible voltage spike generated by surge

The output electrical values have to be tested during the testing. The load must either integrate the following protections or the protections has to be implemented externally:

- The voltage on the output voltage must not cross the voltage value defined in Table 2 for connectors J1, J2 respectively J5, J6. The circuit either built in the load or applied externally must sense the voltage and disconnect the input voltage DC source in case the output voltage crosses the value specified in Table 2
- The output current has to be measured either by the load itself or by an external sensing circuit. In case the output current crosses the limitation of selected MOSFETs, the input DC voltage has to be disconnected

1.6.2 Testing conditions

The ambient temperature during the testing of the board has to be within the thermal range specified in the Section 1.5.

The tested board has to be implemented in the protective cover. The cover has to guarantee the following features:

- The cover avoids anybody present at measurement will not be able to touch the tested board or uninsulated wires connected to input, output, or inductor
- The cover avoids possible touch of the inductor as well
- The cover protects against possible fire on the board
- The cover protects against possible explosion of any components on the board

1.6.3 Inductor used for testing

The inductor parameters applied to pins J3 and J4 can be calculated regarding the recommendation defined in Section 1.10: Inductor.

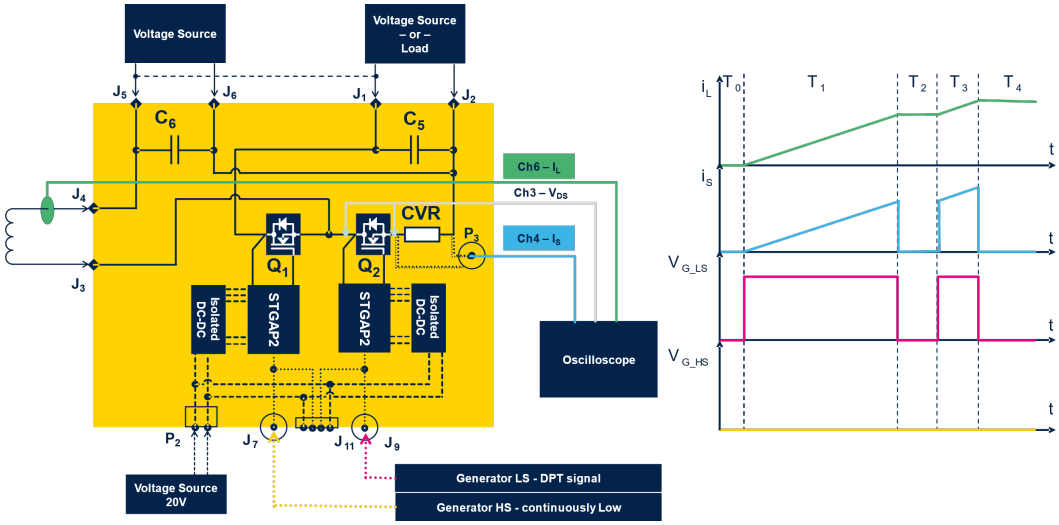
1.7 DPT operation

Double Pulse tests allows for the measurement of the turn ON and turn OFF energy of the low side MOSFET on the tests board. The board is connected in boost configuration or with just one power supply and input and output shorted (J1 and J5). Proper operation of DPT requires proper setting of Gate signal timing. The signal for the high side MOSFET is always set to Low. The low side signal must follow the timing displayed in Figure 5.

The DPT can be divided in several steps - see Figure 5:

1. T_0 period - Both MOSFET are turned OFF - auxiliary and high power sources are connected.
2. T_1 period - Low side MOSFET is turned ON. The High side MOSFET is kept turned OFF. The inductor current is rising up. In the end of T_1 period the MOSFET current reaches level used for MOSFET testing. The duration of T_1 simply allows to program testing current level.
3. T_2 period - If current reached dedicated value the T_2 period starts by low side MOSFET turn OFF. The V_{DS} and I_S are measured during transient for measurement of E_{OFF} energy. Inductor current is closing loop through high side MOSFET. As the Gate voltage of high side MOSFET is turned OFF the current flows through MOSFET body diode.
4. T_3 period - In the beginning of the period the low side MOSFET is turned ON. The V_{DS} and I_S are measured during transient for measurement of E_{ON} energy. This period is finished after the ON energy inputs are collected.
5. T_4 period - Both MOSFETs are turned OFF. Inductor current is flowing through HS MOSFET body diode and inductor is slowly discharging. Period finished after inductor current is 0A.

Figure 5. DPT - timing steps



1.8 Shunt

There are two options of low side MOSFET current measurement.

1. Using resistor R22 - low inductance shunt. The signal from this resistor is connected to MMCX connector P3. On the footprint of P3 are solderable junctions allowing to select to which node the signal will be referred to: either to the source of low side MOSFET or to the GND
2. There is possible to assemble a coaxial shunt on position of R13. In this case the R22 has to be disassembled

Both resistors are in parallel. For proper usage, only one of them should be assembled and the other one must be shorted. For this reason, there are unmasked copper plains between R13 (coaxial shunt) and the smaller foil capacitor C1 on the top layer to short R13. R22 is much easier to short on its original footprint, and for using R13, R22 must be shorted there. In case no shunt is used for measurement (e.g., high power testing), it is possible to bypass the source of Q2 directly to GND and improve the commutation loop by shorting unmasked copper plains on the bottom layer under R22.

1.8.1 Coaxial shunt

Coaxial shunt is not present in the original board assembly, but the PCB layout supports the use of such resistor. The layout is for version with threaded case body with low profile panel nuts - see the R13 type in the BOM.

This type of sense resistor is well applicable for sensing of fast transient signal requiring the bandwidth in range of hundred MHz as it has marginal stray inductance.

Assembling coaxial (R13) shunt is requiring special care in following points:

- R22 is in parallel to R13. The proper current sensing is possible only using one of those shunts. Therefore, in case R13 is assembled, the R22 has to be disassembled and shorted
- The proper measurement is considering the voltage sensing (V_{D-S} and V_{G-S}) is referred to Source point of the transistor. Therefor the body of coaxial shunt, which is in fact grounding point, is connected to the Source of the low side MOSFET. The middle point of coaxial shunt is connected to the Power GND of the board (Power GND means GND connected to input and output capacitors). This fact has to be considered for connecting voltage probes. Connecting coaxial shunt to scope and connecting voltage probe reference to power GND at the same time will cause shorting of coaxial shunt through scope GND and may cause damage to the oscilloscope or probes. The proper connection of voltage probe reference is only to Source point of low side MOSFET
- Note that the signal form the coaxial shunt is inverted: as the reference of R13 is Source of Q2 and signal the power GND
- The coaxial shunt has typically limited average power dissipation. Consider this fact regarding selected operating conditions

1.9 Gate driver supply voltage setting

The isolated part of the driver is supplied by an isolated DC-DC converter. It is based on a fly-buck topology controlled by A6986I.

The converter generates two output voltages by two secondary windings. There is a discrete linear regulator behind each transformer winding. The output voltage of a linear regulator is possible to be set by a resistor divider.

The voltage level connected to the VH pin of STGAP2SICSC is set by resistors R2 and R3. The negative voltage connected to the VL pin of the gate driver is set by resistors R6 and R9. The middle point of each divider is regulated to 2.5 V. The nominal setting of the gate voltage is +18 V/-3 V.

1.10 Inductor

The inductor is not a part of testing board. The applied inductor has to fulfill several requirements:

- The inductance value has to be in appropriate range. The estimation of inductor value is defined below
- The inductance value has not to drop below a certain level due to operating current. In other words, the saturation current of inductor has to be enough high to avoid the inductance will drop below minimum limit during the operation
- The inductor winding must be rated to applied voltages. It means it is rated to voltage applied as input and output protection

The inductor is defined by following parameters:

- Inductance L - inductance of the inductor
- Saturation current I_{sat} - current causing drop of inductor about 20%
- Maximum operating temperature
- Maximum RMS current I_{RMSmax} - current causing the inductor thermal increase will be below allowed operating temperature of the inductor for maximum ambient temperature specified in Table 2.

1.10.1 Inductance value

The value of inductor must guarantee the inductor will not be saturated by pulse current. Expected shortest duration of MOSFET turn ON is considered 1us. The minimum value of inductor can be defined as:

$$L_{min} \geq \frac{t_{ON} V_{IN\_MAX}}{I_{MAX}}$$

Where

- L_{min} is minimum value of inductance
- t_{ON} is MOSFET turn ON time. It is considered 1 us
- V_{IN_MAX} is maximum input or output voltage see Table 2
- I_{MAX} is maximum pulse inductor current

The maximum value of inductance is not limited.

1.11 Heatsink

Primary function of this board is to evaluate switching energies with DPT (see Section 1.5: Maximum and operating values). It could be used for high-power testing too, which requires a heatsink: for this purpose there are four holes to mount it on the bottom side. These are unmarked, but are in 30x60 mm rectangle around the MOSFETs. Three of them are not plated, the fourth is the same as for coaxial shunt R13: as it's power rating won't allow the high-power operation either way.

Several factors must be taken into consideration while using heatsink:

- The non-plated holes have no safety clearance to power tracks. Using isolated screws or pads is highly recommended
- Heatsink should be grounded. It is possible to use the R13 hole for this purpose
- Depends on its geometry but heatsink threats several components with electrical and/or mechanical clearance: mainly the DC bus MLCCs C2, C7, C8 and pins of C1 (or any other capacitor or terminal if large enough). The Gate capacitors C11 and C12 shouldn't collide with the heatsink, but still the clearance may not be sufficient under certain pollution degree.
- Q1 and Q2 must have electrical insulation of Drain pads and proper thermal interface material for good thermal conductivity
- It is possible to mount the heatsink with or without counterplate for the MOSFETs. There are 6mm holes above their packages for spacers for the counterplate. If no counterplate would be used these holes are intended for thermal imaging of the packages to estimate junction temperature of the MOSFETs. Also with no counterplate the PCB must be thick enough to withstand the mounting forces and gap-filling thermal interface is recommended for the MOSFETs. Further about this is written in TN1378

2 Schematic diagrams

Figure 6. **STDES-SICGPHU3 circuit schematic (1 of 2)**

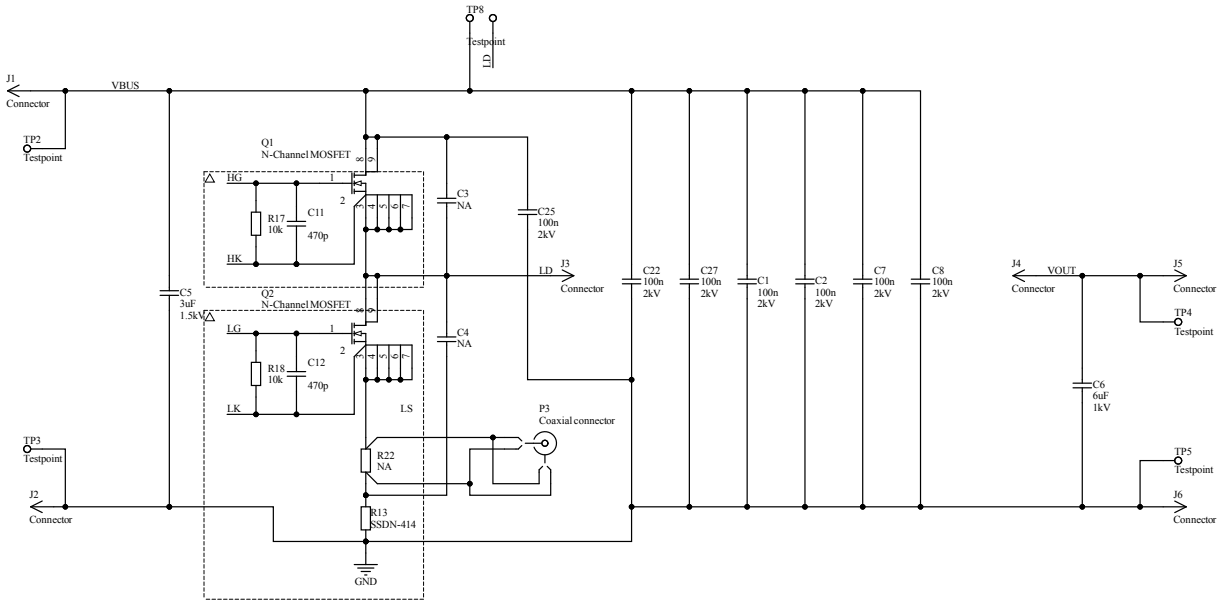


Figure 7. **STDES-SICGPHU3 circuit schematic (2 of 2)**

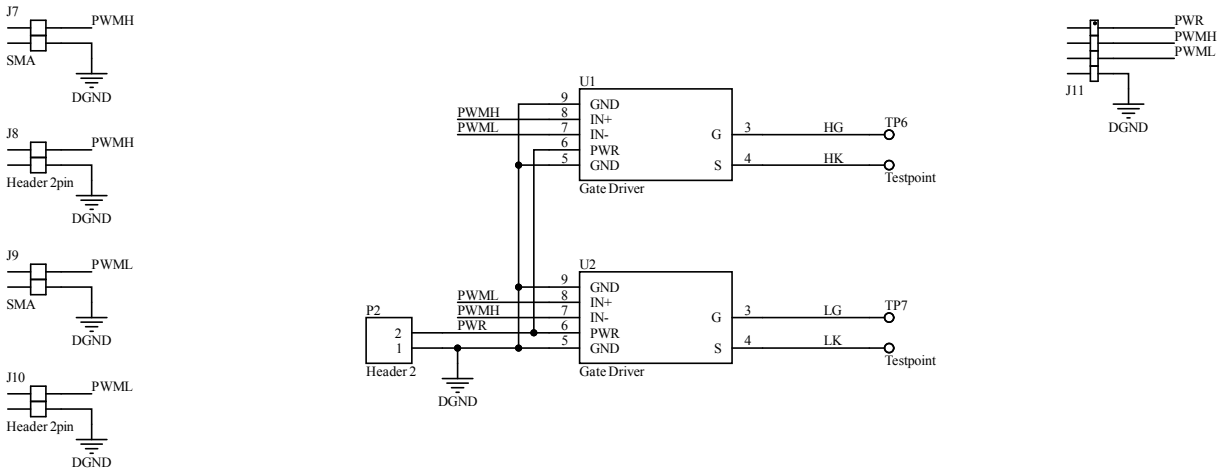


Figure 8. **Driver board**

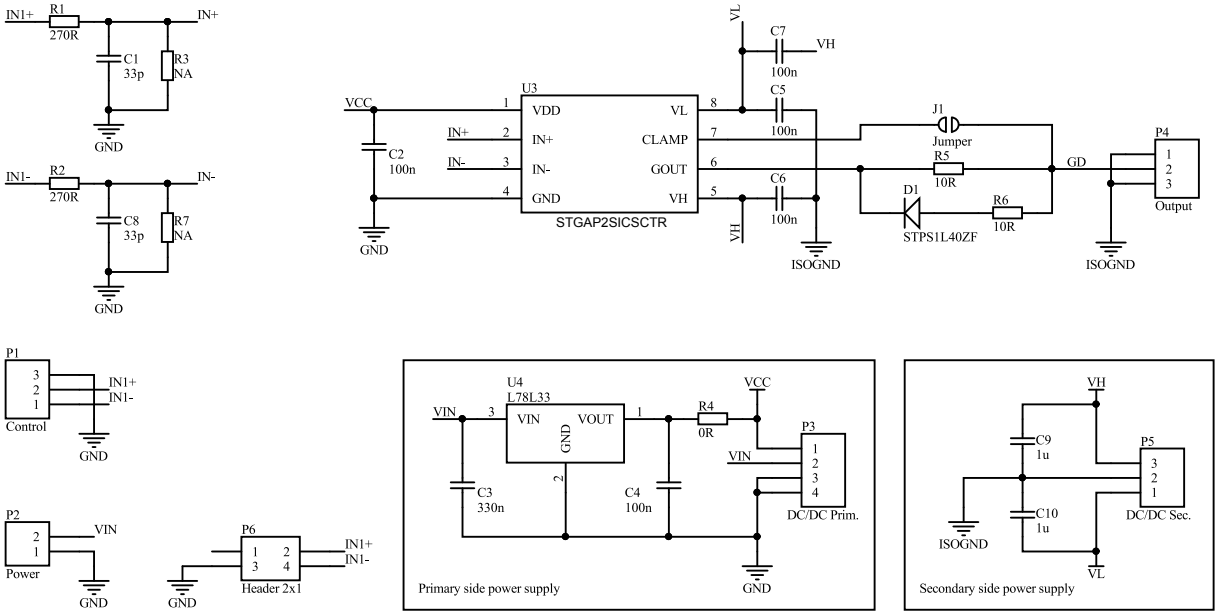
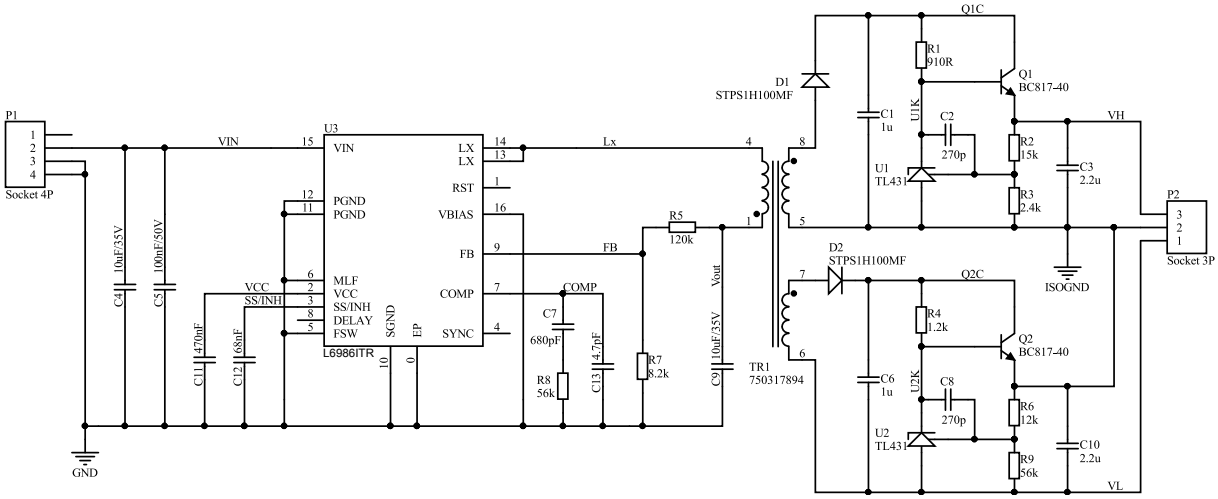


Figure 9. **DC-DC isolated converter**



3 Bill of materials

Table 4. STDES-SICGPHU3 bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	1	C1	Multi-Footprint Foil Capacitor	Foil capacitor		
2	8	C2, C3, C4, C7, C8, C22, C25, C27	Ceramic capacitor 1.2kV	Ceramic capacitor		
3	2	C5, C6	25uF / 1.2kV	Foil capacitor	Würth Elektronik	890744429002CS
4	2	C11, C12	CAP CER 0805 50V 270p	Ceramic capacitor		
5	6	J1, J2, J3, J4, J5, J6	THRBU REDCUBE M5	REDCUBE terminal	Würth Elektronik	74655095
6	2	J7, J9	SMA	SMA_PCB THT Jack Right Angle	Würth Elektronik	60311002111526
7	2	J8, J10	2.54mm 2pin	Male header 2.54mm		
8	1	J11	2.54mm 4pin	Male header 2.54mm		
9	1	P2	CON PCB TERMINAL 2-pole 5mm	Socket	Würth Elektronik	691213710002
10	1	P3	CON MMCX SMD STRAIGHT PLUG	MMCX Connector	Amphenol	908-NM22109
11	2	Q1, Q2	SiC NMOS HU3PAK	N channel SiC MOSFET	ST	
12	1	R13	SSDN-414 Coaxial CVR	Coaxial shunt	Billmann Engineering	
13	2	R17, R18	RES 0805 10k 250mW 1%	Resistor		
14	1	R22	RES 2818 20mR 10W 1%	Resistor	Vishay	WSHP2818R0200FEB
15	7	TP2, TP3, TP4, TP5, TP6, TP7, TP8	Testpoint	Test point		
16	2	U1, U2	Gate driver module	Sub board		

Table 5. STDES-SICGPHU3D - gate driver - bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	2	C1, C8	33p	Ceramic capacitor		
2	4	C2, C5, C6, C7	100n	Ceramic capacitor		
3	1	C3	330n	Ceramic capacitor		
4	1	C4	100n	Ceramic capacitor		
5	2	C9, C10	1u	Ceramic capacitor		
6	1	D1	STPS1L40ZF, SOD123Flat	Diode	ST	STPS1L40ZF
7	1	J1	Jumper	PCB Jumper		
8	1	P1	Control	PCB connector		
9	1	P2	Power	PCB connector		
10	1	P3	DC/DC Prim.	Header 2.54 4pin x 1		
11	1	P4	Output	PCB connector		
12	1	P5	DC/DC Sec.	Header 2.54 3pin x 1		

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
13	1	P6	Header 2x1	Header 2.54 2pin x 2		
14	2	R1, R2	270R	Resistor		
15	2	R3, R7	NA	Resistor		
16	1	R4	0R	Resistor		
17	2	R5, R6	10R	Resistor		
18	1	U3	STGAP2SICSCTR, SO 8 WIDE 300	Isolated Driver	ST	STGAP2SICSCTR
19	1	U4	L78L33ABUTR, SOT-89	Linear Regulator	ST	L78L33ABUTR

Table 6. STDES-SICGPHU3D - fly-buck module - bill of materials

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	2	C1, C6	CAP CER 0805 1uF 50V X7R 10%	Ceramic capacitor		
2	2	C2, C8	CAP CER 270p 0603 50V C0G 10%	Ceramic capacitor		
3	2	C3, C10	CAP CER 0805 2.2uF 50V X7R 10%	Ceramic capacitor		
4	2	C4, C9	CAP CER 10uF 35V 1206 X7R 10%	Ceramic capacitor		
5	1	C5	CAP CER 100nF 50V 1206 X7R 10%	Ceramic capacitor		
6	1	C7	CAP CER 680pF 50V 0603 C0G 10%	Ceramic capacitor		
7	1	C11	CAP CER 470nF 50V 0603 X7R 10%	Ceramic capacitor		
8	1	C12	CAP CER 68nF 50V 0603 X7R 10%	Ceramic capacitor		
9	1	C13	CAP CER 10pF 50V 0603 C0G 10%	Ceramic capacitor		
10	2	D1, D2	STPS1H100MF, STmiteFLAT	Schottky	ST	STPS1H100MF
11	1	P1	CON SOCK 2.54mm 4pin 1row	Header Receptacle 4 pins 1 row		
12	1	P2	CON SOCK 2.54mm 3pin 1row	Header Receptacle 3 pins 1 row		
13	2	Q1, Q2	BC817-40	NPN Transistor		
14	1	R1	RES 910R 0805 125mW 1%	Resistor		
15	1	R2	RES 15k 0603 100mW 1%	Resistor		
16	1	R3	RES 2.4k 0805 125mW 1%	Resistor		
17	1	R4	RES 1.2k 0805 125mW 1%	Resistor		
18	1	R5	RES 120k 0603 100mW 1%	Resistor		
19	1	R6	RES 2k4 0603 100mW 1%	Resistor		
20	1	R7	RES 6.8k 0603 100mW 1%	Resistor		
21	1	R8	RES 56k 0603 100mW 1%	Resistor		
22	1	R9	RES 12k 0603 100mW 1%	Resistor		
23	1	TR1	WE-AGDT Gate Drive Transformer	Transformer	Wurth Elektronik	750317894
24	2	U1, U2	TL431, SOT23	Shunt voltage reference	ST	TL431ACL3T
25	1	U3	L6986I, HTSSOP16	38 V, 5 W synchronous iso-buck controller	ST	L6986ITR

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
14-Feb-2024	1	Initial release.

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