Getting started with STEVAL-A6986IV3 evaluation board based on A6986I, configured as isobuck-boost and delivering four selectable dual voltages

Introduction

The STEVAL-A6986IV3 is an evaluation board based on ST A6986I.

The A6986I is designed for isolated applications and normally implements an iso-buck architecture.

The STEVAL-A6986IV3 board adopts an inverting buck-boost topology at the primary side (instead of a standard buck), hence building an isobuck-boost (so called from now on).

The advantages in using the isobuck-boost instead of a buck are mainly: higher deliverable power at the secondary side, optimization of the transformer design.

The input voltage is up to 28 V. Since the primary side performs an inverting buck-boost conversion, the primary output voltage is negative.

The secondary side of the board consists of four independent windings, each one intended to provide the supply for a gate driver (see block diagram on page 2) thanks to a very accurate post regulation.

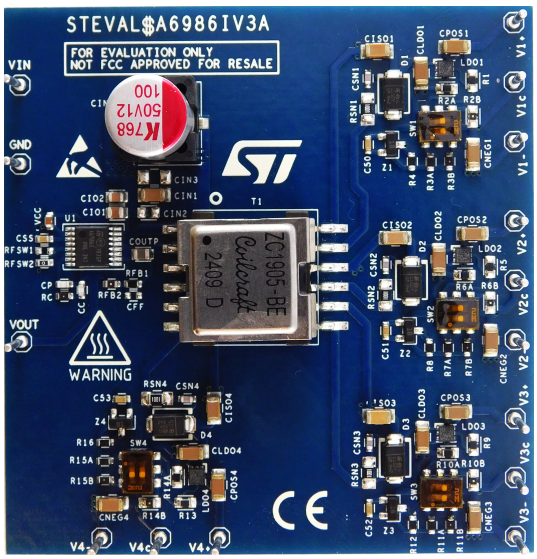
The isobuck-boost architecture exploits the power capability of the A6986I, delivering up to 60 mA for three secondary channels and up to 180 mA for the fourth one.

A microswitch provides the possibility to select two regulated voltage pairs for each channel: 18 V / - 5 V or 15 V / - 8 V. The regulation of these voltages is achieved by using the LDH40 (for the positive voltage) and a shunt regulator TL431B (for the negative voltage). The expanded output voltage range (up to 22 V) of the LDH40 makes it ideal for this kind of application.

Thanks to the LDH40 and the TL431B, the described post regulation allows a voltage accuracy well below ±1%.

The availability of four well-regulated dual voltages makes this solution ideal for gate driving in three-phase inverters.

Figure 1. STEVAL-A6986IV3 board picture



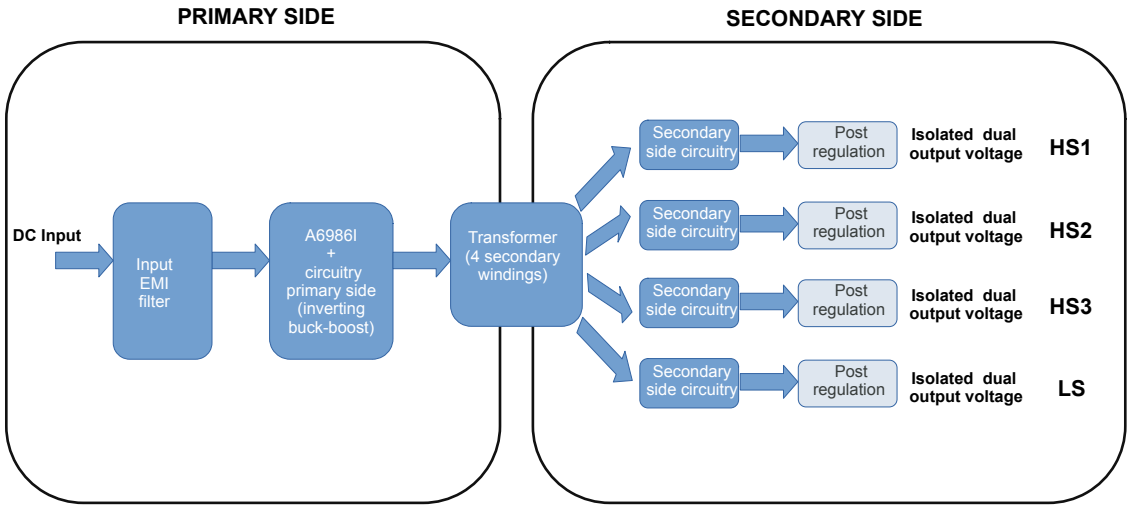
1 Getting started

1.1 Safety instructions

This board is intended for use by skilled technical personnel who are suitably qualified and familiar with the installation, use, and maintenance of power electronic systems. The same personnel must be aware of and must apply national accident prevention rules. The electrical installation shall be completed in accordance with the appropriate requirements (for example, cross-sectional areas of conductors, fusings, and GND connections).

1.2 Functional block diagram

Figure 2. STEVAL-A6986IV3 board block diagram



HS1, HS2, HS3 are the isolated dual voltages intended for three separated gate drivers (for three high side switches), LS is instead intended for the gate drivers of three low side switches (which share the same ground reference).

1.3 Features

- Designed for isobuck-boost topology
- 4V to 28V operating input voltage
- Four isolated outputs with regulated dual voltage
- Selectable isolated voltage pairs: 18V/-5V or 15V/-8V
- Three outputs (HSx) up to 60mA, the fourth output (LS) up to 180mA
- Primary output voltage regulation
- Secondary post regulation dedicated to each output with accuracy <±1%
- No optocoupler required
- 250kHz operating switching frequency
- Peak and reverse current protections
- Protection against overcurrent and short circuit events at the isolated outputs
- Thermal protection

2 How to use the board

The STEVAL-A6986IV3 is configured to generate around -10V at the primary not isolated output and four regulated dual voltages at the isolated outputs. These voltage pairs are selectable by a micro-switch: 18V/-5V or 15V/-8V. The switching frequency is set to 250kHz.

To start any measurement with this board, the below mentioned steps should be followed.

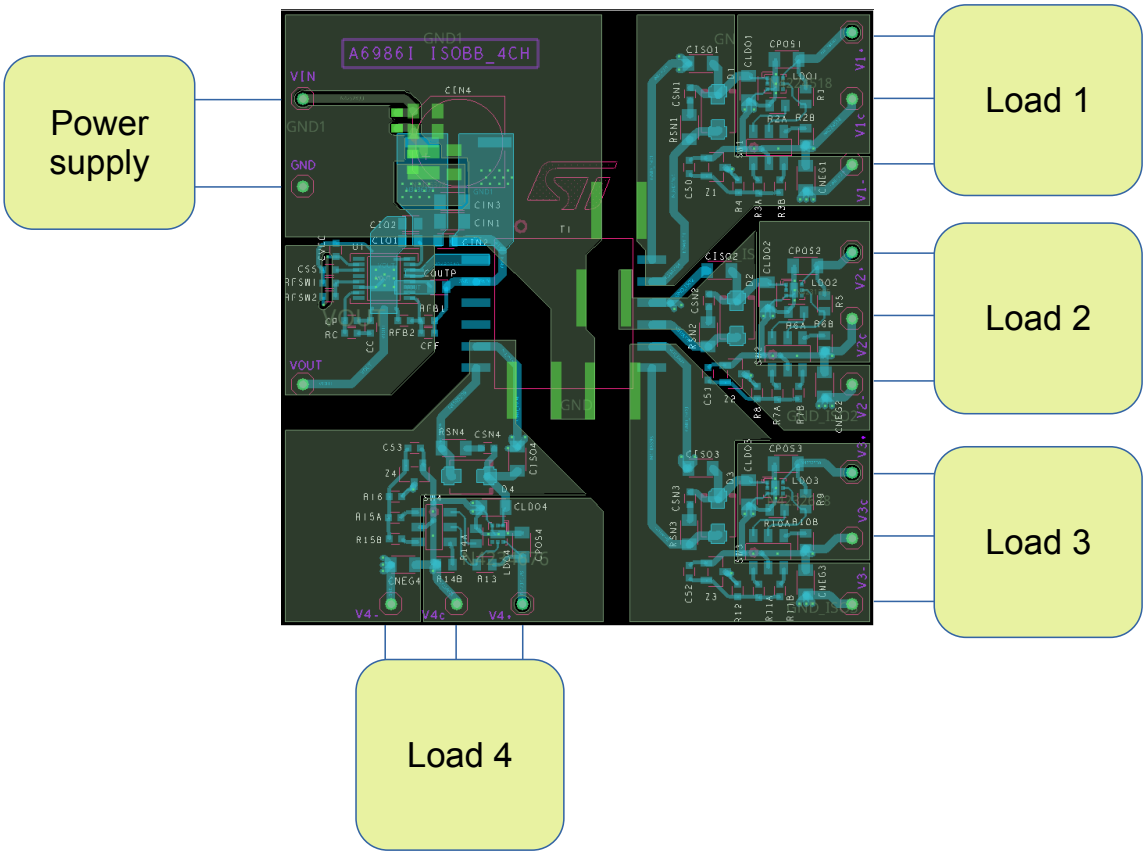
Step 1. Connect the power supply to the test points of VIN and GND.

Step 2. connect the loads to each isolated output. With load it is meant resistor, electronic load or any other suitable load (e.g. gate driver).

Step 3. Set the supply voltage VIN from 4V to 28V and switch the power supply on.

Step 4. Vary the loads (if possible) and read the voltages and/or check the relevant signals.

Figure 3. STEVAL-A6986IV3 board layout



3 Connectors and test points

3.1 VIN

This connector is for input supply voltage. This voltage is provided, through the input EMI filter, to the pin VIN of the device. A power supply ranging from 4V to 28V should be connected to this test point, setting a proper current limit.

The wire connection should be as short as possible to avoid or limit possible oscillations due to the parasitic inductance of the wire and the input capacitor.

3.2 GND

These connectors are for the return path of the input and output capacitors. Wires used for this connection should be as short as possible.

3.3 V_{OUT}

This is the connector for the primary not isolated output voltage. At this test point a negative voltage is available, normally not used.

3.4 V1+, V2+, V3+, V4+

These test points provide the positive regulated isolated voltages, which can be 18V or 15V according to the selection done with the microswitches SWn (where n can be 1, 2, 3 or 4).

3.5 V1-, V2-, V3-, V4-

These test points provide the negative regulated isolated voltages, which can be -5V or -8V according to the selection done with the microswitches SWn (where n can be 1, 2, 3 or 4).

3.6 V1c, V2c, V3c, V4c

These test points provide the reference point for the positive and negative isolated voltages (Vn+ and Vn-, where n can be 1, 2, 3 or 4).

4 Input EMI filter

The STEVAL-A6986IV3 embeds an EMI filter (bottom side).

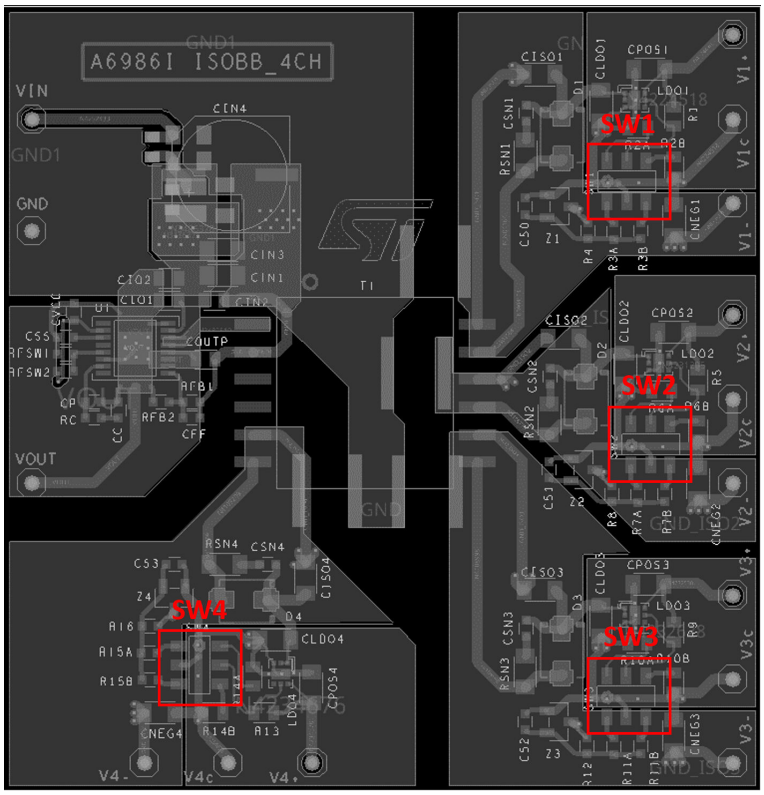
The EMI filter consists of:

- A double pi filter with an inductor (Lf2)
- A ferrite bead (Lf1)
- Three MLCC capacitors (Cf1, Cf2, and Cf3)
- An electrolytic bulk capacitor used as bulk energy storage (Cin4)

5 Board setting capability

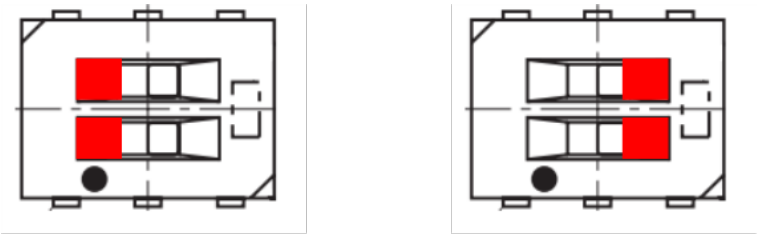
The STEVAL-A6986IV3 provides the possibility to set two different voltage pairs at the four isolated outputs by using the available four microswitches SWn (with n = 1, 2, 3, 4).

Figure 4. Microswitches for isolated output voltage selection



The selection of the desired voltages can be done according to the below figure.

Figure 5. Voltages selection with the microswitches



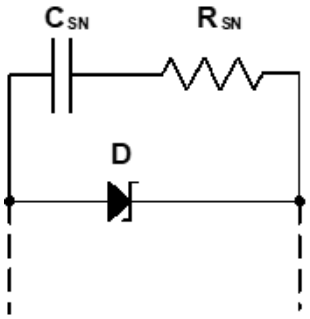
Moving both switches to the left (where the dot is drawn) the pair 18V/-5V for all isolated outputs is selected; moving both switches to the right, the pair 15V/-8V for all isolated outputs is selected. All switches should always be moved both to the same side.

The selection of the switches SW1, SW2, SW3, and SW4 must be done consistent with each other (outputs must be 18V/-5V or all 15V/-8V).

6 Snubber

In parallel with the Schottky diode of each winding a snubber network (resistor and capacitor in series) is implemented (see figure below).

Figure 6. Snubber network in parallel with the Schottky diode



The need for the snubber derives from:

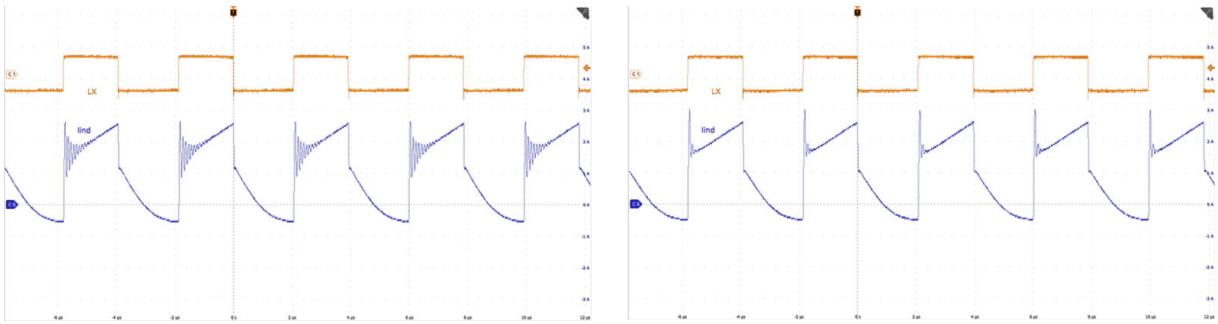
- The presence of oscillations in the primary winding current at the beginning of each on-time. These oscillations are generated by the leakage inductance together with different capacitance contributions (output, transformer, other parasitic effects)
- The implementation of the peak current mode architecture.

The peak current mode architecture requires precise current sensing to generate an appropriate drive signal for the switches. The oscillations are somehow filtered by the extended masking time (T_{ONmin} = 330 ns typ.). Nevertheless, the only presence of this masking time might be insufficient to cover the time period where the oscillations are still significant.

The snubber is therefore used to damp the oscillation and avoid that the remaining oscillations outside of the masking time might affect the regulation loop (the visible effect will be an unstable duty cycle) or even trigger the overcurrent protection (if the oscillation exceeds the peak current limit threshold).

The figure below shows the oscillations when no snubber is implemented and depicts how the snubber is effective in damping them.

Figure 7. Oscillations in the primary winding current without the snubber (left) and damped by the snubber (right)



Since the effect of the snubber is dissipating the energy associated with the oscillations, an evident drawback of its implementation is an increase of the current consumption from the input voltage, which obviously leads to a reduction of efficiency.

A trade-off between the effectiveness of the snubber network against the oscillations and the efficiency should be pursued.

7 STEVAL-A6986IV3 EMC compliance

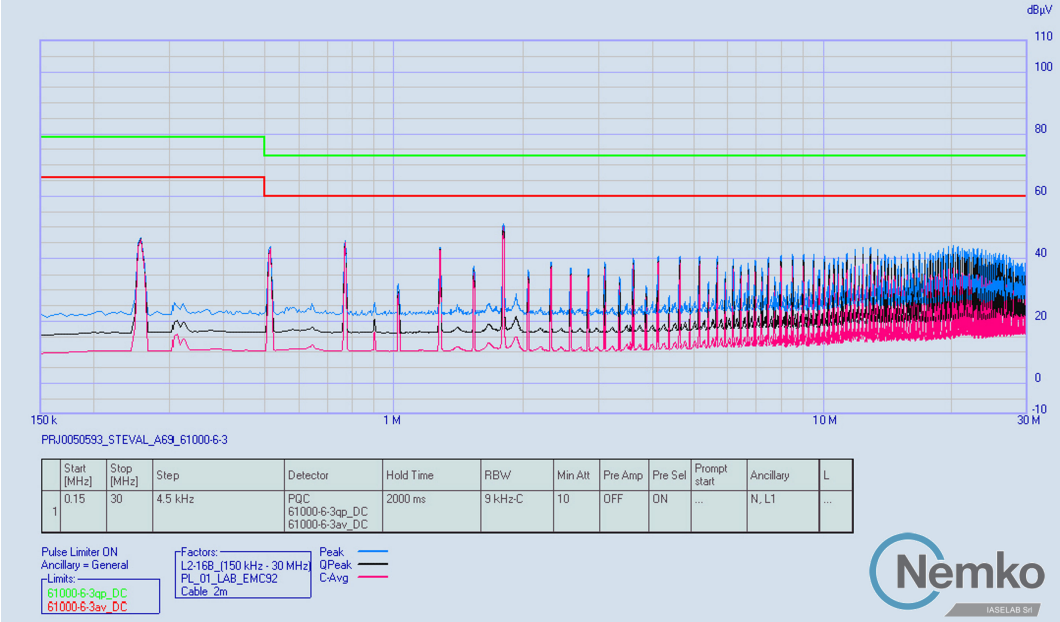
The STEVAL-A6986IV3 is certified by an external supervisor company and Class B compliant with the following standards.

Table 1. List of standards which the STEVAL-A6986IV3 complies with

Reference standard	Standard application
EN IEC 61000-6-1:2019 EN IEC 61000-6-3:2021	Full
FCC CFR 47 Part 15 Subpart B	Full
ICES-003 Issue 7 (2020)	Full

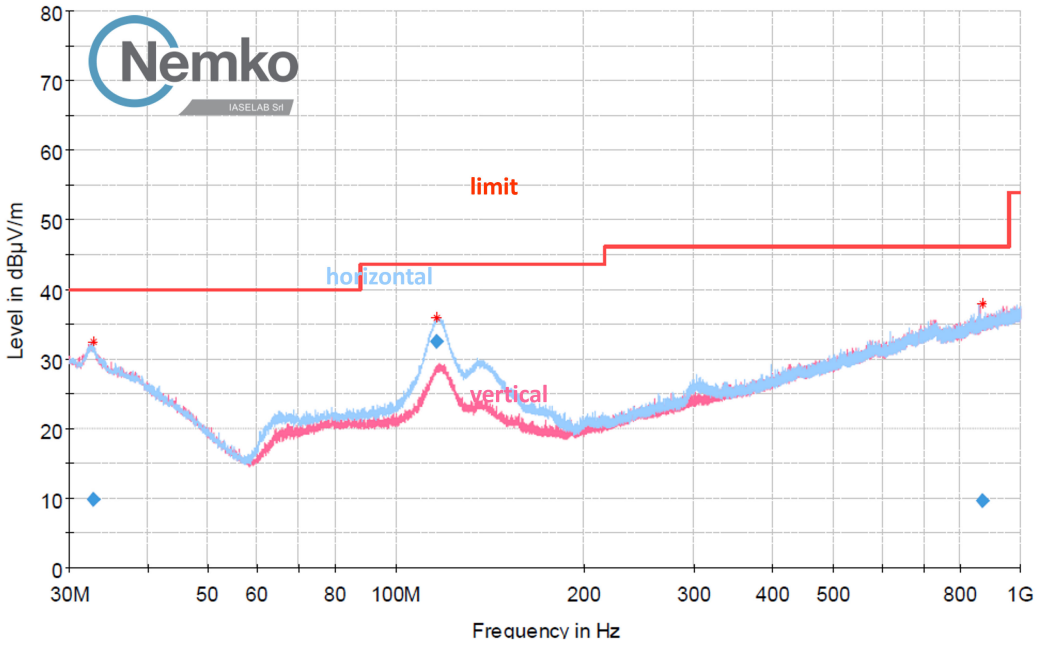
The results of the EMC tests are shown in the Figure 8 and Figure 9.

Figure 8. Conducted EMC test results of the STEVAL-A6986IV1



Note: The graph is extracted from the report REP029174_EMC_61000 issued by NEMKO SpA.

Figure 9. Radiated EMC test results of the STEVAL-A6986IV3



Note: The graph is extracted from the report REP029174_EMC_61000 issued by NEMKO SpA.

8 STEVAL-A6986IV3 performance

The following graphs show the load regulation performances of the isolated output voltages downstream of the postregulation networks.

The cumulative isolated output current indicated on the x-axis is the sum of the current drawn from all the outputs. For each current step from the outputs 1, 2, 3, a triple current value is drawn from the output 4 (e.g. 3 mA from V_{ISO1+}, V_{ISO2+} and V_{ISO3+}, 9 mA from V_{ISO4+}).

Figure 10. Load regulation of the isolated outputs vs total current from all outputs. VIN = 12V option 18V/-5V

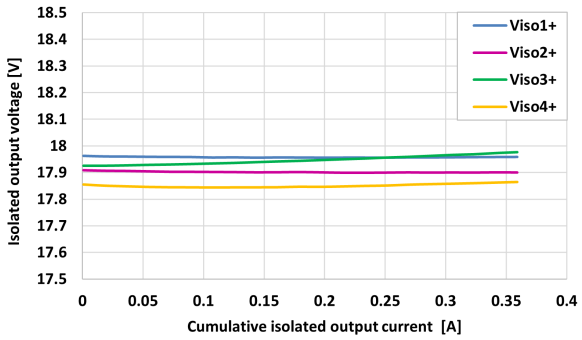


Figure 11. Load regulation of the isolated outputs vs total current from all outputs. VIN = 12V option 18V/-5V

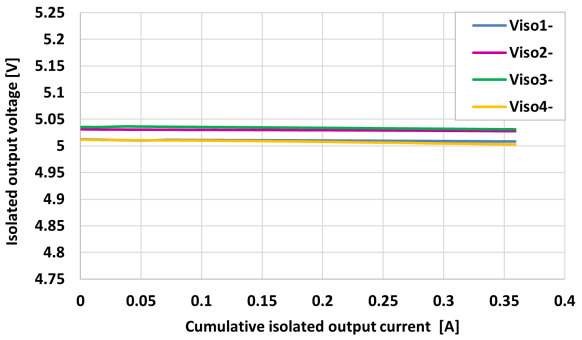


Figure 12. Load regulation of the isolated outputs vs total current from all outputs. VIN = 12V option 15V/-8V

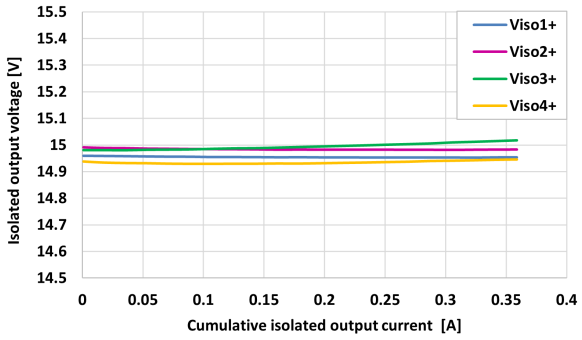


Figure 13. Load regulation of the isolated outputs vs total current from all outputs. VIN = 12V option 15V/-8V

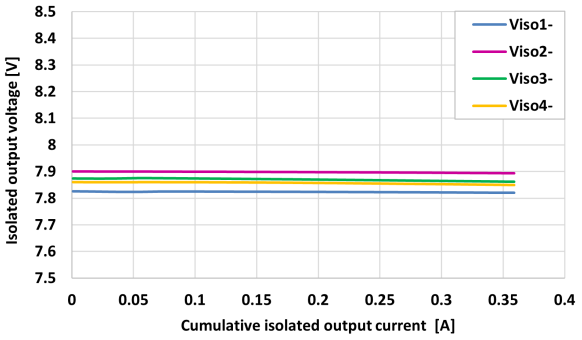


Figure 14. Load regulation of the isolated outputs vs current from each output. VIN = 12V option 18V/-5V

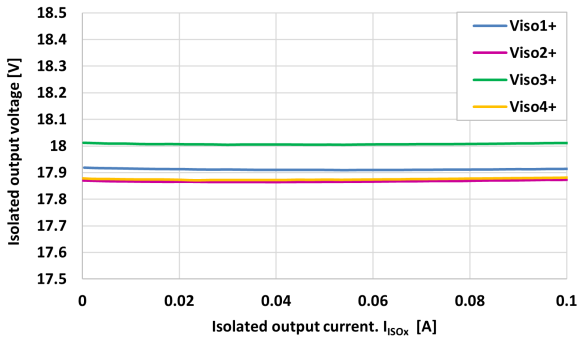


Figure 15. Load regulation of the isolated outputs vs current from each output. VIN = 12V option 18V/-5V

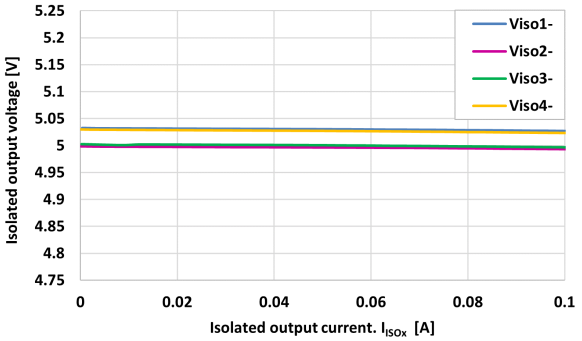


Figure 16. Load regulation of the isolated outputs vs current from each output. V_{IN} = 12V option 15V/-8V

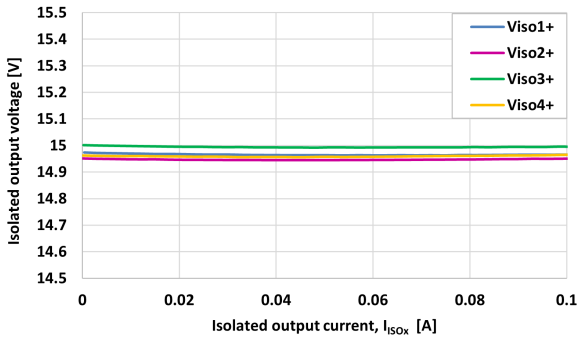
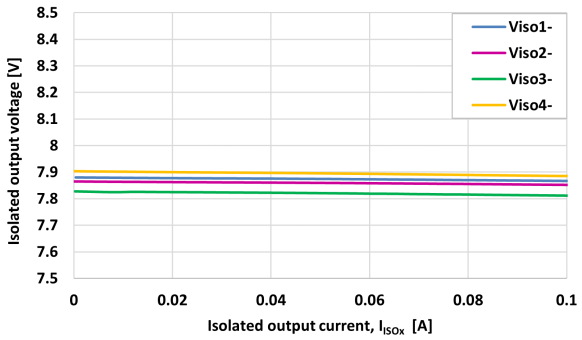


Figure 17. Load regulation of the isolated outputs vs current from each output. V_{IN} = 12V option 15V/-8V



The postregulation helps achieving excellent accuracy of the regulated voltages and is essential to split the isolated voltages of each secondary winding into the desired voltage values.

The postregulation can be implemented in different ways or can be skipped in case the requirements in terms of accuracy are not so strict or it is not required to generate a dual voltage.

Here below the load regulation performance measured upstream of the postregulation networks (Vout_iso*n*, with *n* = 1, 2, 3, 4) are shown, together with the efficiency.

Figure 18. V_{IN} = 12V, load regulation without postregulation

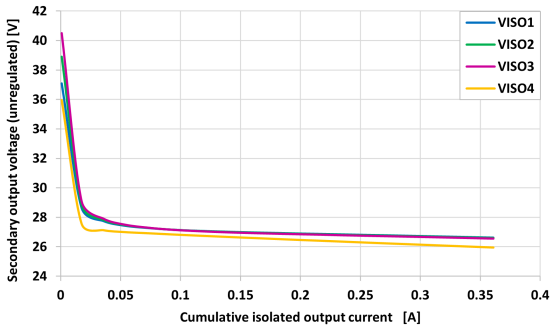
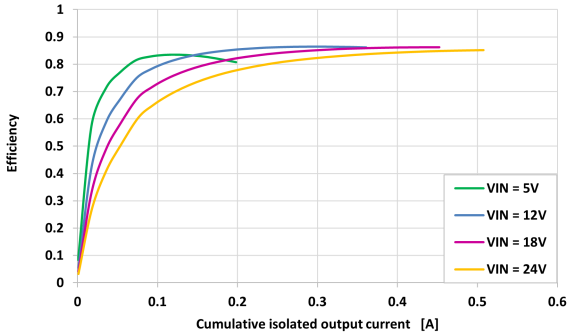


Figure 19. Efficiency at different input voltages



9 Thermal performance

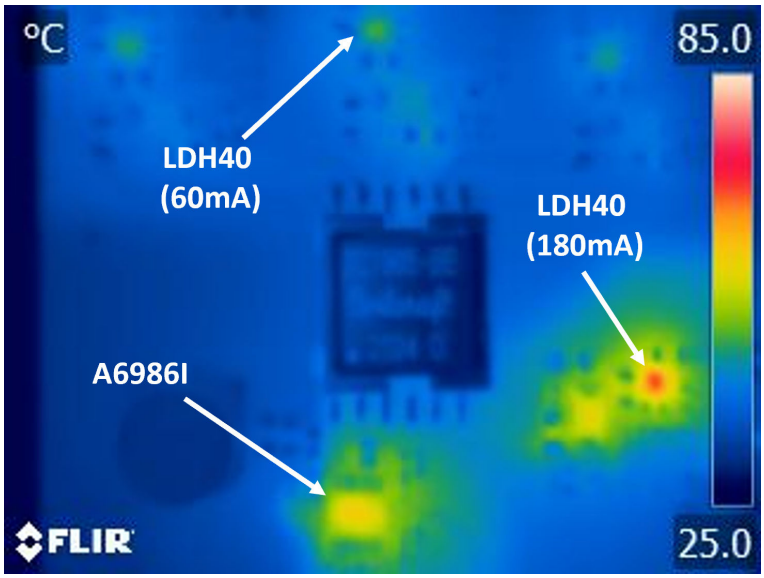
The figure below shows the thermal performance of the STEVAL-A6986IV3 detected by an infrared camera under the specified conditions.

In particular, the temperature of the A6986I and one of the linear regulators LDH40 (the one with the highest current), was monitored.

The temperature of the top side of the package for the A6986I is around 50°C, for the LDH40 is instead around 70°C for the one with 180mA, around 45°C for the ones with 60mA.

Figure 20. STEVAL-A6986IV3 thermal picture

V_{IN} = 12V, I_{ISO1}=I_{ISO2}=I_{ISO3} = 60mA, I_{ISO4} = 180mA, T_{AMB} = 25°C



10 Other voltage settings

According to the final application, different isolated voltages might be required. The voltage pairs provided by the STEVAL-A6986IV3 are mainly suitable for driving SiC and IGBT. Nevertheless, with minor and easy changes, the same board can be used to generate other common voltages.

10.1 Option 6V/-3V

Usually required for driving GaN, the voltage pair 6V/-3V can be generated with the following changes:

- Rfb1 = 4.3kΩ, instead of 11kΩ (reducing the primary output voltage)
- R1, R5, R9,R13 = 3.3kΩ instead of 11.5kΩ (setting 6V for the positive isolated voltage)
- R3a, R7a, R11a, R15a = 2kΩ instead of 10kΩ (setting -3V for the negative isolated voltage)

Micro-switches should be set like the option 18/-5V (see Section 5).

Here below the performance of the board under this new setting.

Figure 21. Load regulation of the isolated outputs vs total current from all outputs. V_{IN} = 12V option 6V/-3V

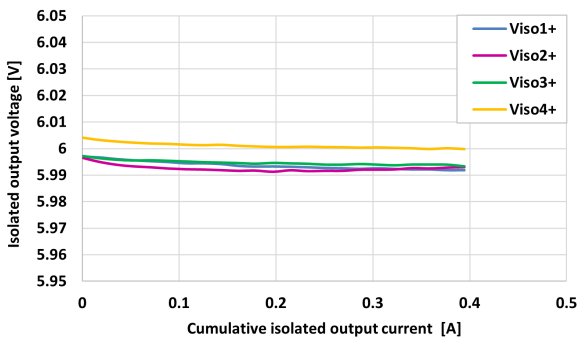


Figure 22. Load regulation of the isolated outputs vs total current from all outputs. V_{IN} = 12V option 6V/-3V

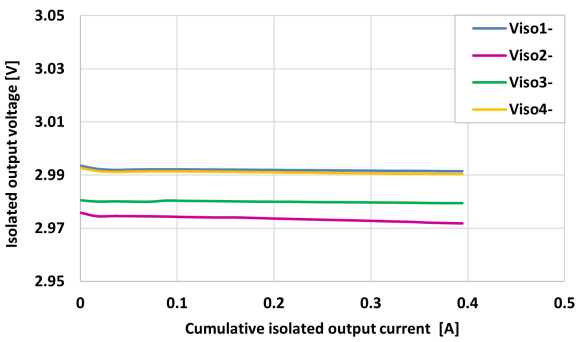


Figure 23. Load regulation of the isolated outputs vs current from each output . VIN = 12V option 6V/-3V

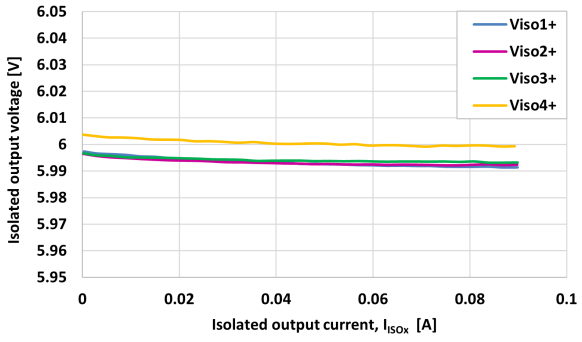
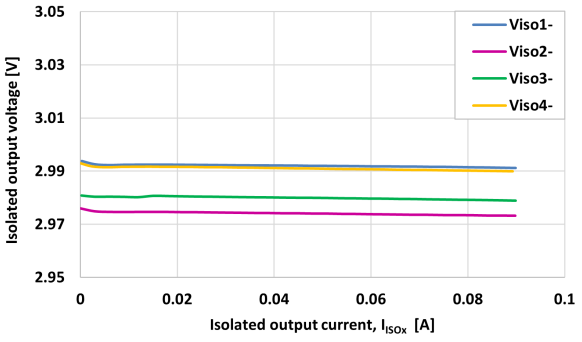


Figure 24. Load regulation of the isolated outputs vs current from each output. VIN = 12V option 6V/-3V

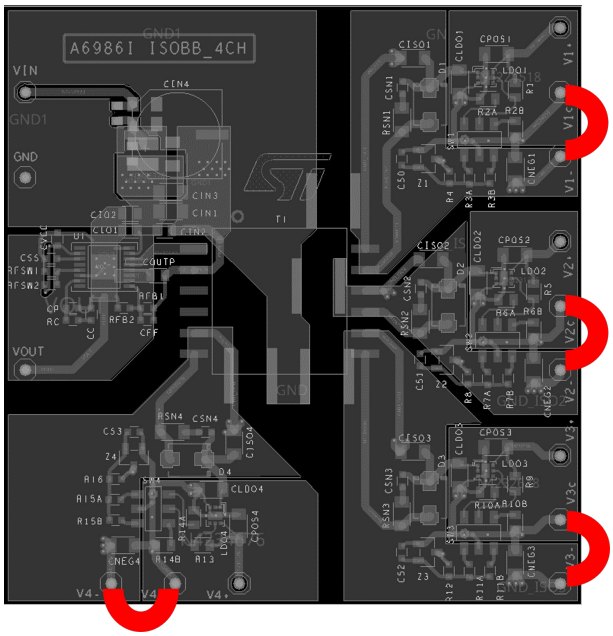


10.2 Option 12V (single)

The single voltage 12V can be generated with the following changes:

- Rfb1 = 5.5kΩ, instead of 11kΩ (reducing the primary output voltage)
- R1, R5, R9,R13 = 7.5kΩ instead of 11.5kΩ (setting 12VV for the positive isolated voltage)
- A short placed between VISO*x*- and VISO_com*x* (with x = 1,2,3,4), like in the picture below.

Figure 25. Shorting the unused negative outputs



Microswitches should be set like the option 18/-5V (see Section 5).
Here below the performance of the board under this new setting.

Figure 26. Load regulation of the isolated outputs vs total current from all outputs. V_{IN} = 12V option 12V single isolated output

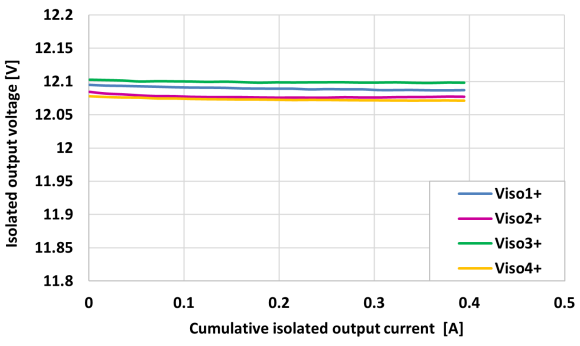
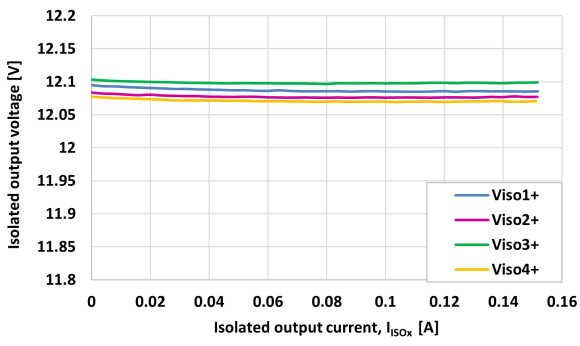


Figure 27. Load regulation of the isolated outputs vs current from each output. V_{IN} = 12V option 12V single isolated output



11 Schematic diagrams

Figure 28. **STEVAL-A6986IV3 circuit schematic (1 of 2)**

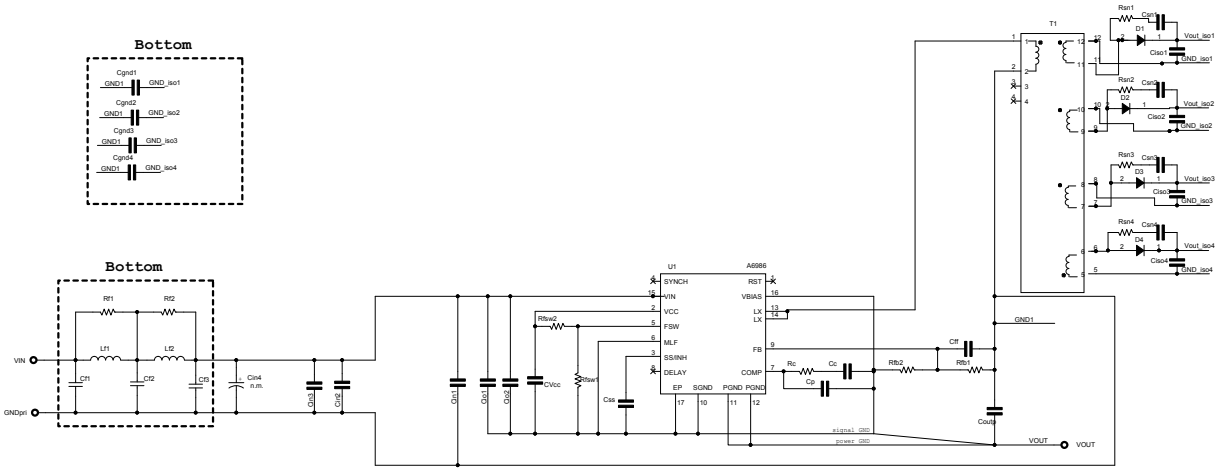
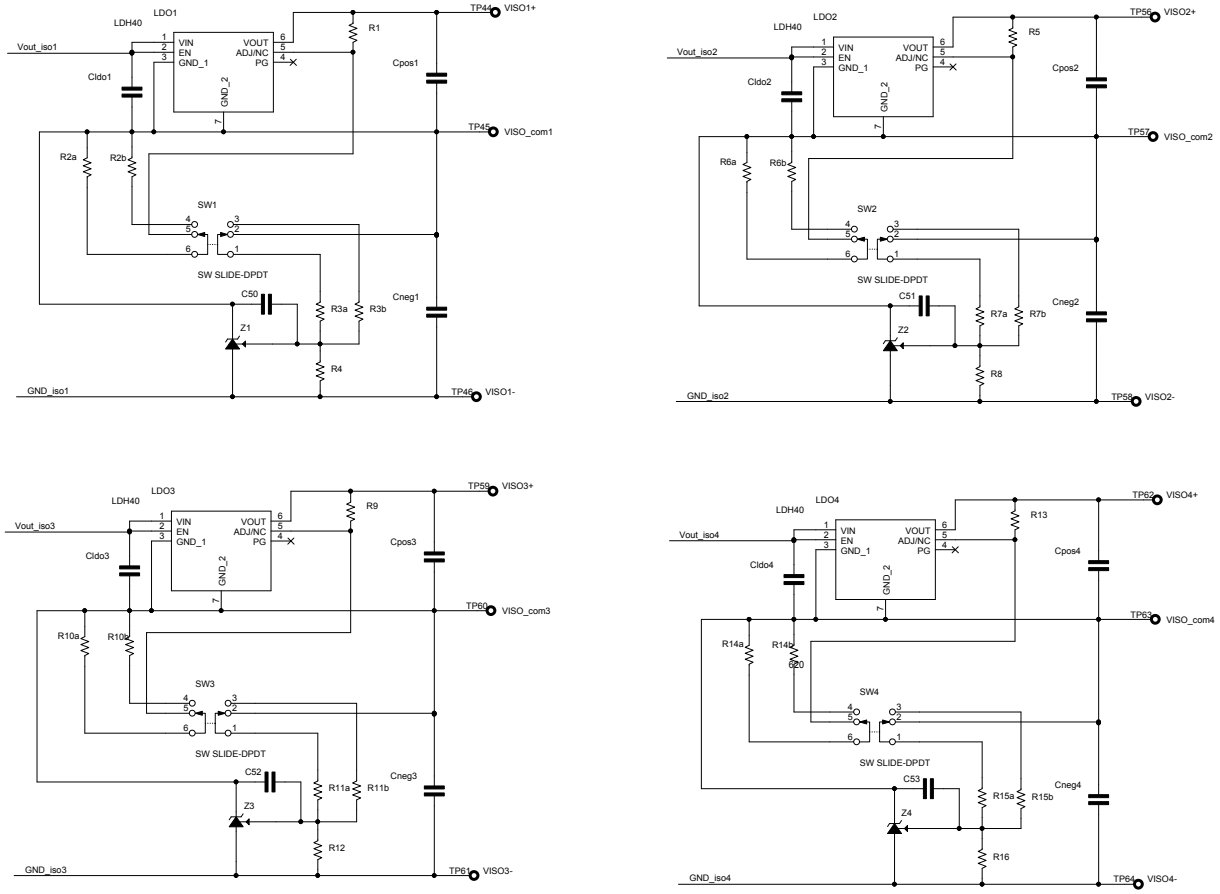


Figure 29. **STEVAL-A6986IV3 circuit schematic (2 of 2)**



12 Bill of materials

Table 2. **STEVAL-A6986IV3 bill of materials**

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
1	1	CVcc	470nF	MLCC	TDK	CGA3E3X7R1H474K080AB
2	1	Cp	4.7pF	MLCC	TDK	CGA3E2C0G1H4R7C080AA
3	1	Cc	680pF	MLCC	Samsung	CAP CER 680PF 50V C0G/NP0 0603
4	1	Cff	-	MLCC		
5	3	Cf1,Cf2,Cf3	4.7uF	MLCC	Samsung	CL10C820JB81PND
6	4	Cgnd1,Cgnd2,Cgnd3,Cgnd4	4.7nF	MLCC	Knowles Syfer	1812Y2K00472KST
7	2	Cin2,Cin3	-	MLCC		
8	1	Cin1	10uF	MLCC	Murata	GRT31CR61H106KE01L
9	1	Coutp	10uF	MLCC	Taiyo Yuden	TMK212BBJ106KGHT
10	1	Cio1	4.7uF	MLCC	TDK	CGA4J3X5R1H475K125AB
11	1	Cio2	100nF	MLCC	Murata	GCM21BR71H104KA37K
12	2	Rf1,Rf2	-	SMD resistor		
13	1	Cin4	100uF	Electrlythic Polymer Aluminum capacitor	Kemet	A768MS107M1HLAV024
14	1	Css	68nF	MLCC	Samsung	CL10B683KB8WPNC
15	1	Rfsw1	-	SMD resistor		
16	1	Rfsw2	0Ω	SMD resistor	Panasonic	ERJ-3GEY0R00V
17	4	Ciso1, Ciso2,Ciso3,Ciso4	10uF	MLCC	TDK	CGA4J3X5R1H475K125AB
18	4	D1, D2,D3,D4	STPS1150-Y, SMA	Schottky diode	ST	STPS1150AY
19	12	Cpos1,Cneg1, Cldo1,Cpos2, Cneg2,Cldo2, Cpos3,Cneg3, Cldo3,Cpos4, Cneg4,Cldo4	1uF	MLCC	Murata	GCM31CL81H105KA55L
20	4	C50,C51,C52, C53	1nF	MLCC	Murata	GCM188R71H102KA37D
21	4	Csn1,Csn2,Csn3,Csn4	82pF	MLCC	Samsung	CL10C820JB81PND
22	4	LDO1,LDO2,LDO3,LDO4	LDH40PURY, DFN 6L 2X2X 0.75 PITCH0.65 AG	LDO	ST	LDH40PURY
23	1	Lf1	MPZ2012S221A	SMD ferrite bead	TDK	MPZ2012S221AT000
24	1	Lf2	4.7uH	Inductor	Coilcraft	XGL4030-472MEC

Item	Q.ty	Ref.	Part / Value	Description	Manufacturer	Order code
25	1	Rc	56kΩ	SMD resistor	Panasonic	ERJ-UP3F5602V
26	1	Rfb1	11kΩ	SMD resistor	Panasonic	ERJ-UP3F1102V
27	1	Rfb2	1kΩ	SMD resistor	ROHM	ESR03EZPF1001
28	4	Rsn1,Rsn2,Rsn3,Rsn4	1kΩ	SMD resistor	Vishay	CRCW08051K00FKEAHP
29	4	R1, R5, R9, R13	11.5kΩ	SMD resistor	Vishay	RCS060311K5FKEA
30	4	R2a,R6a,R10a,R14a	825Ω	SMD resistor	Vishay	RCS0603825RFKEA
31	4	R2b,R6b,R10b,R14b	1kΩ	SMD resistor	ROHM	ESR03EZPF1001
32	4	R3a,R7a,R11a,R15a	10kΩ	SMD resistor	ROHM	ESR03EZPF1002
33	4	R3b,R7b,R11b,R15b	22kΩ	SMD resistor	Panasonic	ERJ-UP3F2202V
34	4	R4, R8, R12, R16	10kΩ	SMD resistor	ROHM	ESR03EZPF1002
35	4	SW1,SW2,SW3,SW4	-	Micro switch	Nidec Components Corporation	CAS-D20TA
Coilc	1	T1	ZC1905-BE	Transfomer	Coilcraft	ZC1905-BE
37	1	U1	A6986ITR, HTSSOP16	Buck regulator	ST	A6986ITR
38	4	Z1,Z2,Z3,Z4	TL431BL3T, SOT23	Shunt voltage reference	ST	TL431BL3T
39	15	TP7, TP44, TP45, TP46, TP56, TP57, TP58, TP59, TP60, TP61, TP62, TP63, TP64, TP65, TP66	Test points		Ettinger	013.14.125

13 Main parameters of the transformer ZC1905-BE

Table 3. Main parameters of the transformer ZC1905-BE

Description	Value
Turn ratio	1:2.7
Magnetizing inductance	20µH
Leakage inductance	250nH
Primary winding resistance	50mΩ
Secondary winding resistance (HS1)	1.95Ω
Secondary winding resistance (HS2)	1.95Ω
Secondary winding resistance (HS3)	1.95Ω
Secondary winding resistance (LS)	1.13Ω

14 Board versions

Table 4. **STEVAL-A6986IV3 versions**

Finished good	Schematic diagrams	Bill of materials
STEVAL$A6986IV3A (1)	STEVAL$A6986IV3A schematic diagrams	STEVAL$A6986IV3A bill of materials

1. *This code identifies the STEVAL-A6986IV3 evaluation board first version.*

15 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2015/863/EU (RoHS).

Notice for the United Kingdom

This device is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK S.I. 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK S.I. 2012 No. 3032).

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
07-May-2024	1	Initial release.

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