VIPower M0-9 standard high side drivers

Introduction

VIPower parallel high side drivers have reached the 9th generation of smart power drivers (internally called M0-9). In this latest set of drivers all the experience and know-how from existing features of the previous generations as well as new features have been implemented.

The continuously increasing demanding requirements from automotive customers in terms of quality, reliability, flexibility and cost effective system solutions represent the basic factor of the new protection feature concept - latch off in overload condition beside the already known auto restart feature. High diagnostic precision has been reached for current sensing available to the microcontroller by “current sense” (CS) pin.

The purpose of this hardware design guide is to give a comprehensive” tool kit” for a better understanding of the behavior of the M0-9 parallel high side drivers in their application usage context and thus allowing the design engineer an easier design in.

1 General items

1.1 Overview about M0-9 standard high side drivers

The M0-9 standard high side drivers are manufactured using ST proprietary VIPower technology. The devices are designed to drive 12 V automotive resistive as well as inductive and capacitive loads connected to the ground. A 3.3 V respectively 5 V CMOS compatible interface to a microcontroller unit is provided. The products feature a very low quiescent current to preserve battery charge during standby mode. Undervoltage shutdown acts below 4 V to ensure that the loads are driven when the charge pump can deliver sufficient power. The overvoltage clamp structure protects the devices effectively from “ISO 7637-2:2011(E)” pulses. At loss of ground the outputs are safely turned-off, the current injected into the outputs is less than 2 mA. At loss of V_{CC} the outputs are also safely turned-off, but special care must be taken when inductive loads are driven, since additional external protection might be required to absorb the demagnetization energy.

Reverse battery protection is provided with external components, and the driver manages the self turn-on of the output channels (except for VNQ9080AJ).

M0-9 standard high side drivers integrate advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off. A FaultRST pin unlatches the output in case of fault or disables the latch-off functionality. A dedicated multiplexed analog output pin delivers sophisticated diagnostic functions including:

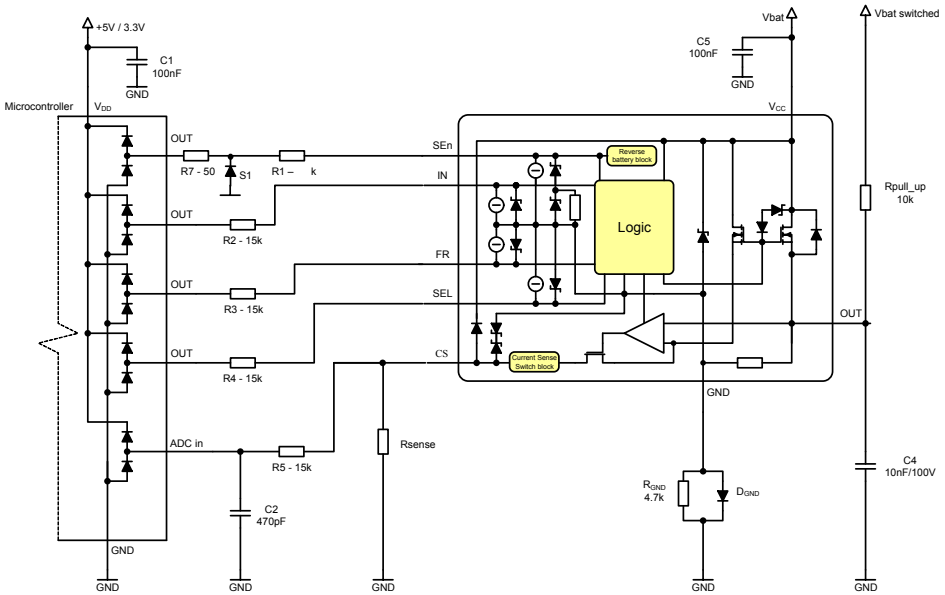
- Proportional load current sense (CS)
- Detection of overload
- Short circuit to ground
- Short to VCC and
- Off-state open-load

A sense enable pin allows off-state diagnosis to be disabled when it is needed to send the module in low power mode. Moreover, thanks to the sense enabled functionality, it is possible to share one common external sense resistor among several devices and so to manage a multidevices diagnostic bus.

1.2 Typical application schematic

Typical application schematics for M0-9 HSDs with automatic turn-on during reverse battery.

Figure 1. Typical application schematics



Note: Schematics with automatic turn on during reverse battery.

1.3 Application schematics – description of external components

Pull-up: This resistor is optional and is needed when the open load in off state diagnostic is required. It must be dimensioned to pull-up the output above the maximum open load in off state detection voltage (V_{OL} max) and make sure that the output voltage stays below the minimum open load in off state detection voltage (V_{OL} min) in case the load is connected. (For details refer to Section 7.2.10: Open load detection in off-state).

R5//C2: A low pass-filter, such as an RC filter, can be placed across the R_{sense} resistor to suppress HF noise. The time constant of this filter ($\tau = RC$) should be long enough to effectively suppress the noise and short enough to allow current sense signal stabilization considering multiplexer delay and settling times. C2 should be placed close to the MCU's A/D input. Also, the ground connection for C2 should be at the same potential as the ground of the A/D reference. The filter resistor R5 is also used to limit the A/D's input pin current.

C4: It is recommended to place a ceramic capacitor on each output to dissipate energy of high frequency, high voltage transients, in particular ESD transient pulses. A 100 V ceramic capacitor generally has sufficient voltage capability. The device ESD robustness of each pin is rated in the absolute maximum rating chapter of the datasheet.

C5: C5 capacitor helps to suppress voltage transients that originate from other actuators connected in parallel and sharing the same battery line. This capacitor is capable to suppressing only low energetic short transient pulses.

Moreover the C5 capacitor helps to suppress HF noise at the VCC pin that is generated by the high side driver device itself. The noise can originate from the charge pump circuitry or from the switching slopes of the PWMed outputs.

Using a 100 nF low ESR ceramic capacitor mounted close to device V_{CC} and GND terminals that the devices meet CISPR25 class 5 requirements measured in conducted emission voltage method in DC- as well as in PWM-operation.

Finally, during a loss of V_{CC} condition, the C5 capacitor supplies load current for the demagnetization of inductive loads.

R_{sense}: R_{sense} resistor converts the CS output current, which is a copy proportional to the load current, into a voltage which can be read by the A/D converter of the microcontroller. The R_{sense} should be dimensioned to ensure proper resolution range and granularity to monitor nominal current as well as detecting open load or overload events. Typical values of R_{sense} are in the range from 1.2 kΩ to 2.5 kΩ, to generate typically 1 V – 2 V sense voltage at nominal load current. R_{sense} selection must also consider maximum power dissipation and maximum current injection during reverse battery conditions and ISO 7637-2:2011(E). Refer to chapter 8 for details of R_{sense} dimensioning rules.

R2-R5: R2-R5 serial resistors are needed on digital inputs in order to limit the current in the input structures as well as in the microcontroller output structures to a safe value during transient and reverse battery conditions. A proper value for such resistors is 15 kΩ.

R1 (R_{SEn}=2.2 kΩ): for all the devices with reverse turn-on feature (for further details, check section 2.3) has been chosen as a trade-off between the input protection during transients (as per R2-R5) and to guarantee the functionality of the reverse turn-on feature. For VNQ9080AY (no reverse battery automatic turn-on), R1=R_{SEn} can be set 15 kΩ like for all the other pins.

S1 and R7: due to the lower resistance in serie to the SEn track, it is suggested for M0-9 devices having the automatic turn-on during reverse battery, to adopt a diode with anode connected to GND and cathode connected to the SEn line. This additional component creates a low impedance path and protects the microcontroller I/O connected to the SEn line, during negative transients happening on VCC pin of the M0-9 HSD and pulling negative the SEn pin. A R7= 50 Ω resistor placed directly at the µC I/O connected to the SEn line might be necessary to shift the triggering of the diode forward bias from the structure embedded in the uC port to the external Schottky S1 as shown in Figure 1. Typical application schematics. These components are not necessary for the VNQ9080AJ (where R1=R_{SEn} is set to 15 kΩ).

No low ohmic impedance paths to GND such as pull-down transistors or capacitors shall be connected directly to the digital inputs. In such conditions, device ground shift may trigger intrinsic parasitic structures and an unlimited, destructive current path from V_{CC} to the digital input will be formed.

Rgnd/Dgnd : a reverse polarity protection network between device ground and module ground is also needed. The diode prevents unlimited destructive current flow through the V_{CC}-GND clamping structure in case of reverse polarity connection. Rgnd paralleled to Dgnd avoids device ground dropping to negative voltage during turn-off of inductive loads and allows the turn-on of the power MOSFET during a reverse battery event. Rgnd recommended value is 4.7 kΩ.

2 Reverse battery protection

2.1 Introduction

A universal problem in the automotive environment is the threat of damage when an end-user inverts the battery polarity.

Users of battery-powered equipment expect safeguards to prevent damage to the internal electronics in the event of reverse battery installation. These safeguards can be either mechanical (use of special connectors) or electronic. In that case, battery-powered equipment designers and manufacturers must ensure that any reverse current flow and a reverse bias voltage are low enough to prevent damage to the equipment's internal electronics. Different concepts applying passive or active reverse polarity protection are possible and described in this chapter to provide these electronic safeguards.

The reverse battery protection needs to be inserted according to the instructions suggested in this chapter. Suppose that the reverse polarity protection is installed on the device GND connection; in that case, the device conducts through the power MOSFET's body diode with the current limited by the external load.

Depending on the type of device (with or without reverse turn ON feature, for classification please refer to Section 4.1: Latch-off functionality), a specific protection could be implemented in order not to exceed the device's reverse capability:

HSDs without reverse turn ON feature (VNQ9080AJ): the reverse battery protection needs to be inserted according to the instructions suggested in this chapter. If the reverse polarity protection is installed on device GND connection, the device conducts through the body diode of the power MOSFET with the current limited by the external load. Since no device intrinsic protection schemes are active in reverse condition, special care must be taken on total power dissipation.

HSDs with reverse turn ON feature: these type of HSD needs external components to protect only the internal logic in case of a reverse battery condition. While, because the output MOSFET turns on in reverse battery condition thus providing the same low ohmic path as in regular operation condition, no additional power dissipation has to be considered. So, if the inverse current is allowed to flow in the power MOSFET, protection only on the GND terminal is needed. Furthermore, the GND resistor, in parallel to the diode or to the N-channel MOSFET connected to GND, is mandatory, otherwise the output MOSFET is unable to turn on and thus the reverse turn ON feature of the driver is disabled.

Note that no protection features are operating under reverse battery conditions for the whole product family.

In the next section Section 2.2: Reverse battery protection of HSDs, the case of HSD without turn-on block will be discussed and then in Section 2.3: Reverse battery protection of HSDs with reverse turn-on feature the case of those with reverse turn-on block.

2.2 Reverse battery protection of HSDs

Reverse battery protection schemes can basically be grouped in the following categories:

- Active or passive reverse polarity protection.
- Reverse polarity protection on supply line (V_{CC} terminal) or on GND line (GND terminal)

Table 1. Reverse battery protection concepts

Reverse battery protection concept	Chapter	Active / passive	V_{CC} terminal / GND terminal	Conduction through output stage
Diode || resistor	2.2.2	Passive	GND	Yes
n-channel MOSEFT	2.2.3 and 2.3.2	Active	GND	Yes
Schottky diode	2.2.1	Passive	V_{CC}	No

In case of device with the reverse turn-on feature, the protection across V_{CC} (on the battery side) it is necessary to protect the load which is not rugged against a polarity inversion. Whereas if the load can sustain an inverse current, only a GND network is always necessary to protect the HSD itself. For such devices it is recommended only one of the protections on the GND path for the correct operation of the reverse turn-on block.

2.2.1 Schottky diode

When the battery is installed backward, the Schottky diode is in reverse–bias and only the rated leakage current IR flows. With respect to a standard diode, the Schottky diode has the advantage of a shallow voltage drop in a forward direction; hence the power dissipation is reduced. However, the disadvantage of using a Schottky diode is that it is typically more expensive than a standard diode.

Below reported, there is a suggested procedure to choose the right device correctly. The following parameters constitute the selection criteria:

- The average current used by the device, electronic module, loads to be reverse battery protected. Failure scenarios, such as an output shorted to GND (load short circuit) has to be considered as well.
- The maximum repetitive peak reverses voltage V_{RRM}
- The maximum ambient temperature T_{amb}
  The following inequality must apply in all cases:

$$T_{amb} + R_{th} \cdot P < T_{jMAX} \quad (1)$$

  Where:

$$P = V_{TO} \cdot I_{F(AV)} + rd \cdot I^2_{F(RMS)} \quad (2)$$

  $I_{F\ (AV)}$= maximum average forward current
  $I_{F\ (RMS)}$= RMS forward current
  R_{th}= thermal resistance (junction to ambient) for the device and mounting in use.
  Rd (small signal diode resistance) and V_{TO} are depending on the particular characteristics of the diode.
  One important thing to consider is the peak reverse voltage limit of the Schottky diode. In case compliance with “ISO 7637-2:2011(E)” pulse 1 test level IV is required, V_{RRM} must be >= 150 V. The main drawback of this method is the power dissipation in the Schottky diode in the forward direction. Depending on the type of package, the R_{th} and the ambient temperature, the maximum affordable power dissipation in the Schottky diode is typically in the range of 1 W. In consequence, the maximum average forward current is limited to the range of 1 A – 2 A.

2.2.2 Diode + resistor in GND line

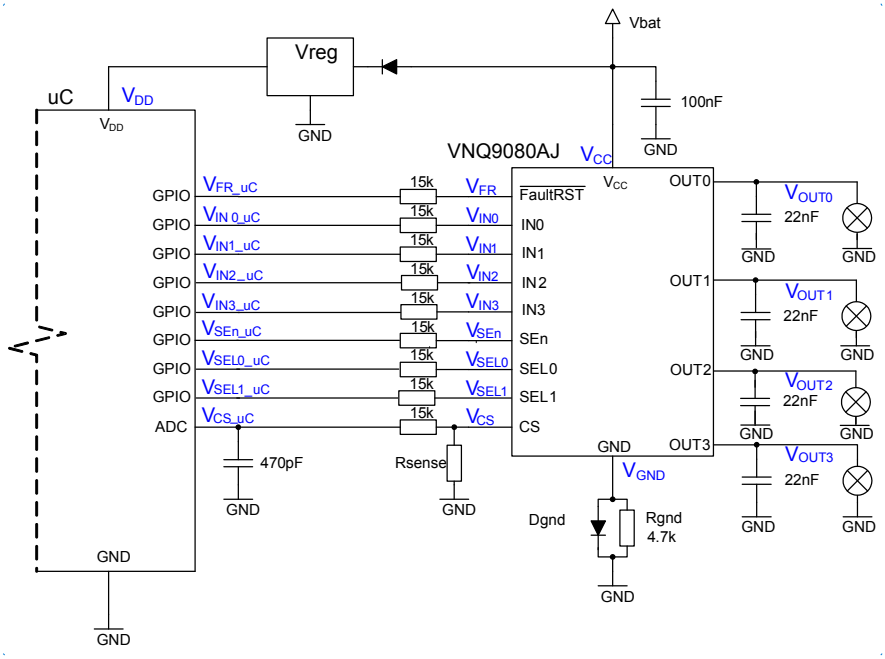
The reverse battery protection is applied to the GND terminal of the driver. This kind of protection leaves the output power stage in reverse battery condition conductive through its body diode. The external load limits the current. Since no thermal protection works in reverse condition, special attention must be paid to the total power dissipation in the device. During the reverse battery event, the peak junction temperature shall remain safely below the maximum allowed junction temperature (T_{TSD_max}). Considering a voltage drop on the internal body diode of V_{F_max}= 0.7 V, the resulting power dissipation in the high side driver per output channel is P_D = 0.7 V * I_{LOAD}. The diagrams of $Z_{thj\text{-}a}$, reported in HSD datasheets, support the user to calculate the maximum affordable load current for a given PCB layout.

Note: That the intrinsic diode between cSPIN and VCC pin will be forward biased in reverse battery condition. The external sense resistor limits the current. A 2.7 kΩ sense resistor dissipates 125 mW about.

For what concerns the GND path of the device, the integrated VCC-GND clamping protection, which circuit behaves like a Zener diode will be forward biased in reverse battery condition. The power dissipation in the GND resistor is therefore determined by P_D= $(V_{bat\_rev}$ - 0.6 V$)^2/R_{GND}$.

The following figure provides an overview of pins' resulting voltage levels in a typical application schematic during reverse battery condition.

Figure 2. Voltage levels during reverse battery (diode + resistor protection)



Out = 5 W bulb

Out 0, 1, 2, 3 = 5 W bulb

Table 2. Reverse battery - voltage on pins (VNQ9080AJ)

Pin voltages [V] VND9xxxAJ		Pin voltages [V] µC	
V_{CC}	-16	VDD	-0.4
V_{FR}	-9	VFR_µC	-0.7
V_{INx}	-9	VIN0_µC	-0.7
V_{SEn}	-5	VSEn_µC	-0.7
V_{SELx}	-9	VSEL0_µC	-0.7
V_{CS}	-15	VCS_µC	-0.7
V_{OUTx}	-15.3		
V_{GND}	-15.4		

GND voltage on the device is dropping to the reverse battery voltage plus the forward voltage of the integrated V_{CC} to GND clamping circuit. The voltage of the cSPIN is dropping to the reverse battery voltage plus the forward voltage across the internal ESD protection diode. The maximum allowed DC output current on the cSPIN (I_{SENSE}) in reverse battery conditions is limited to 20 mA.Therefore the sense resistor R_{SENSE} must be chosen accordingly:

$R_{SENSE} > (|V_{BAT\_reverse} – 0.7\ V|) / 0.02\ A = 765\ \Omega$

For generic R_{SENSE} dimensioning rules, please refer to chapter 8.

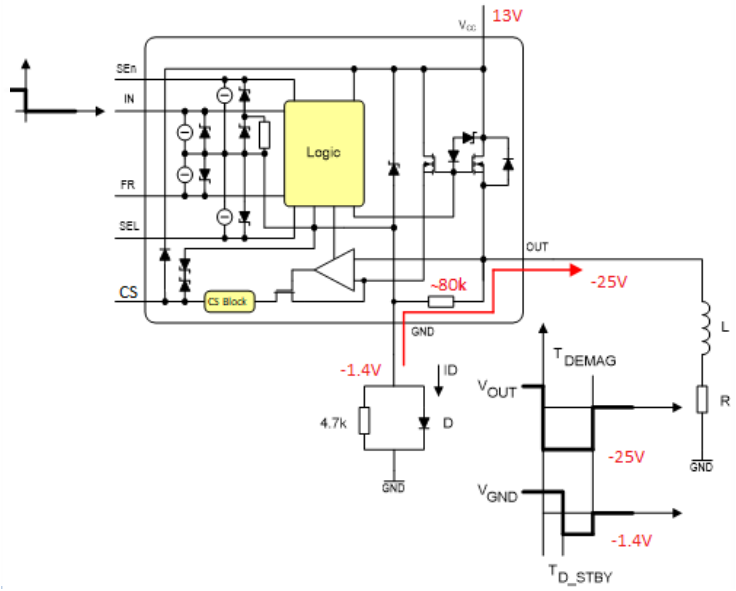
Due to the clamping voltage of the integrated ESD protection diodes on logic pins (faultrst, INx, SEL, SEn), the voltage on those pins is dropping to -9 V. Therefore a serial resistor is needed to limit the current and protect the I/O structure on microcontroller port pins and the high side driver's logic pins.

Furthermore, the ground network shall ensure the device works properly, driving inductive loads and not being damaged when submitted to ISO 7637-2:2011(E) pulse 1 test level IV pulses.

The diode at the GND terminal blocks the current through the forward-biased internal substrate diode of the HSD during reverse battery condition.

A resistor connected in parallel to the diode is recommended if the device drives a high inductive load with a demagnetization time longer than t_{D_STBY} (delay time for the device to reach standby mode after the last logic pin (INx, FaultRST, SEn, and SEL) is set low). The purpose of this resistor is to suppress a negative voltage on the GND pin during the standby mode if the demagnetization phase is still ongoing. Without this resistor, the low supply current in standby mode (I_{soff} = 0.5 µA max at 85 °C) allows the GND pin to be pulled negative by the demagnetization voltage on the output (~ (V_{cc} - V_{clamp}) ~ (13.5–38) V = -24.5 V) via an internal pull-down resistor (~80kΩ) on the output (see figure below).

Figure 3. Negative GND shift (T_{DEMAG} > t_{D_STBY}



If the negative ground shift exceeds the input high level threshold, the device leaves the standby mode and tends to turn on. The GND pin is immediately pulled high (~ 600 mV) by the increased supply current Ison so that the standby mode will be activated again after t_{D_STBY}. As a result, we could see short negative peaks on the GND pin with a period of t_{D_STBY} during the whole demagnetization phase. These peaks are not long enough to activate the HSD output, which means the device works safely even without the GND resistor. However, this resistor is still needed in order to suppress the described parasitic oscillations (if T_{DEMAG} > t_{D_STBY}).

The ground network can be safely shared amongst several different high side drivers, provided they are supplied from the same supply rail. Sharing the ground network is even possible among different HSDs when they are supplied from other supply rails. In this case, special precautionary measures must be applied (for details, refer to section 8.3). The presence of the ground network produces a shift (~ 600 mV) in the input threshold. This shift will not vary if more than one HSD shares the same diode/resistor. The diode at the GND terminal allows the high side driver to clamp positive ISO pulses above 38 V (the typical clamping voltage of the HSD). Negative ISO pulses still pass GND and logic terminals. The diode should withstand clamped ISO currents in case of positive ISO pulses and reverse voltages in negative ISO pulses.

Dimensioning of the GND diode:

The most severe positive “ISO 7637-2:2011 (E)” pulse we have to consider is testing pulse 2a at level III (55 V during 50 µs). This voltage is considered on top of the nominal supply voltage of 13.5 V–so the total voltage is 68.5 V. The M0-9 HSDs have a clamping voltage V_{clamp}= 38 V typical. In a specific device, the remaining voltage is 68.5 V - 38 V - 0.7 V = 29.8 V. The ISO pulse generator output impedance is 2 Ω. With this, the resulting peak current through the diode is 14.9A for a duration of 50 µs.

The most severe negative “ISO 7637-2:2011(E)” pulse we have to consider is test pulse 1 at level IV (-150 V@1 ms). This pulse is directly transferred to the GND pin via the internal clamping. So, the maximum peak reverse voltage of the diode should be at least 150 V.

The diode works in avalanche mode if the pulse level is above the rated reverse voltage.

The dimensioning the GND diode must fulfill the following:

- Max. peak forward current: 14.9 A for 50 µs for ISO 7637-2:2011(E).
- Max. reverse voltage: -150V for ISO 7637-2:2011(E).

Note: As seen from the above explanation, the HSD with a diode protection at the GND pin does not clamp negative ISO pulses on the supply line. Therefore, an appropriate serial protection resistor should be used between µC and HSD (typically 15 kΩ). The resistor value should be calculated according to the maximum injected current to the I/O pin of the used microcontroller and to the maximum input sink current of the HSD.

Note: Diode parameters can be lower if an external clamping circuitry is used (for example, HSD module is supplied from a protected power supply line).

Dimensioning of the GND resistor:

The GND resistor is recommended in case of a high inductive load. To determine if the resistor is needed or not, we need to know the demagnetization time (T_{DEMAG}). The resistor is recommended if T_{DEMAG} is higher than the standby delay time (t_{D_STBY}). A typical t_{D_STBY} value of 350 µs is considered in this comparison.

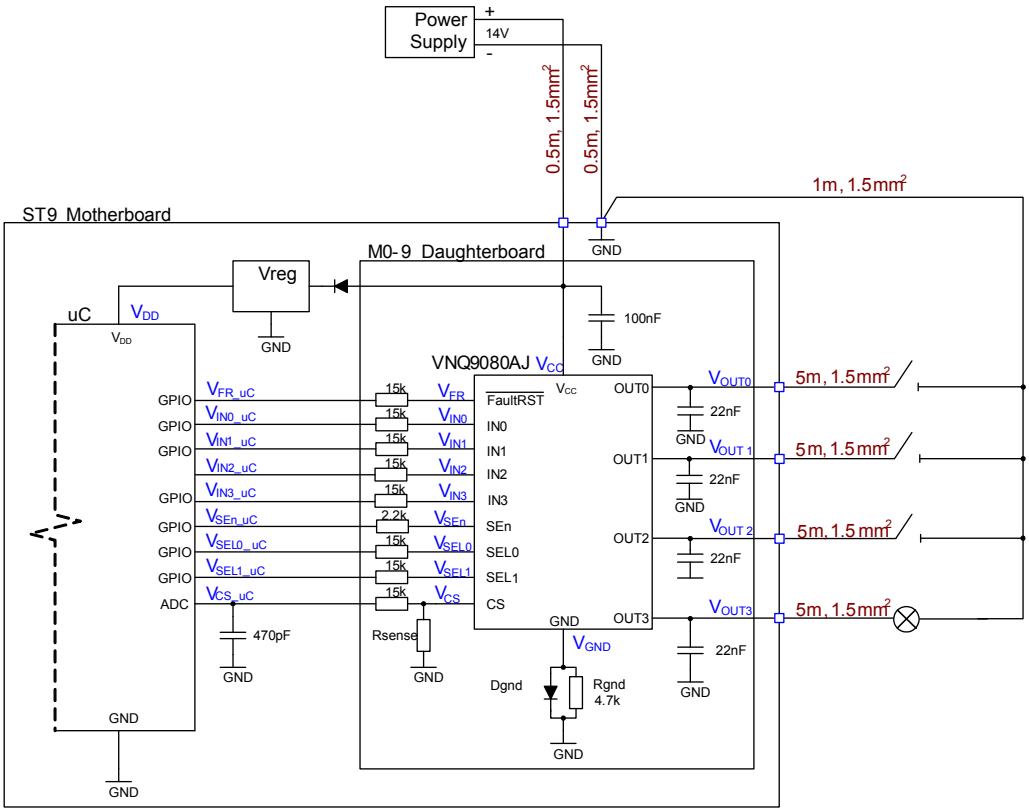
T_{DEMAG} can determined by either measurement (Figure 5, R_{GND} = 4.7 kΩ, load: relay 270 mH / 90 Ω alternatively bulb on a typical wire harness with 6 µH stray inductance) or calculation, using:

$$V_{DEMAG} = V_{BAT} - V_{CLAMP} \quad (3)$$

$$T_{DEMAG} = \frac{L}{R} \cdot ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) \quad (4)$$

The experimental trial, whose setup is shown in the figure below, highlights:

Figure 4. GND resistor requirements (inductive load) – test setup

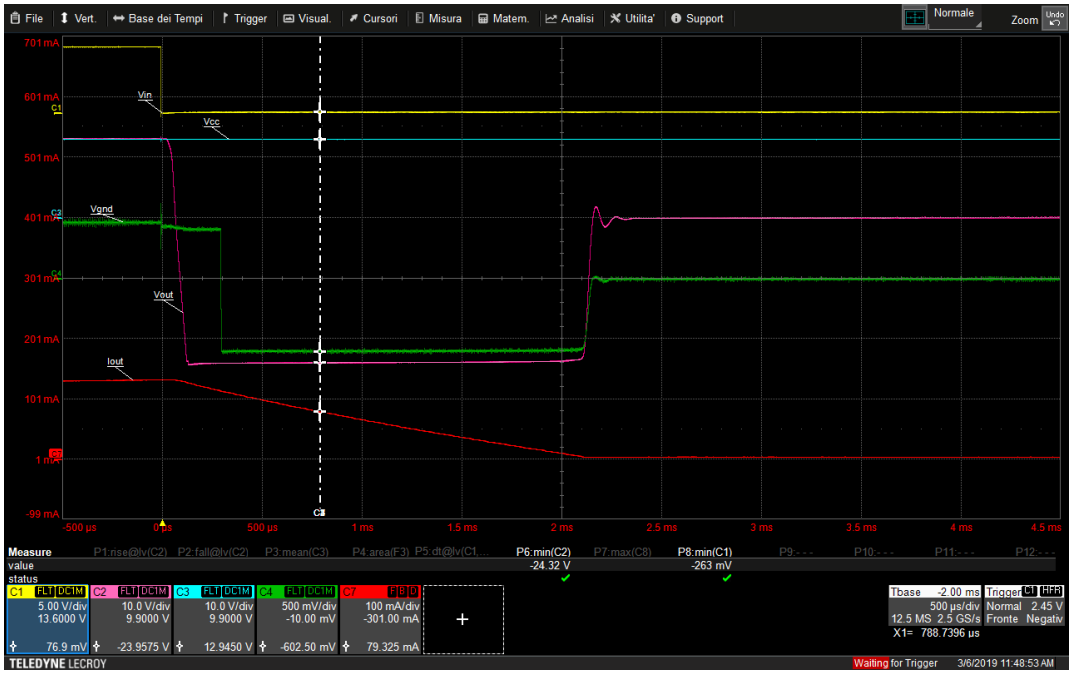


- The operation with a high inductivity load (T_{DEMAG} > t_{d_stby}) is correct even without the GND resistor (only the diode), knowing that the device GND pin oscillation with a period of t_{d_stby} may be present (see Figure 5. Measurement example (T_{DEMAG} > t_{D_STBY}) without GND resistor).

- The 4.7 kΩ appears to be the best compromise between the GND shift safety and power dissipation during static reverse battery condition (~50 mW) (see Figure 6. Measurement example (T_{DEMAG} > t_{D_STBY}) with 4.7 kW GND resistor)

Figure 5. Measurement example (T_{DEMAG} > t_{D_STBY}) without GND resistor

Figure 6. Measurement example (T_{DEMAG} > t_{D_STBY}) with 4.7 kW GND resistor



The value of the resistor should be low enough to be sure that the negative voltage at the GND pin is suppressed as much as necessary to keep the device off. This means the V_{GND} should be kept above -1.3 V.

The minimum resistor value is determined by the maximum DC reverse ground pin current of the HSD in reverse battery condition:

$$R_{GND} \geq \frac{V_{BAT(reverse)}}{I_{GND(reverse)max}\frac{16V}{200mA}} \quad (5)$$

In order to keep the power dissipation on the resistor during reverse battery condition as low as possible, it is recommended to select the resistor value close to the maximum value (4.7 k).

(6)

Summary–dimensioning of the resistor:

Resistor recommended if: $T_{DEMAG} > t_{D\_STBY}$.

Resistance: 4.7 kΩ (or lower).

Voltage capability: Min. 150 V (ISO 7637:2-2011(E) pulse 1 at level IV)

Power dissipation (reverse batt.): Min. 50 mW (4.7 kΩ)

Example with relay coil:

In case of a relay coil connected supposing the following conditions:

Load resistance: R_{LOAD} = 90 Ω

Wiring inductances: L = 270 mH

Initial current I_0: 0.14 A

Applying Eq. (4), yields a T_{DEMAG} = 1.0 ms > t_{D_STBY}

Example with resistive load with long wire harness:

In case of a resistive load connected via long wires, supposing following conditions:

Load resistance: R_{LOAD} = 5 Ω

Wiring inductances: L = 5 µH (in case of very long cabling)

Initial current I_0: 2.7 A

Applying Eq. (4), yields a T_{DEMAG} = 0.4 µs << $t_{D\_STBY\_min}$

Example with short circuit with long wire harness:

In case of a resistive load connected via long wires, supposing following conditions:

Load resistance: R_{LOAD} = 100 mΩ

Wiring inductances: L = 5 µH (in case of very long cabling)

Initial current I_0: 130 A (I_{LIMH_max}-lowest ohmic monolithic HSD VN7010AJ)

Applying Eq. (4), yields a T_{DEMAG} = 18 µs << $t_{D\_STBY\_min}$.

2.2.3 N-Channel MOSFET in GND line

Compared to the solutions described in the previous chapters, reverse polarity protection with MOSFETs offers two main advantages: Lower power losses and minimal voltage drop. Generally, the MOSFET´s body diode is oriented in the direction of normal current flow. When the battery is installed incorrectly, the N-MOS (P-MOS) FET's gate voltage is low (high), preventing it from turning ON.

When the battery is correctly installed, and the portable equipment is powered, the N-MOS (P-MOS) FET's gate voltage is taken high (low), and its channel shorts out the diode.

A voltage drop of $R_{DS(on)} \times I_{son}$ is seen in the ground return path when using the NMOS FET. A voltage drop of $R_{DS(on)} \times I_{load}$ is seen in the power path when using the PMOS FET. In the past, the primary disadvantage of these circuits has been the high cost of low $R_{DS(on)}$, low-threshold voltage FETs. However, advances in semiconductor processing have resulted in FETs that provide minimal drops in small packages.

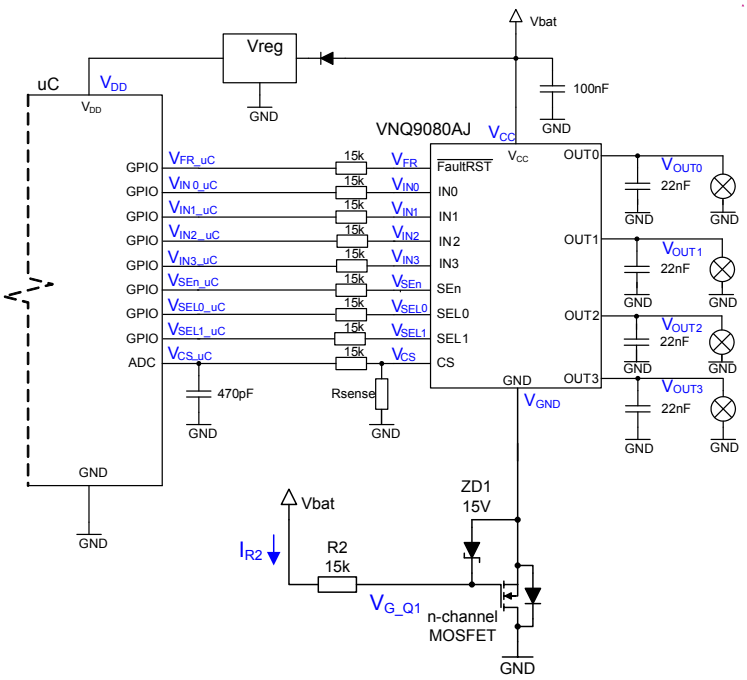
The N-channel MOSFET has its gate driven directly by the battery voltage, and its drain connected to the ground. In normal condition, it is ON while a reverse battery event switches it OFF (because V_{GS} =< 0) and protects the HSD.

The Figure 7. Generic schematic and test setup with N-channel MOSFET in GND line (VNQ9080AJ) reports a generic schematic with an N-channel MOSFET configuration. In this case, like for the solution with diode ||resistor network in the GND line, the HSD´s output stage body diode is forward biased and therefore is conducting during the reverse battery. The external load limits the current.

Since no thermal protection works in reverse condition, special care must be taken on the total power dissipation in the device. During the reverse battery event, the peak junction temperature shall remain safely below the maximum allowed junction temperature (T_{TSD_max}). Considering a voltage drop on the internal body diode of V_{F_max} = 0.7 V, the resulting power dissipation in the HSD per output channel is P_D = 0.7 V·I_{LOAD}.

Z_{thj-a} diagrams reported in HSD datasheets help the user to calculate the maximum affordable load current for a given PCB layout.

Figure 7. Generic schematic and test setup with N-channel MOSFET in GND line (VNQ9080AJ)



The Table 3. Static reverse battery - voltage on pins reports the measurement results VNQ9080AJ: GND voltage on the device is dropped to the reverse battery voltage plus the forward voltage of the integrated V_{CC} to GND clamping circuit (substrate diode). Voltage on the cSPIN is dropped to the reverse battery voltage plus the forward voltage across the internal ESD protection diode. The maximum allowed DC output current on cSPIN (I_{SENSE}) in reverse battery conditions is limited to 20 mA. Therefore, the sense resistor R_{SENSE} must be chosen accordingly:

$R_{SENSE} > (|V_{BAT\_reverse} - 0.7\ V|) / 0.02\ A = 765\ \Omega$

Measured values (VNQ9080AJ):

Table 3. Static reverse battery - voltage on pins

	Reverse battery (V_{CC} = -16 V)
V_{CC} [V]	-16
V_{GND} [V]	-15.3
V_{G_Q1} [V]	-15.9
I_{R2} [µA]	-6.7

Note: For the other voltages such as: VIN, VSEL; VFRESET; VCS_EN, refer to Table 2. Reverse battery - voltage on pins (VNQ9080AJ).

For generic R_{SENSE} dimensioning rules, please refer to chapter 8.

Due to the clamping voltage of the integrated ESD protection diodes on logic pins (FaultRST, INx, SELx) the voltage on those pins is dropping to -9 V about; while, since the clamping voltage of SEn pin is higher, the voltage on SEn pin is dropping to -5 V about. Therefore, a serial resistor is needed to limit the current and protect the I/O structure on microcontroller port pins and the high side driver´s logic pins. The gate voltage of the N-channel MOSFET is pulled down to the reverse battery voltage, ensuring the MOSFET is fully off. In normal operation only the leakage current of ZD1 Zener diode is flowing through R2 to GND. In order to minimize this current even at higher supply voltages, a diode with a higher Zener voltage (that is, 18 V) might be chosen. The Zener voltage should be anyway always lower than the maximum rated gate source voltage V_{gs} of the n-channel MOSFET.

The resistor R2 limits the current through the Zener diode at supply voltages higher than the Zener voltage and limits the charging/discharging current of the gate. In addition, the resistor R2 together with the gate capacitance of the n-channel MOSFET determines the turn-off time when exposed to fast negative transients or abrupt reverse polarity according to the LV 124: 2009-10 standard. The 15kΩ as demonstrated by the experiment reported below appears to be a good compromise between minimizing the charging/discharging current and ensuring a fast turn-off time.

The breakdown voltage BVDSS of the N-channel MOSFET should either be higher than the maximum negative transient peak voltage of ISO 7637:2-2011(E), or the energy capability of the n-channel MOSFET in avalanche must be high enough to sustain the transient pulse energy.

The figure below shows an example of an abrupt reverse battery test changing the battery supply's polarity from 10.8 V to -4 V within a few us. The test setup used a 100 V/80 mΩ n-channel MOSFET with a gate resistor R2=15 kΩ.

The N-channel MOSFET can turn-off within about 10 µs. During this time, the current flowing through the device ground pin remains low. The power dissipation in the HSD is negligible.

Figure 8. Reverse battery test VNQ9080AJ

Note: Reverse battery test VNQ9080AJ (10.8 V ® - 4 V, 80 mΩ, R2=15 kW) as per LV 124: 2009-10 standard.

2.3 Reverse battery protection of HSDs with reverse turn-on feature

A new feature has been introduced in the M0-9 HSD family, it is called “reverse turn ON” and it operates when an inverse polarity is applied on battery terminals. The goal is to avoid high power dissipation. In fact, without the reverse battery block, when the battery is installed backwards, the device would conduct through the body diode of the power MOSFET with the current only limited by the external load and line impedance. The function of the reverse battery block is too turn-on the power MOSFET during the reverse battery mode. The circuit used to provide the protection, is present in all channels and everyone is connected to sense enable (SE_n) and INPUT 0 (IN0) pins. The path to module ground is provided by means the protection resistances R_{IN0} (15 kΩ) and R_{SEn} (2.2 kΩ), and the protection diode of the relative out pin of the microcontroller (see application schematic in figure 9). The use of 2.2 kΩ on the SEn pin is necessary for the correct operation of the block; otherwise, it will not be possible to have enough voltage on the power MOSFET gate and turn it on. R_{SEn} value has a direct impact on device functionality during reverse battery condition; the V_{GS} is acceptable (around 9.1 V) with a maximum R_{SEn} = 2.2 kΩ. As soon as the R_{SEn} value increases, the V_{GS} decreases, leading to a not full RON_rev . Looking only at reverse battery functionality, there is no minimum value for R_{SEn}. Nevertheless, it must be considered that all input pins must be protected in terms of maximum current (see figure 9) by means of a resistor, so a R_{prot} is still required. The protection on gnd line (D_{gnd} //4.7 kΩ) has the function to optimize the behavior of the reverse battery. In the specification, at V_{CC}= -16 V I=I_{nom} T= 25 °C, the Vgs (of the power MOS) will be good enough to guarantee a typical value of RON_rev close to Ron.

Looking at the application schematic shown in figure 9, a Schottky diode and a resistor have been also added to protect the microcontroller during negative pulse transients, ISO pulse 1, according to ISO7637-2:2011 (E).

During ISO pulse 1, a V = -140V voltage is applied on SEn pin that, considering R_{SEn} = 2.2 kΩ, result in a 65 mA current flowing through the ESD diode into the microcontroller, which is considered a high current from the application standpoint.

In the end, to protect the microcontroller during negative pulses a Schottky diode and a 50 Ω resistor must be added.

By doing that, in case of ISO pulse 1 is applied, the current flows through the diode instead of the microcontroller; the purpose of the 50Ω resistor is to limit the current injection from the microcontroller.

2.3.1 Diode + resistor in GND line

The reverse battery protection is applied to the GND terminal of the driver. This kind of protection is necessary to protect the device internal logic circuitry in case of reverse battery condition. No thermal protection works in reverse condition, but, since the current is limited by the external load and because the output MOSFET turns on, no special attention must be paid to the total power dissipation in the device.

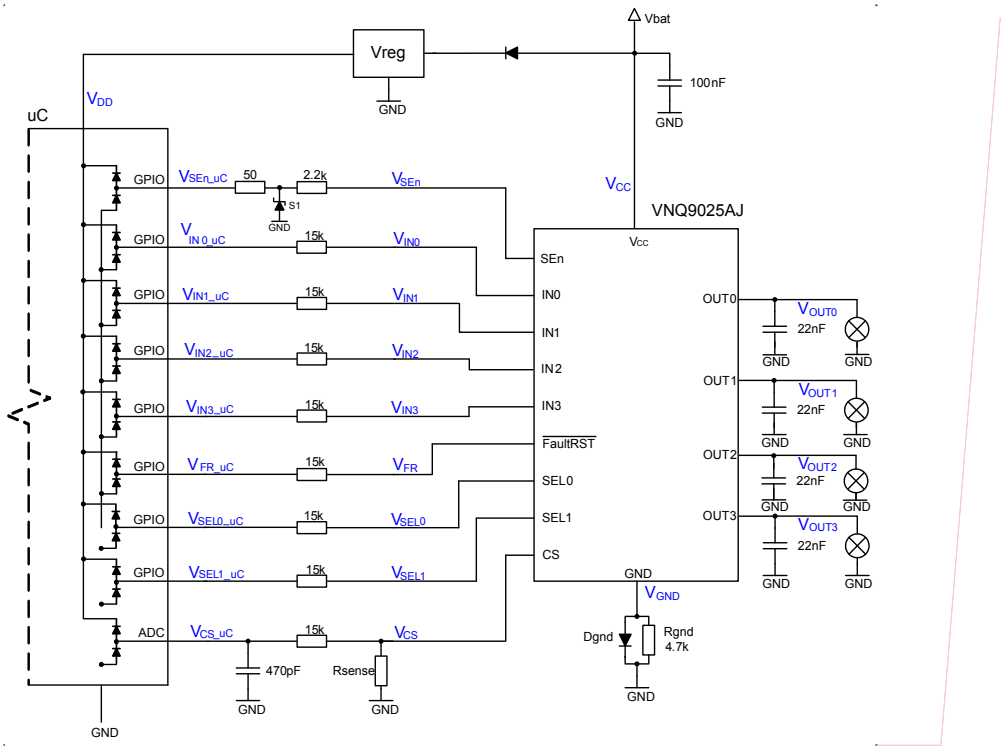
For diode and resistor dimensioning calculations, refer to section 3.2.2.

A special comment is related to the ground resistor in parallel with the diode. This resistor is mandatory for correct operation of the reverse turn ON feature. So, it applies not only in the case or inductive loads as described in Section 2.2.2: Diode + resistor in GND line, but for each type of load (capacitive, resistive, inductive).

The suggested value is 4.7 kΩ, following the same recommendation of Section 2.2.2: Diode + resistor in GND line.

Due to the reverse turn ON feature the voltage levels on device pins are different from the ones of HSDs with reverse turn ON. In particular, the V_{OUTx} voltage is quite close to the V_{CC} voltage since the output MOSFET is turned ON. The following figure provides an overview of the resulting voltage levels on pins in a typical application schematic during reverse battery condition.

Figure 9. Voltage levels during reverse battery (diode + resistor protection)



Out = 27 W bulb

Out 0, 1, 2, 3 = 27 W bulb

Table 4. Reverse battery - voltage on pins (VNQ9025AJ)

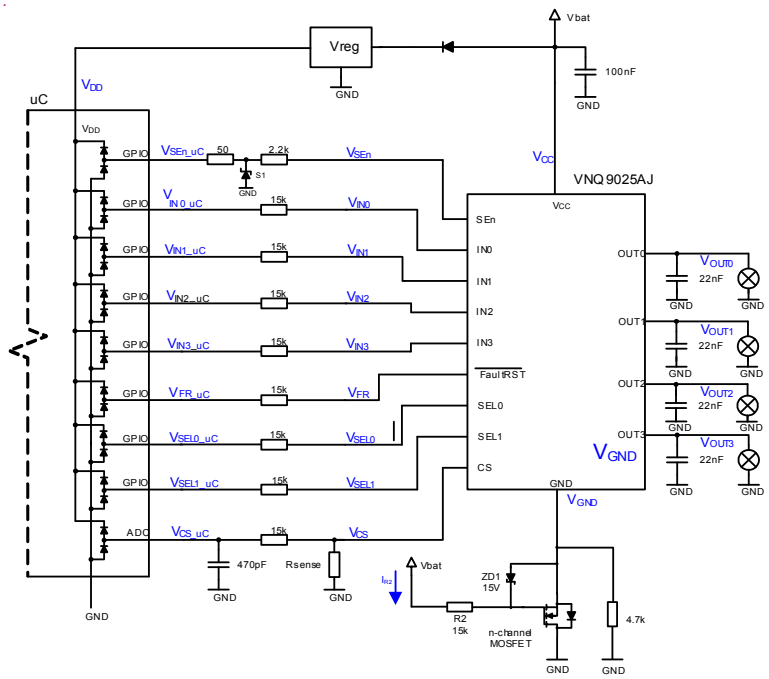
Pin voltages [V] VNQ9025AJ		Pin voltages [V] µC	
V_{CC}	-16	V_{DD}	-0.4
V_{FR}	-9	$V_{FR\_µC}$	-0.7
V_{INx}	-9	$V_{IN0\_µC}$	-0.7
V_{SEn}	-5	$V_{SEn\_µC}$	-0.7
V_{SELx}	-9	$V_{SEL0\_µC}$	-0.7
V_{CS}	-15	$V_{CS\_µC}$	-0.7
V_{OUTx}	-15.9		
V_{GND}	-15.4		

2.3.2 N-Channel MOSFET in GND line

The comments in Section 2.2.3: N-Channel MOSFET in GND line applies also for this case with the following differences:

- This kind of protection is necessary to protect only the device internal logic circuitry. In reverse battery condition the output MOSFET turns on, so no special attention must be paid to the total power dissipation in the device.
- It is mandatory a resistor in parallel to the N-Channel MOSFET. This is needed to allow the correct operation of the internal Reverse turn-on block. The suggested value is 4.7 kΩ, following the same recommendation of Section 2.2.2: Diode + resistor in GND line.

Figure 10. Generic schematic and test setup with N-channel MOSFET in GND line (VNQ9025AJ)



3 Protection against battery transients

3.1 Introduction on automotive electrical hazards

The automotive environment is the source of many electrical hazards. These hazards, such as electromagnetic interference, electrostatic discharges and other electrical disturbances are generated by various accessories like ignition, relay contacts, alternators, injectors, SMPS (that is, HID front lights) and other accessories. Because electronic modules are sensitive to electromagnetic disturbances (EMI), electrostatic discharges (ESD) and other electrical disturbances, caution must be taken wherever electronic modules are used in the automotive environment.

These hazards can occur directly in the wiring harness in case of conduct hazards, or be applied indirectly to the electronic modules by radiation. These generated hazards can impact the electronics in two ways - either on the data lines or on the supply rail wires, depending on the environment.

Several standards have been produced to model the electrical hazards that are currently found in automobiles. As a result, manufacturers and suppliers have to consider these standards and have to add protection devices to their modules to fulfill the major obligations imposed by these standards.

The chapter deals with the robustness of M0-9 devices submitted to ISO7637-2:2011 disturbances on the battery line and mounted in the typical application scheme.

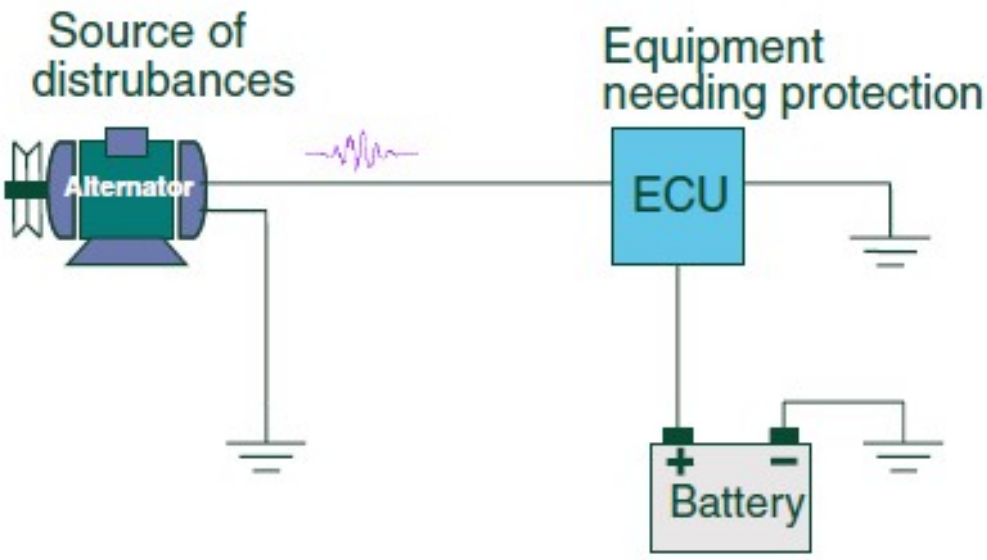
3.2 Source of hazard on automotive

3.2.1 Conducted hazards

These hazards occur directly in the cable harness. They are generated by inductive loads like electro-valves, solenoids, alternators, etc.

The schematic in the figure below a typical configuration

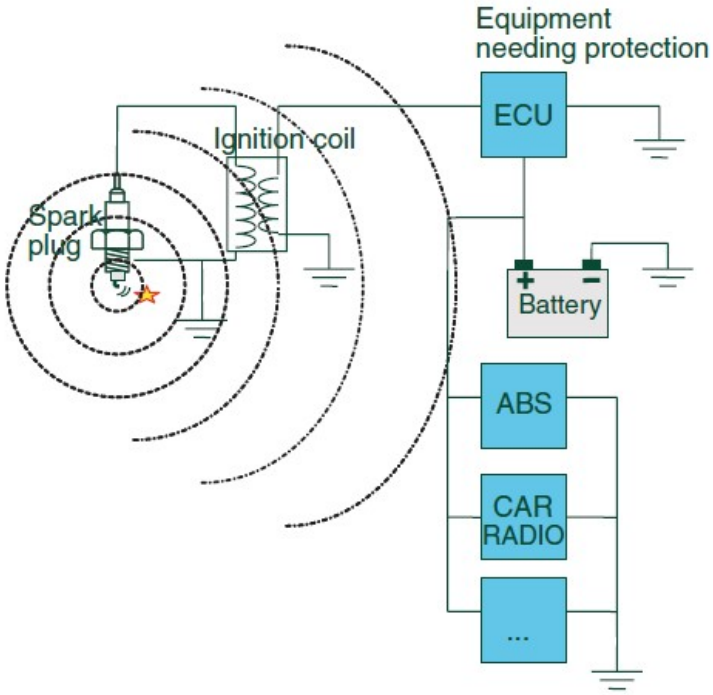
Figure 11. Conducted hazards



These hazards are generated by high current switching like relay contact, high current MOS or IGBT switches, ignition systems, etc. The electromagnetic field generated by these circuits directly affects lines or modules near the source of the electromagnetic radiation.

The schematic diagram in the following figure indicates how electromagnetic radiation creates such hazards as electromagnetic interference in electronic modules.

Figure 12. **Radiated hazards**



3.3 Propagation of electrical hazards on the supply rail

Transients that are generated on the supply rail range mainly concern ISO7637-2 and ISO10605 standards.

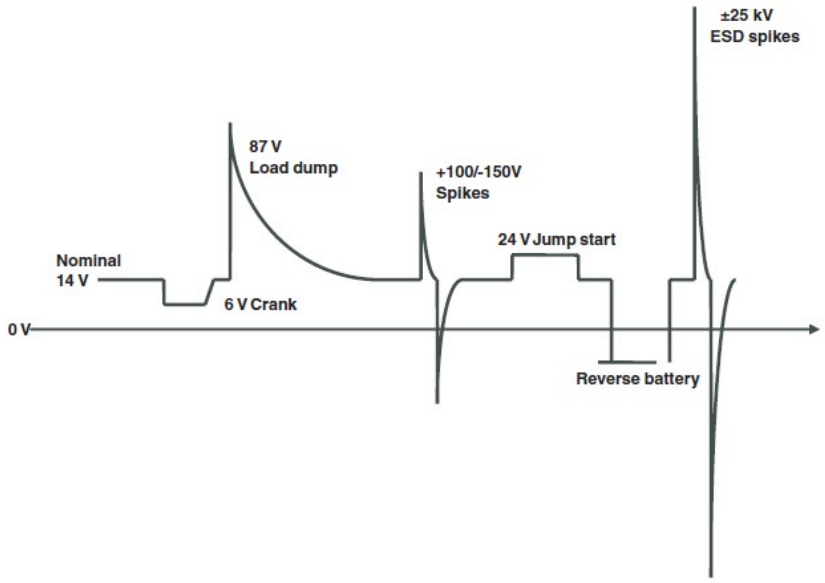
The most energetic transients are those resulting from load-dump and jump-start. But all other hazards may affect the normal operation of electronic modules.

The load-dump is caused by the discharged battery being disconnected from the alternator while the alternator is generating charging current. This transient can last 400 ms and the equivalent generator internal resistance is specified as 0.5 Ω minimum to 4 Ω maximum.

According to the ISO 7637-2 standard, the “positive spikes” are due to supply sudden interruption of currents in a device connected in parallel with the DUT due to the inductance of the wiring harness, while the “negative spikes” are due to a supply disconnection from inductive loads.

This chapter deals with voltage transient pulses, detailed on the ISO 7637-2 standard.

Figure 13. Various surges occurring in the supply rail



3.4 Standard for the protection of automotive electronics

All the hazards indicated above are described by several standards bodies such as the society of automobile engineers (SAE), the automotive electronic council (AEC) and the International standard organization (ISO).

Since the ISO7637 are the most important automotive standards regarding electrical hazards transient, this document mainly concerns the cases considering such standard:

Below the electrical characteristics of ISO 7637-2 2011 edition;

Table 5. ISO 7637-2 - electrical transient conduction along supply line

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S (1)		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4 (2)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						

Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	U_S (1)		min	max	
Test B		35 V	5 pulses	1 min		400 ms, 2 Ω

1. *U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.*
2. *Test pulse from ISO 7637-2:2004(E).*
3. *With 35 V external suppressor referred to ground (-40°C < T_j < 150 °C).*

3.5 Basic application schematic to protect a M09 standard monolithic high side driver

The hardware design techniques used for an application establish the baseline immunity performance. The purpose of hardware techniques is to protect the device from performance degradation or long-term reliability problems.

Below reported, the STMicroelectronics application proposal, for protecting monolithic HSDs under the common stress event mentioned in ISO 7637-2 edition 2011.

To provide these electronic safeguards, manufacturers typically chose either a diode, or resistor or capacitor for protecting both data-line and supply rails.

Components used to suppress or control transients, as well as their implementation details, are described in the next paragraph, providing a basic description of how the most typically used components are employed in low-cost designs for achieving the desired level of transient immunity.

Components used to suppress or control transients can be grouped into two main categories:

- Components that shunt transient currents (voltage limiters)
- Components that block transient currents (current limiters)

Note: That depending on the rise time (frequency bandwidth) of the transient, a component may function as either a shunt or a block. For instance, at a slow rise time (low frequency bandwidth) an inductor has little impedance (a shunt). At faster rise times (higher frequency bandwidth), an inductor will have a greater impedance (a block). As a result, transient suppression components must be carefully selected for the optimal operating conditions. The actual performance of the component in the application depends on the frequency-based characteristics of the component and the board layout.

Resistors:

Series resistance between two nodes can provide inexpensive and effective transient protection blocking or limiting transients with frequency-independent resistance. Resistance can be used to create low-pass filters and to decouple power domains. Series resistance is primarily suited to protecting digital or analog signals that carry low currents and can accept a modest voltage drop (across the series resistance).

Capacitors:

Capacitors are used in a variety of transient protection roles. They can be used to filter the high frequency pulses produced by an ESD event. They also provide switching current to ICs and serve as energy storage bins that limit voltage variation.

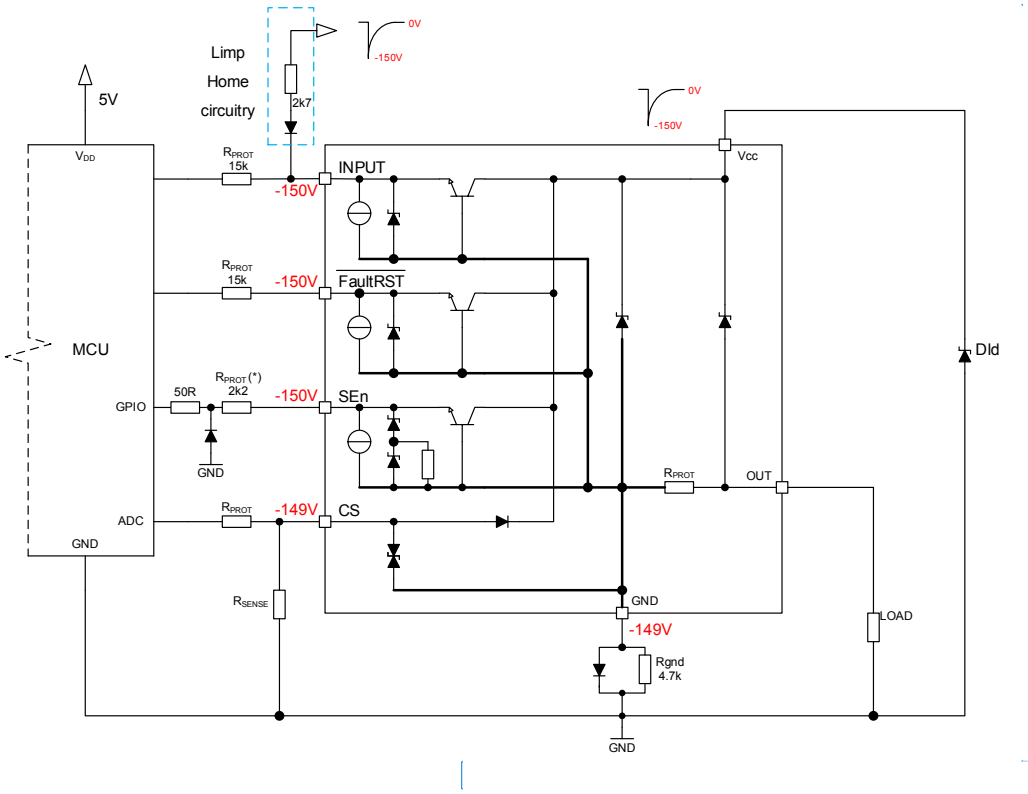
In either role, the capacitor can be used to effectively shunt fast transients of limited energy, such as ESD. Important characteristics to consider, when selecting capacitors, are the maximum DC voltage rating, parasitic inductance, parasitic resistance, and overvoltage failure mechanism.

3.5.1 Components dimensioning

Because the reverse battery event, the device needs to be protected by an external diode plus a resistor network connected in series to the ground pin. In this chapter, the ground network is dimensioned referring to the ISO7637-2 test pulse 1 and 2.

Due to the presence of such a protection network, the negative ISO pulse 1 level IV (-150 V @ 1 ms) is directly transferred to the GND pin via the internal clamping. Then, the HSD with a diode protection at the GND pin does not clamp negative ISO pulses on the supply line. Moreover, the internal parasitic structures of I/O pins, link these pins directly to v_{batt} and then to -150 V (see the figure below). Therefore, an appropriate serial protection resistor should be used between µC and HSD to limit the current injected into these pins.

Figure 14. Internal structures involved during application of ISO 7637-2 pulse 1 in a monolithic HSD and indication of pin voltages



Note: For VNQ9080AJ the R_{prot} on SEn pin is applicable to 15 k without diode to GND.

Besides, since the device input may be driven independently from the µC by a separate hardware, which is supplied directly from the battery, it is mandatory to decouple the signal coming from the µC to the one coming from the limp home circuitry, to avoid any backward supply of one circuit versus the other one. The decoupling is ensured by a signal diode, placed in series to the limp home path connected to the device input.

Dimensioning of the series resistors on the I/O line:

The resistor value should be calculated according to the maximum injected current to the I/O pin of the used microcontroller. That value can be assumed to be about 10 mA. So that, the resistors value should be at least 15 kΩ (150 V/10 mA):

Ri ≥ 15 kΩ

Specific circuitry is applied on SEn pin - Schottky diode and a resistor have been added to protect the microcontroller during negative pulse transients, ISO pulse 1, according to ISO7637-2:2011 (E).

During pulse 1, a V = -150 V voltage is applied on SEn pin that, considering R_{SEn} = 2.2 kΩ, result in a ~65 mA current flowing through the ESD diode into the microcontroller, which is considered a high current from the application standpoint.

To protect the microcontroller during negative pulses a Schottky diode and a 50 Ω resistor is added. By doing that, in case of ISO pulse 1 is applied, the current flows through the diode instead of the microcontroller; the purpose of the 50 Ω resistor is to limit the current injection from the microcontroller.

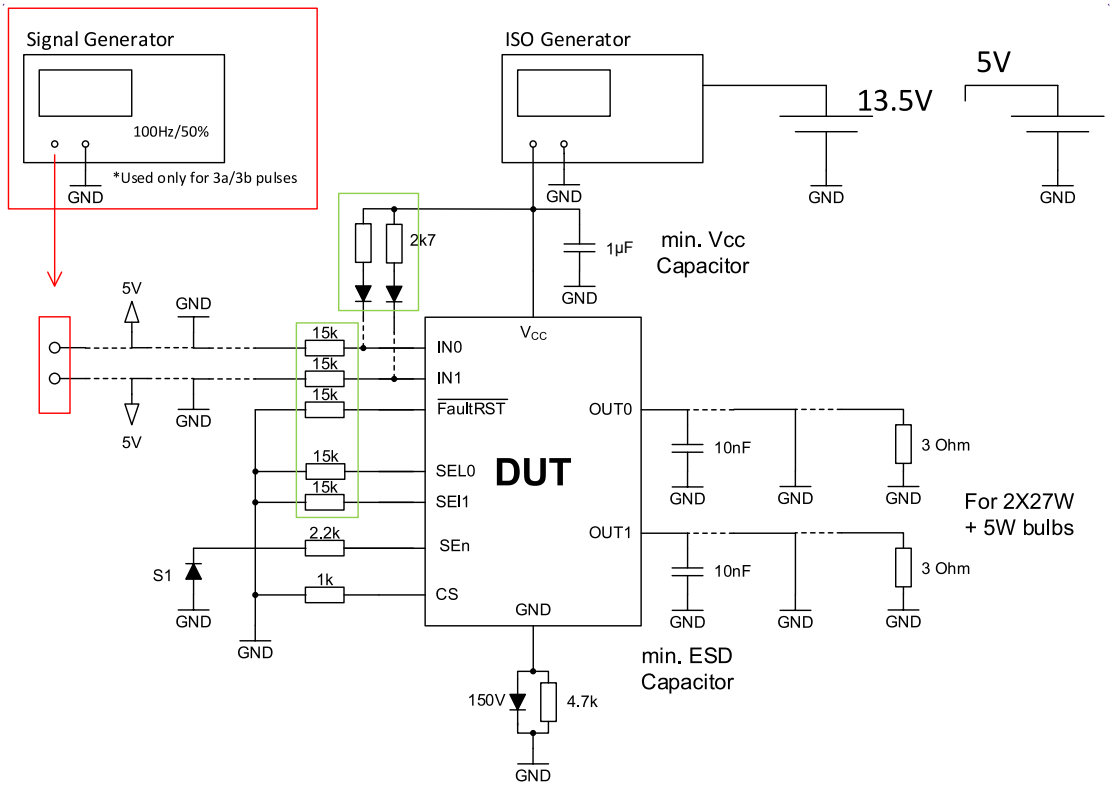
The basic application schematic has been validated to be reliable with the following stress test, based on the ISO7637-2 standard edition 2011, in different operative conditions:

- ISO n1 (2 msec/10 Ω, 5 K pulses);
  Class C must be complied (full operational after each pulse).
- ISO n2a (50 µsec/2 Ω, 5 K pulses);
  Class C must be complied (full operational after each pulse).
- ISO n3a (0.1 µsec/50 Ω, 1h);
  Class B must be complied (full operational even during pulse exposure).

- ISO n3b (0.1 µsec/50 Ω, 1h);
  Class B must be complied (full operational even during pulse exposure).

Basic test setup for ISO 7637-2 pulses applied to VND9025AJ (and the other device with reverse turn-on feature; for the VNQ9080Aj is not needed S1)

Figure 15. Basic test setup for ISO 7637-2



Note: Test set-up for ISO 7637-2 pulses applied to VND9025AJ (and the other device with reverse turn on feature; for the VNQ9080Aj is not needed S1).

Below reported the operative conditions (given for VND9025AJ):

- Applicative configuration with device in **OFF** state and resistive load;
- Applicative configuration with device in **ON** state and resistive load;
- Device naked in **OFF** state.

After test exposure device results are given in the table below (here the most severe pulses are reported):

Table 6. ISO 7637-2 2011 tests and results on M09 HSDs

Test pulse				
ISO 7637-2:2011	1 level III	2a level III	3a level IV	3b level IV
Result (FPSC)	Status II	Status II	Status II	Status II
	Status II: The function does not perform as designed during the test but returns automatically to normal operation after the test Function performed status classification (FPSC) according to ISO 7637-1			

Moreover, M0-9 HSDs pass the load dump clamped pulse test (class C according to Table 6. ISO 7637-2 2011 tests and results on M09 HSDs criteria) relevant to the standard ISO 16750-2:2010 (E) (pulse with 35 V centralized load dump suppressor).

4 Usage / handling of fault reset and standby

As already introduced with M0-7 products, the new M0-9 HSDs family shares the same protection management concept, providing both auto-restart and latch-off, in order to provide maximum flexibility:

- Latch-off functionality (at least one generic input pin high, that is SEn, SELx, FaultRST or one of the INx pin):
  - FaultRST pin = low or left open:
    The drivers will behave like M0-5 enhanced devices (autorestart in case of overload or thermal shutdown).
  - FaultRST pin = high:
    The drivers will latch-off in case of power limitation or thermal shutdown. In order to unlatch the channel(s), a low level pulse on FaultRST pin is required for minimum duration of t_{LATCH_RST}. This time ensure the device latches-off only if required and not accidentally.
  - Stand-by mode (all generic input pins low, that is SEn, SELx, FaultRST and all INx pins):
    - FaultRST pin = low or left open:
      A permanent low level on FaultRST pin, SEn pin, SELx pin and all INx pins disables all outputs and sets the devices in standby mode after elapse of standby mode blanking time t_{D_STBY} (open load diagnostic in off-state is disabled).

4.1 Latch-off functionality

The latch-off functionality is available when the FaultRST pin (logic input) is set high. This pin is common for all device channels.

In case an overload occurs, the related channel is automatically latched-off at the first intervention of either power limitation or thermal shutdown. The latch condition is indicated by V_{SENSEH} level on the related multi sense pin (only if SEn pin is set high and the related channel is selected through the sense selector pin combination, SELx).

All latched channels can be restarted by setting the FaultRST pin low for a minimum time of t_{LATCH_RST} (> 3 µs).

A graphical explanation of the latch-off functionality can be seen in the figure below:

Figure 16. Latch-off mode - intermittent short circuit

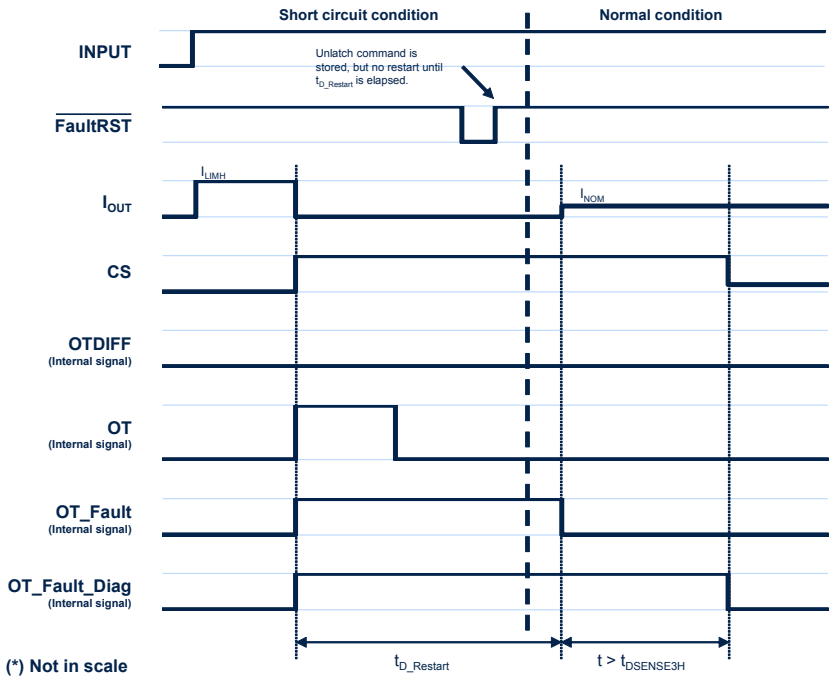


Figure 17. **Auto-restart mode - intermittent short circuit**

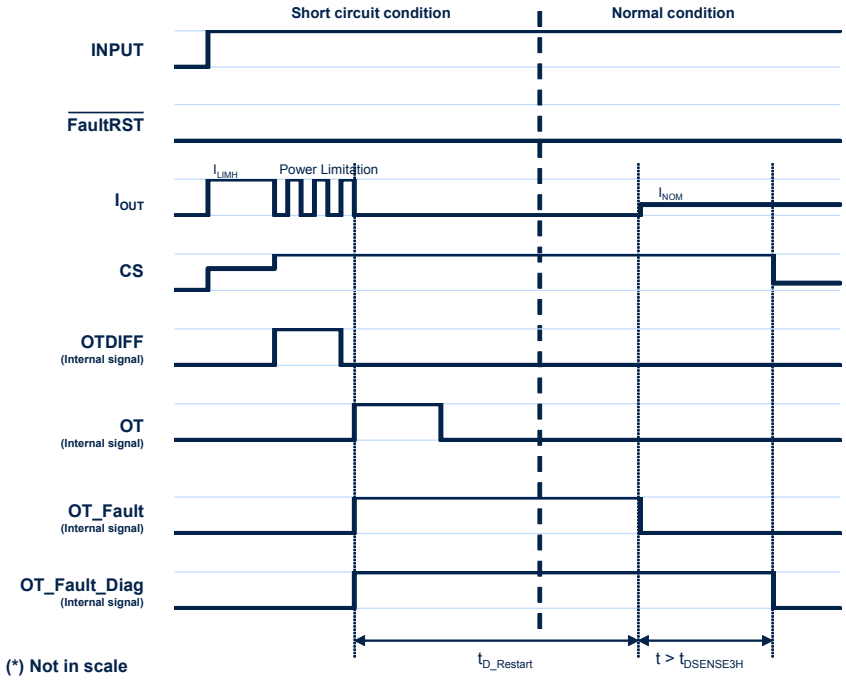
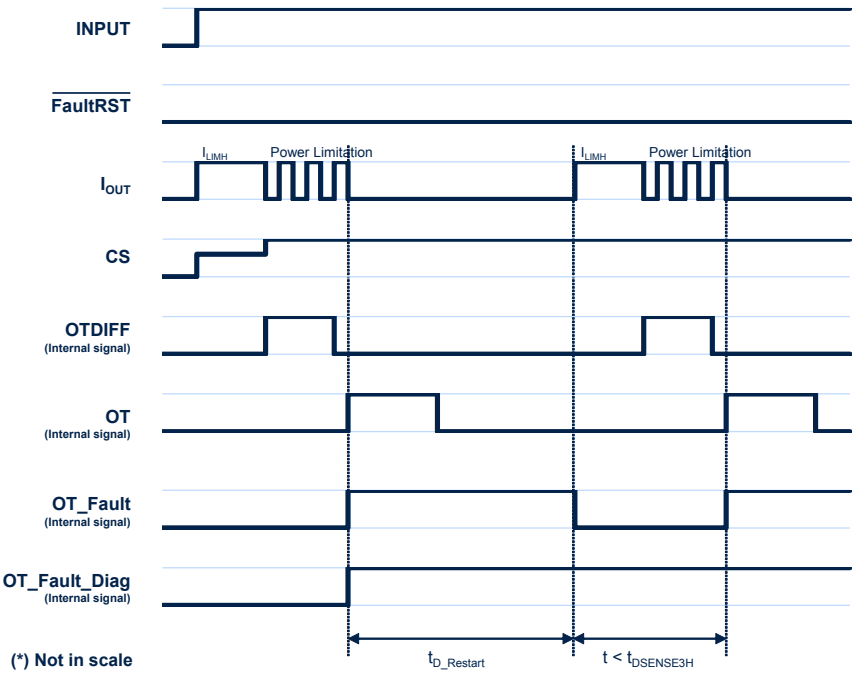


Figure 18. **Auto-restart mode - permanent short circuit**



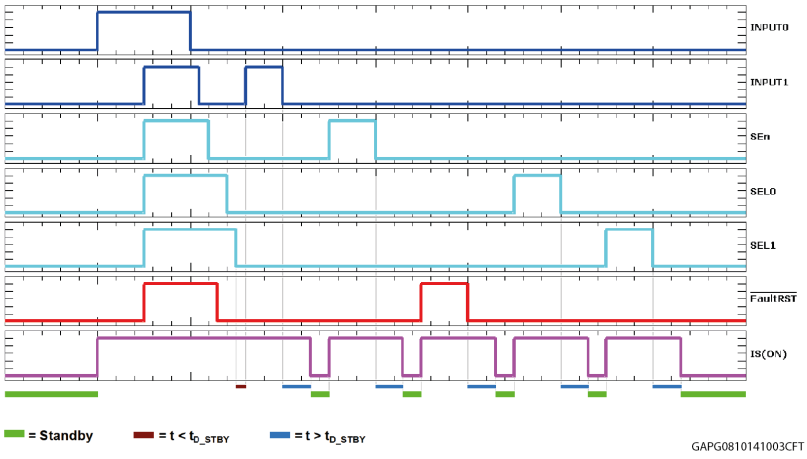
4.2 Standby mode

The standby mode is available when the FaultRST pin, SEn pin, SELx pin and all INx pins are set low and kept in this condition for at least a typical time of t_{D_STBY} = 300 µs. This time, t_{D_STBY}, has been introduced to avoid entering the standby condition in case all generic input pins are low during a commutation, so no accidental standby can occur (see *Figure 19*). In this condition the supply current drops down to 0.5 µA (max @25 °C).

As soon as the device enters the standby mode, all diagnostic latches are reset. This is also caused by the fact that the FaultRST pin is set low for a time $t_{D\_STBY} > t_{LATCH\_RST}$.

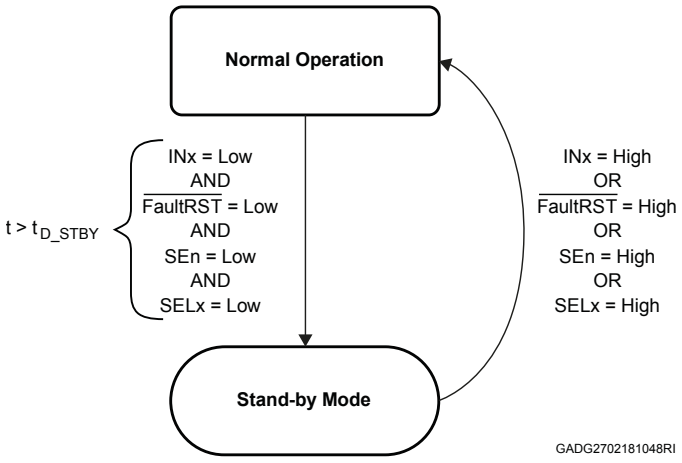
The device exits the standby condition as soon as FaultRST pin, SEn pin, SELx pin or one of the INx pins is set high.

Figure 19. Standby mode activation



The device leaves the standby mode when any of the above-mentioned pins is set high (see the figure below).

Figure 20. Standby state diagram



4.3 Flexible blanking time (fault reset management)

The use of the latch-off functionality can be critical in all cases where the load is compatible with the $R_{DS(on)}$ size but so heavy that power limitation or current limitation is triggered during the start-up (inrush) phase. In that case the lamp could never be turned on. In fact, even though the device could be restarted again by setting FaultRST pin low for a time greater than t_{LATCH_RST}, so that all latches are reset, the latch occurs again as soon as the channel tries to restart.

A possible way to turn on the lamp could be to manage the FaultRST pin in such a way that the latch-off functionality is “blanked” for a time much greater than t_{LATCH_RST}, to bypass the inrush phase of the bulb.

5 Usage / handling of current sense SEL pin

For diagnostic of M0-9 devices one analog monitoring output signal is used. It is capable to provide current sense signal reflecting channel output current or digital failure flag in off state signaling open load (provided by the presence of an external pull-up resistor) or short to V_{CC} diagnostic. Signal output is controlled by SEn pin (enable/ disable CS output signal) and a set of SEL pins (used for diagnostic signal selection). The number of control pins to read the desired channel is one (named SEL) for HSDs with two channels or two (named SEL0, SEL1) for HSDs with four channels.

5.1 SEL pins truth table (device dependant)

The complete encoding and its mapping to devices can be found in the following tables (orange / green / violet color shows mapping between device and SEL pins used)

Table 7. Multiplexed CS implementation

SEL_1	SEL or SEL_0	SEn	Analogue current sense (CS) output signal		
Quad channel control signals					
Double channel control signals					
Single channel control signals					
X	X	L	Hi-Z	Hi-Z	Hi-Z
L	L	H	Current sense	Current sense Ch0	Current sense Ch0
L	H	H		Current sense Ch1	Current sense Ch1
H	L	H			Current sense Ch2
H	H	H			Current sense Ch3

Only quad channel devices have SEL_1 Two channel devices have SELpin. One channel devices do not have any SEL pin	Ron typ [mΩ]	Devices list		
	4	VN9004AJ		
	6	VN9006AJ		
	8	VN9008AJ	VND9800AJ	
	12	VN9012AJ	VND9012AJ	
	16	VN9016AJ	VND9016AJ	
	25		VND9025AJ	VNQ9025AJ
	80			VNQ9080AJ

5.2 Connection of SEL pins with control logic (µC)

SEL pins are usually driven by µC in order to select the CS output signal (for diagnostic purposes). In order to save µC pins, multiple devices SEL pins can be driven in parallel, sharing the same microcontroller pins. To protect devices and microcontroller from disturbances or possible damage, there are valid recommendations for paralleling of SEL pins (for details, see Section 9: Inverse output current behavior).

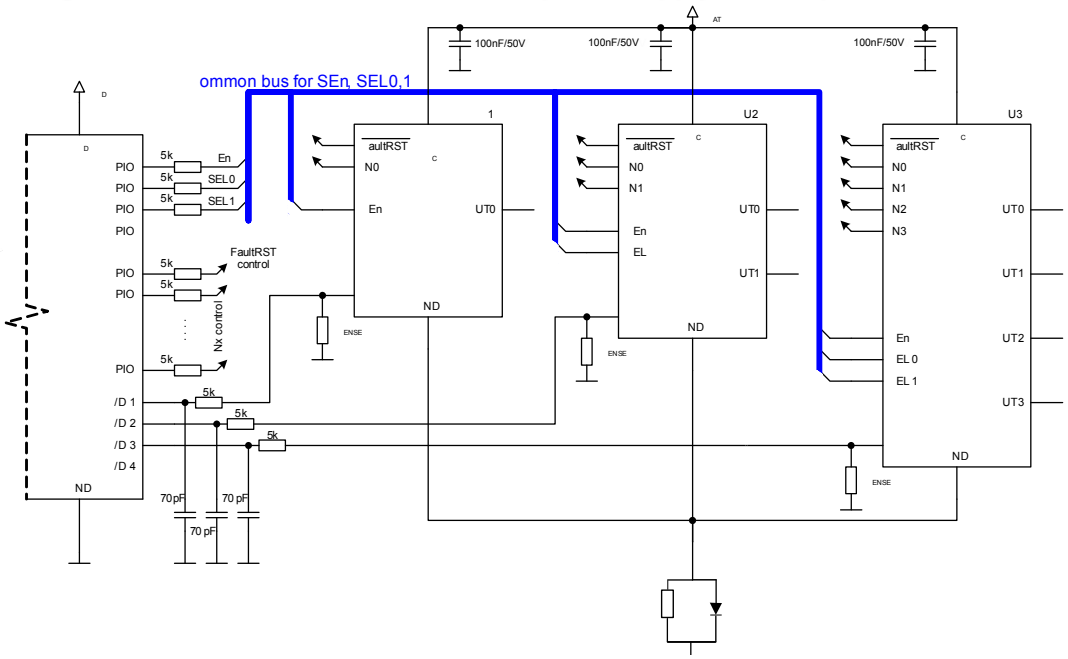
Following examples show possible combinations and influence to HW connection scheme.

Example 1:

- VN9016AJ (U1) + VND9025AJ (U2) + VNQ9080AJ (U3)
- Common power supply, common GND network
- Common SEn, SEL0, 1 (separate CS)

Devices have different number of SEL pins. In order to use only one protection resistor on the side of microcontroller, there must be used common V_{bat} power supply as well as the same ground protection network (fulfilling conditions for paralleling SELn on monolithic devices). Each HSD's CS output is mapped to separate A/D input.

Figure 21. Monolithic devices, common power supply rails, separate CS



Truth table shows signals mapping:

Table 8. Truth table for devices with separate CS signals

SEL_1	SEL (SEL_0)	SEn	A/D 1 U1 VN9016AJ	A/D 2 U2 VND9025AJ	A/D 3 U3 VNQ9080AJ
X	X	L	Hi-Z	Hi-Z	Hi-Z
L	L	H	Current sense (1)	Current sense Ch0	Current sense Ch0
L	H	H		Current sense Ch1 (2)	Current sense Ch1
H	L	H		Current sense Ch0 (2)	Current sense Ch2
H	H	H		Current sense Ch1 (2)	Current sense Ch3

1. *SEL and SEL_1 not applicable.*
2. *SEL_1 not applicable.*

Example 2:

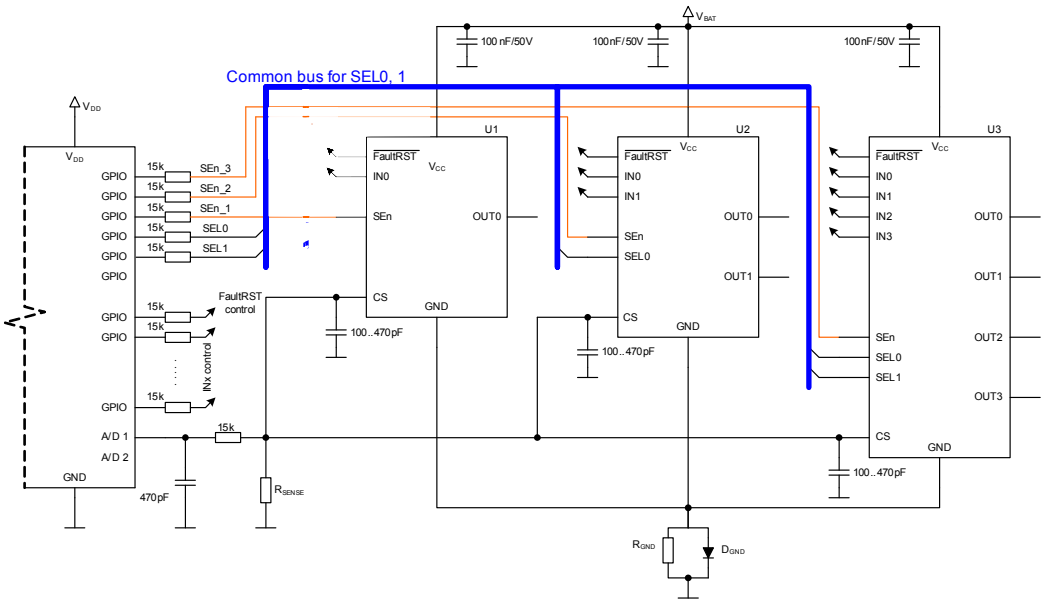
- VN9016AJ + VND9025AJ + VNQ9080AJ
- Common power supply, common GND network
- Common CS (separate SEn control)

The same HSDs are used like in example 1, but different topology is used - separate SEn, common CS signal. This option uses only one A/D channel for all HSDs.

On the other hand, decreased number of analogue channels increase number of control signals - separate SEn Pins control. In total, pin count is the same as in example 1.

Improper configuration on SEn_1...3 outputs causes no valid V_{SENSE} result (multiple CS outputs can be activated - applied into common R_{SENSE}).

Figure 22. Monolithic devices, common power supply rails, common CS



The truth table shows signals mapping:

Table 9. Truth table for monolithic devices, common CS

SEL_1	SEL (SEL_0)	SEn	A/D 1 U1 VN9016AJ	A/D 2 U2 VND9025AJ	A/D 3 U3 VNQ9080AJ
X	X	L	Hi-Z	Hi-Z	Hi-Z
L	L	H	Current sense (1)	Current sense Ch0	Current sense Ch0
L	H	H		Current sense Ch1 (2)	Current sense Ch1
H	L	H		Current sense Ch0 (2)	Current sense Ch2
H	H	H		Current sense Ch1 (2)	Current sense Ch3

1. *SEL and SEL_1 not applicable.*
2. *SEL_1 not applicable.*

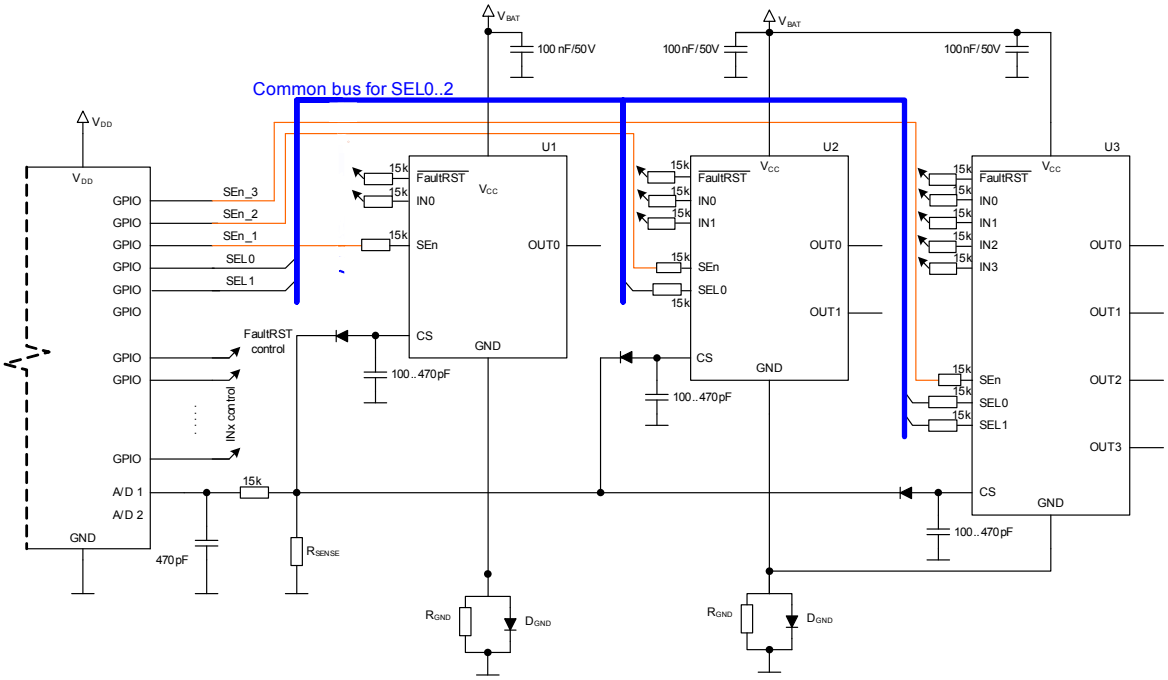
Example 3:

- VN9016AJ + VND9025AJ + VNQ9080AJ
- Separate power supply lines, common GND network
- Common CS (separate SEn control)

Topology of control part (SEn, SEL0,1) is similar to example 2. The main difference consists of using separate power supply lines on HSDs. Due to this fact, there are implemented recommendations of paralleling SEL signals as well as CS input (described in chapter 10):

- CS monitor is using diode in series to on CS outputs.
- Each HSD control signal is using own protection resistor.

Figure 23. Monolithic devices, separate power supply rails, common CS



Signals mapping truth table is the same as in example 2.

6 Load compatibility

6.1 Bulbs

This chapter is intended to suggest drivers that can be used for typical automotive bulb loads or typical combinations of bulbs. A major consideration when driving bulbs is the inrush current generated when starting up a cold filament.

A properly selected driver should allow the safe turn-on of the bulb without any restrictions under normal conditions. Under worst case conditions the driver should still be able to turn on the bulb even if some protection of the driver may be triggered temporarily (for example, maximum saturation time 10 ms to activate channel with no further protections triggering). However, the drivers´ long-term integrity should not be jeopardized. Typical combinations of bulbs and M0-9 devices (R_{ON} classes) are shown in the following table.

Table 10. Typical bulb loads for given M0-9 R_{ON} class

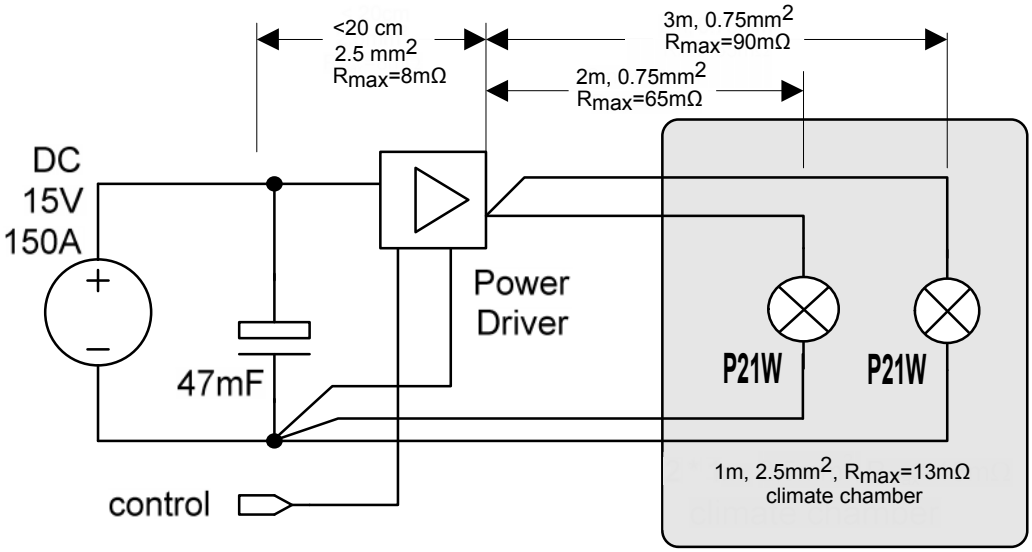
Device R_{DSon} class [mΩ]	Suggested bulb types and combinations
4	H1 (55W) H4 (55W/60W) H7 (55W) H9 (65W) Xenon head lamp (high temperature)
6	H1 (55W) H4 (55W/60W) H7 (55W) H9 (65W) Xenon head lamp (high temperature)
8	H1 (55W) H4 (55W/60W) H7 (55W) H9 (65W)
12	2 x P21W 2 x P27W 2 x P21W + R5W 2 x P27W + R5W
16	R10W 2xR5W P21W P21W + R5W P27W P27W + R5W 2 x P21W
25	R10W 2 x R5W P21W P21W + R5W P27W P27W+R5W

Device R_{DSon} class [mΩ]	Suggested bulb types and combinations
80	R10W 2 x R5W

Experimental measurement example with VND9016AJ–load bulb 2 x 21 W:

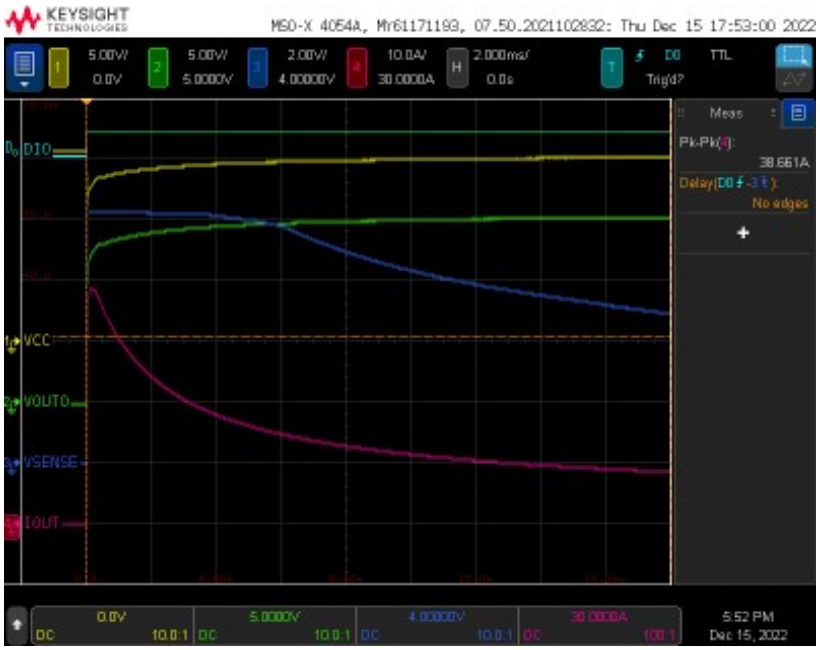
An experimental measurement has been performed to depict that the driver is able to turn on the bulb and matches the requirements under the defined conditions.

Figure 24. Principle of the setup used for the measurement



1. *Normal conditions:*
   - *V_{BAT}: 16 V*
   - *T_{case}: 25 °C*
   - *T_{bulb}: 25 °C*
   - *Requirement: None of the protection functions must be triggered.*

Figure 25. Evaluation result–normal condition



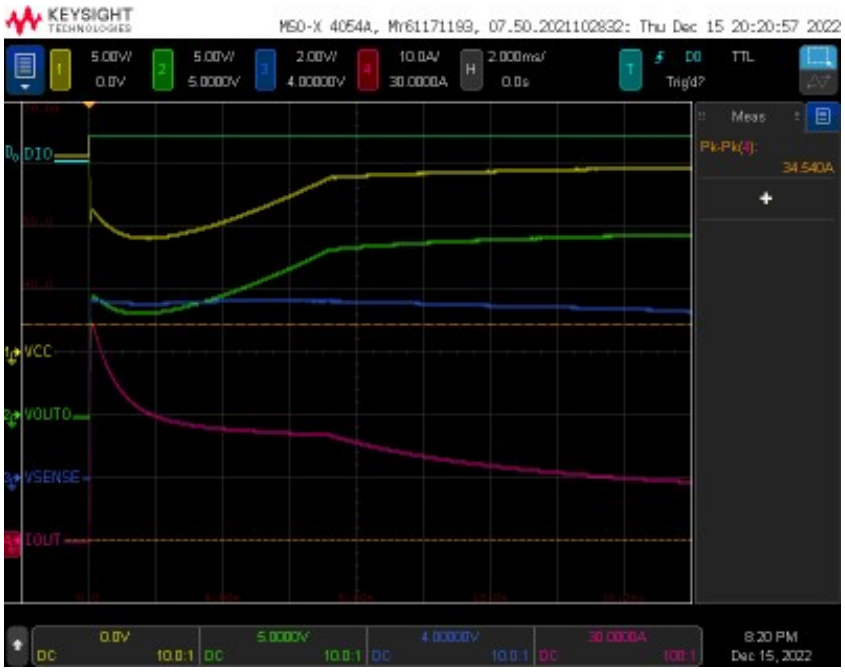
2. *Cold condition:*
   - *V_{BAT}: 16 V*
   - *T_{case}: 25 °C*
   - *T_{bulb}: -40 °C*
   - *Requirement: Power limitation allowed for durations of less than 20 ms (auto restart mode considered).*

Figure 26. ***Evaluation result–cold condition***

3. *Hot conditions:*

- V_{BAT}: 16 V
- T_{case}: 105 °C
- T_{bulb}: 25 °C
- Requirement: Thermal shutdown is allowed for a duration below 20 ms (autorestart mode considered).

Figure 27. **Evaluation result–hot condition**



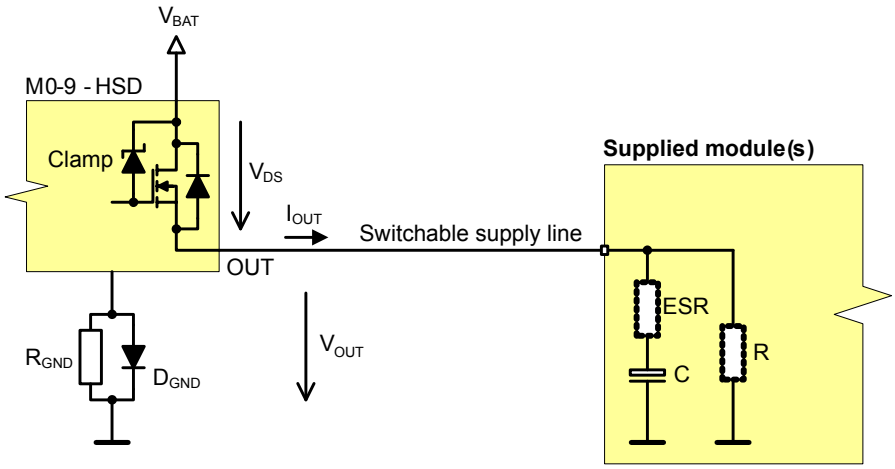
The device can turn-on 2 x 21 W bulbs under specified conditions without triggering the device protection functions (thermal shutdown).

Note: The mentioned evaluation example only refers to the inrush current at turn-on of a cold bulb. Still the steady state power dissipation and, in case of PWM is applied, the additional switching losses of the driver must be considered in order not to exceed the max. possible power dissipation. This obviously becomes more important with a larger number of channels per package (that is, dual or quad channel drivers) and high-power loads applied to more than one channel.

6.2 Capacitive loads

This chapter deals with the devices capability to turn on capacitive loads. A typical application example is the usage of the HSD as a supply voltage switch for other modules (see in the figure below).

Figure 28. **A typical example of HSD combined with capacitive load**



A capacitive character of the load creates an inrush current during the turn-on phase, depending mainly on the load capacitance, switching time and the load resistance (capacitor ESR, wiring resistance…). A typical requirement for the HSD in such applications is the ability to handle the worst-case inrush current without activation of the protection mechanisms (power limitation or thermal shutdown) to ensure correct operation of connected load (module). Since there are several variables and conditions depending on application, there are no calculations provided in this chapter.

The following measurement was performed on several different parts (RDSON classes) to determine what is the maximum capacity which can be switched on without activation of protection mechanisms. In Table 11. Load classes used in capacitive load compatibility testing you find the maximum capacitance values which the devices were able to switch on for different device temperatures and battery voltages. These values were experimentally determined during the in application validation (IAV) of the devices. The resistance values in the table represent the total load resistance (capacitor ESR + wiring resistance).

Table 11. Load classes used in capacitive load compatibility testing

Load name	Capacitor [µF]	Tolerance [%]	Total load R [mΩ]	Total load L [µH]
C47	47	±30	240	2
C100	100	±20	220	2
C220	220	±20	200	2
C330	330	±20	180	2
C470	470	±20	160	2
C820	820	±20	140	2
C1000	1000	±20	120	2
C1500	1500	±20	100	2
C2200	2200	±20	80	2
C3300	3300	±20	60	2

Table 12. Maximum load capacity that can be turned on without limitation

Device	Max C_load @T_{case} = 25 °C V_{bat} = 16 V		Max C_load @T_{case} = 25 °C V_{bat} = 28 V		Max C_load @T_{case} = 85 °C V_{bat} = 16 V		Max C_load @T_{case} = 105 °C V_{bat} = 16 V	
	C [µF]	R [mΩ]	C [µF]	R [mΩ]	C [µF]	R [mΩ]	C [µF]	R [mΩ]
VN9004AJ	8000	>50	2200	80	2200	80	2200	80
VN9006AJ	5500	>50	1500	100	1500	100	1000	120
VN9008AJ	3300	60	1000	120	1000	120	1000	120
VN9012AJ	2200	80	820	140	1000	120	820	140
VN9016AJ	1500	100	470	160	820	140	470	160
VND9008AJ	3300	60	820	140	1000	120	820	140
VND9012AJ	2200	80	820	140	1000	120	820	140
VND9016AJ	1500	100	470	160	820	140	470	160
VND9025AJ	1500	100	470	160	220	200	220	200
VNQ9025AJ	1500	100	470	160	220	200	220	200
VNQ9080AJ	820	140	100	220	33	260	33	260

6.3 Power loss calculations

The power loss calculation is an important step during the application design as it is a basis for further thermal considerations and PCB design.

This chapter is intended to provide guidelines for calculation and estimation of power dissipation in the device in combination with different kind of loads (resistive, inductive, capacitive etc.) and with different modes of operation (steady state, PWM).

All next evaluations are focused on power losses in the power MOSFET of the device. The power dissipation of other parts (control logic, charge pump) is in most cases negligible. If needed, it can be calculated from the device supply current (I_S) and supply voltage value (V_{CC}):

Device control part power dissipation [W]:

$$P_{CTRL} = V_{CC} \cdot I_{GND(ON)} \quad (7)$$

- example for VND9016AJ (control stage current consumption in ON state, all channels on driving nominal load - datasheet value):
- **Table 13. control stage current consumption in ON state**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IGND(ON)	Control stage current consumption in ON state. All channels active.	V_{CC} = 13 V; V_{SEn} = 5 V; V_{FR} = V_{SEL} = 0 V; V_{IN0} = 5 V; V_{IN1} = 5 V; I_{OUT0} = 3.7 A; I_{OUT1} = 3.7 A			4.5	mA

$$P_{CTRL} = V_{cc} \cdot I_{GND(ON)} = 13V \cdot 4.5mA = 58.5mW \quad (8)$$

The next description is divided into 2 subchapters:

- Conduction losses: steady-state losses (during the ON state).
- Switching losses: losses during switching phases.

6.3.1 Conduction losses

The conduction losses are given by the power dissipation of the MOSFET switch due to the ON state resistance (R_{ON}).

ON state power dissipation [W]:

$$P_{ON} = R_{ON} \cdot I_{OUT}^2 \quad (9)$$

ON state energy loss [J]:

$$W_{Rdson} = P_{ON} \cdot t_{ON} \quad (10)$$

(where t_{ON} = ON state duration)

- Example for VND9016AJ (steady state condition, datasheet values I_{OUT} = 3.7 A, R_{ON} at 150 °C = 35.2 mΩ):

Table 14. Steady state condition

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}	On-state resistance	I_{OUT} = 3.7 A; T_j = 25 °C		16		mΩ
		I_{OUT} = 3.7 A; T_j = 150 °C			35.2	
		I_{OUT} = 3.7 A; V_{CC}= 4 V; T_j = 25 °C			27.2	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}	On-state resistance	I_{OUT} = 0.4 A; V_{CC}= 2.7 V; T_j = 25 °C			96	mΩ

$$P_{ON} = R_{ON} \cdot I_{OUT}^2 = 35.2m\Omega \cdot 3.7A^2 = 481.9mW \quad (11)$$

The R_{ON} parameter is dependent mainly on temperature (see measurement on Figure 29. $R_{DS(ON)}$ dependency on temperature (measured on a VND9016AJ sample)). This should be considered during the calculations.

In most cases, it is not necessary to consider the dependency on V_{CC} or I_{OUT}. The R_{ON} is almost independent on V_{CC} down to ~4 V (see Figure 30. $R_{DS(ON)}$ dependency on V_{CC} (measured on a VND9016AJ sample)) and almost independent on I_{OUT} (see Section 6.3.1: Figure 8).

Figure 29. $R_{DS(ON)}$ dependency on temperature (measured on a VND9016AJ sample)

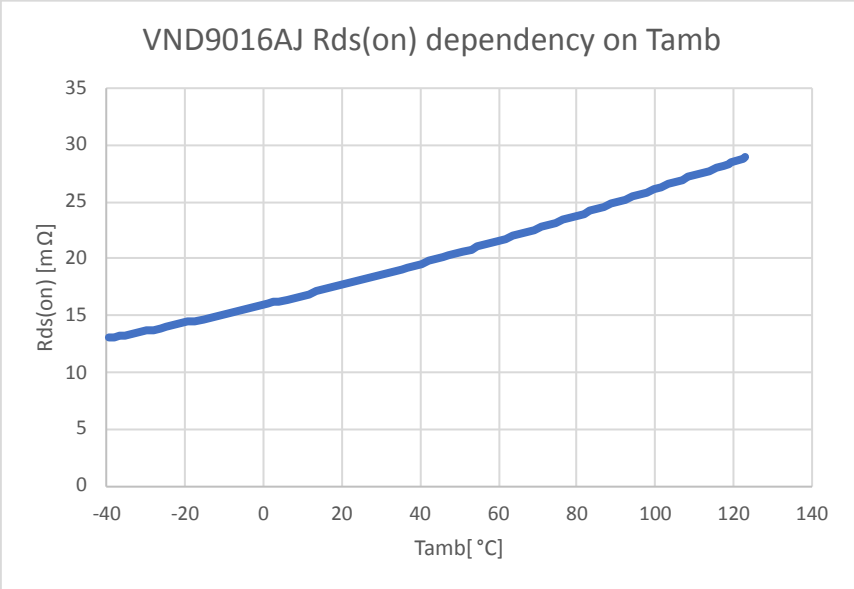


Figure 30. $R_{DS(ON)}$ dependency on V_{CC} (measured on a VND9016AJ sample)

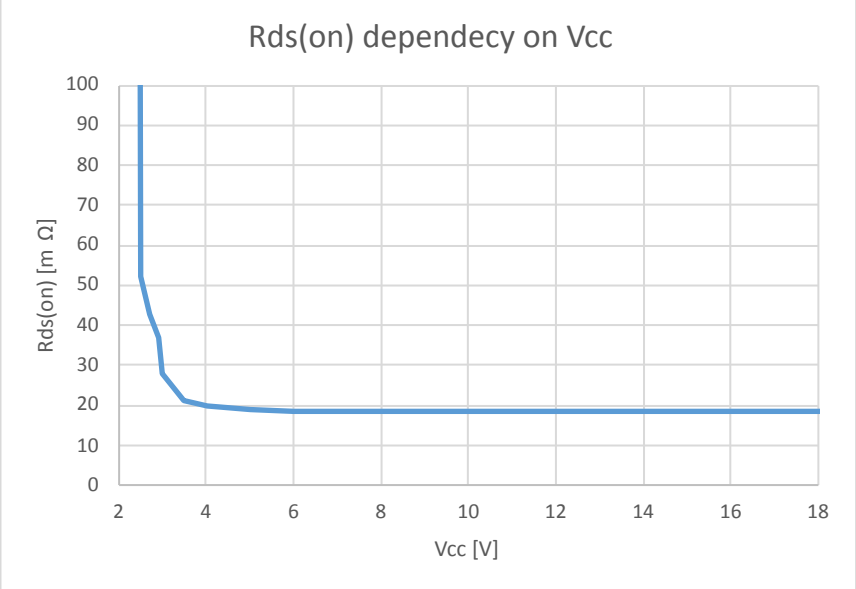
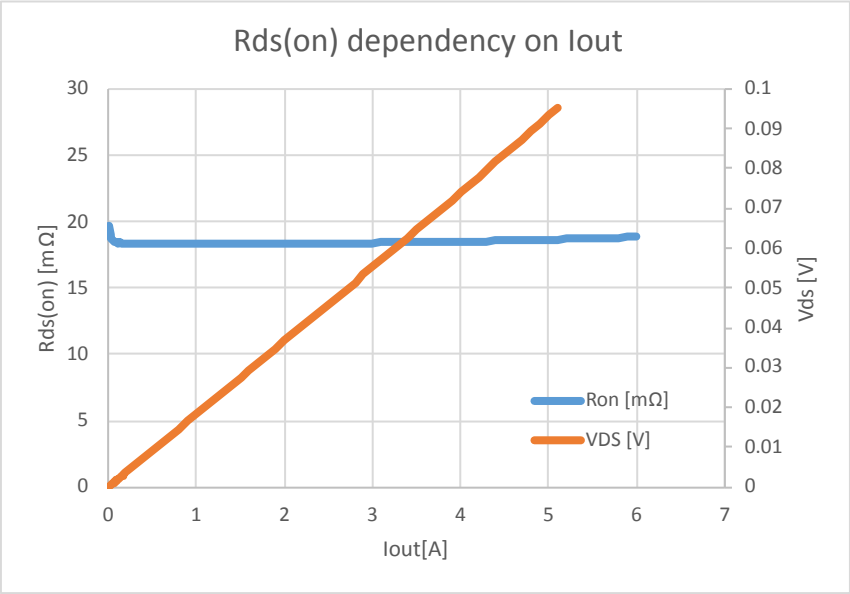


Figure 31. $R_{DS(ON)}$ dependency on I_{OUT} (measured on a VND9016AJ sample)



The calculation of conduction losses in PWM mode is based on similar consideration as in case of steady state losses (focusing on R_{ON}, I_{OUT}, t_{on}), however it is important to consider right PWM on time (corrected with the turn-on/off switching delays and switching times) and right current in on state (for instance in case of bulb it depends on actual duty cycle):

Corrected duty cycle [-]:

$$D_{COR} = D - \frac{t_{don} - t_{doff} - t_{won}}{t_{period}} \quad (12)$$

Where:

$$D = \frac{t_{IN\_high}}{t_{period}} D = \frac{t_{in\_high}}{t_{period}} \quad (13)$$

[-]: Duty cycle applied on input pin

$$\frac{t_{dON}}{t_{dOFF}} \quad (14)$$

[s]: Turn on / off delay time

t_{won} [s]: Turn on switching time

ON state power dissipation [W]:

$$P_{ON} = R_{DS(on)} \cdot I^2_{OUT(ON)} \quad (15)$$

Note: In case of bulb, the load current in on state depends on the actual duty cycle

Average power dissipation: [W]:

$$P_{AVG} = P_{ON} \cdot D_{COR} \quad (16)$$

6.3.2 Switching losses

The switching losses are important especially in PWM operation. Compared to conduction losses, the calculation is dependent on many factors like the load characteristic (resistive, capacitive, or inductive), device characteristics (switching times) and environmental conditions (ambient, temperature, battery voltage).

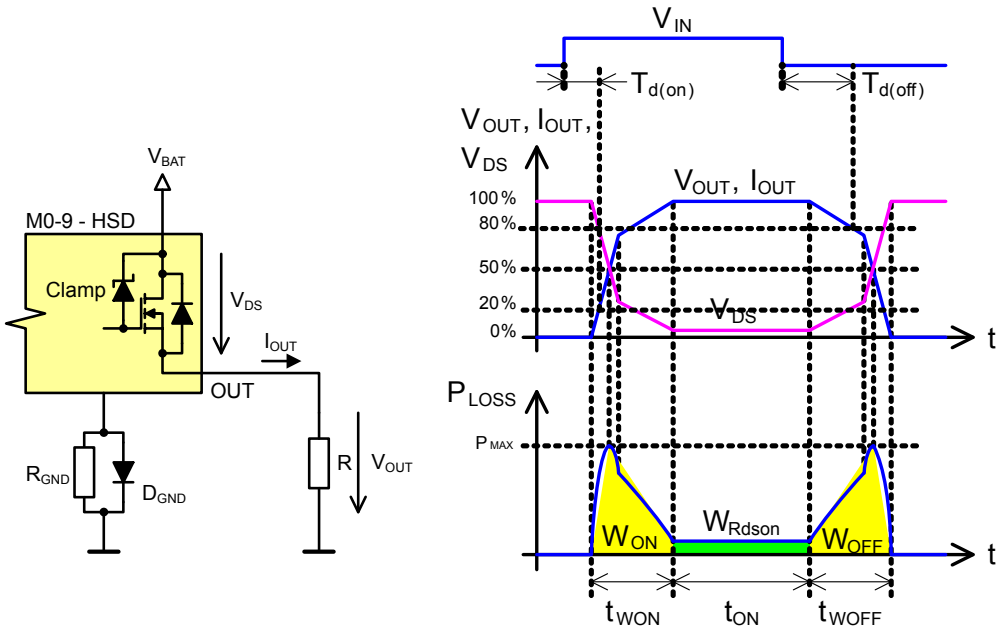
The switching shapes of M0-9 devices are optimized to fulfill the EMC requirements with minimum switching losses. Moreover, the turn-on and turn-off shapes are symmetrical to ensure minimum duty cycle error.

6.3.2.1 *Switching losses - resistive loads, bulbs*

This subchapter deals with all kinds of loads with resistive character (such as bulbs, heating elements etc.). The inductivity of wire harness is neglected (< 5 µH considered). The next calculations are simplified assuming constant resistance of the load. However, it is also applicable for nonlinear resistive loads (bulbs) driven in PWM mode. The PWM frequency is usually high enough (>50 Hz) to minimize the filament temperature (resistance) variation over the PWM period, so it behaves like a constant resistor.

The instantaneous power dissipation in the switch during the switching phase is equal to drain to source voltage (V_{DS}) multiplied by the output (load) current (I_{OUT}). With given switching shapes and resistive load, the instantaneous power dissipation can be approximated by triangular waveform (see yellow area on the figure below).

Figure 32. Switching and conduction losses (resistive loads)



Considering resistive load, the maximum instantaneous power dissipation occurs at half of the nominal output voltage and half of the nominal load current. It is the point where the switch resistance matches the load resistance (maximum power transfer theorem, impedance matching).

Peak power dissipation [W]:

$$P_{MAX} = \frac{V_{OUT}}{2} \cdot \frac{I_{OUT}}{2} \cong \frac{V_{BAT}}{2} \cdot \frac{V_{BAT}}{2 \cdot R} = \frac{V_{BAT}^2}{4 \cdot R} \quad (17)$$

Turn-on (Turn-off) energy loss [J]:

$$W_{ON} = W_{OFF} = \frac{1}{6} \cdot \frac{V_{BAT}^2}{R} \cdot t_{WON} \quad (18)$$

(t_{WON} = t_{WOFF})

Note: Linear shape of the switching phase and symmetrical turn-on / off shapes are considered.

The same calculations are also applicable on the bulb in PWM mode. If the PWM frequency is high enough (>50 Hz) the filament temperature (resistance) variation over the PWM period is negligible so it behaves like a constant resistor.

Note: Typical and maximum switching losses on nominal resistive loads are specified in the datasheet with parameters W_{ON} and W_{OFF} (considering V_{CC} = 13 V, -40 °C < T_j < 150 °C). The switching losses vary with battery voltage. If we suppose constant switching times at varying the battery voltage, this yelds:

- $$W_{ONatVBAT2} = W_{ONatVBAT1} \cdot \frac{P_{LOADatVBAT2}}{P_{LOADatVBAT1}} \quad (19)$$
- $$W_{OFFatVBAT2} = W_{OFFatVBAT1} \cdot \frac{P_{LOADatVBAT2}}{P_{LOADatVBAT1}} \quad (20)$$

Experimental measurements on M0-9 HSDs have highlighted that switching times are slightly decreasing with increasing V_{CC} so the above formulas are approximated.

Calculation example: VND9016AJ:

- Load: 5.2 Ω resistor
- V_{BAT}: 16 V
- t_{WON}, t_{WOFF} : 23 µs → this parameter is not explicitly specified in the datasheet. The value can be obtained by the measurement or estimated from the dV_{OUT}/dt datasheet parameter (this case 16 V / (0.7 V/µs)).

Peak power dissipation [W]:

$$P_{MAX} = \frac{V_{BAT}^2}{4 \cdot R} = \frac{16V^2}{4 \cdot 5.2\Omega} = 12.3W \quad (21)$$

Turn-on / turn-off energy loss [J]:

$$W_{ON} = W_{OFF} = \frac{1}{6} \cdot \frac{16^2}{5.2} \cdot 23\mu s = 283\mu J \quad (22)$$

Switching losses measurement–comparison with calculation:

The switching losses in the HSD were measured by an oscilloscope with mathematical functions. The first function F1 shows the actual power dissipation on the HSD (V_{BAT}-V_{OUT})*I_{OUT}, the second function F4 shows the HSD energy (integral of F1).

Figure 33. Example of switching losses on VND9016AJ with 5.2 Ω resistive load

6.3.2.2 *Switching losses - LED clusters*

The switching losses evaluation in combination with LED loads is much more complex task in comparison with resistive loads. Since there are many different types of the LED string, it is almost impossible to cover all cases with one general calculation formula (like in case of resistive loads). Exact calculation is problematic even for specific LED load (with known behaviour) due to its non-linear V/A characteristic (see examples on next figures). Therefore, it is usually more efficient to do the estimation only or switching losses measurement as shown in this chapter.

Figure 34. LED cluster example 1 – LED test board (6 x 3 LEDs OSRAM LA E67-4)

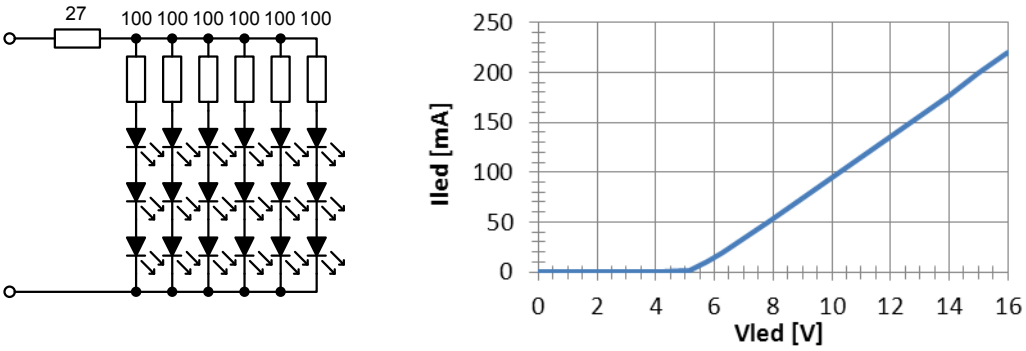
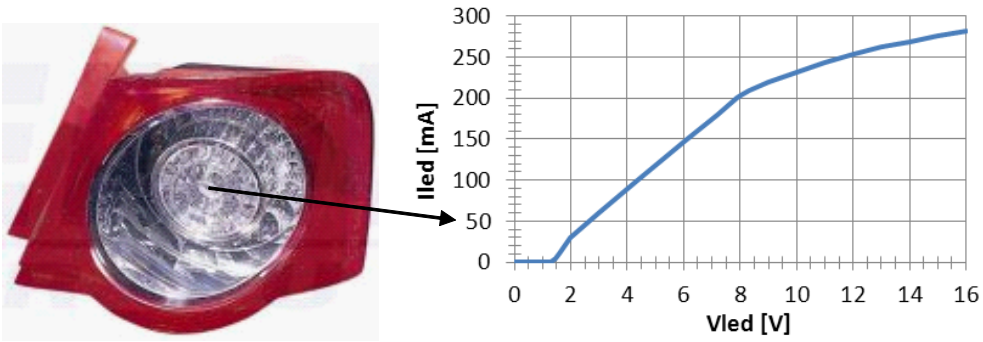
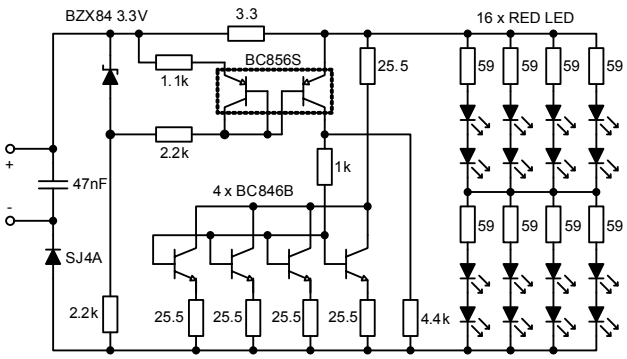


Figure 35. LED cluster example 2 – tail & brake light (VW passat B6)





The first example shows a simple LED cluster with serial-parallel combination of LEDs and resistors. On second example there is a schematic and V/A characteristic measured on real LED lamp (VW passat B6). As seen on schematic, on top of the serial-parallel LED / resistor strings there is a reverse battery protection diode, ESD capacitor on input terminal and “dummy load” circuitry with bipolar transistors. This circuitry is used to adapt the LED string behavior (V/A characteristic) according to diagnostic requirements (open load in on-state, open load in off-state).

Switching losses – measurement example 1:

This example shows switching losses measurement on VNQ9080AJ with LED cluster example 2 (VW passat B6 – tail & brake light) using an oscilloscope with mathematical functions. The first function F1 shows the actual power dissipation on the HSD (V_{BAT}-V_{OUT})*I_{OUT}, the second function F4 shows the HSD energy (integral of F1).

Conditions:

- V_{BAT}: 16 V
- Temperature: 25 °C
- PWM: 200 Hz, 70%
- Load: VW Passat B6 – Tail & Brake (see Figure 35. LED cluster example 2 – tail & brake light (VW passat B6))
- Device: VNQ9080AJ

Figure 36. Slew rate and switching losses (VNQ9080AJ, VW passat B6 –tail & brake)

Measured losses: W_{ON} ~ 30 µJ, W_{OFF} ~ 30 µJ

Contribution to total average power dissipation:

$$P_{SW} = \frac{W_{ON} + W_{OFF}}{T_{PWM}} = \frac{30\mu J + 30\mu J}{\frac{1}{200Hz}} = 18mW \quad (23)$$

6.3.2.3 *Switching losses - inductive loads*

A typical characteristic of inductive loads is the tendency to maintain the direction and value of actual current flow. Applying nominal voltage on inactive load (turn-on), it takes a certain time (depending on time constant □□□L/R) to reach nominal current. Removing the voltage source from the active load (turn-off), the load inductance tends to continue to drive the current via any available path (that is, clamp of the HSD) by reversing its voltage (acts as a source) until the stored energy (E_L=1/2 L I_O ^{2} $E_L = \frac{1}{2} \cdot L \cdot I_0^2$) is dissipated. The time needed to dissipate this energy is called demagnetization time (T_{DEMAG}). This time is strongly dependent on the voltage across the load (V_{DEMAG}) at which the demagnetization is performed (higher $|V_{DEMAG}|$ ⇒ shorter T_{DEMAG}). A typical V_{DEMAG} for M0-9 devices is equal to V_{CC} – 46 V. Corresponding T_{DEMAG} can be calculated as

$$T_{DEMAG} = \frac{L}{R} \cdot ln\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} \quad (24)$$

(neglecting the turn-off switching time of the HSD) where L = load inductance, R = load resistance and I0 = load current at the beginning of turn-off event.

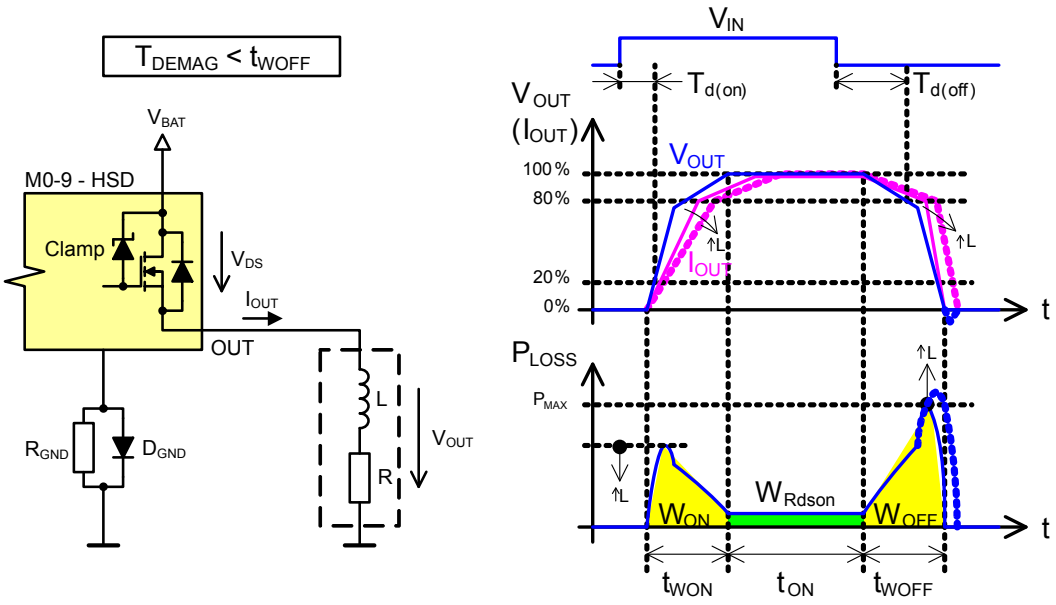
From these considerations it is obvious that instant power dissipation and switching losses in the HSD are usually higher at the turn-off phase. Since the HSD output behavior (voltage/current waveforms) depends on several factors (mainly on the ratio between the demagnetization time and turn-off switching time t_{WOFF}), the next analysis of switching losses is divided into the following parts:

- Low inductance ($T_{DEMAG} < t_{WOFF}$).
- High inductance ($T_{DEMAG} > t_{WOFF}$).
- High inductance ($T_{DEMAG} > t_{WOFF}$) with external freewheeling diode:
  - Steady state operation (single turn-on / turn-off)
  - PWM operation

Low inductance ($T_{DEMAG} < t_{WOFF}$):

If the load inductance is relatively low (so the stored energy is dissipated within the HSD turn-off time t_{WOFF}), the output voltage decays down to 0 (or slightly in negative) without the activation of the output clamp (see the figure below).

Figure 37. Switching losses with low inductance



In this case, the switching losses can be roughly estimated from equivalent losses with pure resistive load (see calculation in previous chapter). Since the output current is delayed from the output voltage, the losses at turn-on phase (W_{ON}) will be lower, while the losses at turn-off phase (W_{OFF}) will be higher (up to factor of 5) in comparison with pure resistive load. This factor was found experimentally in a condition when the demagnetization time (T_{DEMAG}) is matched with turn-off switching time (t_{WOFF}).

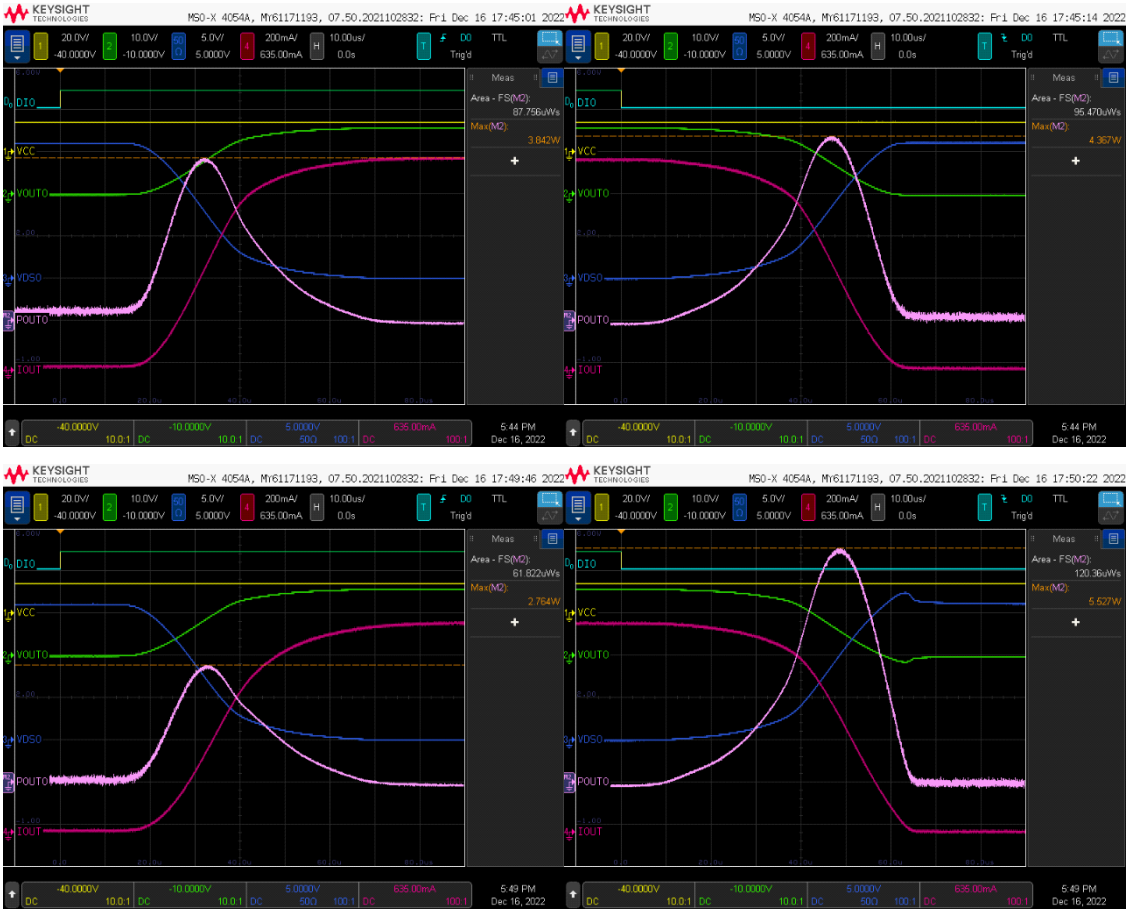
Measurement example–low inductance ($T_{DEMAG} < t_{WOFF}$):

This measurement example compares the switching losses in the VND9025AJ with two different loads–pure resistive 16 Ω and 60 µH at 16 Ω.

Conditions:

- V_{BAT}: 16 V
- Temperature: 25 °C
- PWM: 200 Hz, 70%
- Load:
  - 16 Ω
  - 60 µH at 16 Ω (calculated T_{DEMAG} = 0.53 µs)
- Device: VND9025AJ

Figure 38. **Low inductance (T_{DEMAG} < t_{WOFF})–measurement example**



Measured losses (pure resistive 16 Ω): W_{ON} ~ 88 µJ, W_{OFF} ~ 95 µJ

Measured losses (60 µH at 13.5 Ω): W_{ON} ~ 62 µJ, W_{OFF} ~ 120 µJ

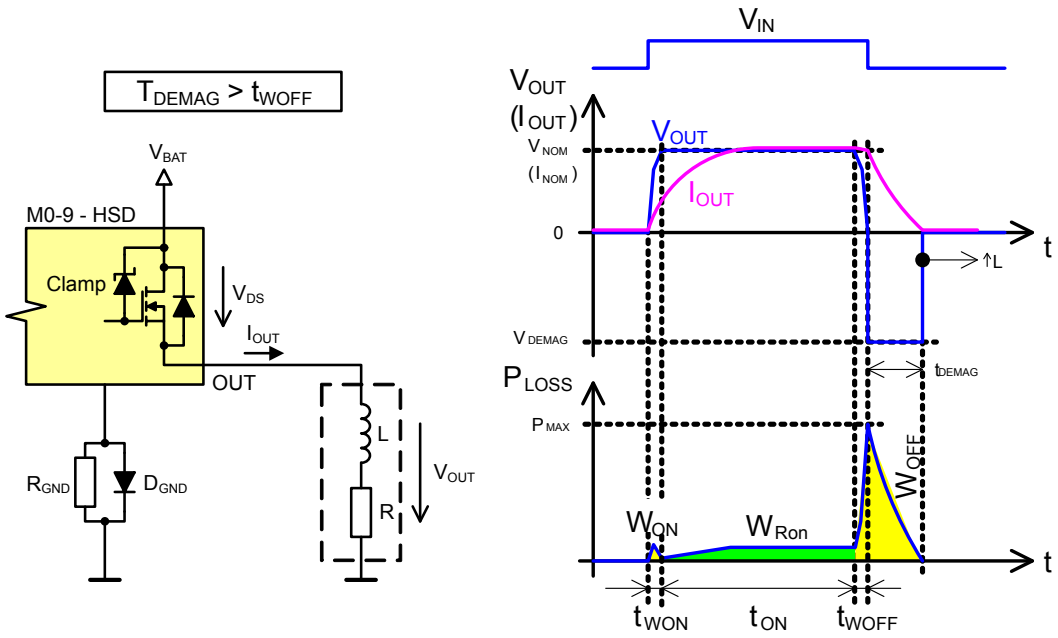
W_{ON} ratio (60 µH versus pure resistive): 62 / 88 = 0.70 x

W_{OFF} ratio (60 µH versus pure resistive): 120 / 95 = 1.26 x

High inductance (T_{DEMAG} > t_{WOFF})

If the load inductance is relatively high (so the time needed for the load demagnetization is much higher than the HSD turn-off time t_{WOFF}), the output voltage at the turn-off phase is forced negative so the load current continues via the HSD output clamp (see the figure below).

Figure 39. Switching losses with high inductance



The above example explains a single turn-on / turn-off event. This means that zero load current is considered at the beginning of the turn-on phase and nominal load current is considered at the beginning of the turn-off phase. Assuming T_{DEMAG} >> t_{WOFF}, the switching losses can be calculated as follows:

- Turn-on energy loss [J]:

$$W_{ON} \sim W_{ON} \approx 0 \tag{25}$$

- Turn-off energy loss [J]:

$$W_{OFF} = \frac{V_{BAT} + |V_{DEMAG}|}{R^2} \cdot L \cdot \left[R \cdot I_0 - |V_{DEMAG}| \cdot \ln\left(\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right)\right] \tag{26}$$

(Losses during transition phases tWON and tWOFF neglected)

Calculation example (single turn-on / off event):

- Load: 20 mH at 16 Ω
- V_{BAT}: 16 V
- V_{DEMAG}: -30 V (V_{BAT} – 46)
- I0: 1.0 A (V_{BAT} / 16 Ω)

$$T_{DEMAG} = \frac{L}{R} \cdot ln\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|} = \frac{0.02}{13.5} \cdot ln\frac{|-30| + 1.185 \cdot 13.5}{|-30|} = 534\mu s \tag{27}$$

$$W_{ON} \sim 0 \tag{28}$$

(T_{DEMAG} >> T_{WON} ⇒ 534 µs >> ~23 µs ⇒ condition fulfilled)

$$W_{OFF} = \frac{|V_{DEMAG}| + V_{BATT}}{R^2} \cdot L \cdot \left(R \cdot I_0 - \left|V_{DEMAG}\right| \cdot ln\frac{|V_{DEMAG}| + I_0 \cdot R}{|V_{DEMAG}|}\right) = \tag{29}$$

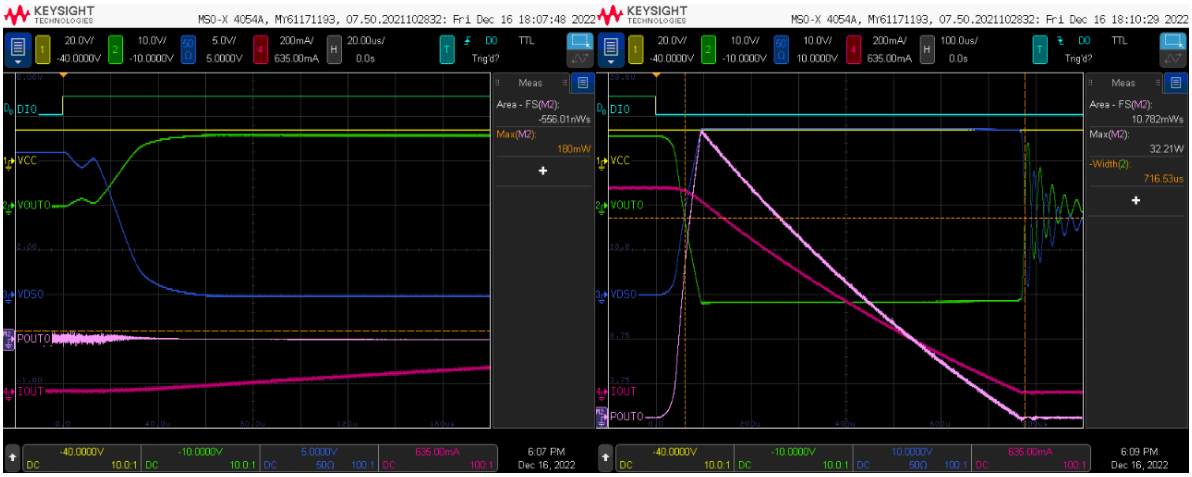
$$\frac{|-30| + 16}{16^2} \cdot 0.02 \cdot \left(16 \cdot 1.0 - |-30| \cdot ln\frac{|-30| + 1.0 \cdot 16}{|-30|}\right) = 11.5mJ \tag{30}$$

Measurement example, comparison with calculation–High inductance ($T_{DEMAG} > t_{WOFF}$):

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 20 mH at 16 Ω
- Device: VND9025AJ

Figure 40. High inductance ($T_{DEMAG} > t_{WOFF}$)–measurement example



Measured T_{DEMAG}: 672 µs (534 µs calculated)

Measured W_{ON}: 0 µJ (0 estimated)

Measured W_{OFF}: 10.8 mJ (11.5 mJ calculated)

Measured losses (pure resistive 13.5 Ω): W_{ON} ~ 88 µJ, W_{OFF} ~ 95 µJ

W_{ON} ratio (20 mH versus pure resistive): 0 / 88 = 0x

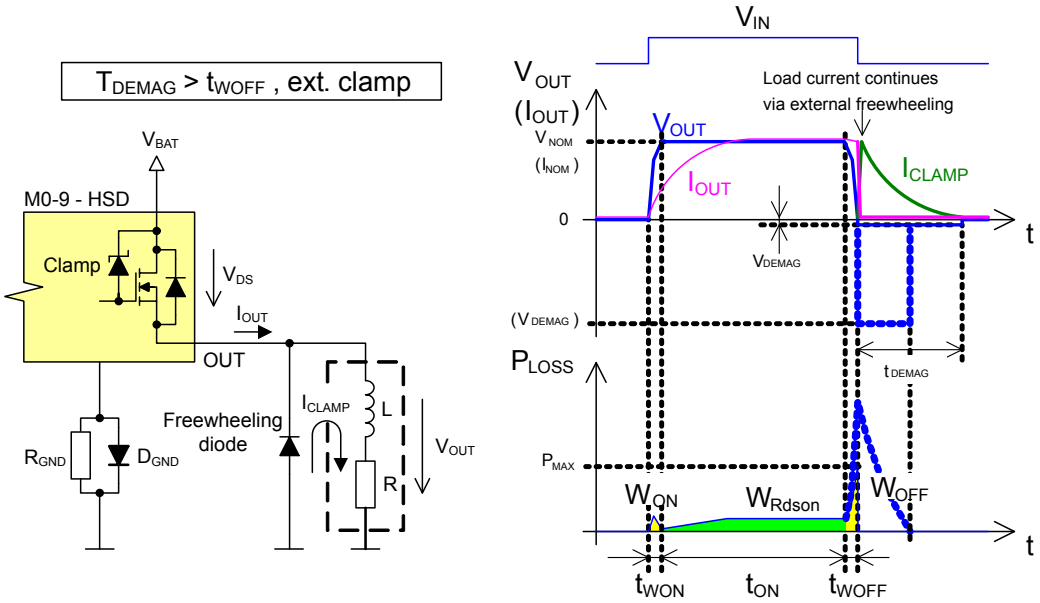
W_{OFF} ratio (20 mH versus pure resistive): 10800 / 95 = 113.7x

Most of the measured values are corresponding to theoretical assumptions and calculations, except for the demagnetization time, which was measured to be approximately 10% longer.

High inductance (T_{DEMAG} > t_{WOFF}) with external freewheeling diode

An external clamping circuitry (that is, freewheeling diode) is usually used to protect the HSD in case the demagnetization energy is exceeding the energy capability of a given HSD. By using a standard freewheeling diode, the demagnetization voltage is reduced from–32 V (a typical V_{DEMAG} of M0-9 device at V_{BAT} = 14 V) to approximately–1 V (depending on forward voltage of the diode - see the figure below). This has an influence to the demagnetization time (lowering $|V_{DEMAG}|$ ⇒ increasing T_{DEMAG}), as can be derived from the TDEMAG equation.

Figure 41. Switching losses with high inductance and external freewheeling (single event)



The above example explains a single turn-on / turn-off event. This means that zero load current is considered at the beginning of the turn-on phase and nominal load current is considered at the beginning of the turn-off phase.

Assuming T_{DEMAG} >> t_{WOFF}, the switching losses can be estimated as follows:

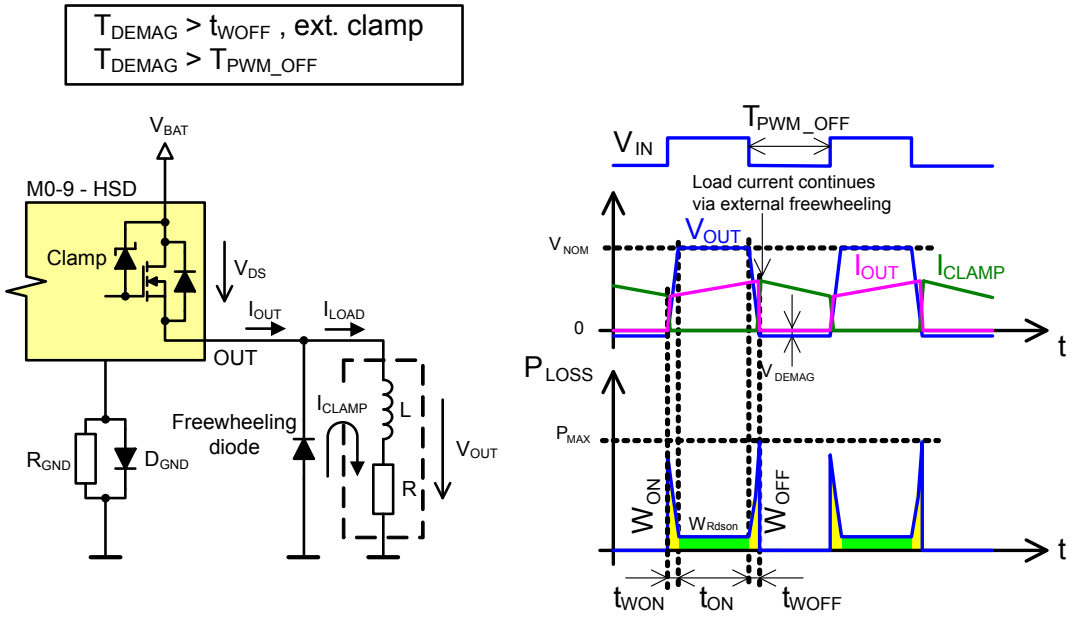
Turn-on energy loss [J]: W_{ON}~~ 3x higher versus pure resistive load

Turn-off energy loss [J]: W_{OFF}~W_{OFF} ~3x higher versus pure resistive load

Note: The factor 3 is the result of experiment (see Table 11. Load classes used in capacitive load compatibility testing and Table 12. Maximum load capacity that can be turned on without limitation)

In PWM operation (or at turn-on with a small delay after the last turn-off) there is a possibility that the turn-on event comes before the end of the demagnetization phase (if the PWM off-state time is shorter that the load demagnetization time: (*TDEMAG* > TPWM_OFF). This means that the turn-on phase is starting while the current is still forced via the freewheeling diode. This makes the turn-on switching loss significant if compared with the case of zero starting current. As a rough estimation a ~3x higher value can be considered versus equivalent resistive load. This way of the operation is frequently used on purpose–for example for the load current regulation by PWM duty cycle (see the Figure 42. Switching losses–high inductance + ext. freewheeling (PWM operation)).

Figure 42. **Switching losses–high inductance + ext. freewheeling (PWM operation)**



Assuming T_{DEMAG} >> T_{PWM_OFF}, the switching losses can be estimated as follows:

Turn-on energy loss [J]: W_{ON} ~ W_{ON}~3x higher versus equivalent resistive load.

Turn-off energy loss [J]: W_{OFF} W_{OFF}~~3x higher versus equivalent resistive load.

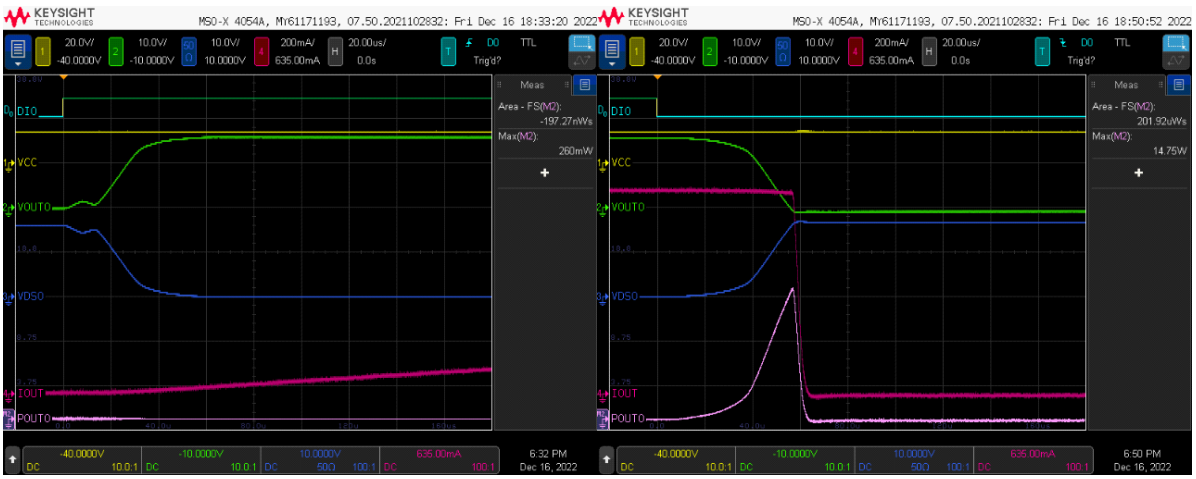
Note: The factor 3 is the result of experiment (see Table 11. Load classes used in capacitive load compatibility testing and Table 12. Maximum load capacity that can be turned on without limitation)

Measurement example 1–high inductance with external freewheeling (single event)

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 20 mH at 16 Ω
- External freewheeling diode: STPS2H100
- Device: VND9025AJ

Figure 43. **High inductance (T_{DEMAG} > t_{WOFF})–measurement example 1**



Measured losses (20 mH at 13.5 Ω): W_{ON} ~ 0 µJ, W_{OFF} ~ 202 µJ

Measured losses (pure resistive 13.5 Ω): W_{ON} ~ 88 µJ, W_{OFF} ~ 95 µJ

W_{ON} ratio (20 mH versus pure resistive): 0 / 88 = 0x

W_{OFF} ratio (20 mH versus pure resistive): 202 / 95 = 2.13x

The measured values confirm that the turn-on switching loss is negligible (zero starting current) while the turn-off switching loss is ~3x higher in comparison with pure resistive load.

Measurement example 2–high inductance with external freewheeling (single event)

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 1 mH at 2 Ω
- External freewheeling diode: STPS2H100
- Device: VN9004AJ

Figure 44. High inductance (T_{DEMAG} > t_{WOFF})–measurement example 2

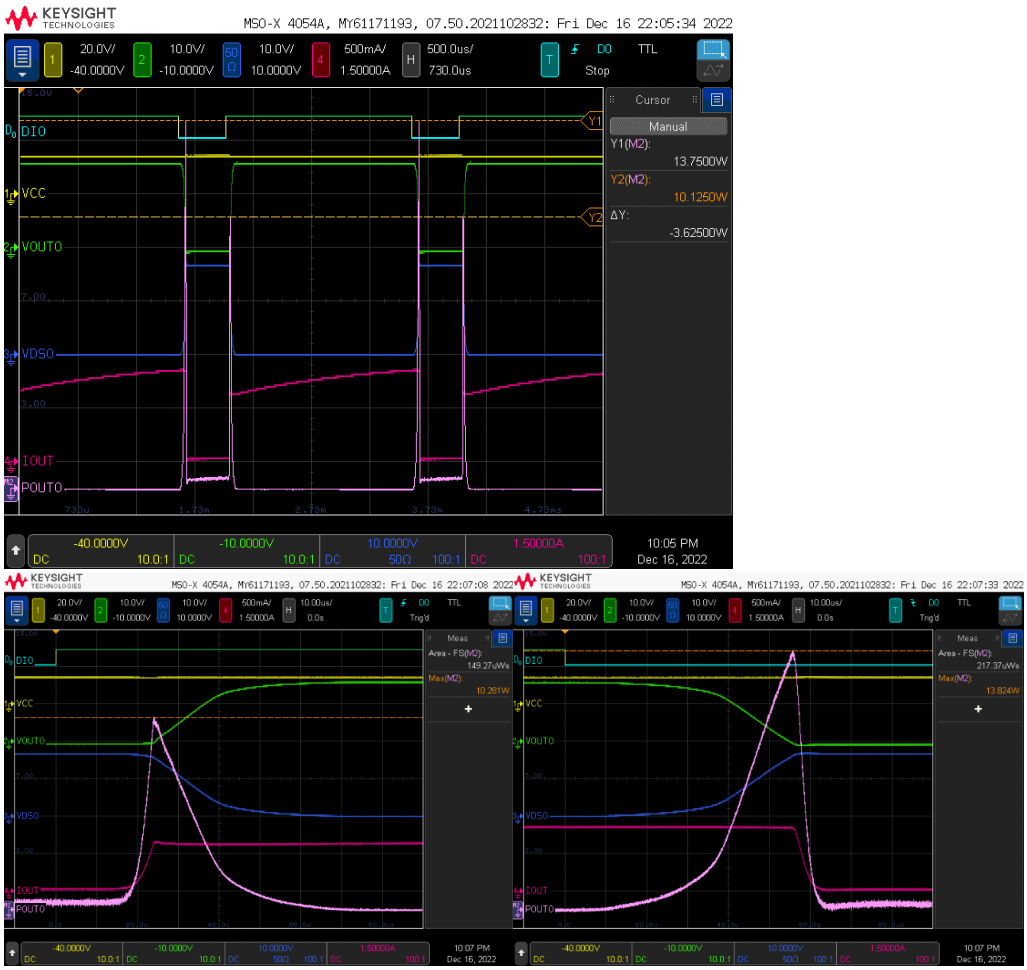
Measured losses (1 mH at 2 Ω): W_{ON} ~ 0 J, W_{OFF} ~ 2.5 mJ

Measurement example 3–High inductance with external freewheeling (PWM operation)

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 20 mH at 13.5 Ω
- External freewheeling diode: STPS2H100
- Device: VND9025AJ
- PWM: 80% at 500 Hz

Figure 45. **Figure 45: High inductance (T_{DEMAG} > T_{PWM_OFF})–measurement example 3**



Measured losses (20 mH at 16 Ω): W_{ON} ~ 149 µJ (I_{OUT} ~ 1 A), W_{OFF} ~ 217 µJ (I_{OUT} ~ 1 A)

Measured losses (resistive 16 Ω): W_{ON} ~ 88 µJ (I_{OUT} = 1 A), W_{OFF} ~ 95 µJ (I_{OUT} = 1 A)

W_{ON} ratio (20 mH versus resistive equivalent): 149 / 88 = 1.69x

W_{OFF} ratio (20 mH versus resistive equivalent): 217 / 95 = 2.28x

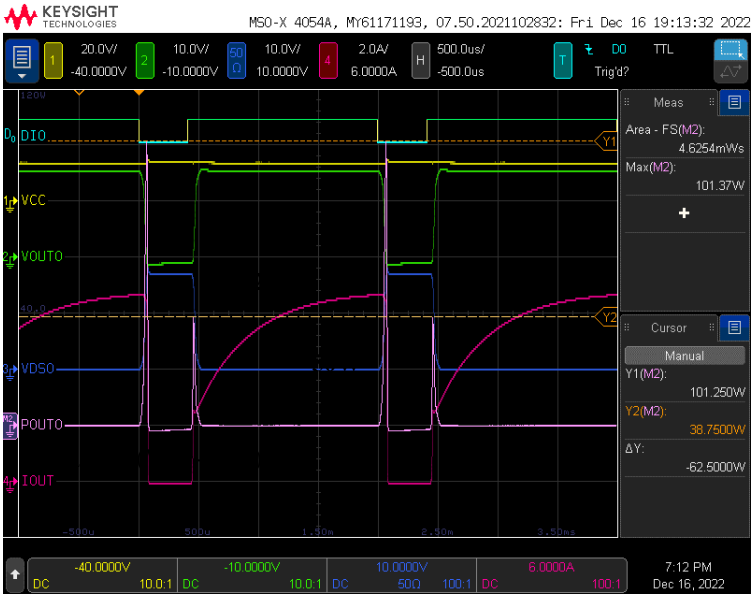
- The measured values confirm that the turn-on and turn-off losses are ~3x higher in comparison with equivalent resistive load.

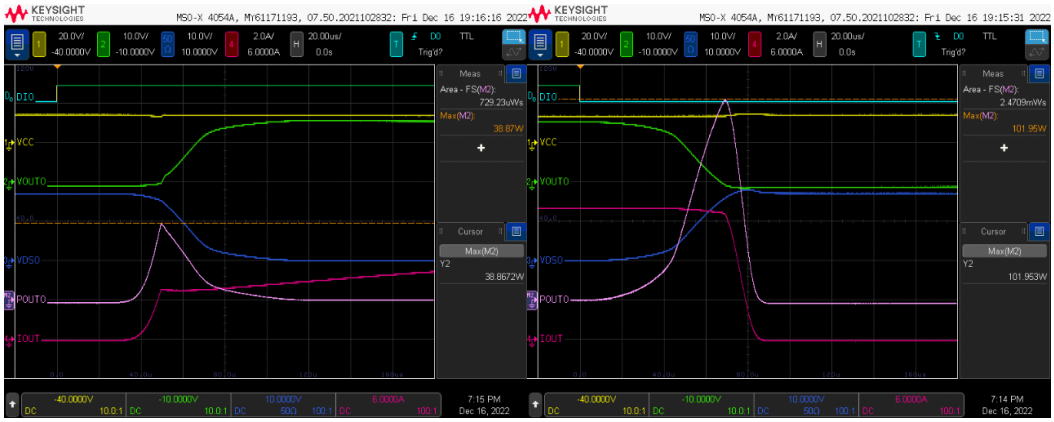
Measurement example 4–high inductance with external freewheeling (PWM operation)

Conditions:

- V_{BAT}: 16 V
- Temperature: 23 °C
- Load: 1 mH at 2 Ω
- External freewheeling diode: STPS2H100
- Device: VN9004AJ
- PWM: 80% at 500 Hz

Figure 46. **High inductance (T_{DEMAG} > T_{PWM_OFF})–measurement example 4**





Measured losses (1 mH at 2 Ω): W_{ON} ~ 0.73 mJ, W_{OFF} ~ 2.47 mJ

Measurement example–switching losses versus L (VND9025AJ)

In order to get a better idea about the switching losses dependency on the value of the inductance, a comparative measurement with different load inductances was performed on VND9025AJ. The summary of this measurement is shown in the tables below. The Table 15. VND9025AJ measurement of switching losses versus L in steady state describes the steady state operation (single turn-on / off event), with or without an external freewheeling diode. For each load inductance, there is a measurement of switching losses and switching times (time between 10-90% of nominal V_{OUT} considered). All switching losses are compared versus the resistive load. In the last column there is a calculation of demagnetization time (considering V_{DEMAG} = -30 V).

$_{VBAT}$ = 16 V single turn-on (I_{LOAD} = 0), single turn-off (I_{LOAD} = nominal = 1.0 A)

Table 15. VND9025AJ measurement of switching losses versus L in steady state

Load		W_{on}		W_{off}		W_{off} (with external freewheeling)		ton [µs]	toff [µs]	T_{demag} (calculated)
L [µH]	R [Ω]	[µJ]	Ratio vs res. load	[µJ]	Ratio vs res. load	[µJ]	Ratio vs res. load	10-90% of V_{out}	90-10% of V_{out}	(at -30 V) [µs]
1.5	16	95.8	1.09	123	1.29	122.2	1.29	25	25.2	0.0
15	16	87.5	0.99	128	1.35	130	1.37	25	25.4	0.4
60	16	75.8	0.86	145.6	1.53	146.3	1.54	25.4	24.7	1.6
300	16	42.6	0.48	277.4	2.92	207.8	2.19	25.2	23.7	8.0
1 000	16	22.6	0.26	650.8	6.85	241	2.54	24.3	32	26.7
3 500	16	16.6	0.19	1844	19.41	243	2.56	23.5	31	93.5
5 400	16	14.4	0.16	2688	28.29	243.7	2.57	22.3	30.9	144.3
20 000	16	14	0.16	11362	119.60	253.6	2.67	20.7	47.8	534.3

The Table 16. VND9025AJ measurment of switching losses versus L in PWM mode (with external freewheeling) describes the PWM operation with high duty cycle (shortest possible PWM off-time adjusted to have complete turn-off / on phase). The measurement was done with external freewheeling only (Schottky diode). In the last column there is a calculation of demagnetization time (considering V_{DEMAG} = -0.6 V).

V_{BAT} = 16 V PWM 94% at 500 Hz (120 µs off-time) ⇒ shortest possible for complete turn-off/on phase.

Table 16. VND9025AJ measurment of switching losses versus L in PWM mode (with external freewheeling)

Load		W_{on} (with external freewheeling)		W_{off} (with external freewheeling)		t_{on} [µs]	t_{off} [µs]	T_{demag} (calculated)
L [µH]	R [Ω]	[µJ]	Ratio vs res. load	[µJ]	Ratio vs res. load	(10-90% of V_{out})	(90-10% of V_{out})	(at -0.6 V) [µs]
1.5	16	89	1.01	107	1.13	23.4	24.1	0.31
15	16	86	0.98	114	1.20	23.5	24.3	3.11
60	16	72.4	0.82	138.6	1.46	23.8	23.8	12.45
300	16	37.8	0.43	192	2.02	23.5	22.8	62.25
1 000	16	26	0.30	229	2.41	22.8	22.6	207.51
3 500	16	91.4	1.04	242	2.55	21.5	22.5	726.30
5 400	16	117	1.33	240	2.53	21.5	22	1120.58
20 000	16	180	2.05	235	2.47	21.8	22	4150.29

1.5 µH ÷ 5.4 mH: air coil (1.5 mm^2 cable).

20 mH: iron powder core inductor (ISAT ~ 3 A).

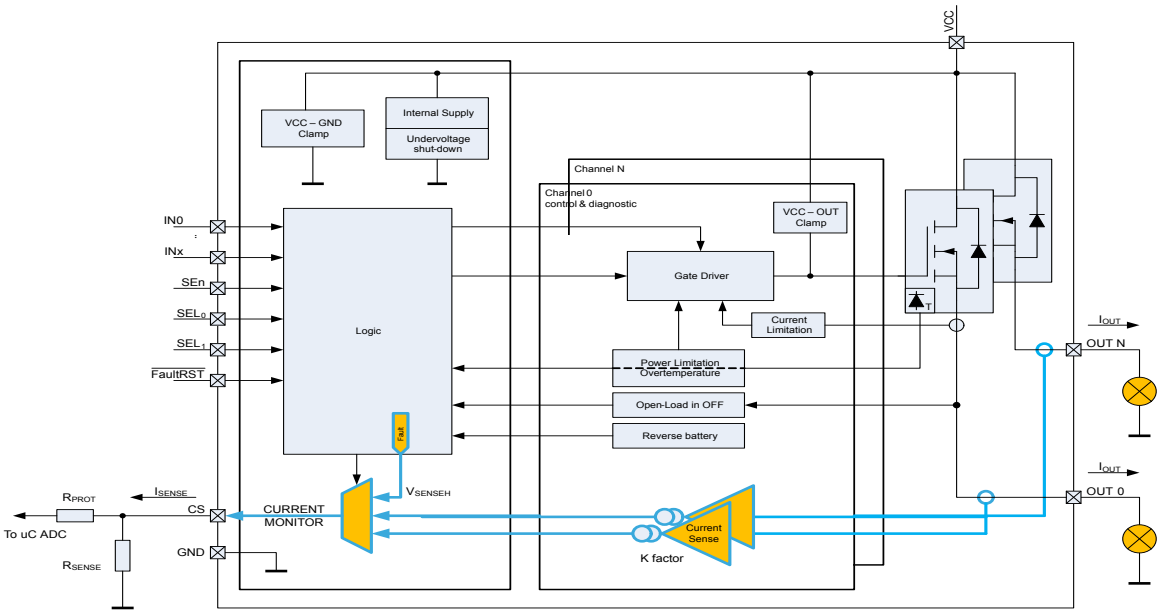
The coil resistance is compensated by adding a serial resistor to reach 16 Ω in total.

7 CS - analogue current sense

7.1 Introduction

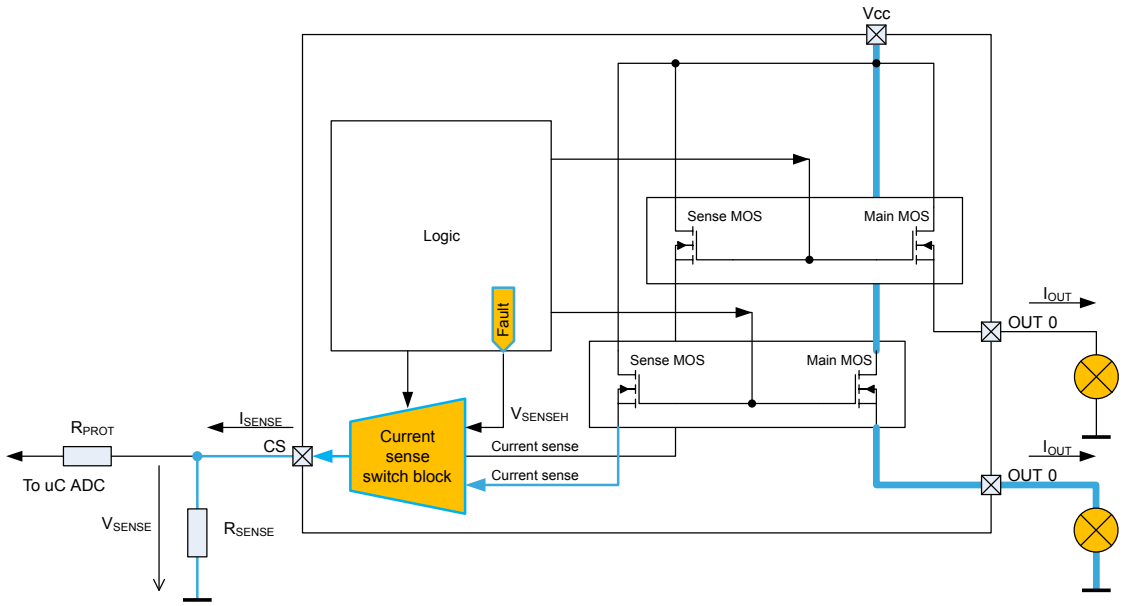
For diagnostic of M0-9 devices an analog monitoring output called current sense (CS) is used. Output is multiplexing analogue feedback of channels output current proportionally mirrored with high precision. Multiplexing is controlled by SELx and SEn pins. SELx pins specify the channel to be monitored, SEn pin allows to set CS output into an inactive - high-Z state.

Figure 47. M0-9 driver with analogue current sense–block diagram



7.2 Principle of current sense signal generation

Figure 48. Structure of current sense signal generation



In general, the current sense output signal operates for V_{CC} < 28 V capable to provide:

- Current mirror proportional to the load current in normal operation.

During no fault conditions (V_{OUT} > V_{OUT_MSD} - see datasheet value), the current flowing through main-MOS is mirrored through sense-MOS. Sense-MOS is a scaled down as copy of the main-MOS according to a defined geometric ratio. Current is passed through current sense switch block fully decoupling current sense signal from output current, delivering current proportional to the load according to known ratio named K.

The current delivered by the current sense circuit can be easily converted to a voltage by using an external sense resistor, allowing continuous load monitoring and abnormal condition detection.

- Diagnostics flag in fault conditions delivering fixed voltage with a certain current capability (up to I_{SENSE_SAT}) in case of:
  - Power limitation, overtemperature in on-state.
  - Short to V_{bat} / open-load in off-state (with external pull-up resistor) condition.

At fault condition, the internal logic switches the current sense output to deliver constant output voltage (named V_{SENSEH}).

7.2.1 Normal operation (channel ON, no fault, SEn active)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using the following simple equations:

Current provided by current sense (CS) output:

$$I_{SENSE} = \frac{I_{OUT}}{K} \tag{31}$$

While the voltage on R_{SENSE}:

$$V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE}\frac{I_{OUT}}{K} \tag{32}$$

Where:

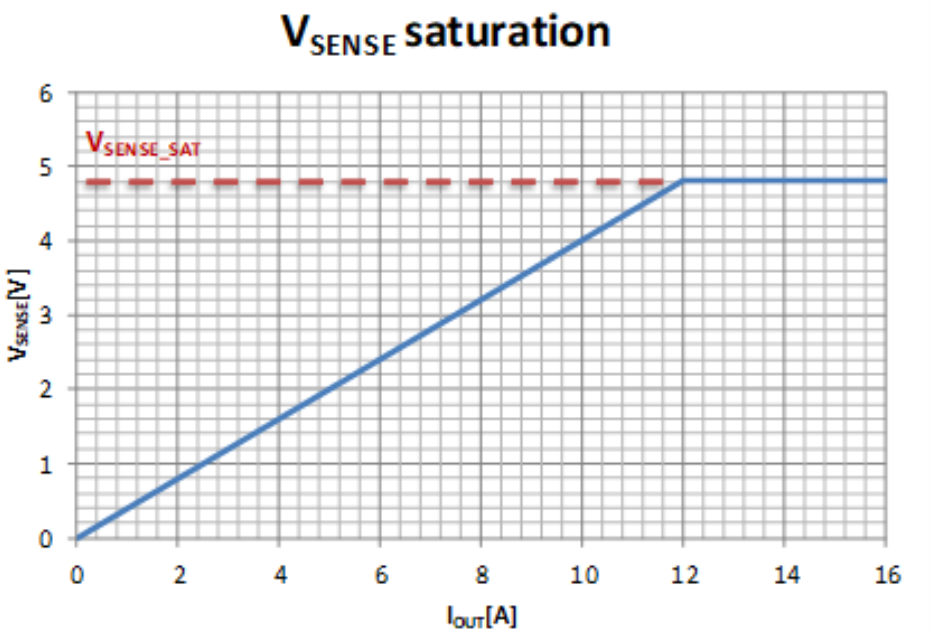
- V_{SENSE} is the voltage measurable on the R_{SENSE} resistor.
- I_{SENSE} is the current provided from the current sense pin in current output mode.
- I_{OUT} is the current flowing through output.
- K factor represents the ratio between Power-MOS cells and sense-MOS cells; Its spread includes geometric factor spread, current sense amplifier offset, and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE}.

7.2.2 Current monitoring range of linear operation

During the current monitoring the voltage on the current sense pin has a certain voltage depending on load conditions and R_{SENSE} value (as default value it can be assumed, for example, that current sense voltage at nominal load current is 1 V). Particular care must be taken for the proper dimensioning of the R_{SENSE} to ensure linearity in the whole load current range to be monitored (the full dimensioning rules on R_{SENSE} please see section 7.2.5). In fact, the current monitoring via current sense is guaranteed until a maximum voltage of 4.8 V (defined as the minimum value of V_{SENSE_SAT} in M0-9 datasheets).

1. EXAMPLE 1 - Current sense - voltage saturation
   VND9025AJ R_{SENSE} selected to have V_{SENSE} = 1 V at I_{OUT} = 2.5 A.
   Considering (for sake of simplicity) K_2 @ 2.1 A = 5000 (typical value)→ I_{SENSE} = I_{OUT} / K2 = 2.5 A / 5000 = 0.5 mA→R_{SENSE} = 1 V / 0.5 mA = 2 kΩ.
   Given a V_{SENSE_SAT} minimum (given in the datasheets) of 4.8 V, the maximum I_{SENSE} = 4.8 V / 2kΩ = 2.4 mA so to have still linearity, and assuming that K_2 remains constant, the maximum I_{OUT} ~ 12 A.
   In other words, with the selected R_{SENSE} any load current greater than 12 A will produce the same V_{SENSE} (see the figure below).

Figure 49. V_{SENSE} saturation example



Moreover, care must be taken to prevent the current mirror output from saturation, then causing again the I_{SENSE} no longer to be proportional to I_{OUT}. This normally happens when the maximum current from the current mirror is reached and corresponds to the minimum value of the parameter I_{SENSE_SAT} (I_{SENSE_SAT} minimum, reported in the datasheets).

2. EXAMPLE 2 - Current sense–current saturation

VND9025AJ R_{SENSE} selected in order to have V_{SENSE} = 2 V at I_{OUT} = 2.5 A.

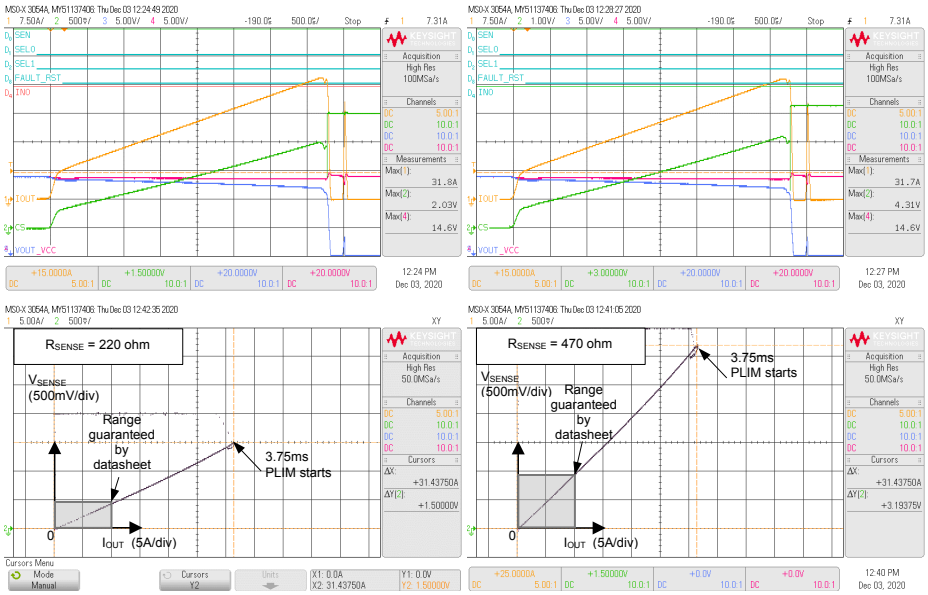
Considering an overload current of 5 A at 3.5 V of current sense pin analog voltage and I_{SENSE_SAT} = 2 mA minimum, R_{SENSE} has to fulfill the following formula:

$$R_{SENSE} > \frac{V_{SENSE}}{I_{SENSESATMIN}} = \frac{3.5V}{2mA} = 1.75k\Omega \quad (33)$$

In the figure below a measurement of current sense of VNQ9025AJ is given. Two different low R_{SENSE} values are connected to the current sense pin and the relevant range of V_{SENSE} versus I_{OUT} is highlighted. The guaranteed range of I_{SENSE} vs I_{out} of is specified by the datasheet parameter I_{OUT_SAT} – output saturation current. In the measured sample the I_{SENSE_SAT} = V_{SENSE} / R_{SENSE} is about 6.8 mA corresponding to a maximum monitorable current of about 30 A.

Plotted V_{SENSE} with increasing I_{OUT} versus time with R_{SENSE} = 220 Ω (left) and R_{SENSE} = 470 Ω (right) for VNQ9025AJ and corresponding XY plot (V_{CC} = 14 V)

Figure 50. **Plotted V_{SENSE}**



Note: V_{SENSE_SAT} and I_{SENSE_SAT} minimum values are guaranteed for the minimum V_{CC} voltage in which all K factor limits are guaranteed (in datasheets this is 7 V) and maximum operating junction temperature (in datasheets this is 150 °C) which represent worst case conditions in the assessment of the maximum load current to be monitored.

Note: Experimental measurements on samples have been performed plotted V_{SENSE} with increasing I_{OUT} versus time with R_{SENSE} = 220 Ω (left) and R_{SENSE} = 470 Ω (right) for VNQ9025AJ and corresponding XY plot (V_{CC} = 14 V).

In Figure 51. Behavior of V_{SENSE_SAT} vs V_{CC} and Figure 52. Behavior of I_{SENSE_SAT} vs V_{CC} plots extracted from experimental data at 25 °C are shown for V_{SENSE_SAT} and I_{SENSE_SAT} respectively. The voltages in the plots refer to module GND so they include the voltage drop on the GND network of about 300 mV.

Figure 51. **Behavior of V_{SENSE_SAT} vs V_{CC}**

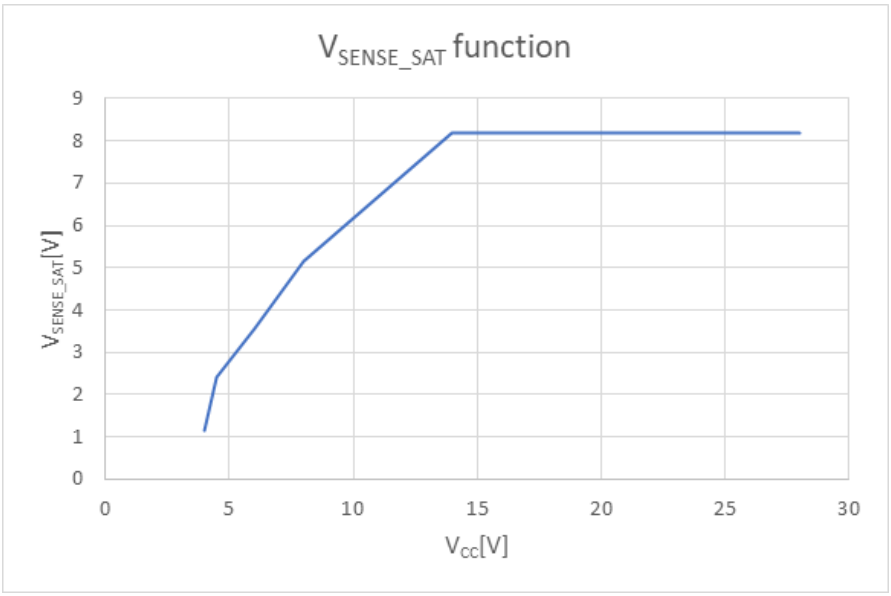
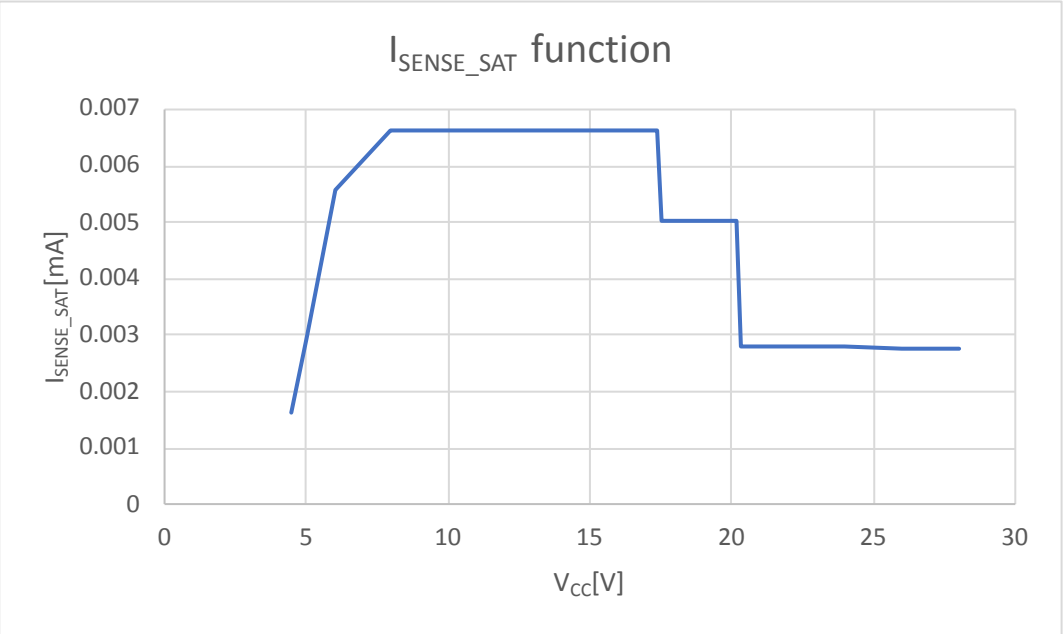


Figure 52. **Behavior of I_{SENSE_SAT} vs V_{CC}**



The I_{SENSE_SAT} decreases significantly for V_{CC} below about 7 V. Above this battery level, there are visible three different I_{SENSE_SAT} steps, corresponding with ILIMH levels at different supply voltage ranges.

Note: The current sense current monitoring linear behavior is featured down to a V_{CC} = 4.5 V and for V_{SENSE} < V_{CC} – 1.5 V (even though relevant specification limits reported in datasheets are not guaranteed anymore).

7.2.3 Impact of the output voltage to the current sense output

The current sense operation for load current approaching the current limitation is not guaranteed and predictable. Indeed, because of the intervention of the current limiter, the output voltage can drop significantly, up to approximately 0 V in the extreme case of a hard short circuit.

Being the whole circuit referred to V_{OUT}, ambiguous and unreliable current values could be sourced by the current sense under such conditions.

In order to bring the current sense into a defined state, a dedicated circuit section shuts down the current sense circuitry when V_{OUT} drops below the threshold V_{OUT_MSD} (typically 5 V).

In conclusion, in normal operation the current sense works properly within the described border conditions. For a given device, the I_{SENSE} is a single value monotonic function of the I_{OUT} as long as the maximum V_{SENSE} (1st example) or the current sense saturation (2nd example) are reached, that is, there is no chance to have the same I_{SENSE} for different I_{OUT} within the given range.

7.2.4 Failure flag indication

In case of power limitation or overtemperature or open load/short to V_{CC} in OFF state, the fault is indicated by the current sense pin which is switched to a “current limited” voltage source.

Indeed, with reference to Figure 48. Structure of current sense signal generation whenever a power limitation / overtemperature condition is reached, the current sense output is internally pulled up to V_{SENSEH}.

The current sense output, in those events are controlled in such a way to develop at least a voltage of V_{SENSEH}(given in the datasheet) across the external sense resistor.

In any case, the current sourced by the current sense in this condition is limited to the I_{SENSEH} (given in the datasheet). In order to allow the current sense pin to develop at least V_{SENSEH} = 6 V, a minimum sense resistor value must be set (for details see section Section 7.2.5: Considerations on current sense resistor choice for current monitor).

The typical behavior of a M0-9 high side driver in case of overload or hard short circuit is shown in the following figures FaultRST set low - auto restart mode:

Figure 53. Failure flag indication - example 1

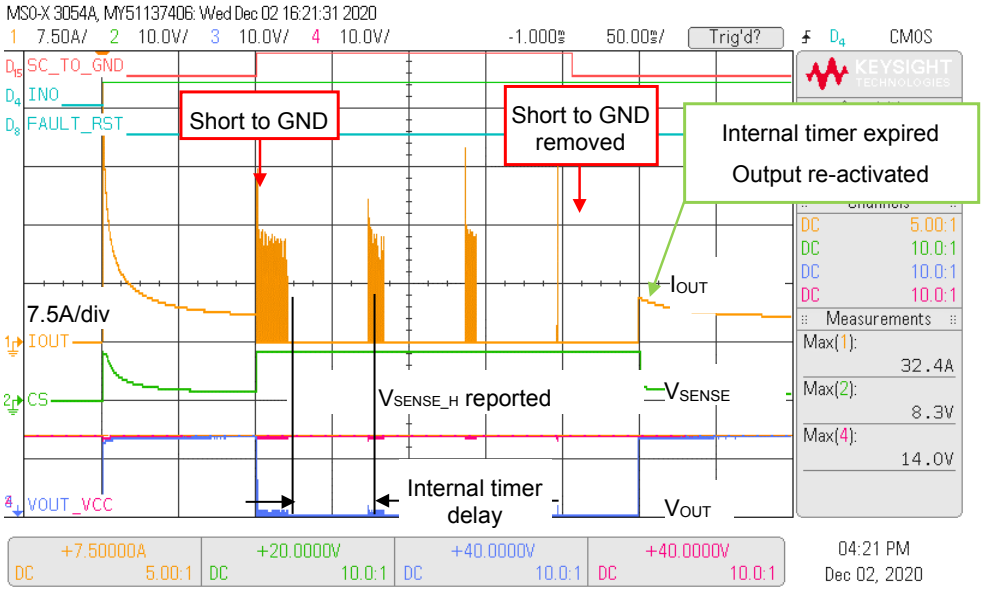
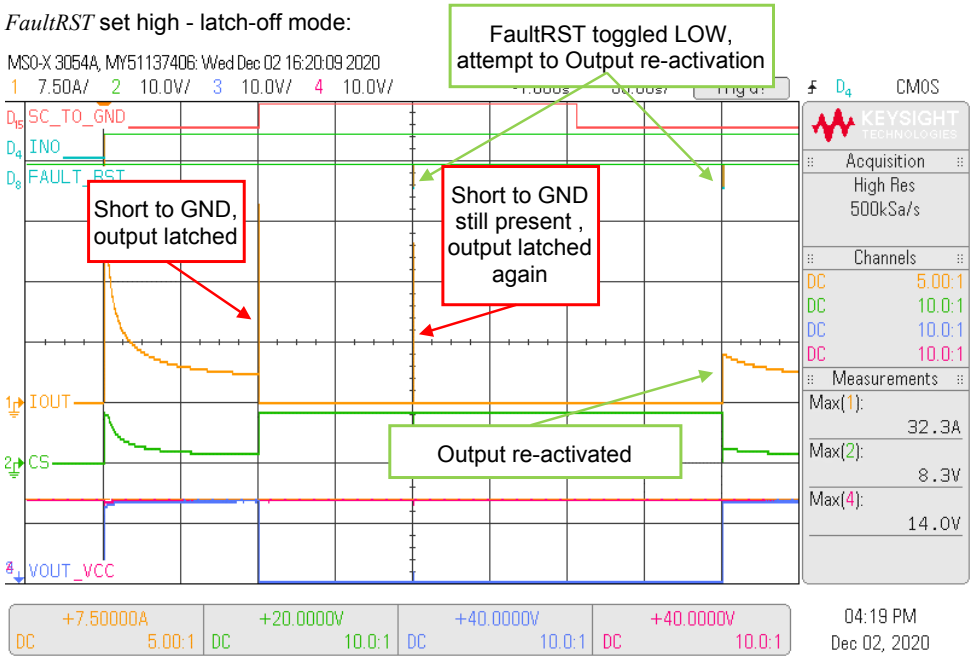


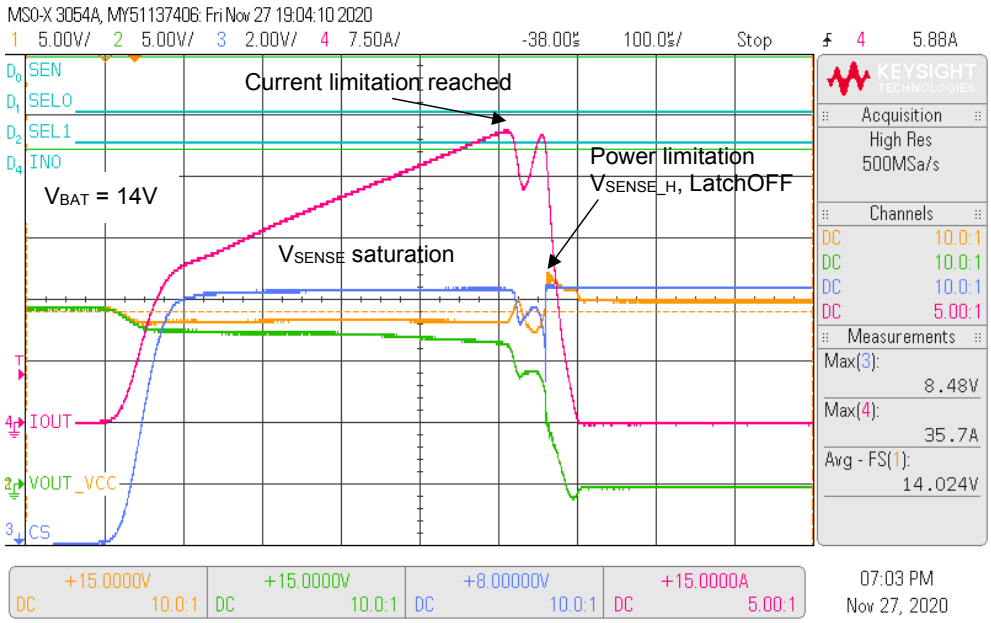
Figure 54. Failure flag indication - example 2



An example of a condition with a progressive increasing of the output current (single shot ramp) by an electronic load supplied by VNQ9025AJ is shown in the figure below. The sense resistor is 2.2 kΩ. The device is set in latch-off mode. The saturation voltage V_{SENSE_SAT} is reached and then the current limitation I_{LIM_H} : afterwards, the thermal protection acts. At this point the current sense (CS) pin issues V_{SENSE_H} voltage and latch. Since, in this case, the FaultRST pin is set high (latch off) the power MOS remains off.

Current sense operation of VND9025AJ in current monitoring with increasing overload and consequent device's latch off due to thermal protection intervention.

Figure 55. Current sense operation of VND9025AJ



Note: Current sense operation of VND9025AJ in current monitoring with increasing overload and consequent device's latch off due to thermal protection intervention.

7.2.5 Considerations on current sense resistor choice for current monitor

In normal operating conditions, the following equation describes the relation between I_{OUT} and V_{SENSE}

$$V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \frac{I_{OUT}}{K} [V] \quad (34)$$

The design value of sense resistor can be calculated from the above equation given the intended voltage at the ADC with the nominal load current and the typical K factor of the device.

The calculated sense resistor implies the following considerations that the hardware designer has to consider:

1. In normal operating conditions, in order not to reach current sense voltage saturation V_{SENSE_SAT} , with the maximum load current that can be read I_{OUT_MAX} , the R_{SENSE} has to fullfill the following equation:

$$R_{SENSE} < K_{MIN} \frac{V_{SENSE\_SAT\_MIN}}{I_{OUT\_MAX}} [V] \quad (35)$$

   Within this maximum current linearity of current sense is guaranteed. If a lower maximum load current needs to be read, like for example in case a LED string, the R_{SENSE} value must be increased.

2. In normal operating conditions , the maximum sense voltage that can be read with the given R_{SENSE} must be higher than a certain ADC threshold. This can be expressed by the following equation:

$$R_{SENSE} > \frac{V_{SENSE:MAX}}{I_{SENSE\_SAT\_MIN}} \quad (36)$$

   Where $V_{SENSEMAX}$ is the maximum voltage that the ADC has to read at the maximum monitored load current. This value can be below or equal 5 V which normally is the maximum operating range of the ADC.

3. In fault conditions (overload, short-circuit to GND that cause power limitation or thermal shutdown and in open load/short to battery in OFF state), to be able to differentiate a normal operating condition from a fault condition, the current sense pin must be capable to develop a voltage above the V_{SENSEH}(value given in the datasheet, V_{SENSEH} = 8 V typically). Therefore the following conditions must be fulfilled:

$$R_{SENSE} > \frac{V_{SENSE\_H\_min}}{I_{SENSE\_H\_min}} \quad (37)$$

4. Finally the current sense resistor is necessary to protect the current sense pin in case of reverse battery. During this event an intrinsic diode between current sense and Vcc pins is forward biased, and the resulting current must be limited (in the datasheet the maximum current sense current that can flow in reverse battery condition is indicated in the absolute maximum ratings table). This value is given in the absolute maximum ratings section of M0-9 datasheets (I_{SENSE} value, in case of VNQ9025AJ this is 20 mA), therefore the minimum R_{SENSE} to protect the current sense pin in case of reverse battery (supposing a static condition of V_{CC} = -16 V) is

$$R_{SENSE} > \cdot \frac{-V_{cc} - V_F}{I_{SENSE\_rev\_max} \frac{16V - 0.7V}{20mA}} \quad (38)$$

In conclusion the R_{SENSE} value must fulfill two opposite conditions for having linearity in normal operating condition: one is avoiding current sense pin current saturation (increase R_{SENSE}), and the other is avoiding current sense pin voltage saturation (decrease of R_{SENSE}). Moreover, the R_{SENSE} value must be dimensioned to distinguish a normal operating condition (linear mode, V_{SENSE} proportional to load current) from a fault condition (constant voltage generator developing V_{SENSE_H} across the R_{SENSE}).

An example about the R_{SENSE} value definition is shown:

Example: Let's consider the VND9025AJ (25 mΩ HSD) with a nominal load current I_N = 2 A which corresponds to an intended V_{SENSE} = 2 V and typical K_2 = 5000 (from datasheet). Let us apply above Eq. (38)

$$R_{SENSE} = K \cdot \frac{V_{SENSE}}{I_{OUT}} = 5000 \cdot \frac{2}{2} = 5k\Omega \quad (39)$$

Let us suppose that the maximum load current the ADC must monitor in linearity is 2 times the nominal current so to say 4 A at $V_{SENSEMAX}$ = 4 V. So, this means that neither V_{SENSE_SAT} nor I_{SENSE_SAT} must be reached and in fault conditions a voltage above 4.8 V must be issued. Let us verify that the R_{SENSE} value chosen is the correct one by applying the above equations Eq. (35), Eq. (36) and Eq. (37):

$$R_{SENSE} < K_{2MIN} * \frac{V_{SENSESATmin}}{I_{OUTMAX}} \approx (5000 - 5000*0.07) * \frac{4.8}{4} = 5.58k\Omega \quad (40)$$

$$R_{SENSE} > \frac{V_{SENSE:MAX}}{I_{SENSE\_SAT\_MIN}} = \frac{4V}{2mA} = 2k\Omega \quad (41)$$

$$R_{SENSE} > \frac{V_{SENSEHmin}}{I_{SENSEHmin}} = \frac{5V}{7mA} = 714\Omega \quad (42)$$

So, the chosen sense resistor of 5 kΩ is correct.

7.2.6 Usage when multiplexing several devices

If several devices are supposed to share one R_{SENSE} resistor, for proper diagnostic only one current sense of each device at a time should be activated.

All other devices sharing the R_{SENSE} should apply the high-Z state on current sense output (SEn=L). In this case, R_{SENSE} is supplied from one device at a time.

If, by mistake more than one current sense is activated, the current sense output in current mode draws a current in the shunt resistor R_{SENSE} defined as:

$$I_{SENSE} = \sum I_{SENSE[N]} \quad (43)$$

where [N] is the number of devices with enabled current output.

There must be considered the possibility of V_{SENSE} saturation (range of linear operation), since current delivered from multiple devices increase voltage drop on R_{SENSE}.

In the case of one device is switched to voltage output (due to fault condition), diagnostic for other devices cannot be applied (since V_{SENSEH} is applied to R_{SENSE}).

7.2.7 LED diagnostic

Diagnostic in OFF state

Considering diagnostic of LED loads, there appears specific situation during diagnostic in the OFF state. While the pull-up resistor is applied during OFF state diagnostic (allowing distinguish between output "short to V_{CC}" and "open-load"), current flowing through the pull-up resistor can create unintended LED light emission.

To prevent such a situation, external circuitry inside the LED load, or a pull-down structure on device level is needed to create sufficient load for detection, without side effect of LED lightning.

Without external circuitry on LED loads, diagnostic in off state is not recommended.

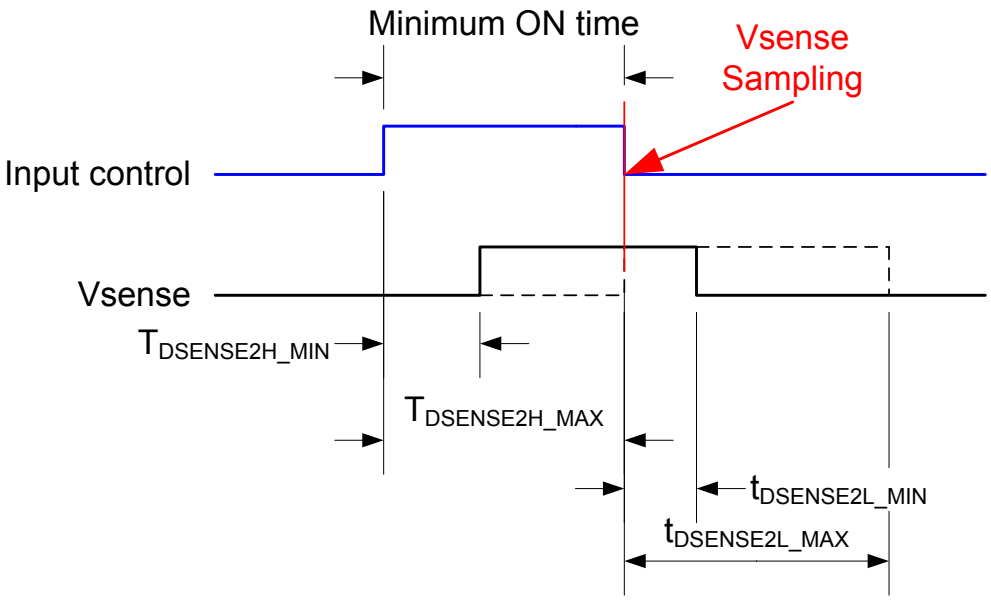
Diagnostic in ON state

Since LED loads are usually driven by PWM signal at low duty cycles, there arise limitations for diagnostic in ON state as well.

Considering the spread of time delay between input switched and current sense output signal (specified in datasheet by $T_{DESENSE2H}$), there is a minimum required ON time, for which diagnostic is possible:

Minimum duty cycle calculation:

Figure 56. Minimum ON time for correct V_{SENSE} sampling



$t_{DSENSE2H}$ ~250 µs (maximum datasheet value).

$t_{ON\_MINIMUM}$ = $t_{DSENSE2H}$ = 25 0µs.

Considering PWM frequency 200Hz →

$$T_{PERIOD} = \frac{1}{200Hz} = 5ms \quad (44)$$

Duty cycle corresponding to

$$t_{ON\_MINIMUM} = 100\% \cdot \frac{250}{5000} = 5\% \quad (45)$$

Result: At PWM frequency 200 Hz, minimum duty cycle is 5% for valid V_{SENSE} diagnostic.

Minimum operating current

Distinguishing between open load and low current load is possible without calibration, as listed in on following example.

Taking reference values of the VNQ9025AJ datasheet: minimum K_{OL} = 2670 at a specified current of 10 mA, considered as maximum failure current gives maximum :

$$I_{OL\_SENSE\_MAX} = \frac{0.01A}{2670} = 3.74\mu A \quad (46)$$

For an output current of 50 mA, considered as detectable load I_{SENSE}, the minimum sense current can be calculated as follows:

$$I_{SENSE\_MIN} = \frac{I_{OUT}}{K_{OUTMAX(@I_{OUT})}} \quad (47)$$

Since the K_{OUTMAX} is not specified for selected evaluated current $I_{OUT} = 50mA$ by the datasheet, linear interpolation is applied to get K factor at such load current.

From the datasheet, two nearest K factors sorrounding the evaluated I_{OUT} are chosen. In the VNQ9025AJ datasheet those are:

$$K_0(I_{OUT0} = 25mA) = 5000 \quad (48)$$

and

$$K_1(I_{OUT1} = 500mA) = 5000 \quad (49)$$

As we are evaluating the minimum I_{SENSE} current corresponding to the measured output current, the K factors are applied with an upper tolerance range:

$K_{0MAX}(I_{OUT0} = 25mA) = 5000$ increased by 35% tolerance, we get $K_{0\_MAX} = 5000*1.35 = 6750$ and $K_{1MAX}(I_{OUT1} = 500mA) = 5000$ increased by 15% tolerance $K_{1\_MAX} = 5000*1.15 = 5750$

Applying the linear interpolation function

$$K = f(I_{OUT}) \quad (50)$$

$$K = a*I_{OUT} + b \quad (51)$$

For two known points

$$K_0 = a*I_{OUT0} + b \quad (52)$$

$$K_1 = a*I_{OUT1} + b \quad (53)$$

Solving these equations we get

$$a = \frac{K_0 - K_1}{I_{OUT0} - I_{OUT1}} \quad (54)$$

and

$$b = \frac{K_1*I_{OUT0} - K_0*I_{OUT1}}{I_{OUT0} - I_{OUT1}} \quad (55)$$

Entering K_0, I_{OUT0}, K_1 and I_{OUT1} data to the solved equation we get coefficients for the K function:

$$a = \frac{6750 - 5750}{0.025 - 0.5} = \frac{100}{-0.475} = -2105.3 \quad (56)$$

and

$$b = \frac{5750*0.025 - 6750*0.5}{0.025 - 0.5} = 6802.6 \quad (57)$$

Results to

$K = -2105.3*I_{OUT} + 6802.6$ applicable for the IOUT in the range from I_{OUT0} = 0.025 A to I_{OUT1} = 0.5 A

For evaluated $I_{OUT} = 50mA$, we can then calculate the KMAX as

$K_{MAX}(@I_{OUT} = 50mA) = -2105.3*0.05 + 6802.6 = 6697$

Putting the K_{MAX} to the I_{SENSE} calculation

$$I_{SENSE\_MIN} = \frac{I_{OUT}}{K_{OUTMAX}(@I_{OUT})} = \frac{0.05A}{6697} \doteq 7.47\mu A \quad (58)$$

Results show, that differentiation between open load of 10 mA ($I_{OL\_SENSE\_MAX} = 3.74\mu A$)and load current of 50 mA ($I_{SENSE\_MIN} = 7.47\mu A$) is possible without calibration.

Diagnostics with different load options

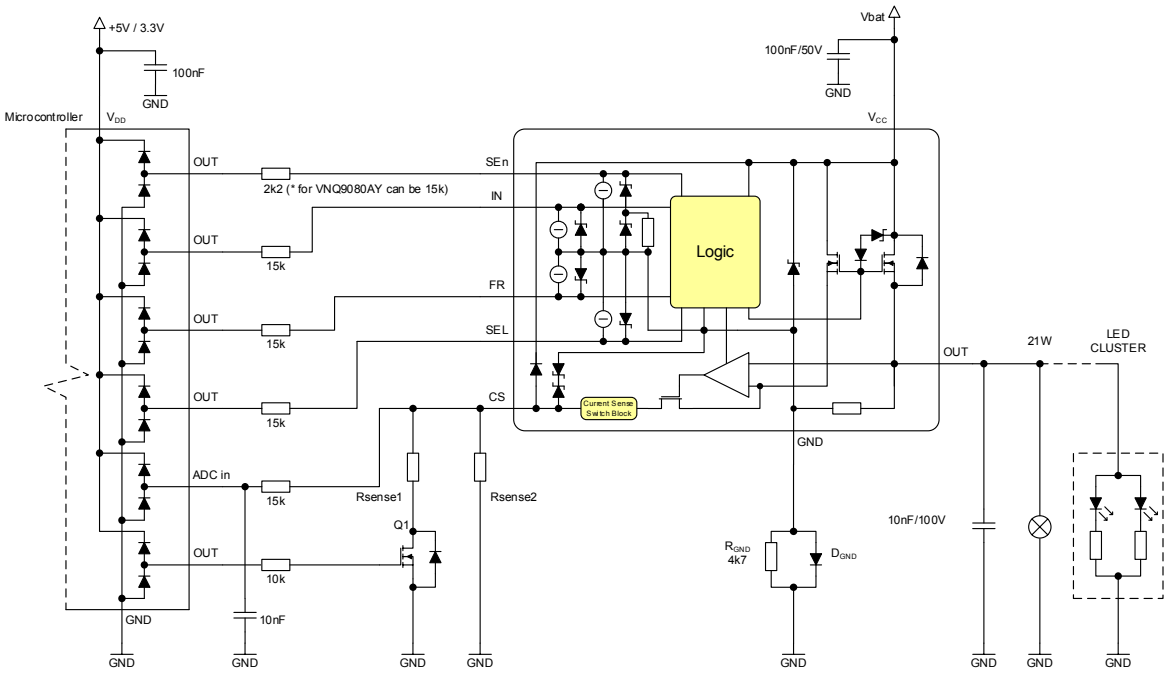
In some cases, the requirement profile asks for alternative loads driven with one and the same high side driver. This could be a bulb lamp with the alternative of an LED (- cluster). In this case the driver:

- Has to handle the high inrush current of the bulb load.
- It has to provide a power dissipation low enough during continuous operation.
- Must not indicate an open load in case of an LED (-cluster) is applied instead of a bulb.

In case of different load options (bulb / LED) there is the possibility to use two different (switch able) sense resistors in order to have the current sense band in the appropriate range matching the different load currents.

An example of a current sense resistor switching circuit can be seen in the figure below. The measured scale can be extended by R_{SENSE1} switched in parallel to R_{SENSE2} by MOSFET Q1.

Figure 57. **Switched current sense resistor**



7.2.8 Diagnostic with paralleled load / partial load detection

Table 17. **Paralleling bulbs–overview on the example of VND9012AJ**

Load	Failure case
2x21W	Failure of one 21 W detectable without calibration
2x27W	Failure of one 27 W detectable without calibration
21W + 5W	Failure of 21 W detectable without calibration, failure of 5 W cannot be detected
2x21W + 5W	Failure of 21 W detectable without calibration, failure of 5 W cannot be detected
2x27W + 5W	Failure of one 27 W detectable without calibration, failure of 5 W cannot be detected

The table above, shows a set of cases where bulbs in parallel, driven by the suitable M0-9 HSD (see as reference in section 6.1) channel are used. The M0-9 HSD family allows the detection of individual bulb failures when in a parallel arrangement. However, if we consider the bulb wattage spread, the HSD K-factor tolerance, the variation of bulb currents vs. V_{BAT} and the resolution of the ADC it is clear that accurate failure determination can be difficult in some cases. For example if there are bigger and smaller bulbs paralleled the detection limit for the lowest power bulb is lost in the tolerances.

To achieve better current sense accuracy, the current sense calibration (K factor measurement) of each HSD can be adopted. This is the subject of the following section.

7.2.9 K factor calibration method

In order to reduce the V_{SENSE} spread, it is possible to reduce the K spread and eliminate the R_{SENSE} variation by adding a simple test (calibration test) at the end of the module production line.

Single point calibration on low current

K factor can be calibrated in “single point” by measurement of I_{SENSE} for specified I_{OUT}.

K is then calculated as

$$K_{CALIBRATED} = \frac{I_{OUT}}{I_{SENSE}} \quad (59)$$

For low currents diagnostic using single point calibration method, it is possible distinguish between open-load (<10 mA) and low current (limit depending on device R_{DSON};

for example VNQ9025AJ datasheet specifies low current level > 25 mA).

For calibration of K factor at I_{OUT} =17.5 mA, T_J =25 °C and V_{CC} = 13 V, in the datasheet of VNQ9025AJ there is specified a maximum drift of K factor ±25% in range I_{OUT} =10 to 25 mA , temperature range of T_J = -40 ºC to+150 ºC and battery range V_{CC}= 7 V to 18 V.

All these parameters allow clear distinguishing between minimum and maximum I_{OUT} within specified range.

Following example shows detection thresholds with no overlapping zone between maximum V_{SENSE} corresponding to open load threshold (at 10mA) and minimum V_{SENSE} corresponding to minimum load (at 25 mA)

Example 3:

I_{OUT} = 17.5 mA

R_{SENSE} = 10 kΩ

V_{SENSE} = 35.1 mV – measured value

$$K_{CALIBRATED} = \frac{I_{OUT}}{I_{SENSE}} = \frac{I_{OUT}}{\frac{V_{SENSE}}{R_{SENSE}}} = \frac{17.5mA}{\frac{35.1mV}{10k\Omega}} \doteq 4986 \quad (60)$$

$$K_{MIN} = K_{CALIBRATED}(-25\%) = 4986 \cdot 0.75 \doteq 3739 \quad (61)$$

$$K_{MAX} = K_{CALIBRATED}(+25\%) = 4986 \cdot 1.25 \doteq 6232 \quad (62)$$

Maximum V_{SENSE} level for open-load detection is then

$$V_{SENSE\_OL} = R_{SENSE} \cdot \frac{I_{OUT}}{K_{MIN}} = 10000 \cdot \frac{10mA}{3739} = 26.7mV \quad (63)$$

And following minimum V_{SENSE} for low current load (at 50 mA)

$$V_{SENSE\_LOAD} = R_{SENSE} \cdot \frac{I_{OUT}}{K_{MAX}} = 10000 \cdot \frac{25mA}{6232} = 40.1mV \quad (64)$$

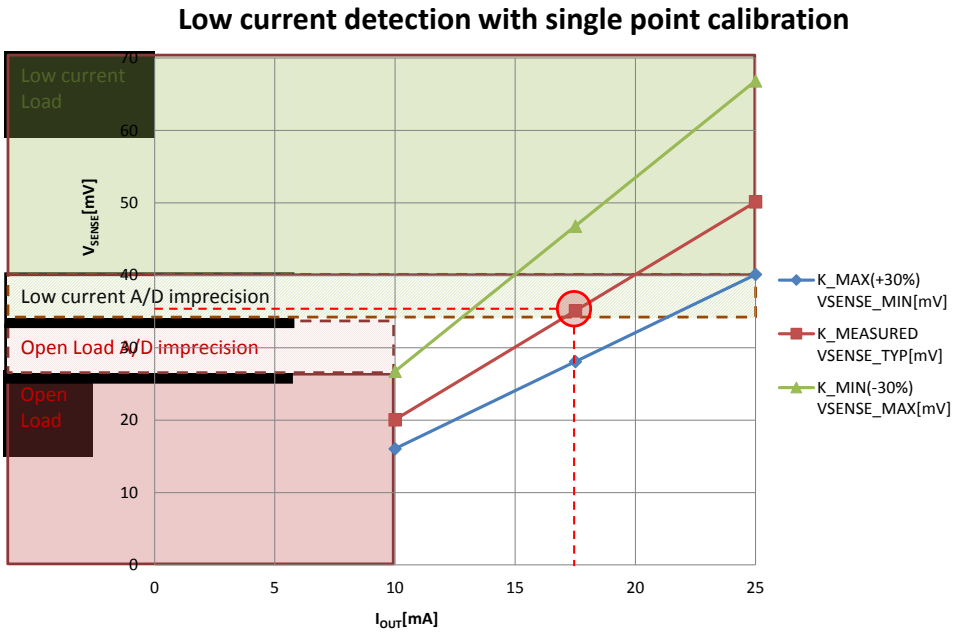
Considering 12-bit A/D converter for V_{SENSE} monitoring with error of 2LSB bits and measurement range 0 - 5 V , gives precision $\pm 2(LSB) \cdot \frac{5V}{4096} = \pm 2.5mV$

Considering a maximum leakage of ± 0.1□A of the ADC, this causes on the 15 kΩ ADC series resistor, an error on ADC voltage of ±1.5 mV. Even applying these errors, result is a non-overlapping threshold for detection of:

- open-load (I_{OUT} < 10 mA), where V_{SENSE} < 26.7 mV ± 2.5 mV± 1.5 mV → max. 30.7 mV
- minimum load(I_{OUT} > 25 mA), where V_{SENSE} > 40.1 mV ± 2.5 mV± 1.5 mV → min. 36.1 mV

The Figure 58. Example of single point calibration at low current for VNQ9025AJ gives a graphical explanation of the example 3.

Figure 58. **Example of single point calibration at low current for VNQ9025AJ**



Two points calibration - how the calibration works.

To calibrate means to measure on a specific device soldered in a module the K ratio at a given output current by a V_{SENSE} reading. Since the relation of I_{OUT}= I_{SENSE}• K is known, it is then easy to calculate the K ratio. However, even if the K ratio measured in a single point eliminates the parametric spread, it does not eliminate the V_{SENSE} variation due to the K dependency on output current.

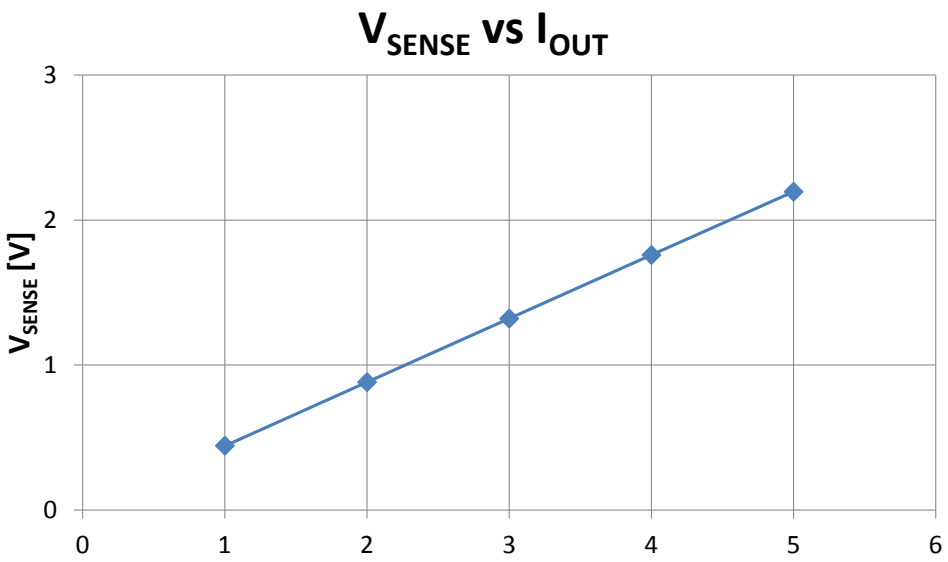
This variation can be eliminated doing the following considerations:

The Table 18. V_{SENSE} measurement and Figure 59. V_{SENSE} vs I_{OUT} measurement show a V_{SENSE} measurement on a sample of VNQ9025AJ with R_{SENSE} = 2.2 kΩ.

Table 18. **V_{SENSE} measurement**

I_{OUT} [A]	V_{SENSE} [V]
1	0.442
2	0.882
3	1.321
4	1.759
5	2.195

Figure 59. V_{SENSE} vs I_{OUT} measurement



The trend is almost linear in the application range and then we can approximate the V_{SENSE} trend with the following equation:

$$V_{SENSE} = m \cdot I_{OUT} + a \quad (65)$$

Where “m” [Ω] is the rectangular coefficient and “a” [V] is a constant.

Inverting this equation, it is easy to get a relation where the output current can be calculated as:

$$I_{OUT} = M \cdot V_{SENSE} + b \quad (66)$$

Instead of $I_{OUT} = I_{SENSE} \cdot K$, once M [S] and b are known, it is possible to evaluate the I_{OUT} with a high accuracy leaving only the spread due to the temperature variation.

The current sense ratio maximum fluctuation is expressed in the datasheet with the parameter dK/K (maximum relative error in the full current sense V_{CC} and T_J specification range versus K at V_{CC}= 13 V and T_J = 25 °C).

How to calculate M and b

To calculate M and b two simple measurements, done at the end of the production line, are needed. Chosen two reference output currents, I_{REF1} and I_{REF2}, the relevant V_{SENSE1} and V_{SENSE2} have to be measured. Then these 4 values can be stored in an EEPROM in order to let the µC use this information to calculate M and b using the simple formulas reported below.

Since we defined

$$I_{OUT} = M \cdot V_{SENSE} + b \quad (67)$$

it is also true that:

$$I_{REF1} = M \cdot V_{SENSE1} + b \quad (68)$$

And

$$I_{REF2} = M \cdot V_{SENSE2} + b \quad (69)$$

Solving these two equations we get the following relations:

$$I_{OUT} = M \cdot V_{SENSE} + b \quad (70)$$

$$M = \frac{I_{REF1} - I_{REF2}}{V_{SENSE1} - V_{SENSE2}} \quad (71)$$

$$b = \frac{I_{REF2} \cdot V_{SENSE1} - I_{REF1} \cdot V_{SENSE2}}{V_{SENSE1} - V_{SENSE2}} \quad (72)$$

Example 4: M, b calculation for the chosen device.

Fixing I_{REF1} = 2 A and I_{REF2} = 4 A according to Table 18. V_{SENSE} measurement, we get V_{SENSE1} = 0.882 V and $_{SENSE2}$ = 1.759 V, then:

M = 2.281 [S]

b = -0.011 [A]

I_{OUT} is then:

$$I_{OUT} = 2.281 \cdot V_{SENSE} - 0.011 \quad (73)$$

An easy algorithm can give the M and b values. During the EOL the pairs (V_{SENSE1}, I_{REF1}) and (V_{SENSE2}, I_{REF2}) or alternatively only M and b can be stored in the microcontroller relevant EEPROM. After the calibration the current sense variation is still influenced by the device temperature. Eq. (73) is still affected by an error proportional to the sense current thermal drift.

This drift is reported in the datasheet as dK/K. The drift decreases when increasing the output current, e.g. in the VNQ9025AJ-E datasheet the drift is +/-25% at 0.01 A and it decreases down to +/-5% when the output current is 6.3 A.

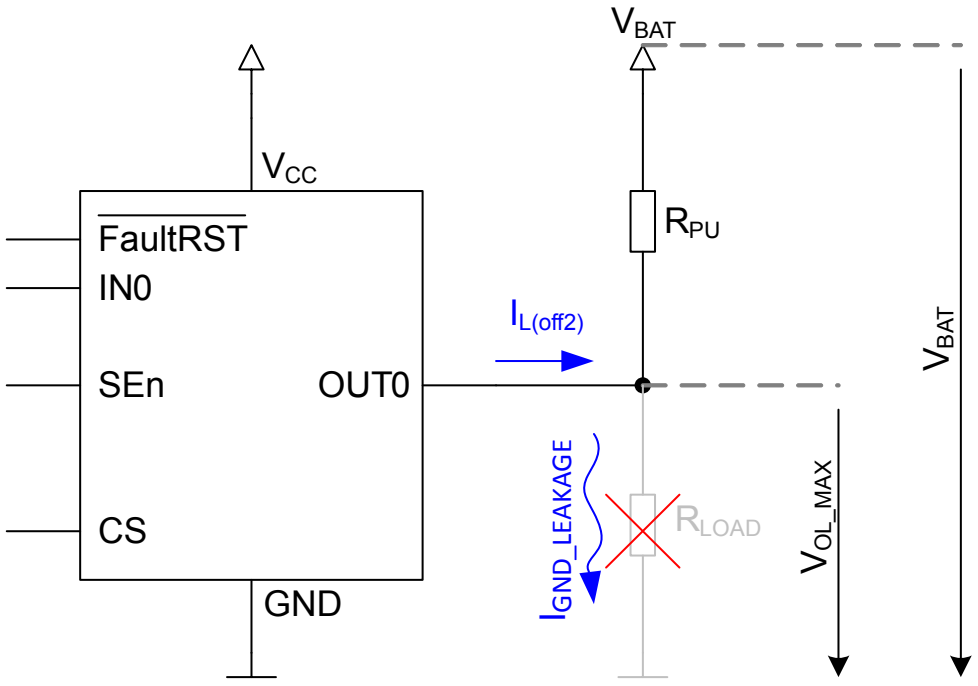
7.2.10 Open load detection in off-state

- Available if SEn pin is set high.
- Indicated by V_{SENSEH} on current sense pin.
- External pull-up on the output needed.
- Possibility to distinguish between open load in off-state and short to V_{BAT} using switchable pull-up resistor.

Maximum R_{PU} calculation during open-load condition:

Switchable resistor R_{PU} must be selected in order to ensure $V_{OUT} > V_{OL\_MAX}$ (value given in the datasheet) considering maximum leakage current for V_{OL_MAX}, as well as additional leakage current flowing to GND (for example, due to humidity)

Figure 60. RPU calculation with no load connected



Resistor R_{PU} connected to V_{BAT} supply results to:

$$R_{PU} < \frac{V_{BAT} - V_{OL\_MAX}}{I_{GND\_LEAKAGE} - I_{L(off2)\_MIN}} \quad (74)$$

Where $I_{L(off)}$ is a value present in the datasheet

Considering V_{BAT} = 7 V, ground leakage current $I_{GND\_LEAKAGE}$ = 0 and $I_{L(off)}$ = -150 µA

$$R_{PU} < \frac{7V - 4V}{150\mu A} = 20k\Omega \quad (75)$$

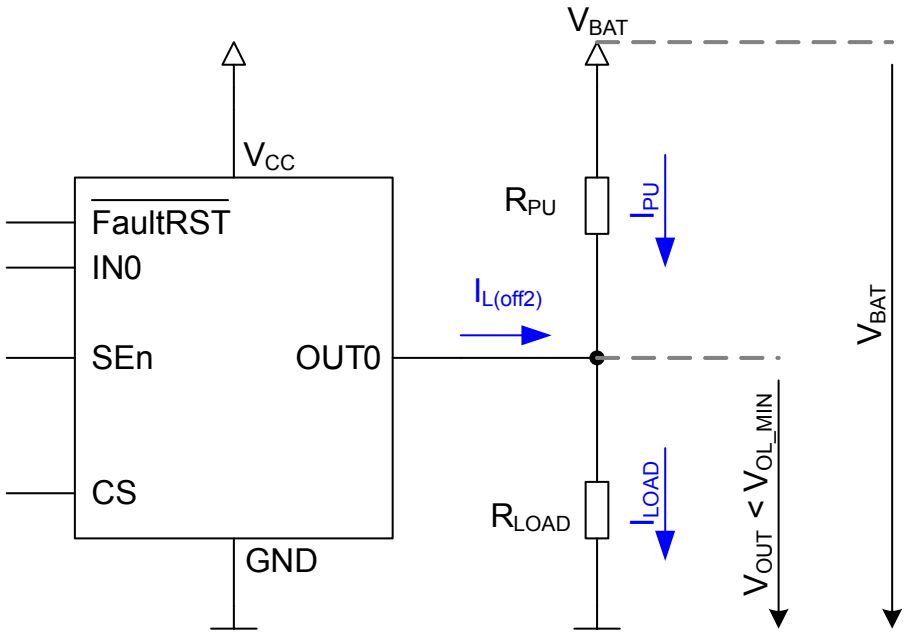
For V_{BAT} = 7 V, R_{PU} should be applied less than 20 kΩ to identify open load in off-state.

Minimum RPU calculation while load is connected

In order to ensure that no OL in off state failure flag set, if the load is connected, minimum R_{PU} must be evaluated.

Minimum R_{PU} can be calculated as follows:

Figure 61. RPU calculation with load connected



Considering:

$$I_{LOAD} = \frac{V_{OUT}}{R_{LOAD}} = I_{L(off)} + I_{PU} \quad (76)$$

$$R_{PU} = \frac{V_{BAT} - V_{OUT}}{I_{PU}} \quad \Rightarrow \quad I_{PU} = \frac{V_{BAT} - V_{OUT}}{R_{PU}} \quad (77)$$

Then:

$$\frac{V_{OUT}}{R_{LOAD}} = I_{L(off)} + \frac{(V_{BAT} - V_{OUT})}{R_{PU}} \quad , with\ V_{OUT} < V_{OL\_MIN} \quad (78)$$

Results to:

$$R_{PU} > \frac{R_{LOAD} \cdot (V_{BAT} - V_{OL\_MIN})}{V_{OL\_MIN} - R_{LOAD} \cdot I_{L(off)\_MAX}} \quad \left(I_{L(off)\_MAX}\ is\ negative\right) \quad (79)$$

Example 5:

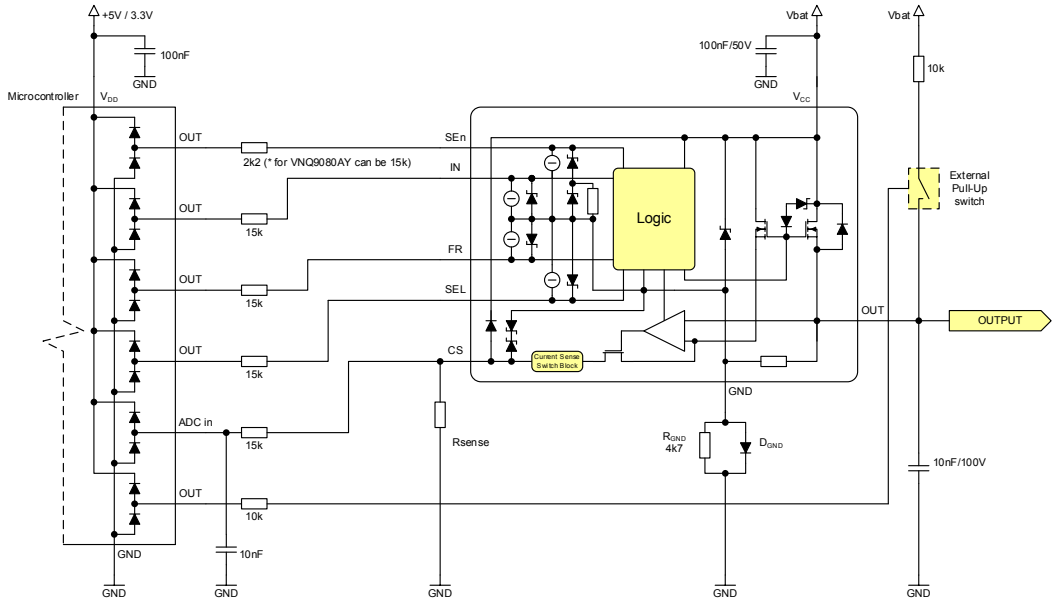
Let us consider VND9025AJ driving a load with R_{LOAD} = 4 Ω and following parameters: V_{OL_min} = 2 V and V_{BAT} = 18 V (as worst-case battery)

$I_{L(off2)MAX}$ = -5 µA

Applying below formula the pull-up resistance in order not to generate a false OL diagnostic is:

$$R_{PU} > \frac{4\Omega \cdot (18V - 2V)}{2V - 4\Omega \cdot (-5uA)} = 32\Omega \quad (80)$$

Figure 62. **Analogue HSD – open load detection in off-state**



In The following plots delay times for the OL detection in off state vs settings of Inx and SEn are shown. The relevant delay times t_{DSTKON} and t_{D_VOL} are given in the datasheets.

Figure 63. **Open load / short to V_{CC} detection in OFF state - delay after Inx is set from high to low**

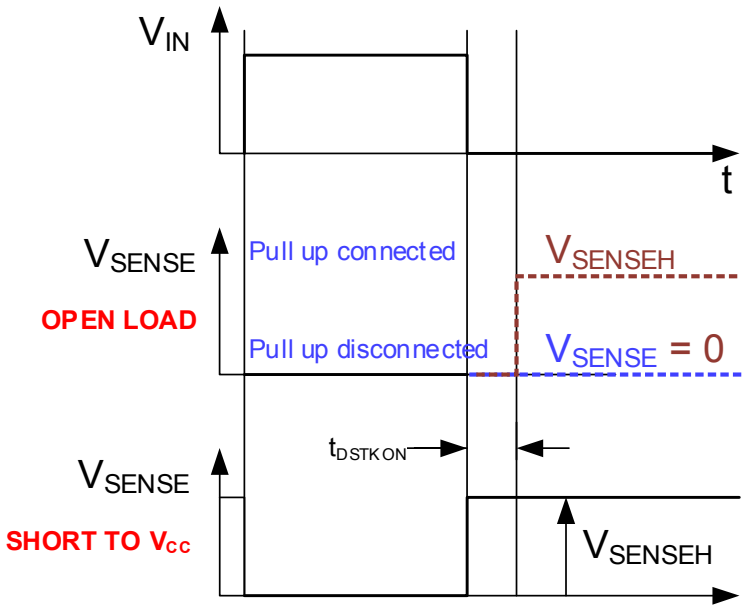


Figure 64. **Open load / short to V_{CC} detection in OFF state - delay after SEn is set from low to high**

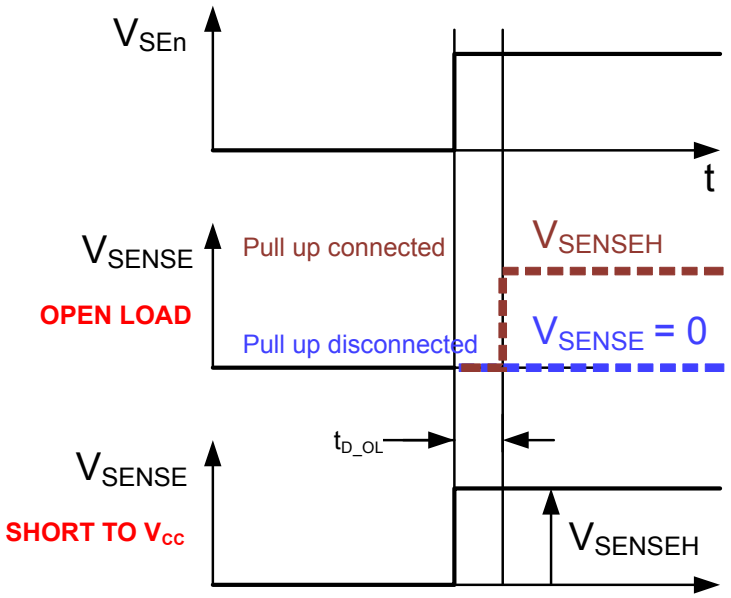


Table 19. **Current sense pin levels in off-state**

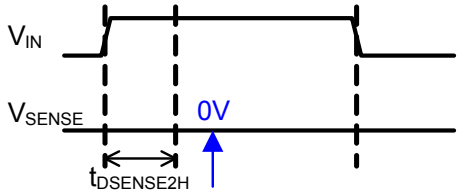
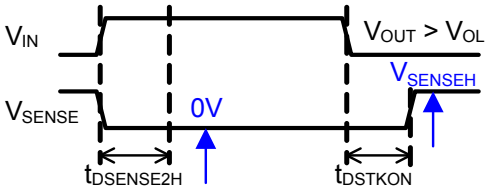
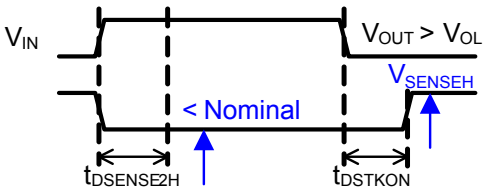
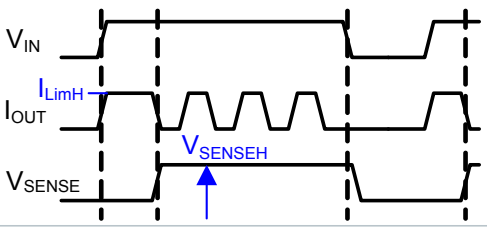
Condition	Pull up	Current sense	SEn
Open load	Yes	0	L
		V_{senseH}	H
	No	0	L
		0	H
Short to V_{CC}	Yes	0	L
		V_{senseH}	H
	No	0	L
		V_{senseH}	H
Nominal	Yes	0	L
		0	H
	No	0	L
		0	H

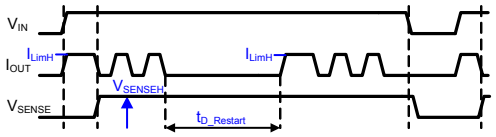
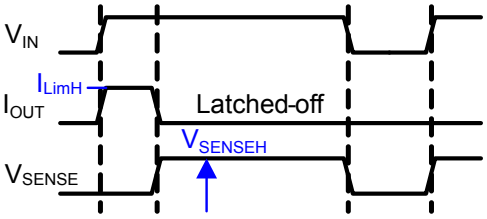
It is recommended to avoid permanent low impedance paths from the device OUTPUT to a voltage potential higher than Vol max. In fact, in those conditions and the device in standby mode, there is an additional current leakage from OUTPUT to device's GND, typically 110 µA. Such leakage current may contribute to an early car battery discharge. Therefore, switched pull-up resistor for open-load detection is a good practice.

Diagnostic summary

The table below summarizes all failure conditions, the V_{SENSE} signal behavior and recommendations for diagnostics sampling.

Table 20. Diagnostics overview

Fault Condition	Signal	Value	
Open load (without pull-up)	V_{IN}	L	H
	V_{SENSE}	0 V	0 V
	Notes		Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms Sampling		
Open load (with pull-up)	V_{IN}	L	H
	V_{SENSE}	V_{SENSEH}	0 V
	Notes	Delay time from falling edge of IN pin must be considered (t_{DSTKON}).	Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms Sampling		
Short circuit to V_{BAT}	V_{IN}	L	H
	V_{SENSE}	V_{SENSEH}	< Nominal
	Notes	Delay time from falling edge of IN pin must be considered (t_{DSTKON}).	Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$).
	Waveforms Sampling		
Power limitation or Over temperature (Autorestart mode)	V_{IN}	L	H
	FR	L	L
	V_{SENSE}	0 V	V_{SENSEH}
	Notes		Current sense delay response time from rising edge of IN pin must be considered ($t_{DSENSE2H}$, respectively trip time to Power limitation/Overtemperature shutdown whatever is longer).
	Waveforms Sampling	Case1 – thermal shut-down not reached 	

Fault Condition	Signal	Value	
Power limitation or Over temperature (Autorestart mode)		Case2 – thermal shut-down; out reactivation after tD_Restart 	
Power limitation or Over temperature (Latch mode)	V_{IN}	L	H
	FR	H	H
	V_{SENSE}	0 V	V_{SENSEH}
	Notes		Current sense delay response time from rising edge of IN pin must be considered (tDSENSE2H, respectively trip time to Power limitation/Overtemperature shutdown whatever is longer). Output latched-off after the first intervention of power limitation or thermal shutdown. Can be unlatched by a low level pulse on the FR pin (T_{PULSE} > T_{LATCH_RST}).
	Waveforms Sampling		

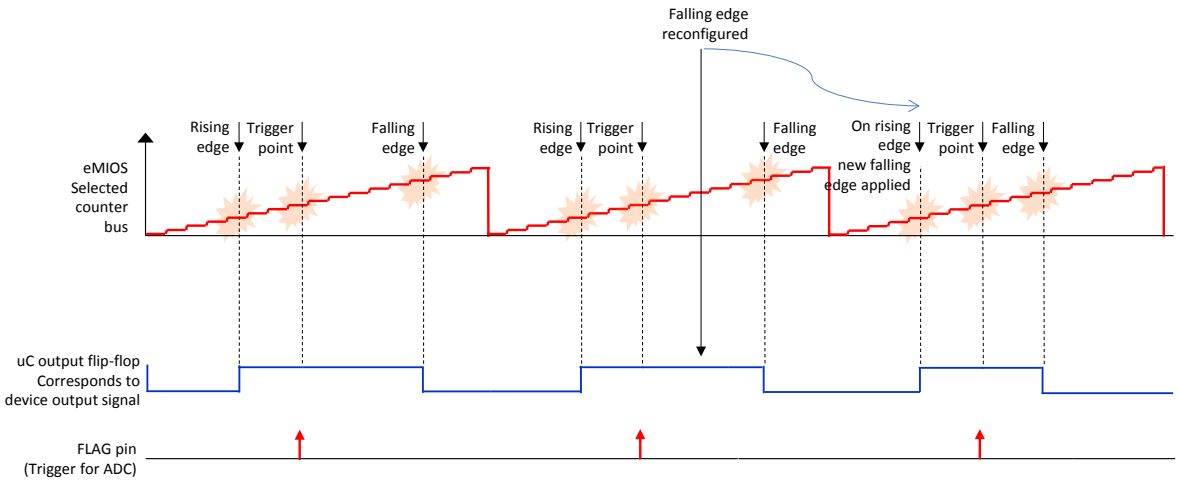
7.2.11 Current sense diagnostic evaluation on a microcontroller

Considering analogue monitoring for several outputs, appropriate µC must be used. Choosing a power PC microcontroller, dedicated hardware blocks can be used with advantage to monitor multiple C_{SENSE} signals (together with automated current sense channel switching).

A power PC microcontroller equipped with a sophisticated timer module (eMIOS or GPT) is capable to generate independent PWM signals for multiple outputs. It includes capability to specify trigger position within the PWM period for signal A/D conversion without any software intervention (0% CPU load in software task used for mux switching and A/D conversion triggering).

The figure below shows specific eMIOS modes, applicable for PWM generation and A/D conversion triggering (OPWMT mode)

Figure 65. eMIOS PWM generation mode principle



eMIOS block is able to control many channels applying independent configuration of rising, falling edge position (duty cycle), together with trigger, specifying sampling point for current sense signal. For example, on SPC58x - up to 2x31channels are available for this purpose (other models can contain different number of eMIOS channels). These channels can be mapped directly to control INx signals of multiple HSDs.

Additional block aligned with M0-9 devices current sense control, is ADC external multiplexer. This peripheral use MA[2:0] control pins capable to control external analogue multiplexer (in this case M0-9 devices are in the role of external multiplexer). SEL0..2, SEn pins are controlled by MA[2..0] outputs.

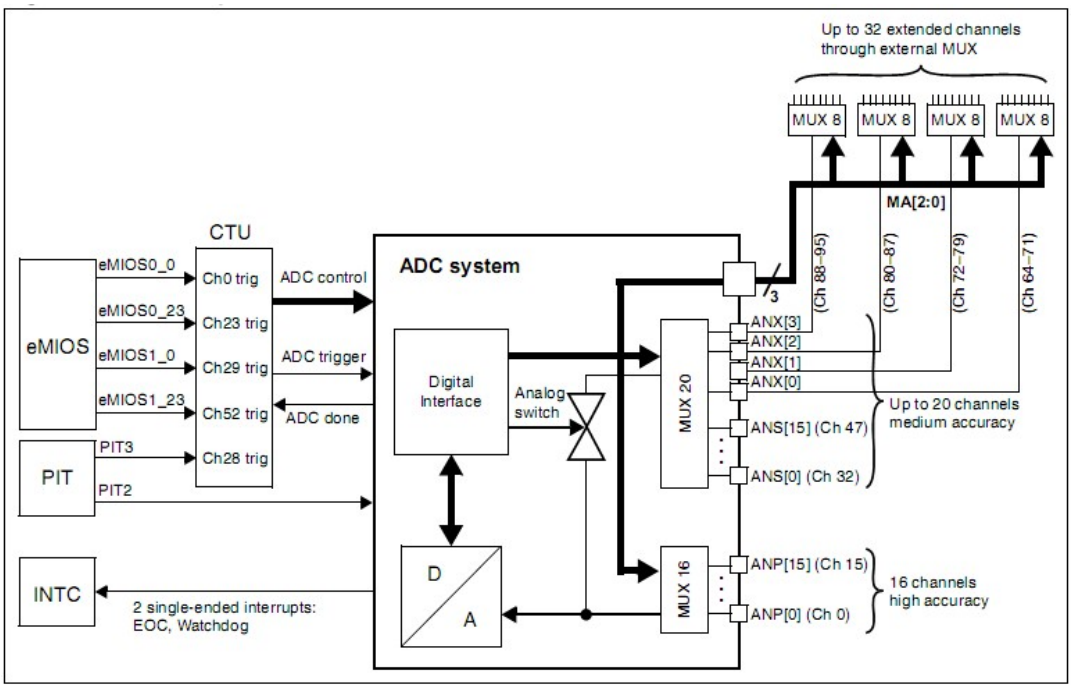
Four analogue input channels ANX[3:0] linked with MA[2..0] selector outputs create the possibility to monitor 4(A/D inputs) x 8 (possible combination of MA[2..0]) = 32 analogue signals, driven by MA[2..0] outputs.

Depending on the system complexity, multiple devices can be diagnosed using extended ADC channels without the need of software control on the uC side. eMIOS block creates trigger measurement points, pass them to the ADC external multiplexer. It drives MA[2..0] outputs applied to M0-9 HSDs SELx pins (selecting the relevant monitored channel). Selected current sense feedback passed to one of the A/D inputs is automatically measured by the uC A/D converter at preconfigured time. This operation applies to all channels using MA[2..0] (external multiplexer).

For simple/medium complex systems (up to 32 analogue monitored channels), analogue monitoring of all channels can be applied without impact on CPU load (using extended ADC attached to eMIOS/ GTM channels in OPWMT mode).

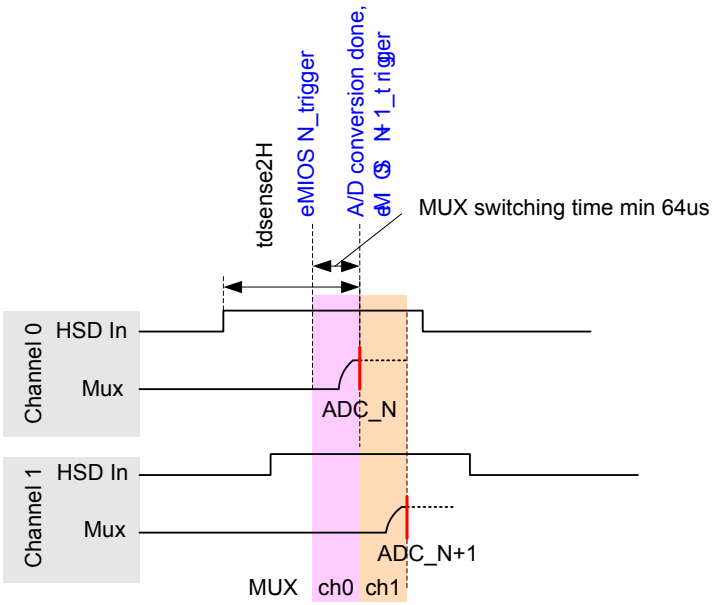
On a more complex systems (analogue monitoring more than 32 channels) additional logic must be involved, see example 1.

Figure 66. SPC extended ADC channels block diagram



While ADC external MUX control is used on SPC, it is important to preconfigure the minimum delay (tD_XtoY max = 24 µs) between mux switching and A/D conversion. This delay covers time necessary to switch M0-9 internal multiplexer to a newly selected channel/signal together with time needed for signal stabilization caused by low-pass filter used on A/D input. Additionally, it must be ensured a valid current sense signal during A/D conversion. It means that there must be a delay between HSD channel switch ON and ADC sampling, at least $t_{dsense2H}$ time. After ADC is sampled, MUX can be changed to following channel/signal. (Via MA [2..0])

Figure 67. C_{SENSE} diagnostic approach principle

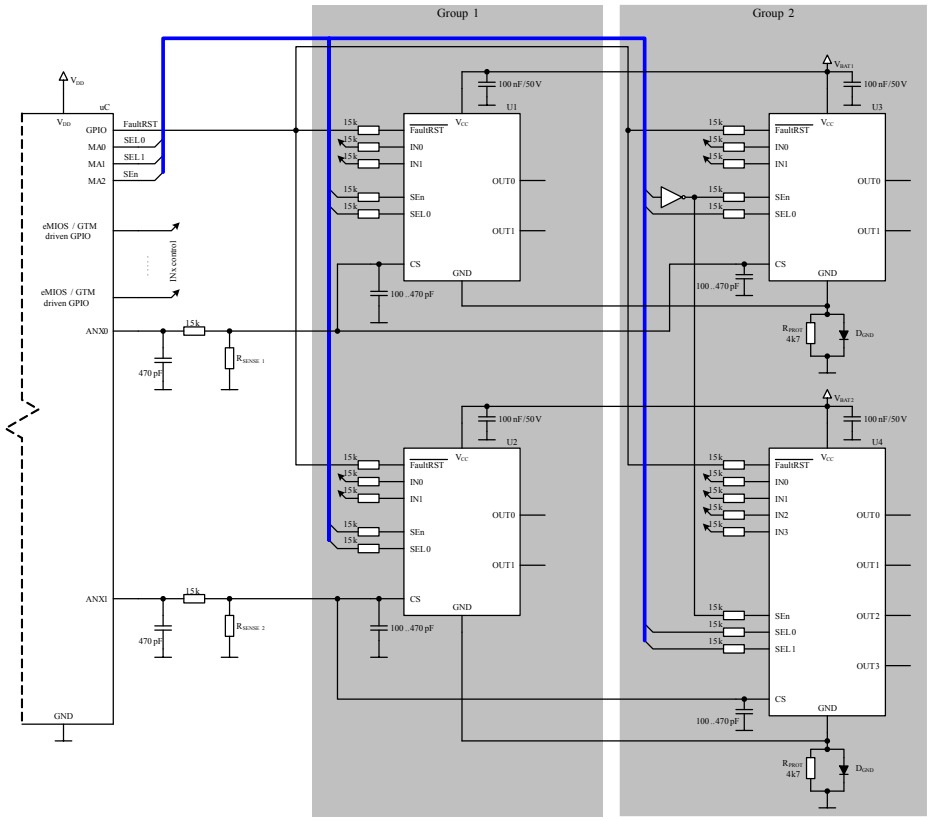


Example configuration applying 0% CPU load (MUX switching done by uC hardware peripherals).

In the following example two groups of drivers are given. Each group consists of two devices (maximum can be 4–given by µC A/D peripheral - number of analogue input channels linked to external multiplexer ANX0..3, see the figure below), where SEL pins are connected in parallel (selecting the same MUX channel on all devices). During diagnostic, groups 1 and 2 are alternated by SEn signal (every time, only one group is active for diagnostic, group 2 use inverter on SEn signal).

The PowerPC diagnostic interface is using externally multiplexed A/D channels ANX0 and ANX1 linked with control SEn and SEL0..1 pin automatically without any µC load.

Figure 68. Example of connection of multiple HSDs to SPC using external ADC mux control



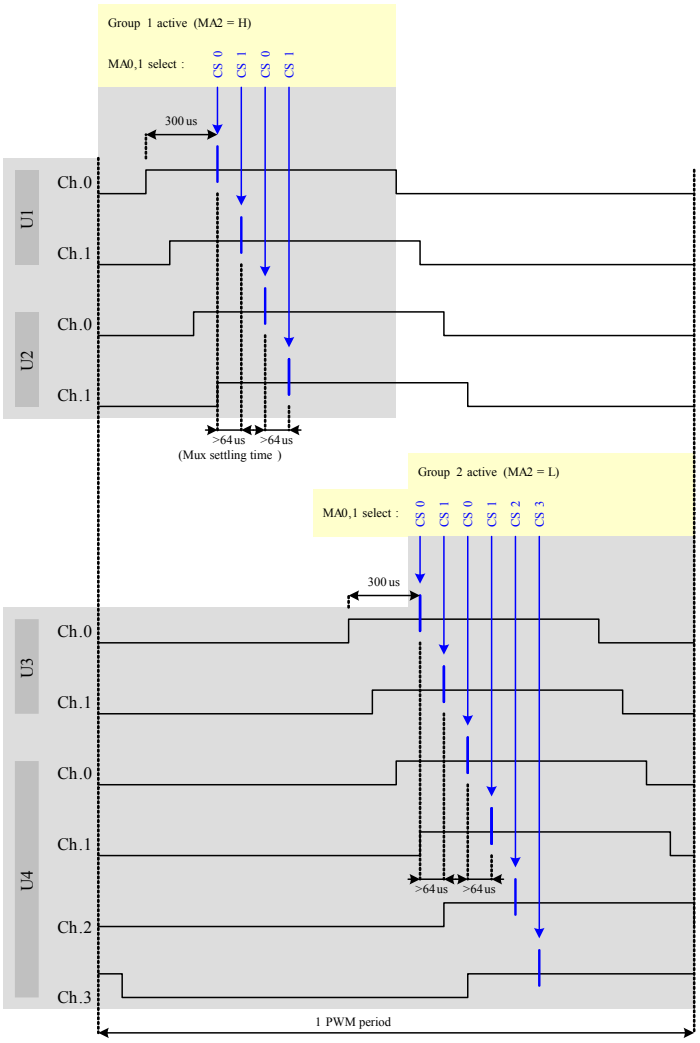
In the table below, the mapping between SEL0.2, SEn control signals and ANX0, ANX1 signals is shown:

Table 21. Power PC example signal mapping

MA1	MA0	MA2	Negative MA2	ANX0		ANX1		
(SEL_1)	(SEL_0)	SEn U1+U2	SEn U3+U4	(CS)		(CS)		
L	L	H	L	Current sense Ch0	CS U1 VND9016AJ	Current sense Ch0	CS U2 VND9025AJ	Group1
L	H	H	L	Current sense Ch1		Current sense Ch1		
H	L	H	L	Current sense Ch0		Current sense Ch0		
H	H	H	L	Current sense Ch1		Current sense Ch1		
L	L	L	H	Current sense Ch0	CS U3 VND9012AJ	Current sense Ch0	CS U4 VNQ9025AJ	Group2
L	H	L	H	Current sense Ch1		Current sense Ch1		
H	L	L	H	Current sense Ch0		Current sense Ch2		
H	H	L	H	Current sense Ch1		Current sense Ch3		

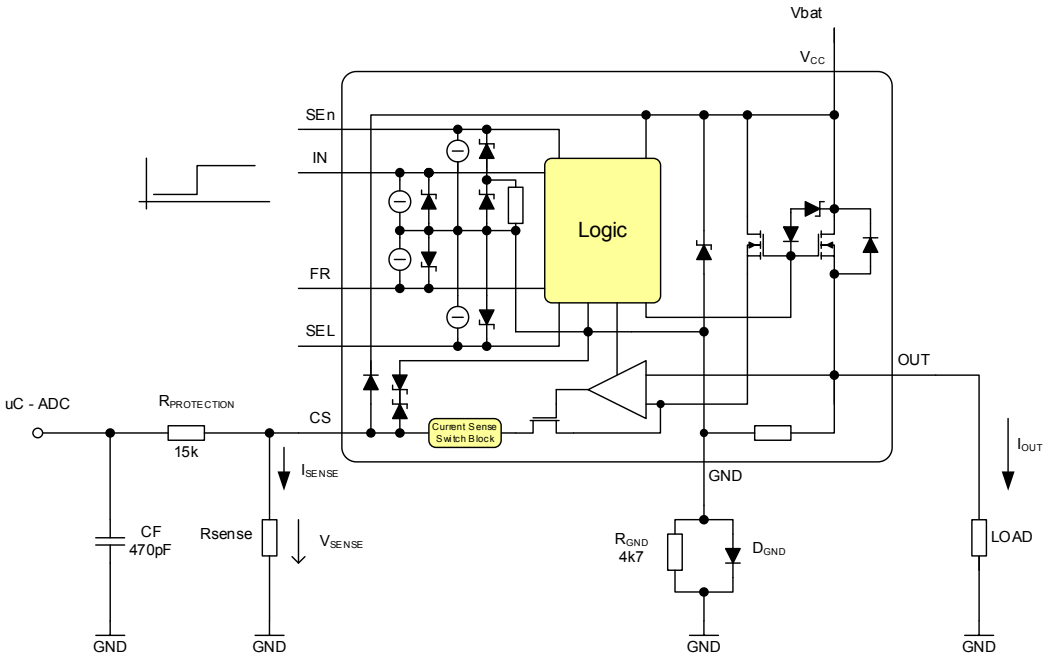
Time diagram shows the A/D trigger points of current sense diagnostic:

Figure 69. **Power PC example current sense trigger points**



7.2.12 Current sense low pass filtering

Figure 70. **Low pass filter connection**



The current sense voltage is usually connected through a 15 kΩ protection resistor to the ADC input of the µC. In case of V_{SENSEH} level the voltage is limited by the µC internal ESD protection (~5.8 V) while the ADC shows maximum value (0xFF in case of 8-bit resolution). The capacitor CF is used to improve the accuracy of the V_{SENSE} measurement (refer to the figure below).

This capacitor acts as a low impedance voltage source for the ADC input during the sampling phase. Together with a 15 kΩ serial resistor, it creates a low pass filter (with cutoff frequency of ~22 kHz) against potential HF noise on the current sense line (especially if a long wire is routed to the µC). This capacitor should be connected close to the microcontroller.

Chosen value of filtering capacitor (470 pF) together with $R_{PROTECTION}$ = 15 kΩ results in a time constant lower than settling times between multiplexer selection (control of SEL 01 pin) so with a minimized delay between SEL0.1 setting and sampling at the ADC.

8 Paralleling of devices

8.1 Paralleling of logic input pins

The following chapters describe the paralleling of logic input pins (SEn, INx, SELx and FaultRST) of different HSDs, considering device technologies M0-7, M0-9 and their combinations and supply line configuration (either the same or separate supply lines for each HSD).

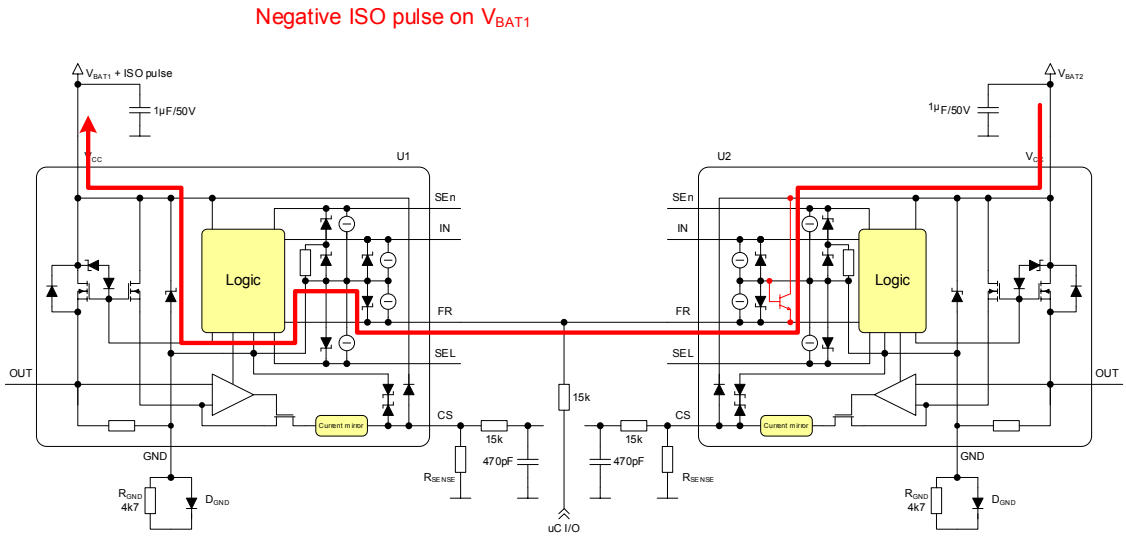
Direct paralleling of logic pins is generally an allowed operation in case of devices designed in the same technology (monolithic or hybrid) supplied from one supply line. In all other cases (like combination of monolithic with different supply lines) we should use additional components to ensure a safe operation under conditions in the automotive environment (ISO pulses, reverse battery …).

The clamp structure of all logic input is same (except slight difference on SEn pin on M0-9 devices containing reverse battery self-turn on during reverse battery condition and FaultRST pin on M0-7 technology), therefore all the explanations related to the paralleling of SEn pins are applicable also to paralleling of other logic input pins (including the FaultRST pin).

8.1.1 Monolithic HSDs supplied from different supply lines

Paralleling of FaultRST pins of monolithic HSDs is possible, however some precautions in schematic should be applied if the HSDs are supplied from different supply lines. In this case, the direct connection of FaultRST pins (as shown in the figure below) is not safe.

Figure 71. Direct connection of FaultRST (FR) pins (not recommended)



Direct connection of FaultRST pins is not safe in the following cases:

- Negative voltage surge on either on V_{BAT1} or V_{BAT2}
- Positive voltage surge either on V_{BAT1} or V_{BAT2} while:
  - Device GND pin disconnected.
  - Dgnd not used (resistor protection only).
  - Positive pulse energy higher than HSD (or Dgnd) capability - all paralleled devices could be damaged.

A negative voltage surge (ISO7637-2 pulse 1, 3a) either on V_{BAT1} or V_{BAT2} could cause unlimited current flow between both supply lines via the FaultRST pins of connected devices. This current could lead to malfunction or even failure of one or both of the HSDs. The mechanism (current path) is shown graphically on example on Figure 71. Direct connection of FaultRST (FR) pins (not recommended) 70.

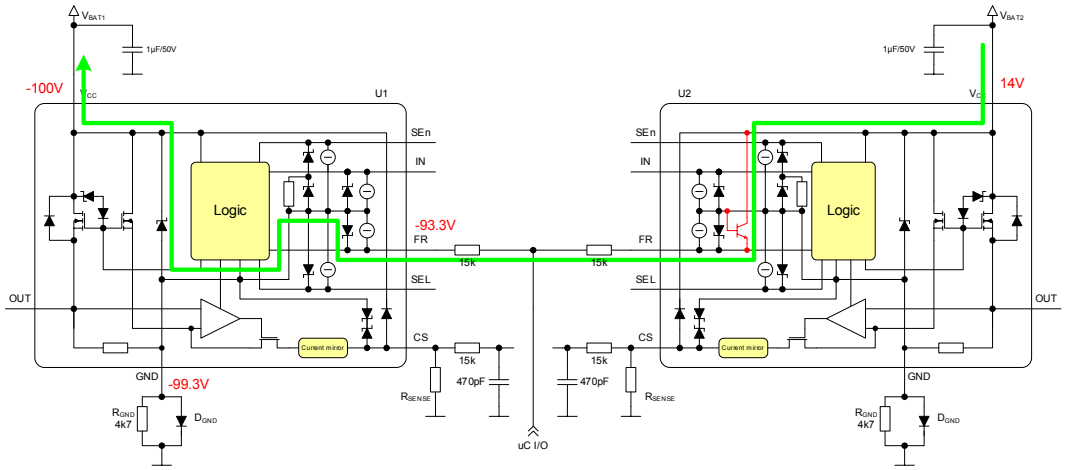
The negative transient (that is, -100 V) on VBAT1 (device U1) is transferred to the GND pin via the VCC-GND clamp (~0.7 V voltage drop ⇒ -99.3 V) and consequently to the FaultRST pin via the FaultRST-GND clamp (~6.3 V voltage drop ⇒ -93 V). Since the FaultRST pin of second device U2 is pulled negative, a parasitic NPN bipolar structure on the FaultRST pin is activated (emitter pulled negative versus base) and pulls the FaultRST pin high towards the VCC pin (V_{BAT2}). Since this parasitic NPN structure does not allow the FaultRST pin to be pulled negative to -93 V, an unlimited current can flow between the devices.

A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on V_{BAT1} or V_{BAT2} could lead to the increase of the GND pin voltage (in case of missing Dgnd, Dgnd failure or GND pin disconnected). As soon as this occurs, the voltage on FaultRST pin is rising also since a parasitic NPN bipolar structure is activated (base positive versus emitter). Since the second device (with properly connected GND pin) does not allow the voltage on FaultRST pin to rise above the clamp voltage (~6.3 V) an unlimited current can flow between the devices. This could lead to malfunction or even failure of one or both of the HSDs.

In order to avoid such failures, it is recommended to add a 15 K resistor in series to each FaultRST pin (see the figure below).

In principle the same applies to all other logic input pins as well (since the clamp structure is similar).

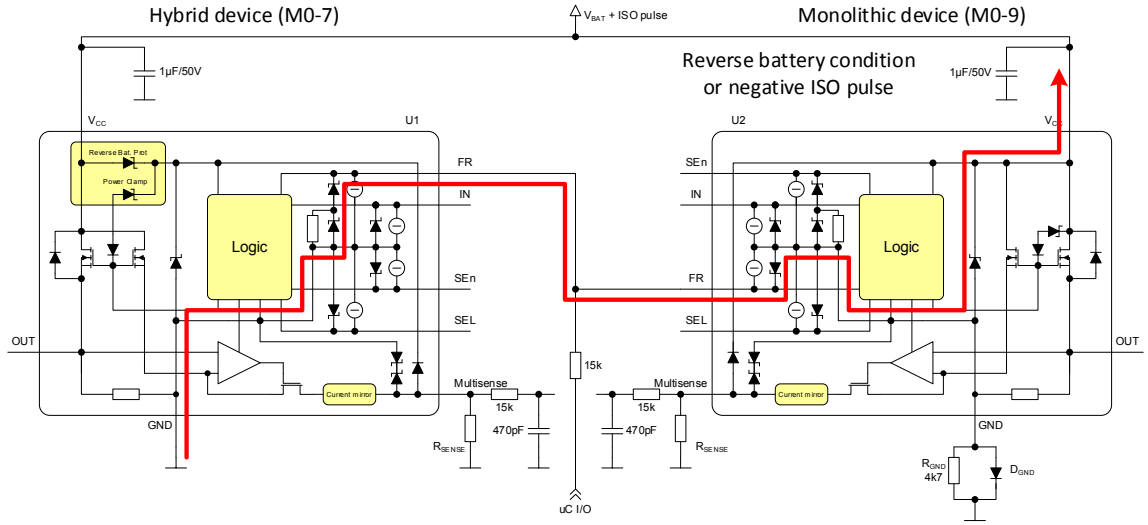
Figure 72. Proper connection of FaultRST (FR) pins



8.1.2 Mix of monolithic (M0-9, M0-7) and hybrid HSDs (M0-7)

Paralleling of FR pins between monolithic (M0-9 or M0-7 family) and hybrid (M0-7 family) HSD is possible, however some precautions in schematic must be applied. The direct connection of FR pins (as shown in Figure 73. Direct connection of FR pins combining monolithic and hybrid devices (not recommended)) is not safe (even if we consider the same power supply for both devices).

Figure 73. Direct connection of FR pins combining monolithic and hybrid devices (not recommended)

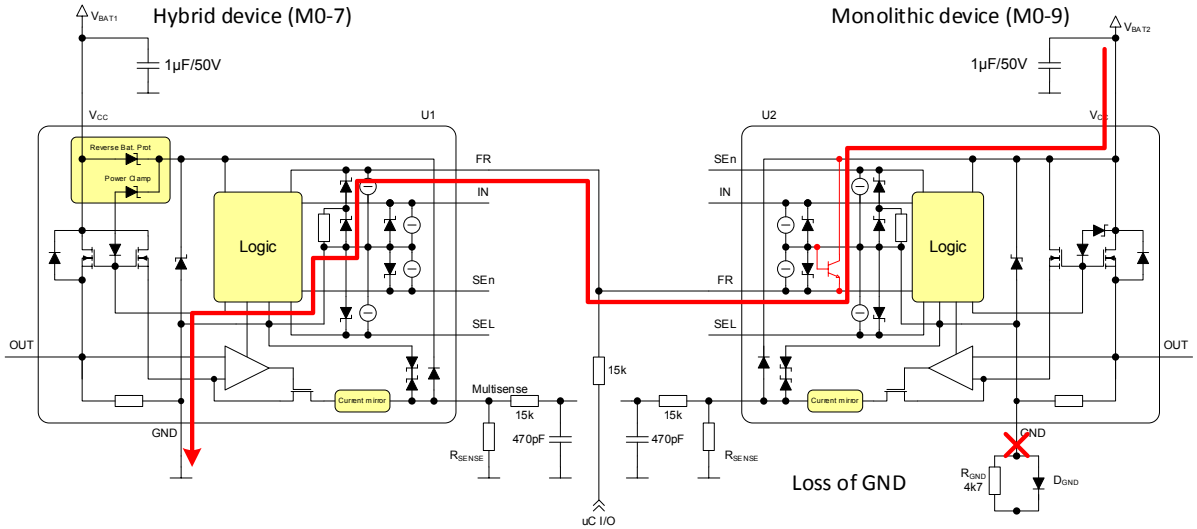


Direct connection of FR pins is not safe in the following cases:

- Reverse battery (single supply line considered).
- Negative ISO pulse (single supply line considered).
- Loss of GND connection(separate supply lines considered) + ISO pulse.

Due to the different concepts of reverse battery protection of hybrid and monolithic devices, there is a way for unlimited current flow between both devices in case of reverse battery condition. The hybrid device has an integrated reverse battery protection in V_{CC} line, while the monolithic device needs an external diode/resistor in series with GND pin (refer to Chapter 3 of this document). The different potential on each GND pin (hybrid: ~ 0V, monolithic: $-V_{BAT}$ - 0.7 V) is leading to the activation of both FaultRST clamp structures when V_{BAT} is below ~ -7.5 V ($V_{SEnCLAMP}$ + two diode voltage drop). The resulting current can lead to malfunction or even failure of one or both of the HSDs.

Figure 74. Direct connection of FR pins combining monolithic and hybrid devices (not recommended) during loss of GND



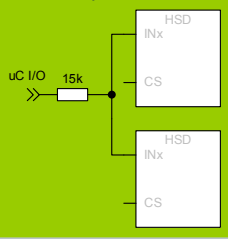
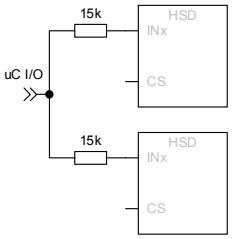
In configuration of separate supply lines where the GND connection of one device is lost, positive as well as negative ISO pulses on the associated supply line are not clamped anymore (considering no other devices connected to this supply line). If the transient voltage is large enough to activate the involved structures, there could be unlimited current flow between both supply lines through FaultSRT pins. This current could lead to malfunction or even failure of one or both of the HSDs.

In order to avoid such failure it is recommended to add a 15 kΩ resistor in series to each FaultRST pin (in the same way as already described in case of paralleling of monolithic devices–see previous section Section 8.1.1: 8.1.1).

In principle the same applies to all other logic input pins as well (since the clamp structure is similar).

Following table is summarizing possible combinations of HSDs with paralleled inputs relative to the used power supply networks.

Table 22. Paralleling of inputs summary

Technology	The same power supply network (VBAT + GND network)	Different supply networks (different VBAT or different GND protection network)
Monolithic + monolithic	Single resistor on µC side, HSD input in parallel 	
Monolithic + hybrid		Each HSD use separate protection resistor 

8.2 Paralleling of current sense

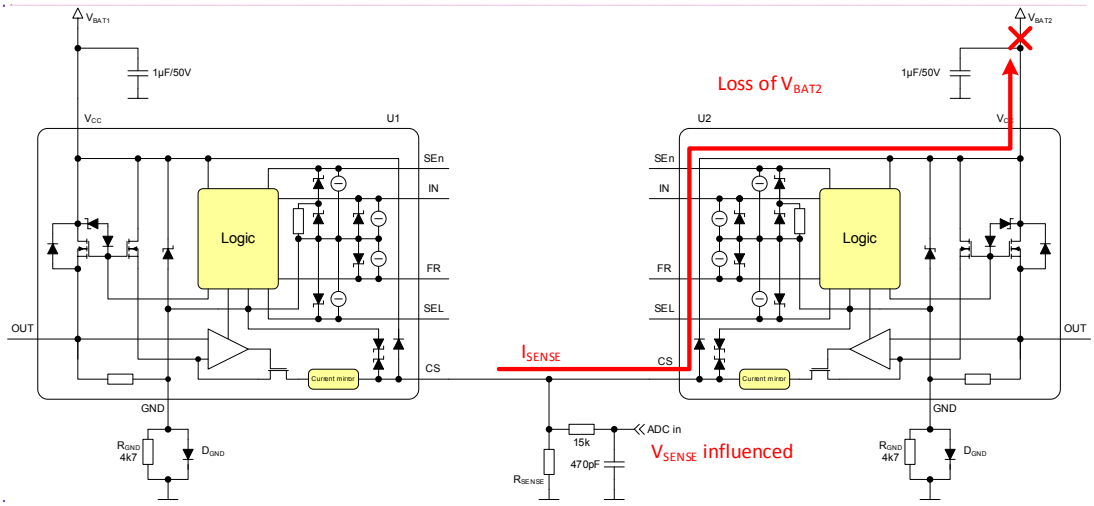
The following chapters describe the paralleling of current sense pins of HSDs, considering supply line configuration (either the same or separate supply line for each HSD).

Direct connection of current sense pins is an allowed operation without any restriction when the devices are supplied from one supply line, sharing the same GND network. In case of separated supply lines or separated GND protection networks, we should use additional components to ensure a safe operation under conditions in the automotive environment (ISO pulses, reverse battery …).

8.2.1 HSDs are supplied from different supply lines

Paralleling of current sense pins of monolithic HSDs is possible, however some precautions in schematic should be applied if the HSDs are supplied from different supply lines. Direct connection of current sense pins (as shown in Figure 75. Direct connection of current sense pins (not recommended)) is not safe.

Figure 75. Direct connection of current sense pins (not recommended)



Direct connection of current sense pins is not safe in the following cases:

- Negative voltage surge on either on V_{BAT1} or VBAT2.
- Positive voltage surge either on V_{BAT1} or V_{BAT2} while:
  - Device GND pin disconnected.
  - Dgnd not used (resistor protection only).
  - Positive pulse energy higher than the HSD (or Dgnd) capability-all paralleled devices could be damaged.
- Loss of V_{BAT1} or V_{BAT2}

A negative voltage surge (ISO 7637-2 pulse 1, 3a) either on V_{BAT1} or V_{BAT2} is directly coupled to the current sense pin through the internal V_{CC}-Current sense clamp structure. If the negative voltage on the current sense line is large enough to activate the V_{CC}- current sense clamp structure, there could be an unlimited current flow through both current sense pins. This current could lead to malfunction or even failure of one or both of the HSDs.

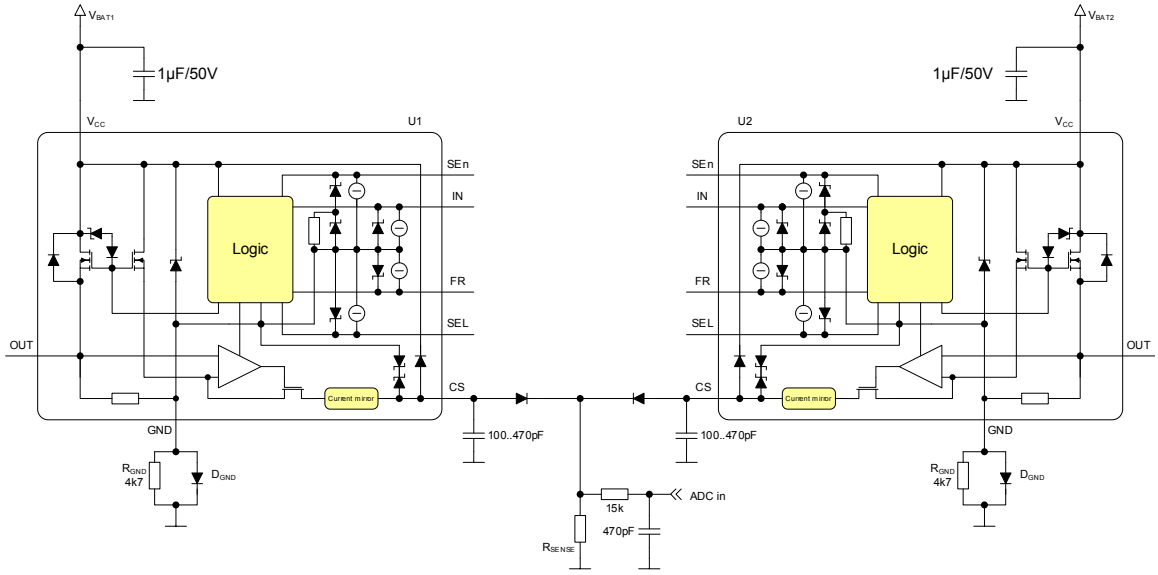
A positive voltage surge (ISO7637-2 pulse 2a, 3b) either on V_{BAT1} or V_{BAT2} together with missing Dgnd (Dgnd not used, Dgnd failure or GND pin disconnected) can activate the V_{CC} - current sense clamp structure (clamp voltage similar to V_{CC}-GND clamp). As soon as this occurs there could be an unlimited current flow through both current sense pins. This current could lead to malfunction or even failure of one or both of the HSDs.

Loss of either V_{BAT1} or V_{BAT2} is leading to a wrong current sense signal. If V_{BAT2} is lost, U2 (and other components connected to V_{BAT2}) is supplied by U1 current sense signal through the internal V_{CC} - current sense clamp structure. Therefore, the voltage on the current sense bus drops to almost 0 V and we have no valid V_{SENSE} reading anymore.

To protect the devices during ISO pulses and to ensure a valid current sense signal as well, we can add a diode in series to each current sense pin (as shown in the following schematics). To suppress the rectification of noise injected to the sense line, it is recommended to add a ceramic filter capacitor between each cSPIN and ground.

However, the voltage drop on diodes in series with current sense pin can have an influence on the dynamic range of current sense, temperature and current sense accuracy.

Figure 76. **Safe solution for paralleling current sense pins**



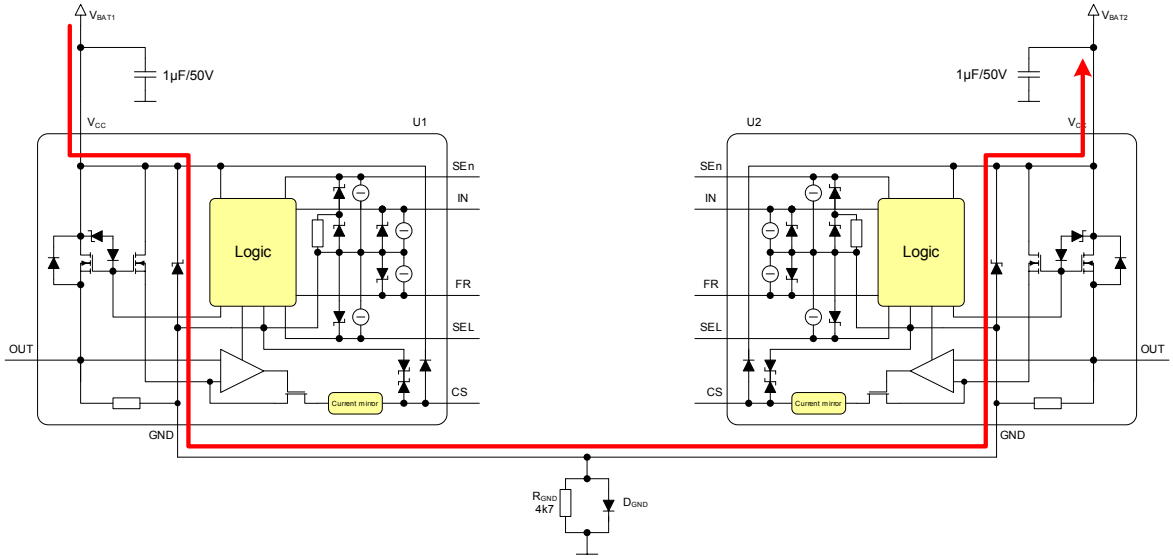
8.3 Paralleling of GND protection network

Sharing a common ground protection network of monolithic HSDs is safe in case of using the same power supply line. If different supply lines are required, an external clamp must be present on both supply lines to clamp the negative transients to a voltage lower than the minimum V_{CLAMP}, so that $V_{BAT} + |V_{NEG\_PEAK}| < 40$ V. During the negative voltage exposure, the outputs of all paralleled devices linked to stable battery line turns-on (since the logic input thresholds are exceeded by pulling the GND pins negative).

Applying different supply lines (without an external clamp protection) is not safe in case of:

- Negative ISO pulse on V_{BAT1} or V_{BAT2}

Figure 77. **Common GND network with different supply lines (not recommended)**



8.4 Paralleling of outputs

Paralleling of outputs (within one device) is usually considered when higher current capability is needed. The aim of this subchapter is to show the device behavior with paralleled outputs and highlight potential issues (especially in combination with inductive loads). Considerations and conclusions concerning this chapter are based on experimental measurements in a limited sample size for each indicated part number.

8.4.1 Current balancing with resistive load

Following experimental measurements show the current sharing between the channel and behavior of current sense with different load current. Two M0-9 devices (one high and one low ohmic) are considered.

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device
  - VNQ9025AJ (OUT0 + OUT1 paralleled)
- To be checked:
  - Sharing of load current & current sense
  - Behavior at low current (V_{ON} regulation)

Figure 78. Test set up – paralleling of outputs (load current sharing)

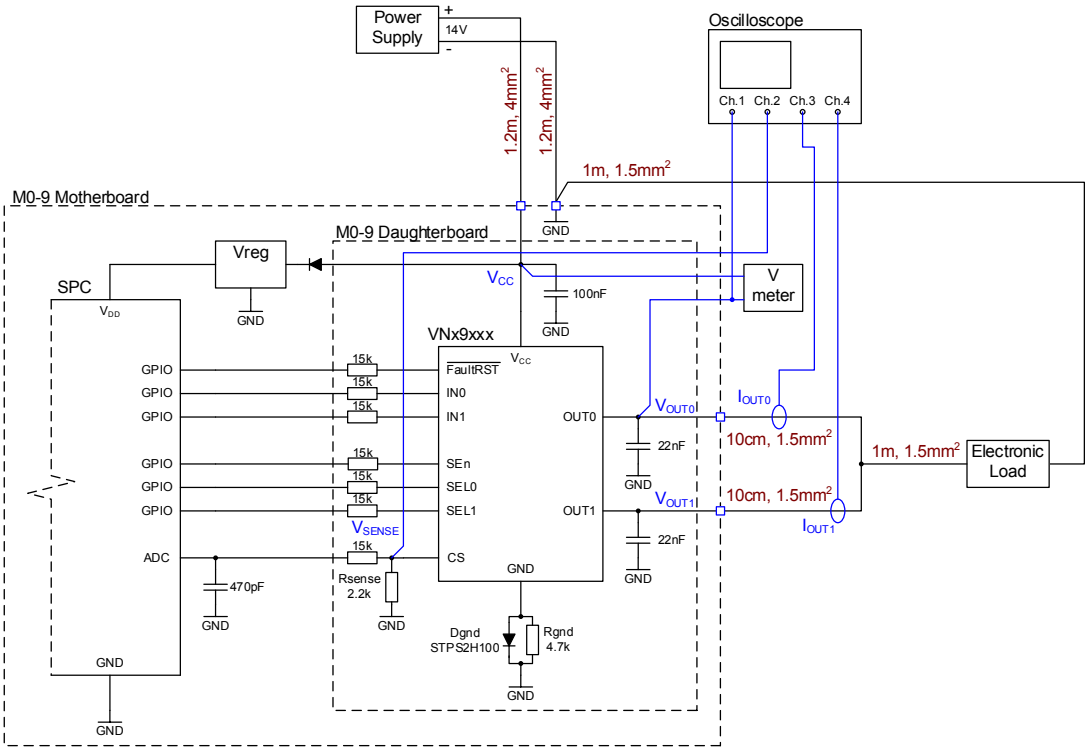


Figure 79. **Sharing of load current, V_{ON} regulation (VNQ9025AJ OUT0+1)**

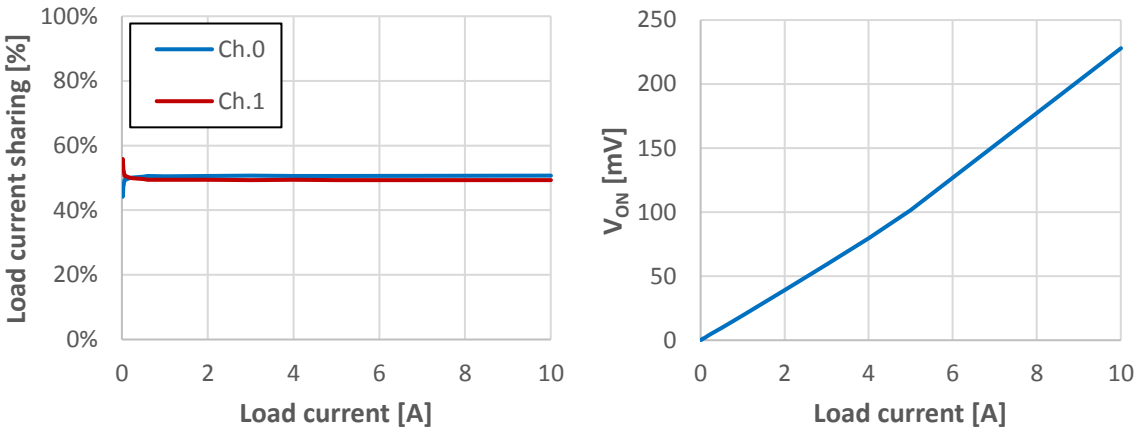
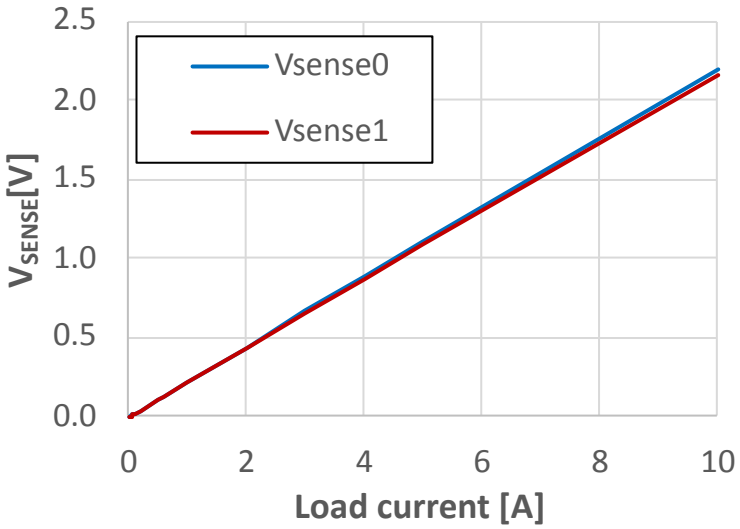


Figure 80. **Current sense behavior at low current (VNQ9025AJ OUT0+1)**



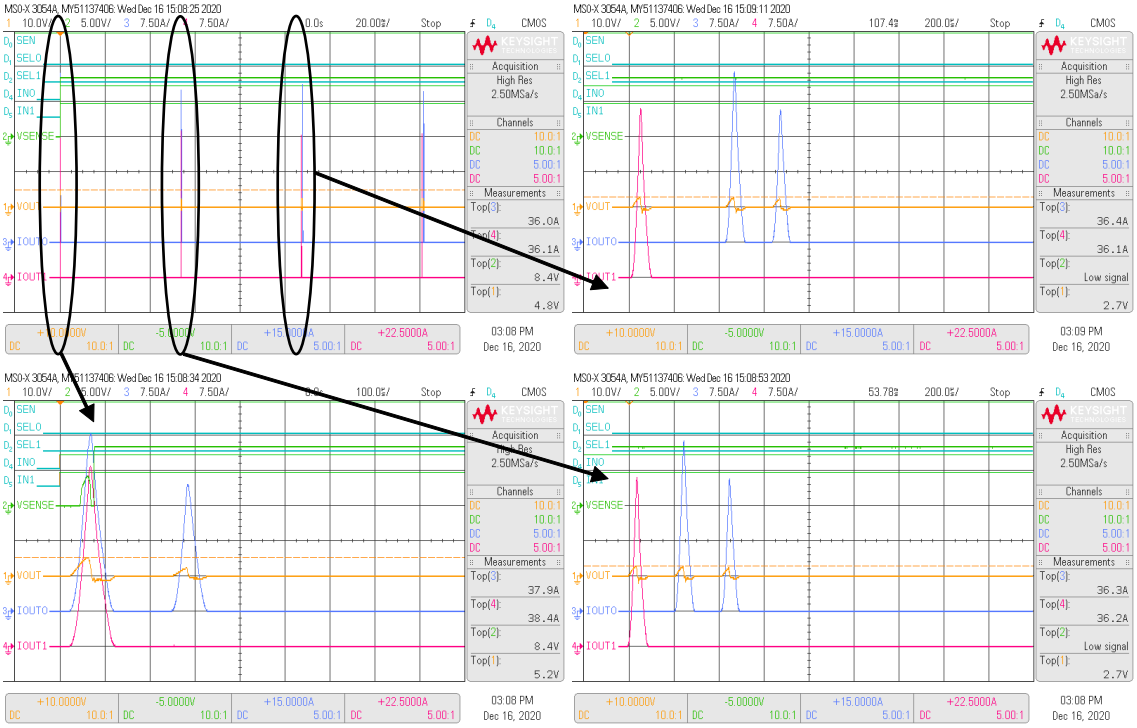
The current balancing is almost constant at high current levels. Reducing the load current increases the current unbalance. The current sense values well correspond to actual output currents. This leads to the requirement for reading of both current sense values at low current levels (only the sum of these values ensure correct diagnostic).

8.4.2 Overload behavior with resistive loads

This experiment shows the behavior during the overload conditions on a VND9025AJ sample with paralleled outputs (same test setup as for the load current sharing test).

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device
  - VND9025AJ (OUT0 + OUT1 paralleled).
- To be checked:
  - Behavior during overload condition (cold bulb start up).

Figure 81. **Behavior during overload condition (VNQ9025AJ, Ch.0 + Ch.1)**



After turn-on of both channels in overload condition, both channels are in current limitation and contribute equally to the total load current. The current regulation is stable on both channels. The first intervention of power limitation (turn-off) comes almost synchronously on both channels. However, the next power limitation or thermal shutdown cycling is asynchronous. The cycling frequency is same but the phase shift is varying.

8.4.3 Driving inductive loads

Following part checks the load current sharing during the demagnetization phase at various load conditions (standard load with long wire harness, high inductance load with or without external freewheeling on VND9025AJ device with paralleled outputs.

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device & load
  - VND9025AJ (OUT0 + OUT1 paralleled)
    - Bulb + 10 µH wire harness.
    - 2 mH / 2.8 Ω (with or without external freewheeling.)
- To be checked:
  - Demagnetization phase - sharing of load current & current sense.
  - With or without external freewheeling.

Figure 82. **Test set up–paralleling of outputs (inductive loads)**

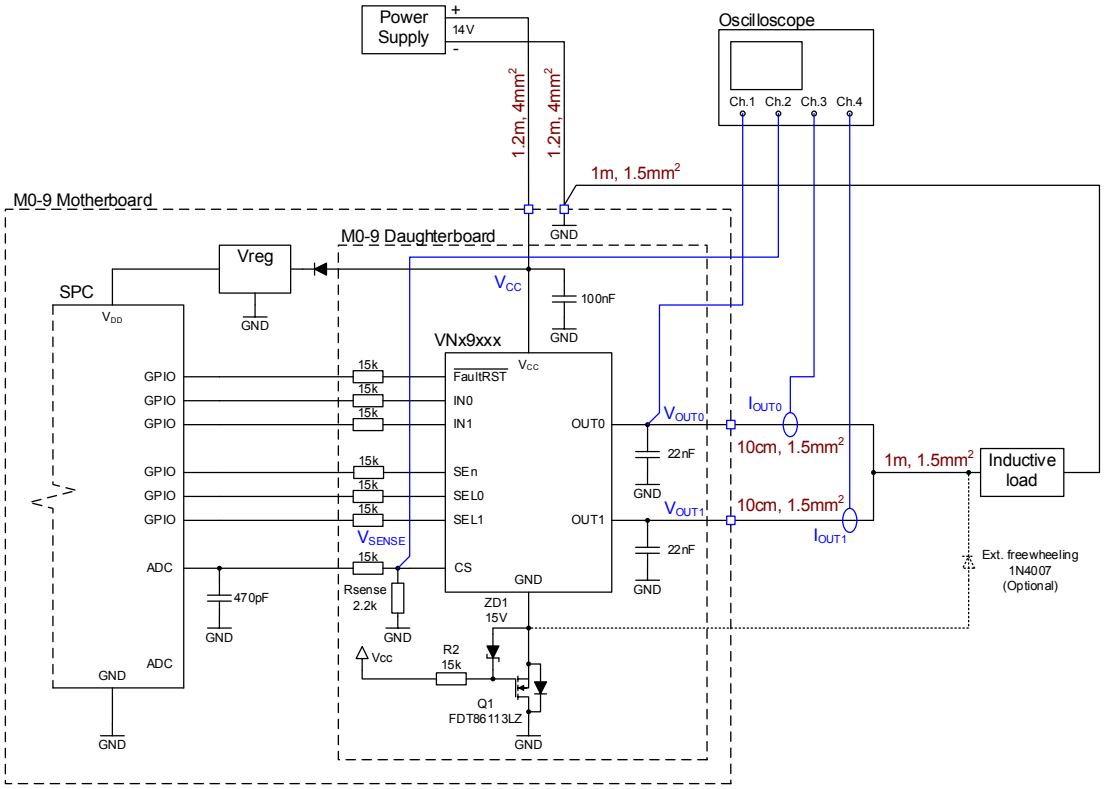


Figure 83. **Bulb with 10 µH (VNQ9025AJ, Ch.0 + Ch.1)**

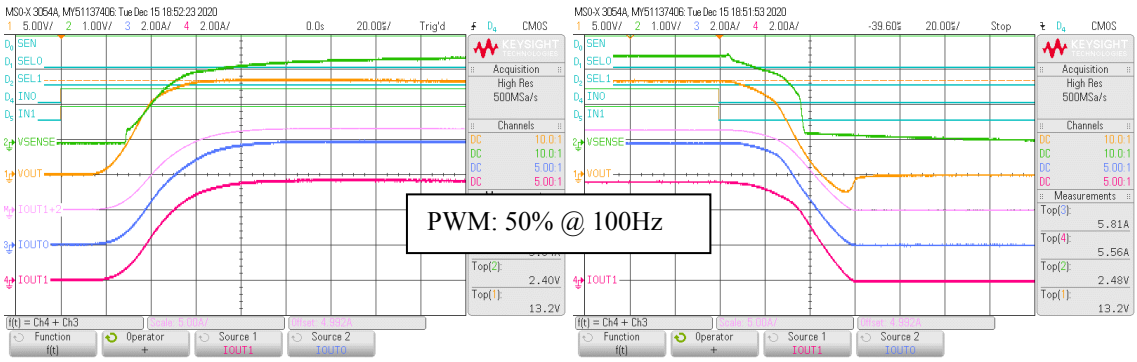


Figure 84. **2 mH / 2.9 Ω (VNQ9025AJ, Ch.0 + Ch.1)**

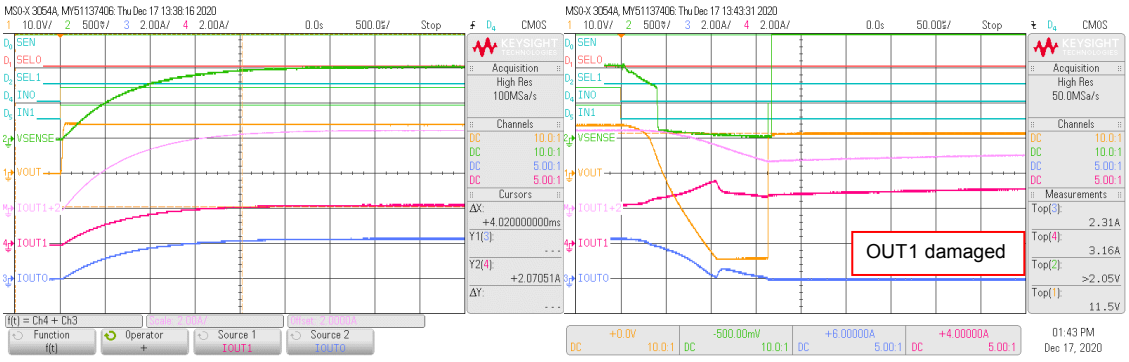
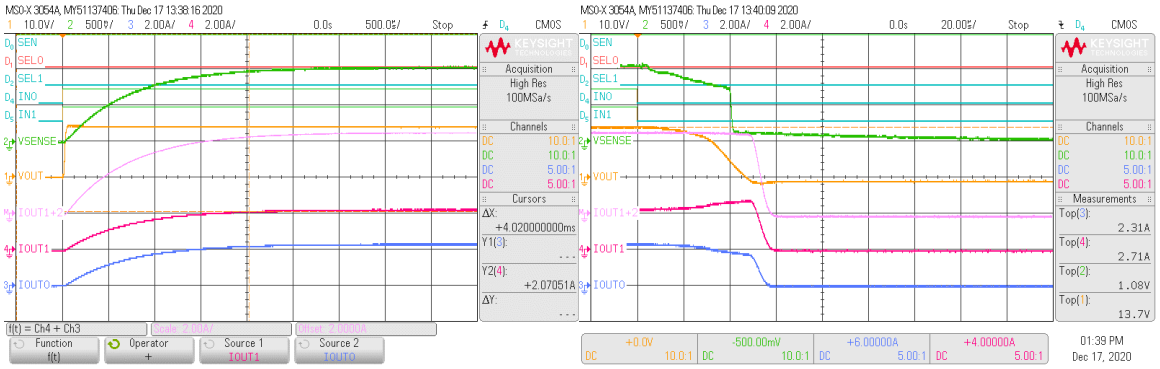


Figure 85. **2 mH / 2.9 Ω with external freewheeling (VNQ9025AJ, Ch.0 + Ch.1)**



Significant current imbalance is observed during the turn-off phase, even at relatively low inductance values (10 µH) or with external freewheeling. Nevertheless, this behavior does not impact the total power dissipation in the device or functionality in steady state conditions. The load current sharing during the demagnetization phase is unstable (see measurement with 2 mH / 2.8 Ω). This leads to the conclusion that, in the worst case, total demagnetization energy could be dissipated in one channel only. Therefore, the energy capability of a single channel must be sufficient to sustain the whole demagnetization energy. If this is not the case - as depicted in the Figure 84. 2 mH / 2.9 Ω (VNQ9025AJ, Ch.0 + Ch.1) where OUT1 got damaged, an external protection must be added.

The following measurement demonstrates the overload condition (turn-on into the short circuit) on VNQ9025AJ device with paralleled outputs, configured in latch mode:

- V_{BAT}: 14 V
- Temperature: 25 °C
- Device
  - VNQ9025AJ (OUT0 + OUT1 paralleled).
- Short circuit parameters
  - 5 µH / 50 mΩ (coil from 1.5 mm_2 cable).

Figure 86. **Test set up–inductive short circuit test with paralleled outputs**

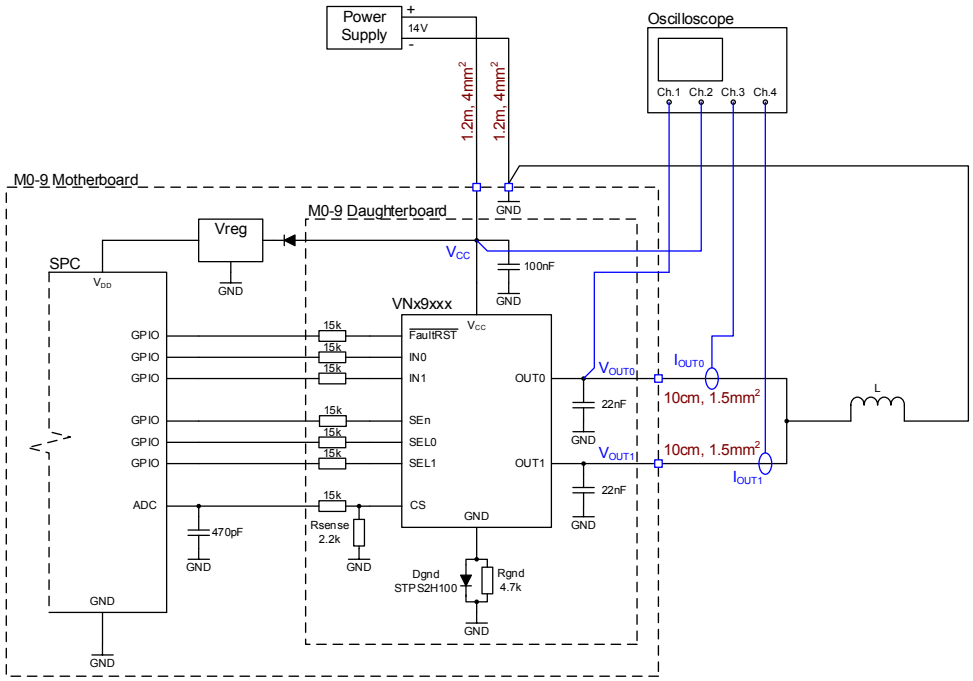
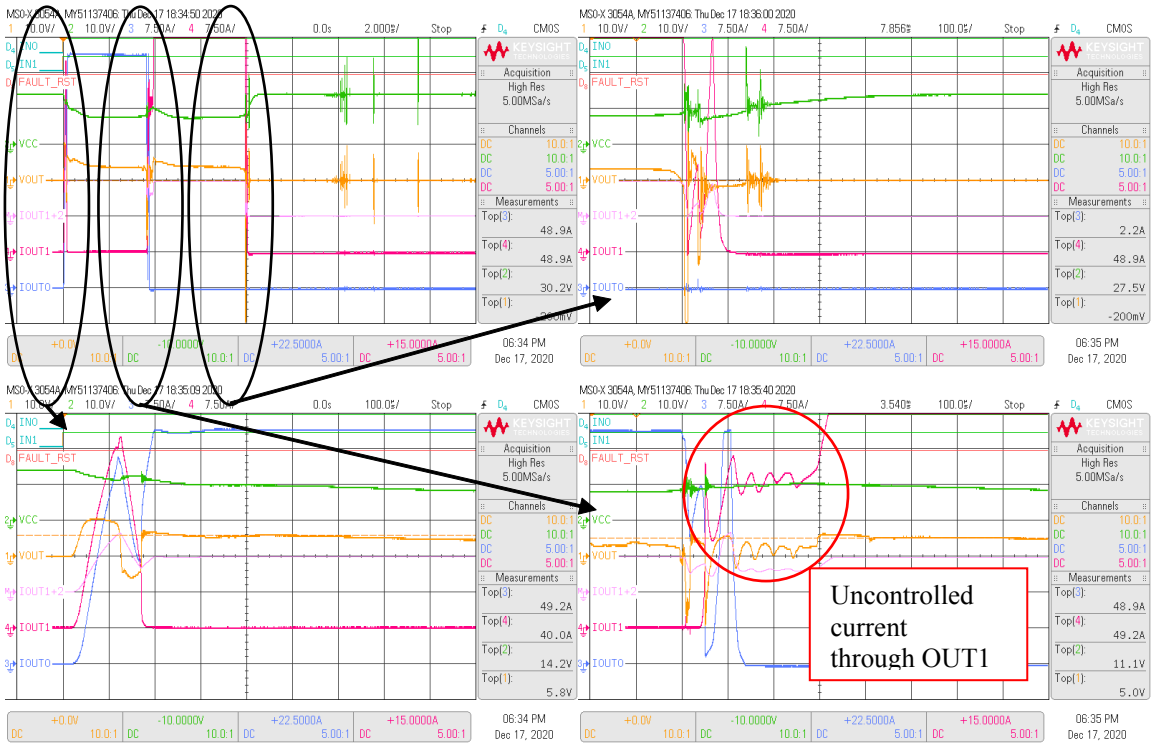


Figure 87. Inductive short – 5 µH/50 mΩ (VNQ9025AJ, Ch0 and Ch1 in parallel, latch mode)



As seen from the measurement the device got malfunctioned after the first power limitation pulse (OUT1 deactivated, while the OUT0 was reactivated again despite the latch-off configuration. Another turn-off cycle caused uncontrolled current flowing through OUT1 causing device destruction.

Paralleling of output channels should be restricted to exceptional cases. Due to the significant stray inductance of the wire harness, a paralleling of output channels implies the exposure to a critical high demagnetization energy in case of short circuit conditions impacting the component lifetime. Even a small difference between the channels (turn-off shapes, actual clamping voltage) could lead to almost 100% current imbalance during the demagnetization phase. In the worst case, all inductive energy is dissipated by only one channel. Since the inductive energy is proportional to the square of the load current, the stress in the channel could be four times higher in comparison with non-parallel operation at half of the current with the same inductance. Therefore, there is a potential risk of damage even at relatively low inductance values in the range of standard wire harness.

In case the paralleling of outputs is required, the devices must be configured in latch mode, to avoid the repetitive demagnetization stress during the power limitation or thermal shutdown cycling.

A special care must be taken in case of inductive V_{BAT} connection (long wire harness). Even a few µH of inductance of the supply line can generate a positive overvoltage pulse on VCC pin at turn-off (latch-off) of the outputs in case of short circuit conditions. This positive pulse could activate the VCC-GND signal clamp and cause damage of the device. Therefore it is recommended, in case of long battery cables, to add >100 µF low ESR electrolytic capacitor between the VCC pin and GND to keep the V_{CC} peak voltage safely below the minimum clamping voltage V_{CLAMP}. It is always recommended to run an experimental verification on module level to confirm the correct dimensioning and placement of the capacitor.

9 Inverse output current behavior

9.1 Introduction

The objective of this chapter is to describe the robustness of M0-9 devices submitted to disturbances injected on output in a typical application scheme.

Sometimes, devices operate in condition where the output voltage can be higher than the supply voltage V_S, for instance because the device is driving a capacitive (see Figure 88. Inverse current injected by a capacitive load) or inductive load (for example in case of electrical motor driving in H-Bridge configuration (see Figure 89. Inverse current injected by an inductive load in the high side driver of an H-Bridge), or because accidentally the outputs are wired to the battery (see Figure 90. Inverse current injected by a short circuit to battery) or moreover in case of a persistent ripple induced by a disturbance sources (for instance ISO pulses on battery which could create transient voltages on output power stage).

Figure 88. Inverse current injected by a capacitive load

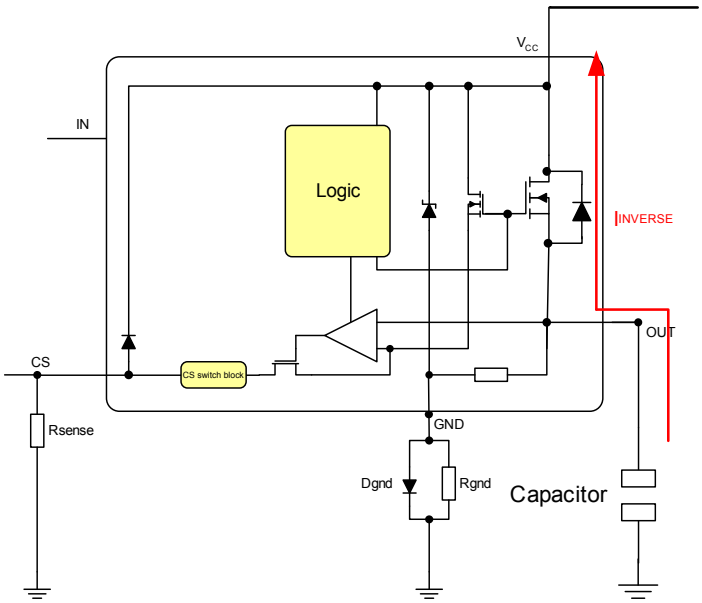


Figure 89. **Inverse current injected by an inductive load in the high side driver of an H-Bridge**

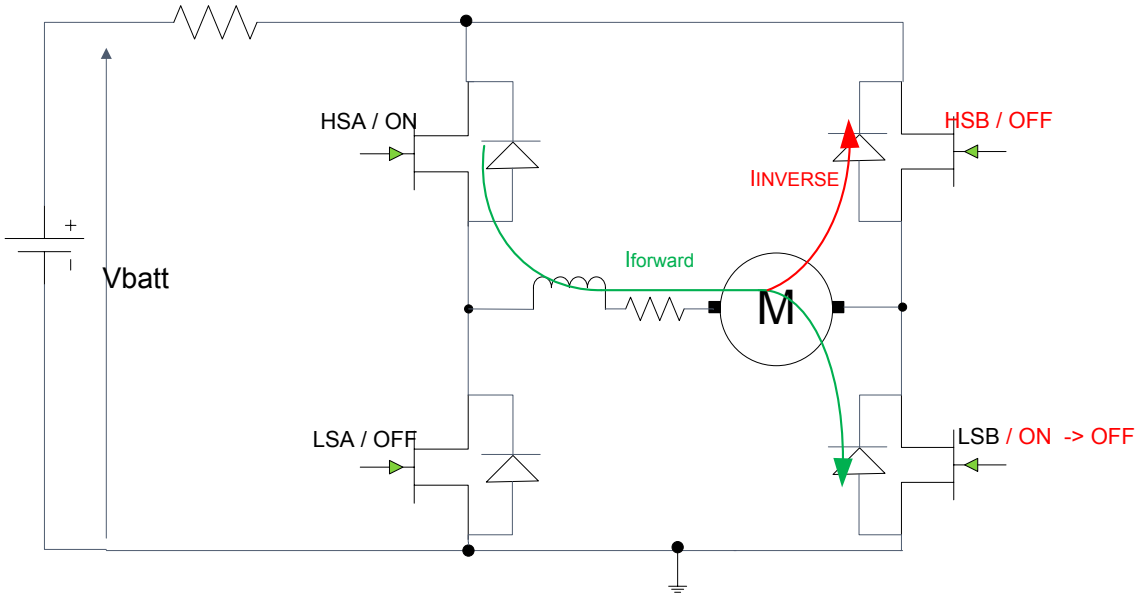
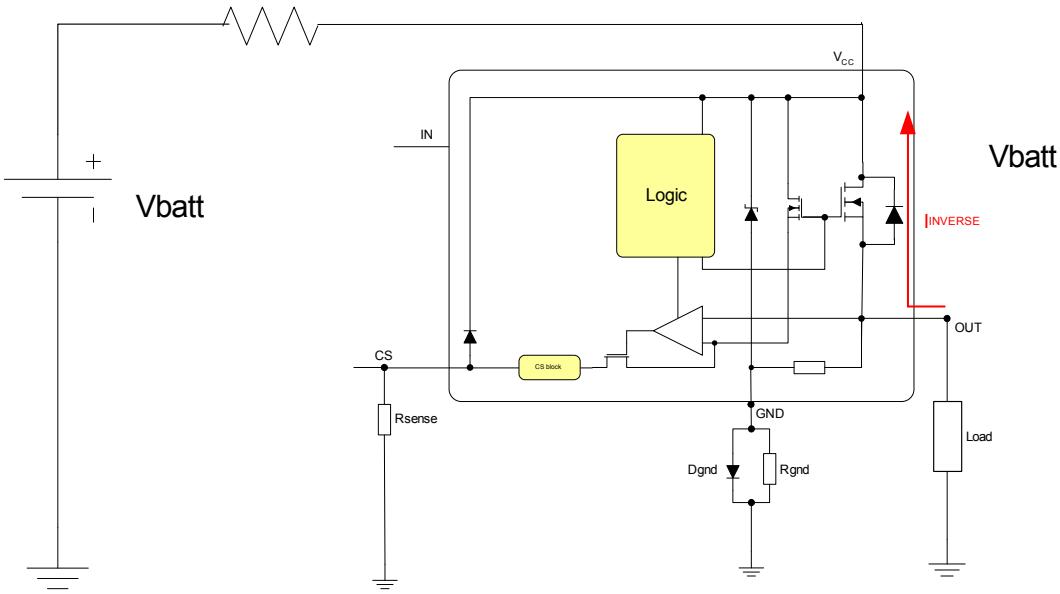


Figure 90. **Inverse current injected by a short circuit to battery**



We define $I_{INVERSE}$ the current that flows into the device from the output.

Generally, the conditions above described could become permanent, in case of output short circuit to battery, creating an extra stress on the solid switch.

9.2 Device capability versus inverse current

Considering a generic multichannel high side driver, in case of inverse current disturbance injected into output, several cases can occur depending on the combination of channels operating conditions (ON or OFF state).

A single channel HSD can be intended as a subset of a generic multichannel high side driver.

The inverse current ($I_{INVERSE}$) could modify the behavior of the channel under test (ChUT) and of the others close by. The analysis is performed both while the channels operate in a static way (permanent operation) and while they are dynamically controlled (PWM operation). The first $I_{INVERSE}$ value that modifies the expected channels behavior is called $I_{INVERSE(th)}$ (inverse current threshold).

In case of static operation (channel permanently ON or OFF) the $I_{INVERSE(th)}$ changes either the ChUT and the others previous state.

In case of dynamic operation, the $I_{INVERSE(th)}$ inhibits the effect of the input command used to change the channel state (for instance the $I_{INVERSE(th)}$ inhibits the turn ON of the ChUT and the others while are in OFF state at the time the inverse current is applied).

Moreover the effects of the $I_{INVERSE}$ are reported looking at the behavior of the diagnostic that could be modified by this current injection.

Effects of $I_{INVERSE}$ are reported in the two following operating conditions:

1. Device in steady operation (DC operation);
2. Device in PWM operation.

9.2.1 Device in steady state

Based on channels permanent status, three major cases can be identified as below reported:

Device sensitivity of channels permanently ON for dynamic inverse output current

Device state: all channels in ON state (inputs high) and loaded.

Test execution: increasing inverse current is injected in a channel (the ChUT), up to the $I_{INVERSE(th)}$.

Device sensitivity of channels permanently OFF for dynamic inverse output current

Device state: all channels in OFF state, with all channels loaded (inputs low).

Test execution: increasing inverse current is injected in a channel up to the $I_{INVERSE(th)}$.

Device sensitivity of channels either permanently ON or OFF for dynamic inverse output current while ChUT state is opposite to the one of the adjacent channel.

1. Channel “ch_i” set in OFF state while other channel “ch_j” is in ON state, and loaded. .
2. Channel “ch_i” set in ON state while other channel “ch_j” is in OFF state, and loaded.

Table 23. Example of channels configuration on a dual channels HSD

Test ID	Channels Configuration Chi/Chj	ChUT	MCS status	Signals monitored	
1.	ON / ON	Chi	Enable	Vout	Current Sense and Diagnostic Flag
3.-i	OFF / ON				
3.-ii	ON / OFF				
2.	OFF / OFF				
1.	ON / ON		Disable		
3.-i	OFF / ON				
3.-ii	ON / OFF				
2.	OFF / OFF				

This analysis results are reported in the Section 9.2.1: Device in steady state. Test conditions: V_{batt}=12 V, and room temperature (values in the table are representative of experimental results on a limited sample base).

In the following figure symbols are given:

- [V_F] is the body-diode forward voltage at room temperature.
- [d] is a delta voltage between V_{CC} and V_{out}, with a value lower than Vf.
- [V_{SENSEH}] is the fault voltage in CS diagnostic pin.
- [V_{OL}] is the OFF state open-load detection threshold.

Inverse current threshold experimental values according to channels status (Ch0 is the channel under test) and with CS enabled in current monitor mode.

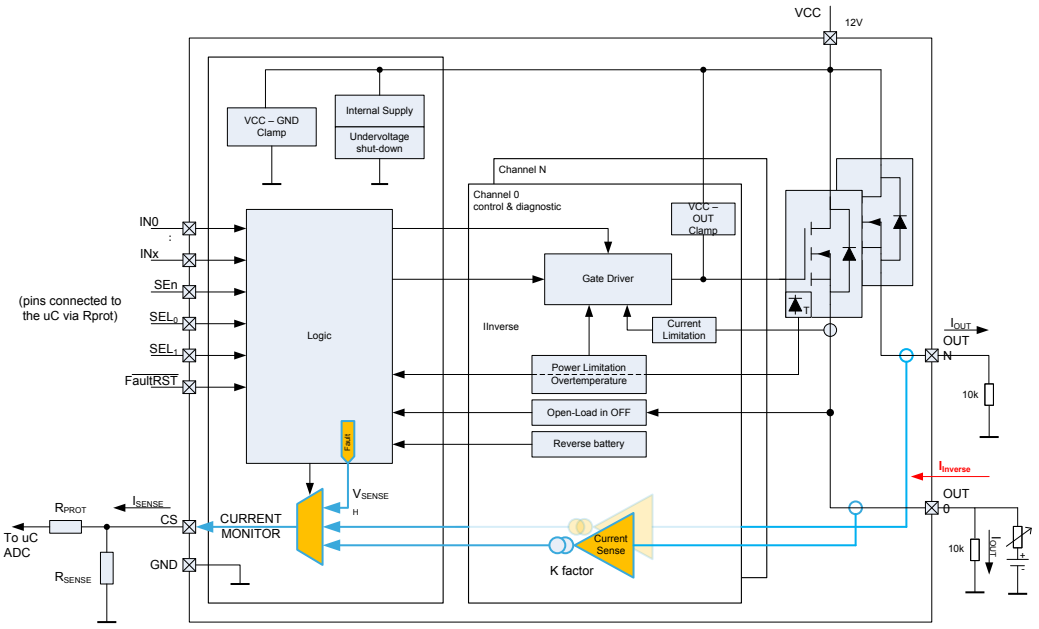
Table 24. Inverse current

Part number		Channel configuration									
		ON/ON					ON/OFF				
		RL_Ch0= 10 k/ RL_Ch1= 10 k					RL_Ch0= 10 k/ RL_Ch1= 10 k				
		I_injected on Ch0 [mA]	V_{out}[V]		CS voltage [V]		I_injected on Ch0 [mA]	V_{out}[V]		CS voltage [V]	
			Ch0	Ch1	Cs0	Cs1		Ch0	Ch1	Cs0	Cs1
VN9004AJ		125000	V_{CC}+d	-	0		-	-	-	-	-
	I_INVERSE(th)	127000	V_{CC}+Vf	-	0	-	-	-	-	-	-
VND9025AJ		19500	V_{CC}+d	V_{CC}	0	0	19500	V_{CC}+d	0	0	0
	I_INVERSE(th)	20000	V_{CC}+Vf	V_{CC}	0	0	20000	V_{CC}+Vf	> V_{ol}	0	$V_{SENSE H}$
VNQ9080AJ		6400	V_{CC}+d	V_{CC}	0	0	6400	V_{CC}+d	0	0	0
	I_INVERSE(th)	6500	V_{CC}+Vf	V_{CC}	0	0	6500	V_{CC}+Vf	> V_{ol}	0	$V_{SENSE H}$

Part number		Channel configuration									
		OFF/ON					OFF/OFF				
		RL_Ch0= 10 k/ RL_Ch1= 10 k					Ch0 floating / RL_Ch1= 10 k				
		I_injected on Ch0 [mA]	V_{out}[V]		CS voltage [V]		I_injected on Ch0 [mA]	V_{out}[V]		CS voltage [V]	
			Ch0	Ch1	Cs0	Cs1		Ch0	Ch1	Cs0	Cs1
VN9004AJ		-	-	-	-	-	129	V_{CC}+d	-	$V_{SENSE H}$	-
	I_INVERSE(th)	-	-	-	-	-	130	V_{CC}+Vf	-	$V_{SENSE H}$	-
VND9025AJ		3,2	V_{CC}+d	V_{CC}	$V_{SENSE H}$	0	3.2	V_{CC}+d	0	$V_{SENSE H}$	0
	I_INVERSE(th)	30000	V_{CC}+Vf	V_{CC}	$V_{SENSE H}$	0	650	V_{CC}+Vf	> V_{ol}	$V_{SENSE H}$	$V_{SENSE H}$
VNQ9080AJ (1)		-	V_{CC}+d	V_{CC}	$V_{SENSE H}$	0	0.4	V_{CC}+d	0	$V_{SENSE H}$	0
	I_INVERSE(th)	-	V_{CC}+Vf	V_{CC}	$V_{SENSE H}$	0	590	V_{CC}+Vf	> V_{ol}	$V_{SENSE H}$	$V_{SENSE H}$

1. *For VNQ9080AJ the side channel of Ch0 is Ch3 (instead of Ch1).*

Figure 91. Current injection test set-up and concerning a double channel HSD



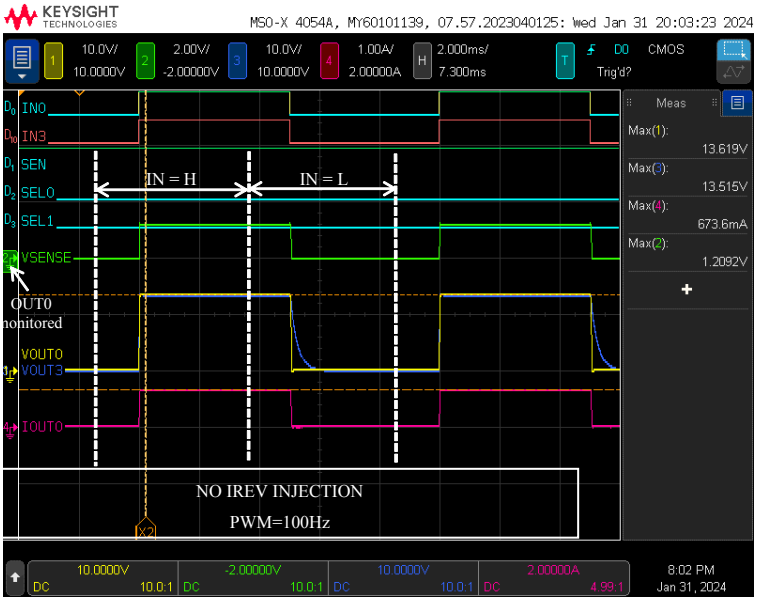
9.2.2 Device driven in PWM

Effects of $I_{INVERSE}$ are evaluated for devices driven in PWM as well.

Example of VNQ9080AJ device operation (in this case VNQ9025AJ) without inverse current injection is shown on following figure. Both channels (OUT0, OUT3 are driven by PWM 100 Hz, 50% duty cycle. Current sense output reflects OUT0 (SEL0, SEL1=0, SEn=1)

OUT0 R_{LOAD} = 20 Ω, OUT3 RLOAD = 10 k

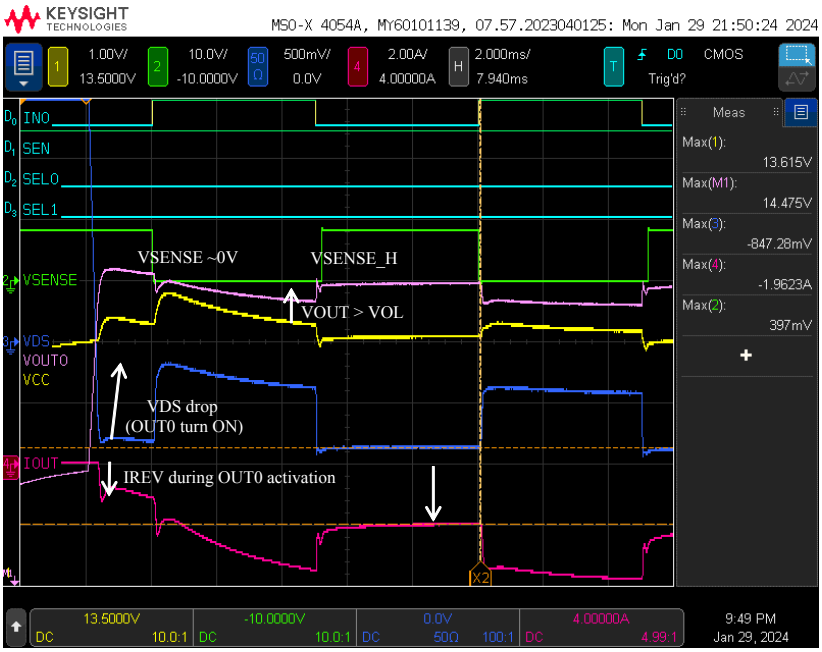
Figure 92. Standard device operation with no inverse current injection



During inverse current injection four major cases can be identified:

1. Inverse current injected to output does not exceed $I_{INVERSE(th)}$, output activation is possible
   Picture shows device behavior during this condition:

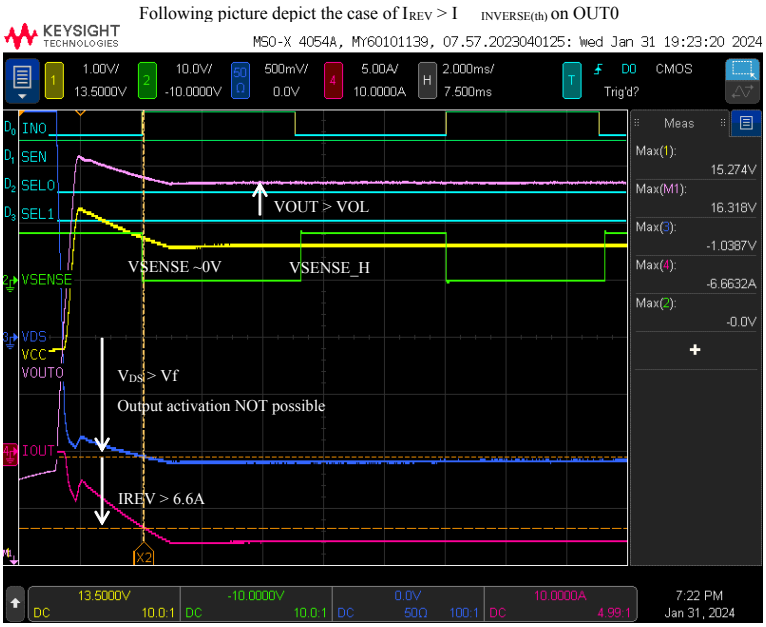
Figure 93. Vf threshold not exceeded on OUT0, output activated (I_{REV} > 2 A)



In this case, when the INPUT control signal goes from low to high on a channel with inverse current, the output is turned ON. Output stage turn-on is reflected by VDS significant drop (~200 mV).
Current sense output reporting channel with inverse current can be identified as an open load during output ON state (V_{SENSE} ~0 V). While the channel is turned OFF, CS monitor signal VSENSE_H. Such is due to output voltage being higher than VOL threshold (inverse current is given by the V_{OUT} higher than V_{CC}).
The next PWM period channel shows the capability to turn output ON even with I_{REV} > 2 A (with V_{DS} ~840 mV).

2. Inverse current injected to output is much higher, exceed $I_{INVERSE(th)}$, output activation NOT possible. Following pictures depict the case of $I_{REV} > I_{INVERSE(th)}$ on OUT0

Figure 94. Vf threshold exceeded on OUT0, output cannot be activated (I_{REV} > 6.5 A)

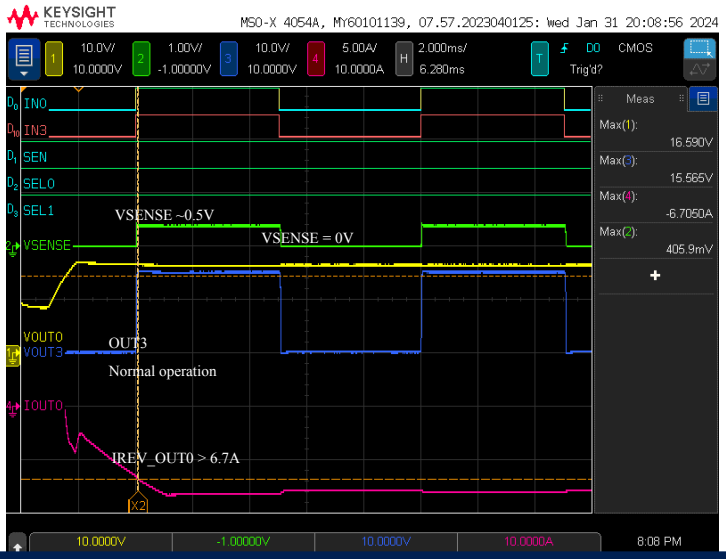


In case I_{REV} exceeds $I_{INVERSE(th)}$ on channel (V_{DS} >V_F), it is not possible to activate output by INPUT control. The situation remains until IREV drops below $I_{INVERSE(th)}$ level. Such case is documented in example picture above.
During INPUT activation for OUT0 the I_{REV} reach level ~6.6 A. No V_{DS} drop is seen, output stage remains deactivated. Inverse current flows through body diode of the channel.
C_{SENSE} output behaves in the same way as described in the previous case:

– When INPUT = HI, current sense outputs ~0 V (current flowing in opposite direction not detected, C_{SENSE} behaves as in open load condition)
– For INPUT= LO (OFF state), current sense outputs V_{SENSE_H} (because of V_{OUT} >V_{OL}).

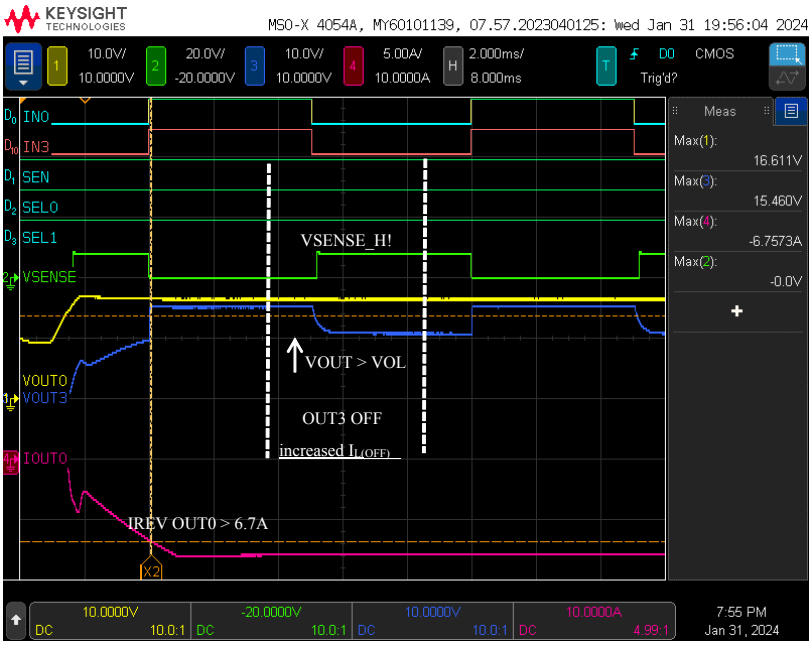
Inverse current injected to output has no impact to side channels controllability
Regardless of the dynamic state of channel with inverse current (either ON or OFF), remaining channels without inverse current injection are controllable without any limitation. Such is shown on the example picture:

Figure 95. Side channels controllability during inverse current injection



3. Inverse current injection leads to increased $I_{L(Off)}$ on side channels, position dependent.
   As soon as the $I_{INVERSE}$ is applied on a channel, all other channels show increased $I_{L(Off)}$, position dependent. The closer is the channel to the ChUT, the higher is the $I_{L(Off)}$.
   The following picture reflect inverse current on OUT0 impacting OUT3 OFF state (OUT3 is the closest channel to the OUT0, therefore highest influence of $I_{L(Off)}$ can be seen).

Figure 96. Device behavior when a $I_{INVERSE}$ current is applied to an output



In the example, high resistive load (R_LOAD = 10 k) was applied on OUT3. As can be seen, during the OUT3 OFF state, there is increased leakage current, consequently increasing output voltage to level ~10 V. Such voltage level exceeds the V_{OL} (open-load) threshold, causing V_{SENSE} reporting open-load condition (V_{SENSE_H}).

9.3 Conclusion

In case of inverse current disturbance injected into output, the device works properly, and the output stage follows the state of the IN pin, as long as the injected current does not exceed a certain threshold.

The inverse current threshold value, which modifies the device functionality depends on channels status (ON or OFF state).

In particular, the inverse current which inhibits device operation, with channels in ON state, is proportional to the ratio of Vf on R_{ON}:

$$I_{INVERSE(th)} \propto \frac{V_f}{R_{ON}} \quad (81)$$

Where:

- V_f is the body-diode forward voltage at room temperature: typical vale 0.6 V.
- R_{on} is the value of ON state resistance of power MOS at room temperature.

10 ESD protection

10.1 EMC requirements for ESD at module level

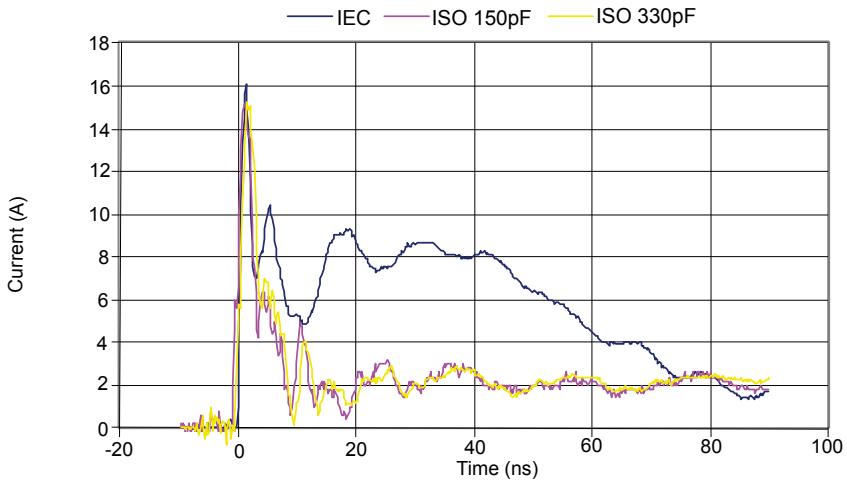
An electrostatic discharge (ESD) pulse on any ECU connector pin is an expected event during the life of a car. A transfer of discharge when a person approaches the ECU (for example during maintenance, reparation or installation) is a typical event that could damage the ECU and in particular an IC whose pins are connected to the outside environment.

Standards and limits are applied in order to simulate those events, but they strongly depend on the car maker specification and on the application. Some international standards for testing schemes and requirements have been introduced for the electrical systems such as car modules. They include IEC 61000-4-2 and the automotive standard ISO 10605.

The two standards use different values for the C/R components. IEC 61000-4-2 uses a 330 Ω resistor and a 150 pF capacitor. ISO 10605 uses both 330 Ω and 2000 Ω resistors, respectively in case of person approaching through a metal object or not, but different capacitances depending on condition. A 150 pF capacitor is used to simulate a person reaching into an automobile (for example a module load repair or change can be reproduced by this standard). A 330 pF capacitor is used to simulate ESD events for a person sitting in the passenger compartment in a vehicle.

Such ESD pulses are made by two components: a capacitive and a resistive one; the first one, made by a pure peak current in the first nanoseconds of the pulse, strongly depends on the distributed capacitance of the ESD simulator body. The resistive one is made by the RC content of the standard used (see the figure below).

Figure 97. ESD current pulses according to different standards



Typical car makers ESD requirements at module level are the followings:

1. Module not powered during the test.
   This test simulates any possible handling of the module prior to being assembled in the car.
   Connector pins to test are normally the ones that go out of the module:
   – Supply pins are protected and/or filtered as per the datasheet.
   – Output pins are protected and/or filtered as per typical design practice (for example, ceramic capacitor).

   Standard applied is the ESD HBM automotive acc. IEC61000-4-2 (150 pF/330 Ω).
   Required acceptance limits are in the ± 4 kV - ± 8 kV range (contact discharge).
   Test execution requires a sequence of 3 to 5 ESD pulses applied with a fixed delay time (1 s typically). Pulses are applied either by touching the pin under test with the ESD gun (contact discharge) or without touching it (air discharge). Test is passed if no pin to pin I/V characteristic degradation is reported after pulse exposure.
   This test simulates any possible handling of the module prior being assembled in the car. In some cases, extra test with a modified HBM network (for example 150 pF/2 KΩ) contact discharge is required.
2. Module power during the test
   This test normally simulates any possible stress that could be applied to the connector pins with the module already assembled in car.

The standard typically applied is the ISO10605 (330 pF/2KΩ).

Acceptance limits are in the ± 8 kV range (contact discharge) and ± 15 kV (air discharge).

In some cases, if higher pulse level is required, the applied network changes in (150 pF/2 KΩ).

Test execution requires a sequence of 3-5 ESD pulses applied with a fixed delay time. Real car battery must be used.

The module must be inserted in a test environment that simulates the in car one. It is normally ESD tested in real configuration (loads on, load off, driver in PWM…).

Pulses are applied to the pins that go out of the module such as outputs, transceivers pins…

The test is passed if no pin to pin I/V characteristic degradation is reported after pulse exposure.

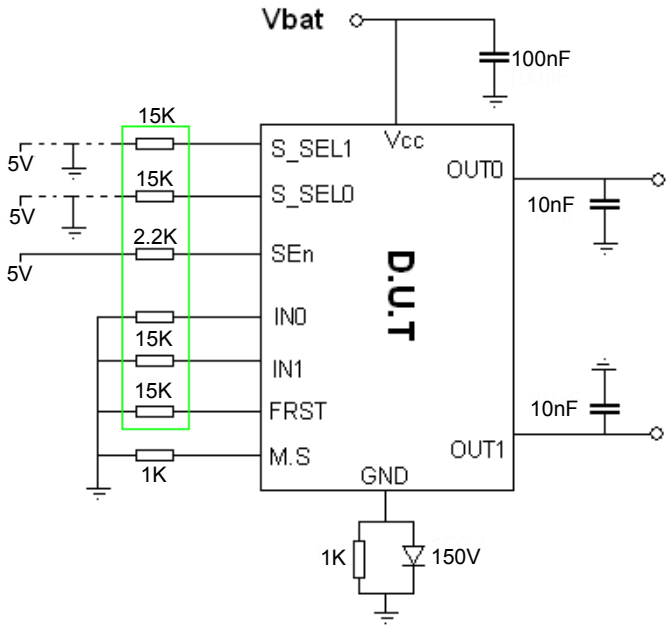
ESD pulses are applied between the pin under test and module ground connected to the ESD GND plane by a minimum wire.

It has been demonstrated some variability of the ESD. Main causes of such variability are in general the environmental conditions (humidity mainly), the ESD simulator pulse spread (specifically of the initial current pulse) and the test execution as well.

The M09 HSDs are characterized with powered and unpowered module ESD tests.

In the figure below the application schematic for a power test performed on a dual channel device which is the device under Test (DUT) is shown:

Figure 98. **ESD test application scheme for HSD placed on a powered module**



Test set-up:

- The wire length between V_{batt} and DUT V_{CC} and between board GND and ESD ground plane is minimized. ESD simulator ground is identical to battery ground. Both are connected on GND plane.
- DUT board is placed above the GND plane by means 50 mm thick insulating support.
- Filtering ceramic (X7R series) capacitors are placed on V_{CC} and on outputs.
- DUT outputs not loaded.
- In case of unpowered module test, the supply voltage is not present, and the device signal pins are connected to GND via the commonly used protection resistances.
  Test conditions:
- V_{batt} from real car battery= 12.6 V (in case of powered module test only).
- Room temperature.
  Test execution:
- Tests are performed, typically on a device in the OFF state, in case of powered module test.
- ESD discharges are applied on output board trace.
- Incremental discharge voltage levels from 1 kV up to 30 kV are applied with a 1 kV voltage step.
- 5 discharges on discharge pad OUTx with delay time of 1 sec are applied.
- Failure test by I/V curve check.
- Previous points are repeated till failure (if any).

Test procedure:

Devices' performances are guaranteed by margin to failure reported during characterization.

The test is performed on specific ESD test boards where specific ESD layout rules are applied.

The ESD characterization has demonstrated the capability of M0-9 HSDs to pass the ESD levels normally required. The following results are reported:

Table 25. **Results**

M0-9 HSDs ESD results	ESD at module level (powered)	ESD at module level (unpowered)
ESD pulse level	> |+/-8 kV|	> |+/-8 kV|

10.2 EMC requirements for ESD at device level

ESD tests for electrical components such as integrated circuits include:

- Human body model (HBM).
- Charged device model (CDM).

Those ESD test methods for integrated circuits are intended to ensure that the circuits can be safely handled in an ESD controlled environment during manufacture.

HBM:

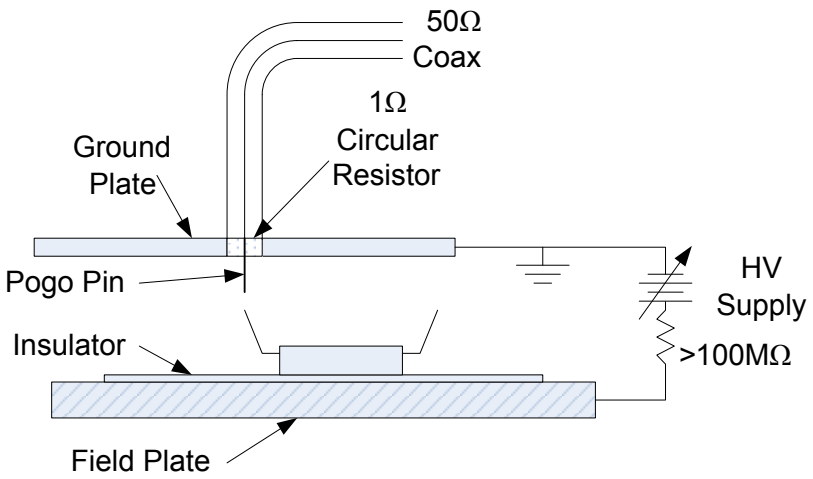
It is intended to simulate a charged person touching an integrated circuit. A person has approximately 100 pF of capacitance and skin and body resistance limit the current during a discharge. HBM test results, according to AEC-Q100-002, are reported in M0-9 datasheets absolute maximum ratings.

CDM:

This test (CDM-AEC-Q100-011) emulates an integrated circuit which becomes charged and discharges when it touches a grounded metal surface. There is no fixed value of a capacitor to discharge; the capacitance to be charged is the capacitance of the integrated circuit to its surroundings. The discharge path, consisting only of the circuit's pin and the arc formed between the pin and the metal surface, has very little impedance to limit current.

In the field induced CDM, the most popular implementation, the integrated circuit is placed pins up, on top of a field plate, with only a thin insulator between the circuit and the field plate. The thin space between the circuit and the field plate creates a capacitance whose value depends on the size of the integrated circuit and the package geometry. A ground plane is positioned by a pogo pin over the field plate as per below picture

Figure 99. ESD charge device model test scheme



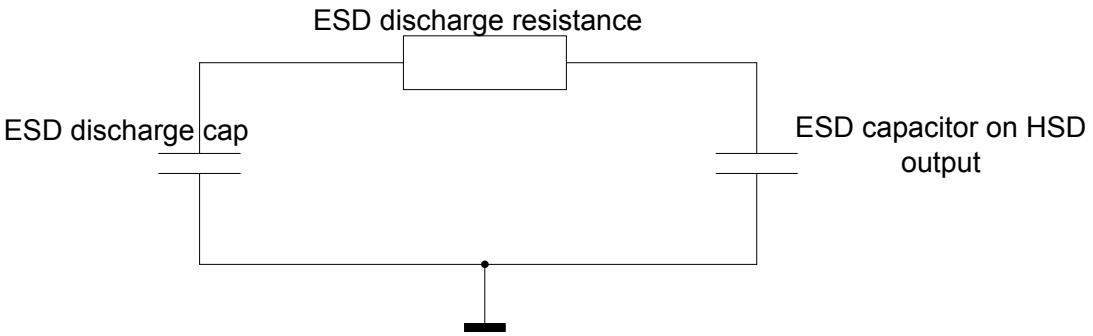
To perform the CDM test an uncharged circuit is placed on the field plate. The field plate is charged to a high voltage and the circuit's potential tracks the field plate. The ground plane is then moved so that the pogo pin touches the integrated circuit, grounding it. The result is a very fast redistribution of charge between the field plate to ground plate capacitance and the integrated circuit to field plate capacitances. 500 V is the commonly used value.

Results relevant to CDM-AEC-Q100-011 are reported in M0-9 datasheet's absolute maximum ratings. Devices' performances are guaranteed by margin to failure reported during characterization.

10.3 Design and layout basic suggestions to increase ESD failure point level

When the ESD pulse level required to be passed exceeds the standalone device capability, the HSD needs an external protection. The easiest and less expensive design practice is the use of a ceramic capacitor on the output. The capacitor goal is to limit the voltage and then the energy discharged into the device. This external capacitor builds a capacitive divider with the internal ESD pulse one (see the figure below).

Figure 100. **Equivalent circuit for ESD protection dimensioning**



A preliminary estimation of the capacitor value can be obtained applying the following formula:

$$V_{Final} = V_{ESD} * \left(\frac{C_{ESD}}{C_{ESD} + C_{EXT}} \right) \quad (82)$$

Where V_{ESD} is the ESD pulse level required, C_{ESD} is the ESD simulator capacitor value and V_{final} is the maximum allowed voltage across the HSD (roughly 37 V).

It is in any case necessary to verify the choice of the external capacitor, given by the above formula, with the real test. The main reason of that is the behavior of the capacitor impedance over the frequency. More specifically, since an ESD pulse has a frequency content in the range of hundreds of MHz the capacitive value of a real capacitor is lower than the theoretical one.

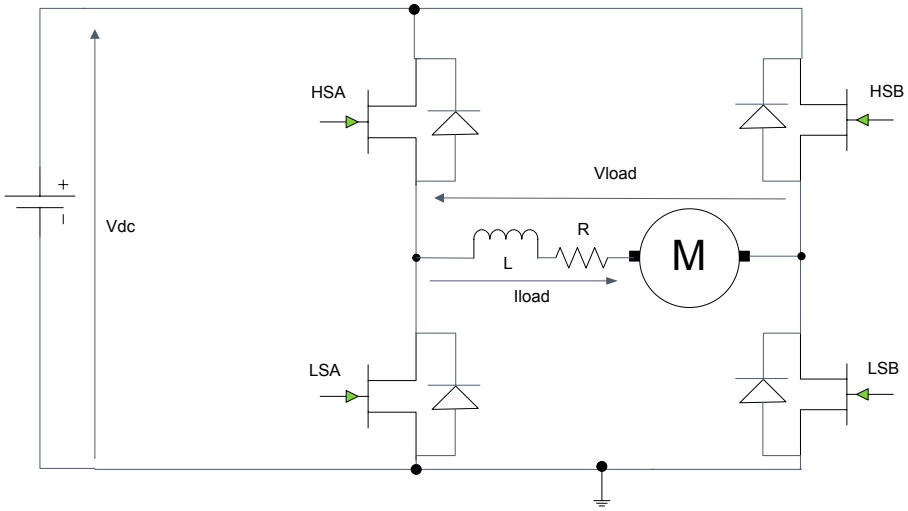
The ESD pulse destruction value strongly depends on the module layout. In order to make the module pass the required stress level, it is recommended to add a ceramic capacitor to the output close to the connector whose value could be in the range of tens of nF. This capacitor decreases both the applied voltage gradient and the maximum output voltage seen by the HSD.

11 Usage in “H-Bridge” configurations

11.1 Introduction

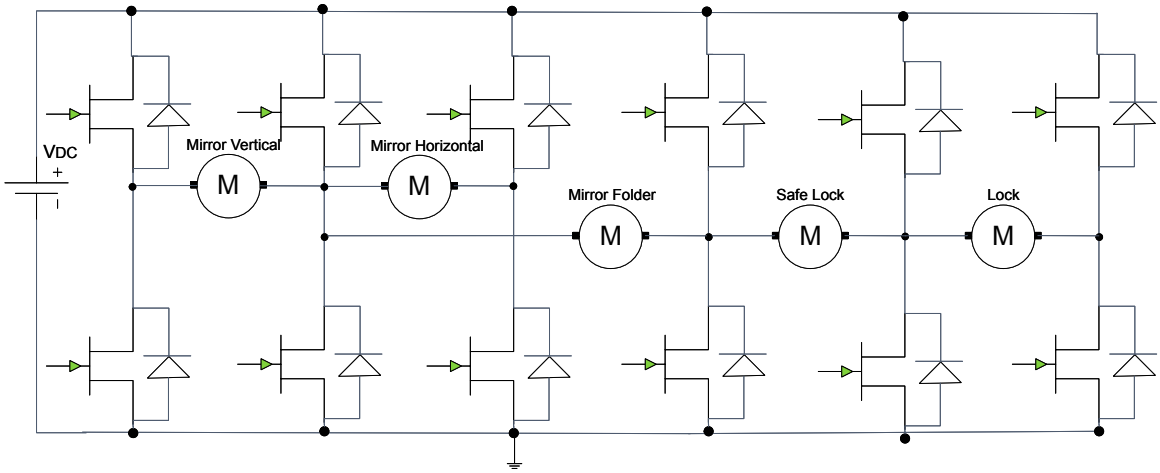
The term H-Bridge refers to the typical graphical representation of such a circuit. An H-Bridge is built with four switches (solid-state or mechanical). Two of them are connected between the battery and the load (high side switches), the other two between the load and the ground (low side switches). When the switches HSA and LSB (according to the Figure 101. H-Bridge scheme, where a basic circuit with four MOSFETs driving a bidirectional DC motor is shown) are closed (and HSB and LSA are open) a positive voltage will be applied across the motor. By opening HSA and LSB switches and closing HSB and LSA switches, this voltage is reversed, allowing reverse operation of the load (in most cases a DC motor).

Figure 101. H-Bridge scheme



Using the nomenclature above, the switches HSA and LSA (or HSB and LSB) should never be closed at the same time, as this would cause a short circuit on the input voltage source. This condition creates the so called cross current. A simpler configuration called half bridge, consists of a single high side driver which opens or closes the load towards the battery, the loads itself which is directly grounded and a low side driver in parallel to the load (normally inductive), which is activated only to connect the load to ground. The low side driver in this way absorbs the inductive energy which otherwise would be completely discharged through the high side driver with a consequent possible damage in case the energy exceeds its capability. In case of a DC motor, the low side driver, when turned on after having turned the high side driver off, brakes the motor safely to ground and stops it. Finally, more than two half bridges can be connected together in order to drive at least two different loads in cascaded configurations. The independent activation and diagnostic reading of each switch gives large flexibility in those configurations.

Figure 102. **Example of automobile multi-motor driving connection**



11.2 M0-9 high side drivers in “H-Bridges” : specific considerations

The M0-9 high side drivers, single and multichannel, can be used to drive various bidirectional loads in H-Bridges configurations. Some general guidelines, should by the way, be applied in order to avoid these issues. An overview of some potential issues is given in the following paragraphs.

11.2.1 Short circuit event to ground and to battery

In case of short of one output of the H-Bridge to GND the M0-9 high side driver protects the H-Bridge with its well know protections circuitry (current limitation, power limitation, thermal shutdown with autorestart or latch off). Current sense pin will signalize V_{SENSEH} like already explained in paragraph 8.2.4.

In case of short circuit of one output of the H-Bridge to V_{CC} , the H-Bridge needs an external protection during ON state because in this case the low side of the faulty leg will be submitted to the total battery voltage (in case of hard short circuit) or to a part of it (in case of a weak short circuit) with its possible damage. A possibility to guarantee the protection in these conditions would be to implement a drain-source monitoring of the low side drivers directly via the microcontroller I/Os or to use fully protected low side drivers (for example LSD belonging to ST’s OMNIFET families).

11.2.2 Cross current events

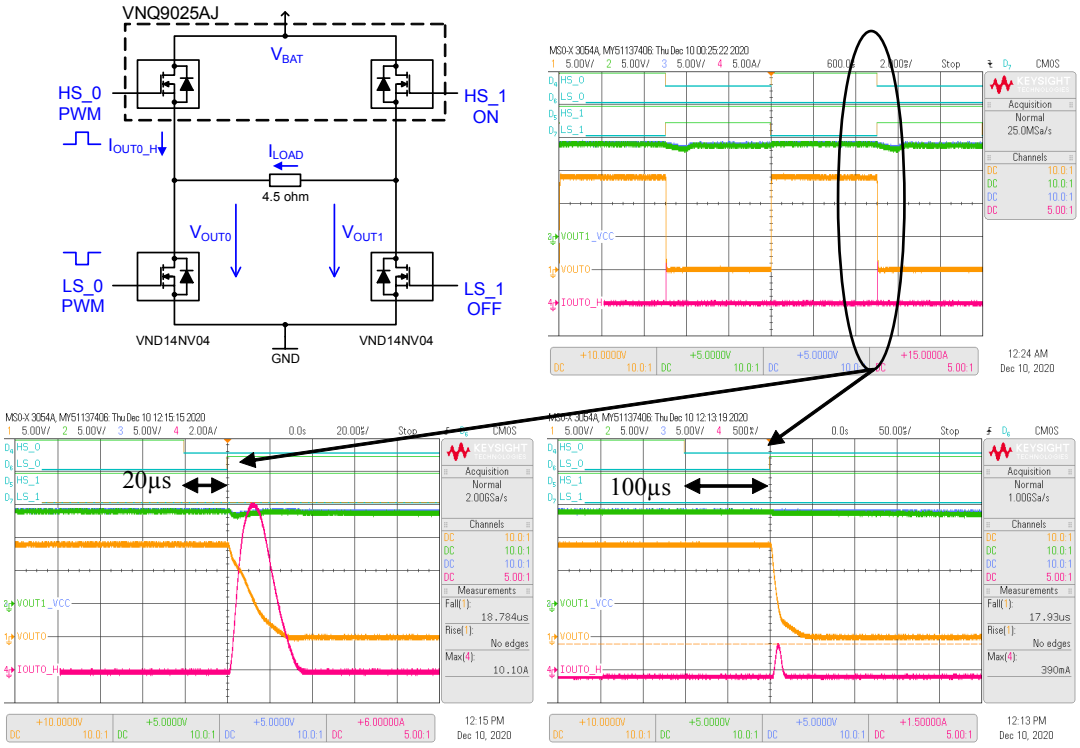
11.2.2.1 Cross conduction due to MOSs delay times

A common issue which can affect one leg of an H-Bridge occurs when both HSD and LSD are on at the same time. This condition, called cross current, can happen even if it is not intended to drive the HSD and LSD simultaneously and can cause significant extra power dissipation which can become critical especially during PWM driving. For instance, when the HSD is turned off and the LSD is turned on (in order for example to change a motor direction), logic propagation delay and the time required to discharge and charge respectively the HSD and LSD gate capacitances can cause the HSD still to be half on when the LSD is turned on.

Let us consider a practical example where a VNQ9025AJ is used in combination with two VND14NV04 (belonging to the OMNIFET II family) to build an H-Bridge. For the sake of simplicity, a resistive load of 4.5 Ω is driven. The HSD_0 and LSD_0 on the left leg is driven complementarily with a PWM signal and with different delay times between switching off of the HSD_0 and switching on of the LSD_0; In order to see the effect of the cross conduction and how it can be attenuated or eliminated, a delay has to be introduced. Let us quantify in this example the delay. Current in HSD_0 is plotted.

In the left side plot of the figure below a delay of 20 µs only is given, on the right side a delay of 100 µs is given and still it is possible to see a residual cross current.

Figure 103. VNQ9025AJ cross conduction with different OMNIFET delay times



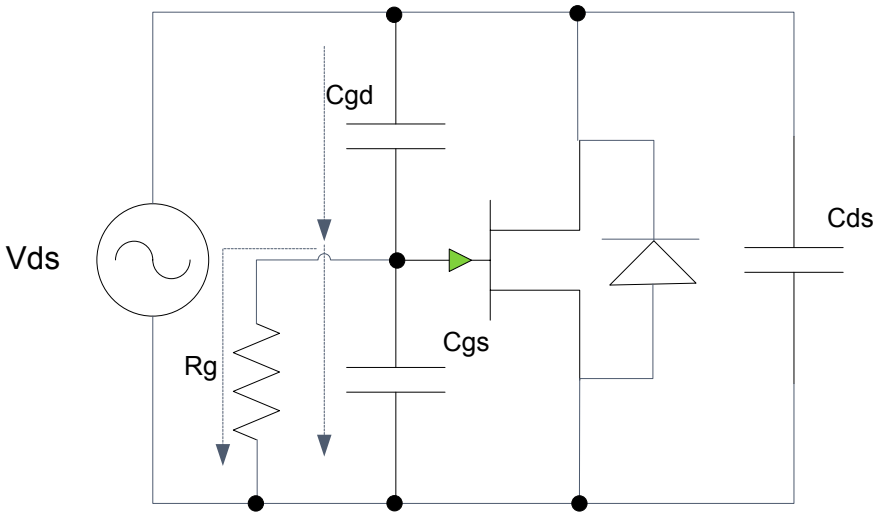
At 20 µs in this case, the cross-current spike is eliminated. Similar considerations can be applied when the HSD must be switched on after the LSD is switched off, but in this case the switching off times of the OMNIFET II are much shorter than the switching times of the HSD, so in this case the cross conduction shall not take place. To avoid the cross conduction, due to the mechanism explained before, the low side drivers must to be driven with delay times, named also “dead times” when for example, in case of a DC motor, it is requested to change direction in the rotation.

As general rule for M0-9 HSD, minimum dead time to be introduced in the low side driver is about 400 µs.

11.2.2.2 *Cross conduction due to MOSs capacitances*

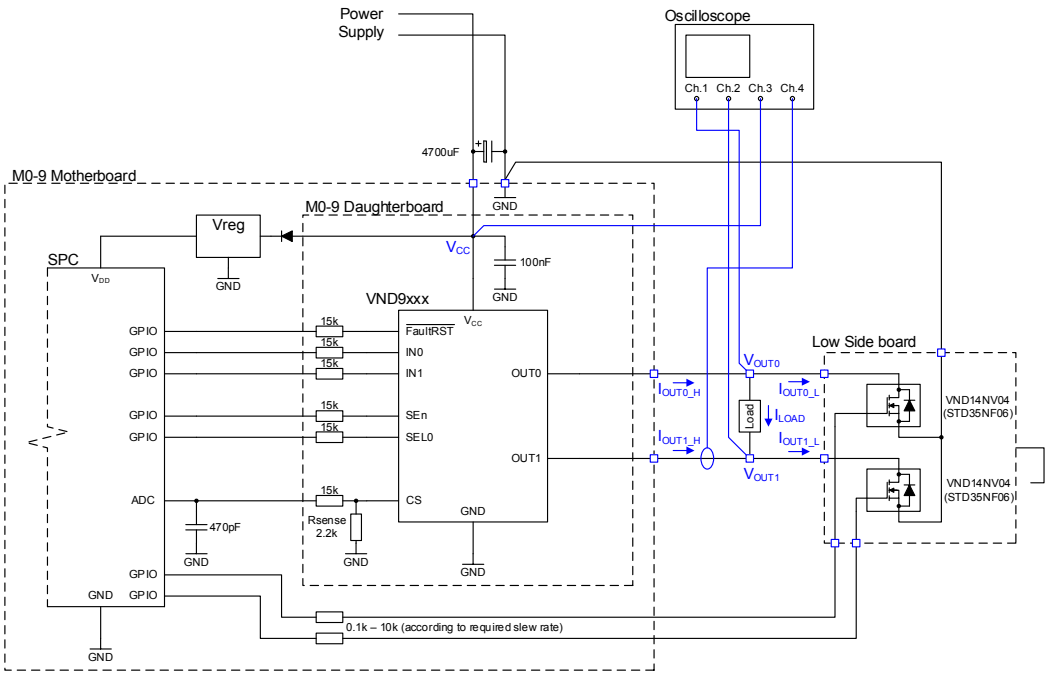
Another event causing cross conduction is related to dynamical effects inside HSD and LSD and precisely to high voltage gradient which can occur across them. Let us consider a H-Bridge in which one of the two MOSFETs of one leg (e.g. HS_1) is completely off and the LSD_1 is switched on. Due to this, the drain-source voltage of HS_1 is submitted to a fast increase (high dV_{ds} / dt) and considering the simplified equivalent model of the MOSFET of the HS_1 (represented in Figure 104. Power MOS capacitance effect during high dV_{DS}/dt) this gradient injects a current in the gate-drain capacitance and the gate-source capacitance. The current component flowing on the C_{gs} causes the gate voltage to increase, and if the gate voltage reaches the PowerMOS threshold a consequent turn on of the HS_1 takes place. As this event occurs, the HS_1 and LS_1 conduct for a limited time simultaneously creating a cross conduction event, in this case called also “shoot-through”.

Figure 104. **Power MOS capacitance effect during high dV_{DS}/dt**



A practical example follows in which (see the figure below) a test set up with two VND14NV04 (or STD35NF06 for fast transient) and one VNQ9025AJ connected in H-Bridge configuration is aimed to reproduce the shoot-through.

Figure 105. **Test set up for H-Bridge cross current**



Test set up contemplates driving through a microcontroller of HSDs and LSDs. The latter can be set with adjustable switching times via different input series resistors (OMNIFET II). In this way it is possible to measure the sensitivity to shoot-through of the HSD according to decreasing LSD input resistances (this means increasing switching slopes). A 4.5 Ω resistance is supplied by turning HS_0 and LS_1 on and LS_1 is submitted to a 100 Hz PWM. So the shoot-though relevant critical element is HS_1 (driven OFF). Result is that in this case the shoot-through is eliminated in wide range of dV/dt, negligible current of 79 mA leakage current was measured at highest reached factor ~300 V/µs.

The shoot through mechanism is a limitation factor of PWM frequency of H-Bridge with Standard M0-9 HSDs (frequently use in case of speed control of DC Motors can be up to 30 kHz) because at each period an extra power dissipation, due to the cross current, is summed up to the existing continuous and switching losses of each element. Therefore,the frequency of M0-9 HSD should be carefully evaluated. In Table 26. Maximum switching slopes which vs the peak current on VNQ9025AJ a summary of the maximum leakage current measured on a typical sample which cause no shoot-through in the given test set up for VNQ9025AJ.

Table 26. Maximum switching slopes which vs the peak current on VNQ9025AJ

Device	Slew rate of the low side switch [V/us]	Maximum measured peak current [mA]
VNQ9025AJ	5.1 V/µs	3.7
	10 V/µs	7
	17 V/µs	12
	300 V/µs	79

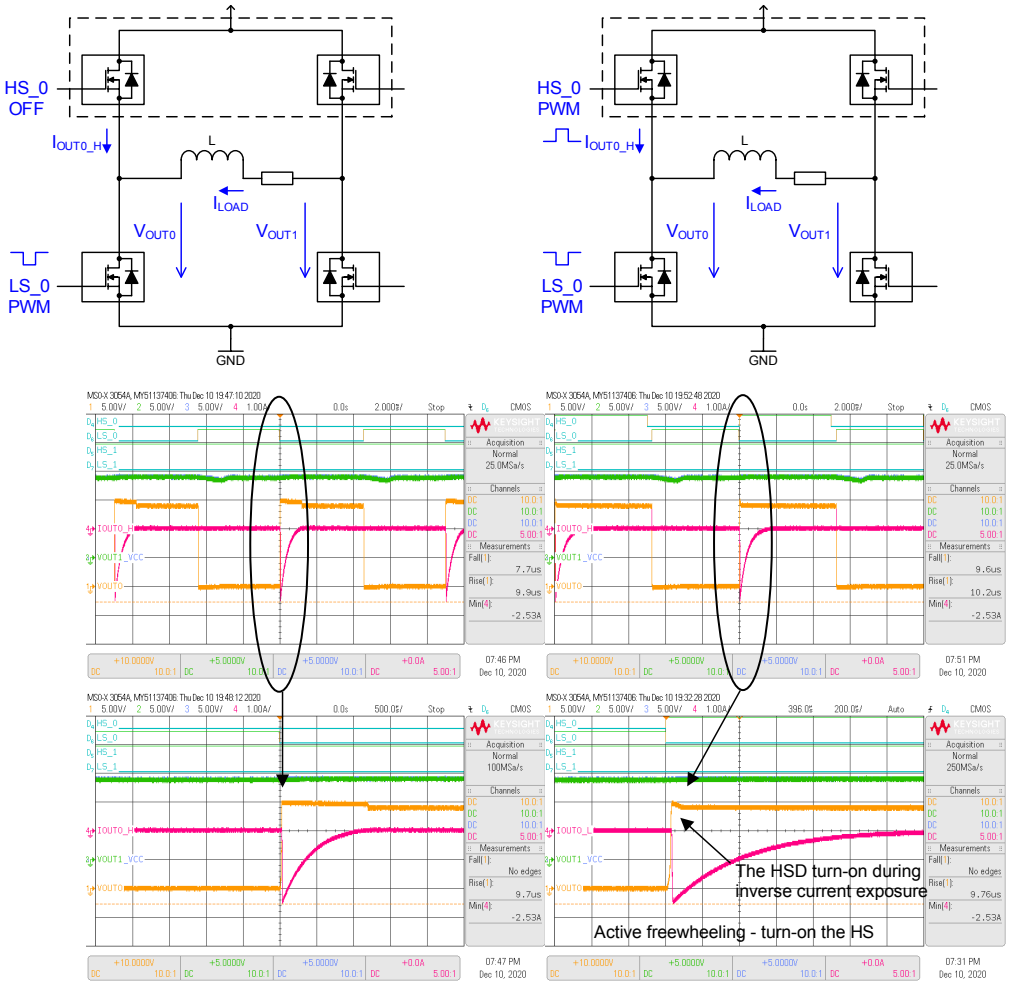
11.2.3 Freewheeling current of inductive loads

The driving in PWM of inductive loads is a common technique to control the average load power according to application requirement (acting as speed control for example in case of DC motors).

If the PWM signal is applied to the LSD, during its off state the inductive load current re-circulates in the body diode of the M0-9 HSD. If during this phase, the HSD input is driven ON, the current will keep on flowing through the body diode until the HSD gets activated. In the Figure 106. High side freewheeling phase an example with VNQ9025AJ combined with two OMNIFET II LSDs, driving an inductance explains this behavior (the current in HS_0 output is plotted as well). On the left side is depicted behavior with no active freewheeling (current flows through the body diode of HSD), right side shows active freewheeling, where the current flows at the beginning flows through HS_0 body diode first, within ~100µs current continues to flow through activated HS_0.

H-Bridge formed by one VNQ9025AJ and two OMNIFETs II showing the high side freewheeling phase.

Figure 106. **High side freewheeling phase**



12 Operation during cold cranking

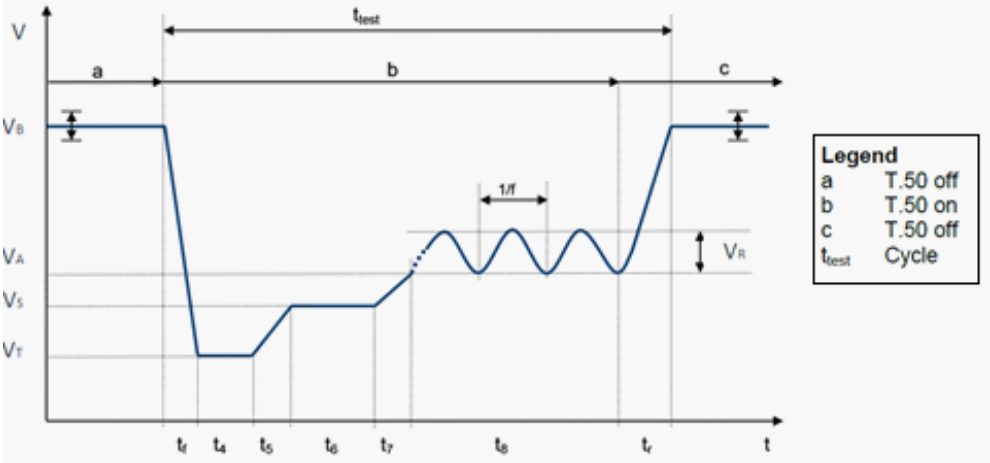
As the automotive electronic component count increases, standards agencies such as the international standards organization (ISO) and the society of automotive engineers (SAE) are toughening the qualification tests regarding the cranking event.

During cranking operation on a traditional 12 V power system, the battery-driven starter motor must rotate the engine until combustion begins. In that event, it is drawn a heavy current causing a reduction of the battery voltage from its normal level.

The LV124 E-11 start pulse test has two levels, "normal" and "severe"; each one defines a particular set of voltage levels and times according to the cranking profile shown in the figure below that shows a typical test profile.

A typical cold-crank test profile (voltage over time) that simulates an engine crank during different stages.

Figure 107. Typical cold-crank test profile



As shown in Table 27. E-11 severe start pulse parameters, the voltage is initially at V_B, indicating the battery voltage under quiescent conditions. As the simulated engine starts to turn over, the load on the simulated battery increases causing the test voltage to drop to a lower voltage V_T, where it remains for time t_4 until slowly recovering.

Table 27. E-11 severe start pulse parameters

Parameter	"Severe" test pulse
V_B	11.0 V
V_T	3.2 V
V_S	5.0 V (0%, -4%)
V_A	6.0 V (0%, -4%)
V_R	2 V
t_f	≤1 ms
t_4	19 ms
t_5	≤1 ms
t_6	329 ms
t_7	50 ms
t_8	10 s
t_r	100 ms

Parameter	"Severe" test pulse
f	2 Hz

The M0-9 family is designed to work during engine start pulses. In particular, the device remains on with full function during and after the LV 124 E-11 test for both "normal" and "severe" start pulses.

Figure 108. Application schematic of VNQ9025AJ for the severe cold cranking test shows the application schematic and the test condition used during severe cold-cranking, whereas the test conditions are highlighted in Table 28. Test parameters and pin configuration.

Figure 108. Application schematic of VNQ9025AJ for the severe cold cranking test

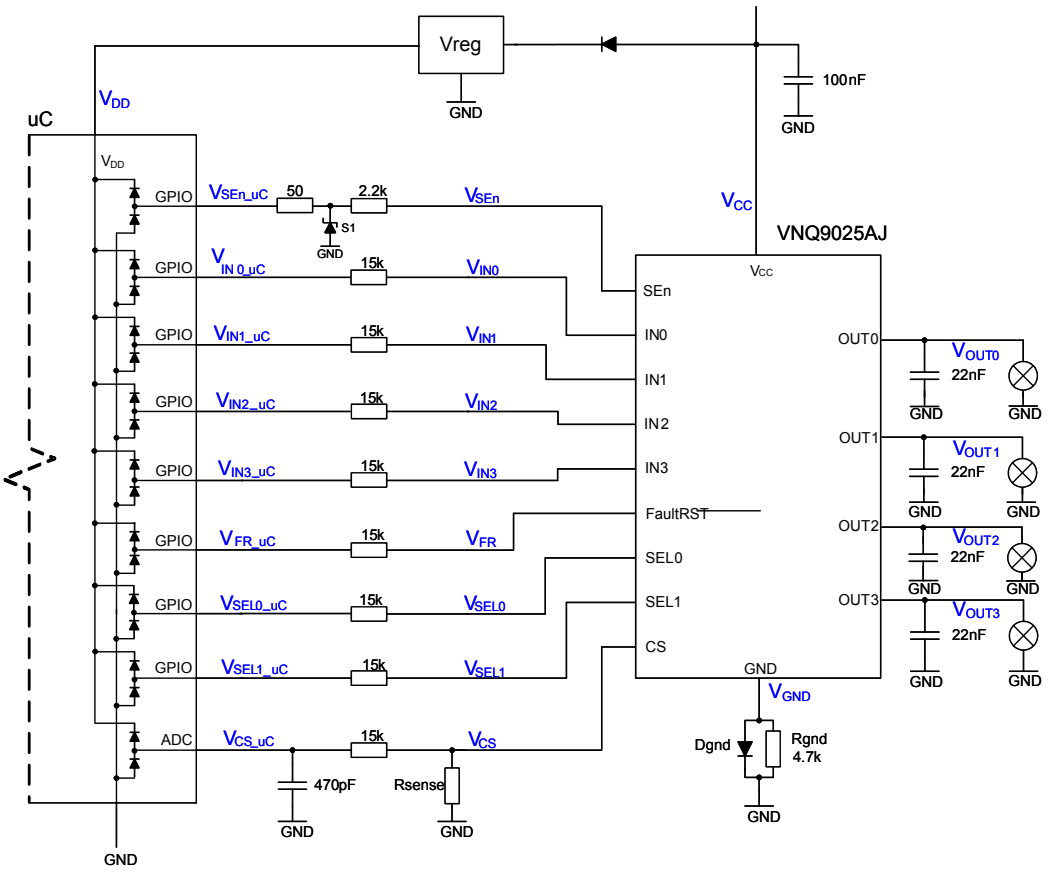


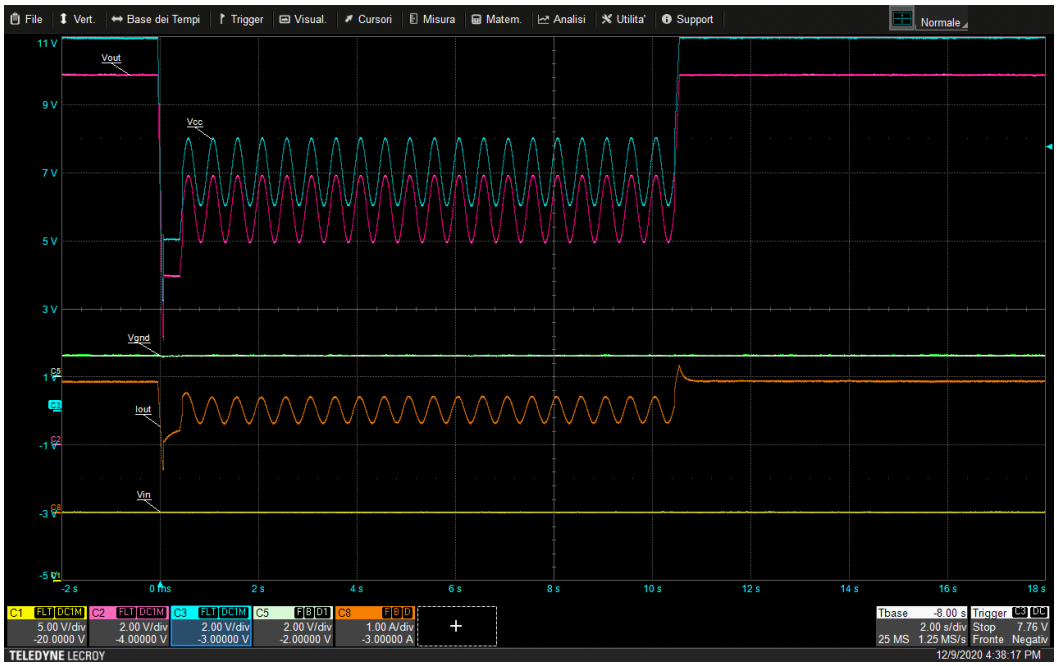
Table 28. Test parameters and pin configuration

Pin configuration / test parameter	Value
T_{amb}	25 °C
SEn	5 V
SEL1= SEL0	0 V
Vin0	5 V
FRST	0 V
Load	P27W

During the cold cranking, the device remains switched on, thus the channel remains on but with Ron not too far from the target typical value specified in the datasheet for each device.

The figure below shows the severe cold start according to the test conditions and application schematic previously shown.

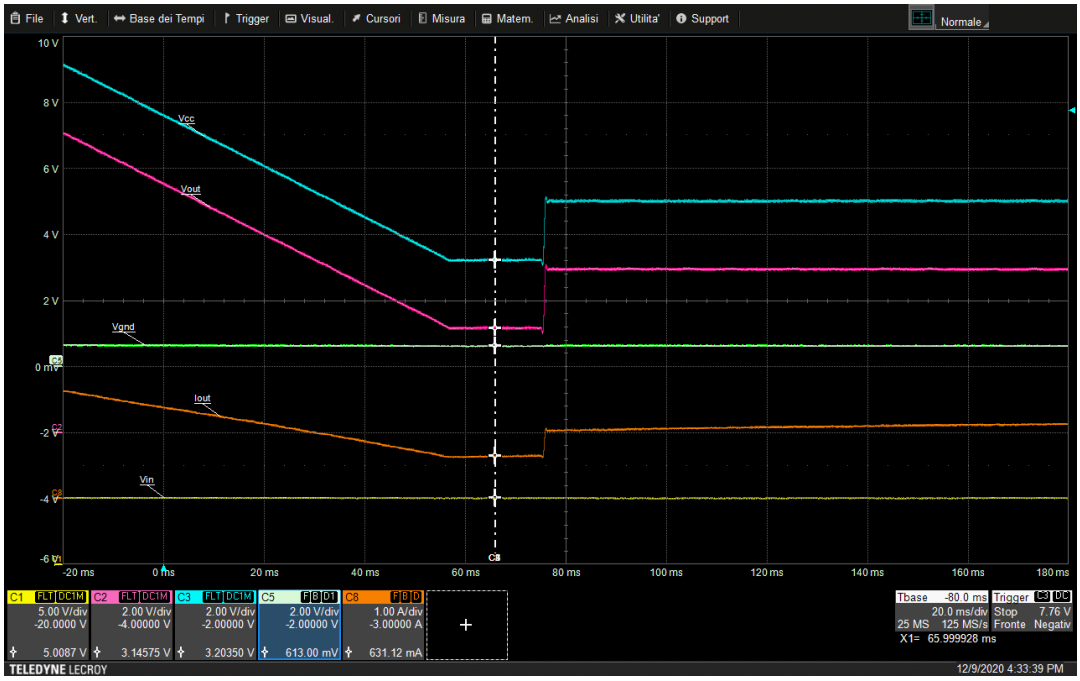
Figure 109. Severe cold start test result



The device can remain on with a slightly higher Ron in this phase than the typical value specified at 13 V of battery voltage. In such a way, the load does not suffer any significant variation and the VNQ9025AJ can ensure the operational continuity of the load during the cold start.

The shows a detail of the severe cold start, placing the cursor at V_{CC} = 3.2 V. The Ron in this condition can be calculated as follows: (VCC–VOUT) / I_{OUT} = (3.2 V-3.146 V)/630 mA ≈ 86 mW.

Figure 110. Severe cold start detail at V_{CC}=3.2 V



In the scope plot, Vgnd has been inserted to show the effect of the D_{GND}. The minimum voltage between V_{CC} and device GND pin (when V_{batt} = 3.2 V) is about 2.6 V.

In conclusion, due to the ground shift we notice that the device under test and its internal logic sees 2.6 V (and not 3.2 V) due to the presence of D_{GND} (0.6 V drop) as a reverse battery protection scheme.

Revision history

Table 29. **Document revision history**

Date	Revision	Changes
25-Jun-2024	1	First release.

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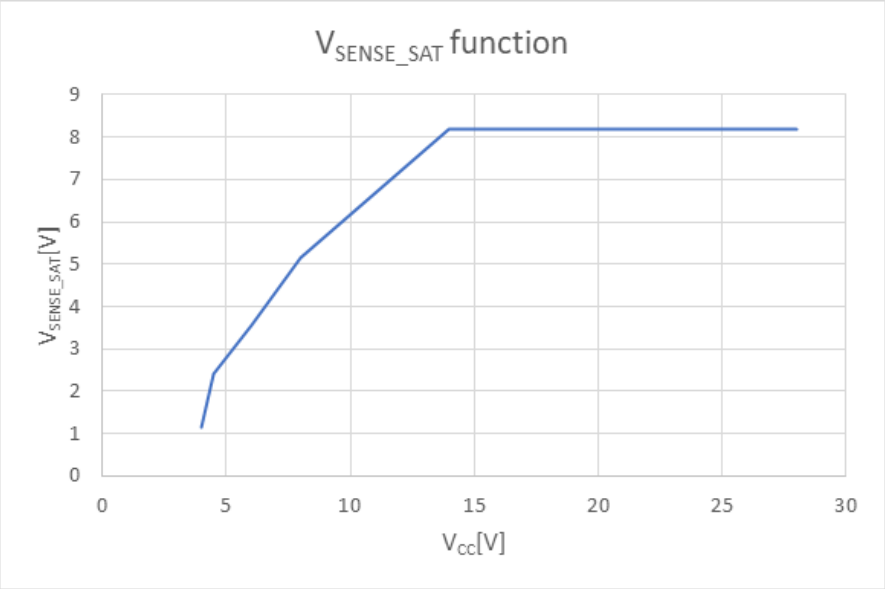

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