ST-ONEMP parameter configuration

Introduction

This user manual provides information about the parameters of the ST-ONEMP device and the setup procedures for the most important ones.

The ST-ONEMP is the world's first digital controller embedding an Arm® Cortex® M0+ core, an offline programmable controller with synchronous rectification, and USB PD PHY in a single package. Such a system is specifically designed to control ZVS non-complementary active clamp flyback converters to create high power density chargers and adapters with a USB Power Delivery interface.

The device includes a configuration memory that allows the user to configure the ST-ONEMP, tailoring it for the required application.

ST-ONEMP offers a parameter set that differs from ST-ONE to accommodate the Multiport behavior.

This user manual goes through all the parameters in detail and explains how to set them in a real application. For any further information about the ST-ONEMP product, please refer to the ST-ONEMP datasheet (see www.st.com).

1 Prerequisites

To easily program the ST-ONEMP during the development of a new application, a graphical user interface (GUI) has been developed. The GUI strictly works with a communication interface board and allows real-time monitoring of the device, calculates the key hardware elements of the application and programming of the ST-ONEMP. For more information about the GUI and the interface board, refer to the DB4310 - USB to I²C/UART interface board for STNRG digital power controller products (STNRG01x and ST-ONE).

The default firmware loaded by factory does not provide the debug option, so it is possible to modify the parameter but not execute the live fine-tune of the application. To do this, refer to st.com to download the debug firmware and related user guide.

2 Digital parameters configuration

This section describes the procedures to set up the most important IC parameters according to the board specifications and components.

By setting the parameters, the user can define the type of communication protocol (for example, USB PD) and the relative options, the thresholds, and behavior of IC protections such as the overtemperature, and the switching control loop parameters.

The parameters are divided into 4 different groups:

- Application setup parameters
- Application code parameters
- USB PD related parameters
- Power parameters

Attention: *If the user sets the USB PD protocol, you cannot use CC lines for debug purposes or for changing parameters, so you must relocate the serial line on GPIOs the first time of programming..*

2.1 Application setup parameters

In this area, the user defines if the USART interface is active and on which pin. Moreover, in this area it is possible to enable the application code write to protect.

Note: If the application code is protected but UART is active, it is possible to erase the entire area and reload a different setup or application entering in boot mode.

In the next section all the digital parameters of this portion of area are described.

2.1.1 BCMode

This field selects the boot code activity and, depending on the selection, enables the application code to run or not.

Available values are:

- 0x01 = BCM1 = Jump to application if present (no debug)
- 0x02 = BCM2 = No jump to application area. BCM2 is also called “Programming Mode”
- 0x03 = BCM3 = Equal to BCM1 but add the possibility to use the external command (available only with debug firmware)

By default, the BCMode parameter is set to BCM2 so the IC is not allowed to start up. To start the system up, put this parameter in BMC1, otherwise, put this parameter in BMC3 to live fine-tune the parameters (debug code download needed).

2.1.2 USART_enable

This field selects which USART interface is selected.

Available values are:

- bit0 = UART enable [Disabled (0) / Enabled (1)]
- bit1 = UART Rx enable [Enabled (0) / Disabled (1)]
- bit4 = UART mapping [GPIO0-GPIO1 (0) / CC1-CC2 (1)]
- bit7 = Recovery mode [Enabled (0) / Disabled (1)]

Note: If bit0=0, it means UART disabled, the other bits are not considered.

Note: If UART Rx is disabled (bit1=1) the device could send messages while reception of UART (command) messages is disabled. It could be enabled for security reasons in case UART cannot be disabled.

2.1.3 Internal PULL-UP on GPIOX

Internal PULL-UP on GPIO0 and GPIO1 pads configuration.

Available values are:

- bit0 = internal PULL-UP on GPIO0 [Disabled (1) / Enabled (0)]
- bit1 = internal PULL-UP on GPIO1 [Disabled (1) / Enabled (0)]

2.1.4 ACP_protection

The Application Code Protection area defines which page (2 Kbytes size) is hardware protected, that is, write/erase page commands are rejected:

- If 0, no pages are protected.
- When n > 0, protection is applied on pages from 0 to (n-1) and page 31, where n=1÷31. For example:
  - If 1, protection is applied on page 0 and page 31 (that is, data @0x00010000÷@0x000107FF and data @0x0001F8000÷@0x0001FFFF).
  - If 2, protection is applied on pages from 0 to 1 and page 31.
- If 31 the entire main flash is protected (that is, code @0x00010000@0x0001FFFF).

Note: Performing the main flash area Mass Erase, the protection is removed, and write/erase page commands are executed.

Note: Please note that in case the device is in boot mode, the protections are disabled. To completely protect the device, please follow these steps:

- *Set the ACP_protection value to 31*
- *Once you program the device:*
  - *Remove the UART*
  - *Do not allow the boot entering*
    - *(Recovery mode bit set to disable)*

2.1.5 APPL_SETUP

This field defines if, and which, protocol is used to communicate with the SINK.

Available values are:

- 0x00 = No stacks enabled–fixed 5 V 1.5 A
- 0x04 = USB PD stack enabled
- 0x06 = Multiport application with USB PD stack enabled
- 0x0F = Fixed output, voltage from Vout default and Iout default – no stack enabled
- 0x1F = Fixed output CC, same as 0x0F with Constant Current enabled

2.1.6 PWD_SETUP

This field defines if the power module (firmware to control the power application) starts or not.

Available values are:

- 0x00 = Power module disable, never starts
- 0x01 = Power module starts immediately after power-on
- 0x02 = Power module starts only when requested by SVC command (function enabled only with debug firmware)

2.1.7 Vout default

This parameter sets the V_{out} voltage when APPL_SETUP is set to “Fixed” (0x0F) or “Fixed CC” (0x1F). This field is expressed as 1 mV / LSB; accepted values are from 5000 (as for 5 V) to 21000 (as for 21 V). In USB PD mode, must be set to 5000.

2.1.8 Iout default

This parameter sets the I_{out} current limit when APPL_SETUP is set to “Fixed” (0x0F) or “Fixed CC” (0x1F). This field is expressed as 1 mA / LSB; accepted values are from 1000 (1 A) to 5200 (as 5.2 A). In USB PD mode, must be set to 3000.

2.1.9 APP_MV_Add2_Init

This parameter is used to select the SRGD clamp functionality match with the external circuit. Bitfield definition is:

- Bit 0 – synchronous rectifier enable (=1) or disable (=0)
- Bit [1-2]
  - If 00 = Charge pump clamp voltage at 11 V
  - If 01 = Charge pump clamp voltage at 9 V
  - If 10 = Charge pump clamp voltage at 7 V
  - If 11 = Charge pump clamp voltage at 5 V
- Bit [3] – unused – reserved
- Bit [4-5] – select ZCD filter
  - If 00 = No filter enabled
  - If 01 = 50 ns
  - If 10 = 100 ns
  - If 11 = 150 ns
- Bit [6] – unused – reserved

- Bit [7] – Charge pump functionality enable (=1) or disable (=0)

2.2 Application code parameters

This area defines the power limit during a WTP or OTP event and related temperature limits.

2.2.1 ACP_PWWTP_1

This parameter defines the maximum output power (10 mW/step) when internal temperature is over WTP point as per ACP_WTP_INT (example: 0x1388 → 50 W).

2.2.2 ACP_CLWTP_1

This parameter defines the maximum output current (1 mA/step) when internal temperature is over WTP point as per ACP_WTP_INT (example: 0x6A4 → 1700 mA).

2.2.3 ACP_WTP_INT

This parameter defines the internal warning temperature trigger point, the higher this value (degree), the output is limited to ACP_PWWTP_1 power and ACP_CLWTP_1 current (0x46 → 70 °C). Put this value less than ACP_OTP_INT.

2.2.4 ACP_OTP_INT

This parameter defines the internal overtemperature trigger point, the higher this value (degree), the output power is switched off if remaining for one minute over (0x64 → 100 °C).

2.3 USB PD PDOs and APDOs

This area defines the USB PD parameters as the PDO and APDO data; the maximum power provided by ST-ONE applications and other values related to this communication protocol.

2.3.1 5V-PDO

This field defines the first PDO used on the USB PD protocol. The suggested default PDO is 5 V@3 A and is equal to the 0x0801912C hex value. NOTE: This field is mandatory as 5 V.

2.3.2 UCPDOx (1 to 6)

This field defines the PDO or APDO used on the USB PD protocol. This structure is a one-to-one map of the structures described in USB PD 3.1 protocol specifications. For more details, see the official USB PD specifications.

This field can be used for either PDO or APDO.

In the case of PDO, the available values are:

- Dual-role power: set to disabled, enable not supported
- USB suspend supported: set to disable, enable not supported
- Unconstrained power: set to disable, enable not supported
- USB communication capable: set to disable, enable not supported
- Dual role data: set to disable, enable not supported
- Unchuncked extended messages supported: set to disable, enable not supported
- Peak current: 100%, other values not supported
- Max. voltage: target voltage to regulate at this PDO, minimum value 5 V, maximum value 21 V
- Max. current: maximum current allowed for this PDO, minimum value 1 A, maximum value 5 A

In the case of APDO, the available values are:

- PPS power limit: set to disable, enable not supported
- Max. voltage: maximum voltage allowed by this APDO, minimum value 5 V, maximum value 21 V
- Min. voltage: minimum voltage allowed by this APDO, minimum value 3.3 V, maximum value 20 V
- Max. current: threshold current for entering in constant current mode, minimum value 1 A, maximum value 5 A

2.3.3 PPS_HIGH

This field is the Programmable Power Supply - high limit or PDP used for some USB PD messages (100 mW/step).

2.3.4 VOLT_REG

This field is the Voltage Regulation field on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.5 HOLDUP_TIME

This field is the Holdup Time field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.6 COMPLIANCE

This field is the Compliance parameter field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.7 TOUCH_CURRENT

This field is the Touch Current field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.8 PEAK_CURR1

This field is the Peak Current 1 field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.9 PEAK_CURR2

This field is the Peak Current 2 field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.10 PEAK_CURR3

This field is the Peak Current 3 field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.11 TOUCH_TEMPERATURE

This field is the Touch Temperature field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.12 SOURCE_INPUTS

This field is the Source Input field used on Source Capabilities Extended Message. Please refer to USB PD 3.1 standard for a more in-depth explanation.

2.3.13 USBPD_XID

This field is the XID value provided by the USB-IF assigned to the product. Refer to the USB PD 3.1 standard for a more in-depth explanation.

2.3.14 USB_A_FILTER_LENGTH_CONN

Deglitch filter length when USB-A is connected (input logic signal on GPIO1).

$$CF[ms] = 1$$

2.3.15 USB_A_FILTER_LENGTH_DISCONN

Deglitch filter length when USB-A is disconnected (input logic signal on GPIO1).

$$CF[ms] = 1$$

2.3.16 POWERGOOD_ENABLE

If this parameter is different from 0, ST-ONEMP sets GPIO0 from 0 to 1 as soon as the voltage regulation on Vout is stable (typically 100ms).

2.3.17 UCPDO1 without type-C enabled

If 0, VSRC is set to vSafe5V when no type-C cable is attached, otherwise the VSRC is set to the UPCD01 value (UCPDO1 to be 9 V).

2.3.18 HARD_RESET_IN_OCP

ST-ONEMP sends a Hard Reset if OCP is triggered when this parameter is different from 0.

2.3.19 EXT_PORT_CONN_LOGIC_LEVEL

External port detection logic level (0 or 1) on GPIO1. If this parameter is set to 0, a logic 0 on GPIO1 is detected as an external port connection request for power sharing, otherwise ST-ONEMP requires a logic level 1 for request.

2.3.20 5V-PDO_LIMITED and UCPDOx_LIMITED (1 to 6)

These fields define the PDOs or APDOs used in power sharing mode. Refer to the same fields in the ST-ONE section for configuration (see Section 2.3.1 and Section 2.3.2). ST-ONEMP switches to this set of PDOs and APDOs if there is an external power sharing request.

2.4 Power parameters legend

Note: These parameters must be taken from the datasheet as table values in this section could be outdated. They are taken only the typical value for simplicity (for more details see the ST-ONEMP datasheet). For more details on how to practically tune power parameters, follow 'How to design an application guide'.

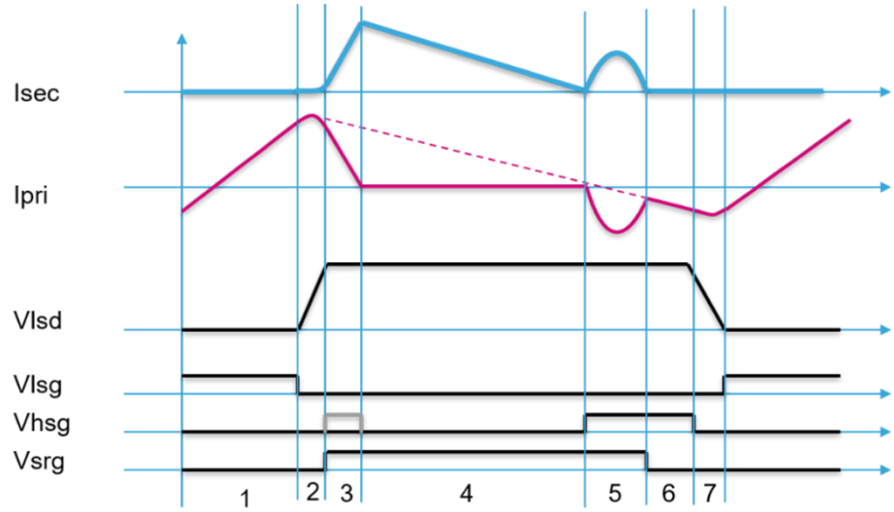
Table 1. Constant details

Name	Value	Meaning
G_{TV}	0.66 V/µs	Time to voltage conversion ratio, used for ipk computing
F_{clk}	133 MHz	High clock system frequency
$f_{clkslow}$	66 kHz	Low clock system frequency
$V_{IPEAKCLAMP}$	0.525 V	

Table 2. Variable details

Name	Meaning
R_{pri}	Current sense resistor at primary side
R_{sec}	Current sense resistor at secondary side
T_{OFF}	Secondary side conduction phase (see Figure 1, phase 4)
T_{ON}	Primary side conduction phase (see Figure 1, phase 1)
V_{ThOVP}	OVP overvoltage protection threshold, compared to V_{out}
V_{ThUVP}	UVP undervoltage protection threshold, compared to V_{out}
V_{drv}	SR driving voltage
V_{out}	Actual output voltage
V_{tgt}	Target voltage regulating, value after compensation, in typical cases equal to V_{tgtset}
T_{HS1}	Clamp conduction phase (see Figure 1, phase 3)
T_{HS2}	Clamp bump phase (see Figure 1, phase 5+6)
I_{Pk}	Peak current on primary side
V_{tgtset}	Target voltage, set by user or protocol, for example 5 V 9 V

Figure 1. Typical switching waveforms



2.5 Power parameters

The following parameters are used to set up and tune the power conversion control, including loop compensation, switching cycle timings, light load modes thresholds, etc.

The conversion factor, CF, is given for each parameter. The conversion is already performed by the GUI. CF is useful for understanding the resolution that can be achieved for each parameter.

However, it is possible to compute the raw value of a parameter by computing:

$$Parameter[RAW] = Parameter[measure\ unit] \cdot CF$$

Where not specified, CF is equal to 1. For many parameters the CF is set as 7.52 ns to comply with the SMED's clock regime. In these cases, it is not possible to increase timing resolution more than this factor.

2.5.1 Rsns_Iout

This parameter sets the conversion factor between the secondary output current and the internal IC representation. This value should be chosen according to the secondary side sense resistor. Pay attention that also parasitic resistance given by PCB traces and component solder pads needs to be considered.

$$CF[m\Omega] = 0.047$$

2.5.2 Vout_th_ChgPmp

This parameter sets the turn-off threshold of the charge pump that generates V_{drv} in case V_{out} is too low to directly power on the SRGD MOSFET.

If V_{out} is greater than $V_{out\_th\_ChgPmp}$ – 0.3, the charge pump is disabled. In this case:

$$V_{drv} = V_{out} - 2 \cdot V_{fdiode}$$

If V_{out} is less than $V_{out\_th\_ChgPmp}$ + 0.3, the charge pump is enabled. In this case:

$$V_{drv} = 2 \cdot (V_{out} - V_{fdiode})$$

Where V_{fdiode} is the forward voltage of the two diodes connected to the PUMP pin. Set a value of 2.5 V to fully disable the charge pump. The default value is 8.19 V suitable for most MOSFETs. For logic level MOSFETs, this value can be decreased, for example to 5 V.

$$CF[V] = 0.000375$$

2.5.3 Ton_SR_ext

This parameter sets the maximum SR ON-time duration after the IZCD comparator is triggered (see Figure 1, phase 5). This parameter has to be set to a half resonance period of the leakage inductance with the clamp capacitor.

$$CF[ns] = 7.52$$

2.5.4 Ton_HS2_max

This parameter sets the maximum HS ON-time duration for the second HON pulse (see Figure 1, phase 5). It is particularly useful to limit its duration at very low output and high input voltage, as this condition would lead to very long HS ON pulses, increasing the primary side conduction losses while having only limited gain in terms of switching losses.

A rule of thumb is to decide this parameter value for obtaining soft switching up to 9 V output at 230 V_{AC} input.

$$CF[ns] = 7.52$$

2.5.5 Ton_HS2_min

This parameter sets the minimum HS ON-time duration for the second HON pulse (see Figure 1, phase 5).

$$CF[ns] = 7.52$$

2.5.6 Ton_HS2_gain

This is the main parameter that is used for adjusting the HS ON-time duration to obtain soft switching in almost all conditions.

The second HON duration is determined by the controller as:

$$T_{HS2} = \text{Ton\_HS2\_gain} \cdot \frac{T_{OFF}[s]}{T_{ON}[s]}$$

Ton is the LS ON-time including LS-HS deadtime (see Figure 1, phases 1 and 2), while Toff is the LS OFF-time (see Figure 1, phases 3 to 6). The HS-LS deadtime is excluded from the operation since its impact is negligible.

Attention: *This value is saturated between $T_{on\_HS2\_min}$ and $T_{on\_HS2\_max}$.*

$$CF[ns] = 7.52$$

2.5.7 Ton_HS1_adjust

This parameter sets the first HON duration (see Figure 1, phase 3).

The first HON duration is defined as:

$$T_{HS1}\left[s\right] = \text{Ton\_HS1\_adjust} + \frac{1}{2}\begin{cases} T_{HS2}[s], & T_{HS2}[s] < SRG\_satplus \\ SRG\_satplus, & T_{HS2}[s] \geq SRG\_satplus \end{cases}$$

That is, the first HS ON-time is determined as half of the duration of the SR pulse after the IZCD is triggered plus or minus, a value determined by this parameter.

This parameter can be adjusted by observing the current in the HS FET or the voltage on the transformer primary side. A too long HS ON pulse can cause a reversal of the primary side current during phase 3, leading to a spike in the transformer voltage when the HS FET turns OFF.

$$CF[ns] = 7.52$$

2.5.8 Tdly_HS2-on_LS-off

This parameter sets the deadtime between HS ON and LS ON signals (see Figure 1, phase 7).

This time has to be set long enough to obtain soft switching, while avoiding the LS body diode conducting for too long.

$$CF[ns] = 7.52$$

2.5.9 Tvalley_V-SKIP

This parameter is set as the oscillation period of the LS drain voltage during valley skipping mode.

$$CF[ns] = 7.52$$

2.5.10 Tdly_HS2-on_V-SKIP

This parameter sets the time delay from when the ZVS comparator is triggered to the first valley in valley skipping mode.

$$CF[ns] = 7.52$$

2.5.11 Tadv_I2-ZCD

This parameter sets an offset on the ZCD0 threshold (that is, between phases 4 and 5, see Figure 1) to anticipate its detection.

This parameter must be set to 0 if the application has no ZCD advance circuitry.

$$CF[ns] = 7.52$$

2.5.12 Tsw_off_max

This parameter sets the maximum duration of secondary side conduction (see Figure 1, phases 3 to 5).

$$CF[ns] = 7.52$$

2.5.13 Vout_slope_ctrl

This parameter sets the rising time for soft-start and for voltage transitions. The falling time is set 4 times slower than this value.

Note: This parameter sets only the target slope. At some low load conditions, this value could not be respected.

$$CF[V/ms] = 0.00555$$

2.5.14 T_Autorestart_OCP

This parameter sets the timeout for re-attaching the load switch after a secondary side Overcurrent Protection event.

$$CF[ms] = 1$$

2.5.15 T_Autorestart_BO

This parameter sets the timeout for re-attaching the load switch after a Brown-out event.

$$CF[ms] = 1$$

2.5.16 Ipeak_max

This parameter sets the maximum value for the Ipeak computed by the Internal PI control loop, limiting the current peak at the primary side during the LON phase.

The maximum peak current allowed in the application can be computed as:

$$I_{PkMax}\left[A\right] = \frac{1}{R_{sense\_pri}[Ohm]}\frac{G_{TV}[V/\mu s]}{2048 \cdot F_{CK}[Hz]}\text{IpeakMax[RAW]} \approx \frac{2.42[\mu V]}{R_{sense\_pri}[Ohm]}\text{IpeakMax[RAW]}$$

$$CF[\%\ of\ maximum\ Ipk] = 0.0004648$$

2.5.17 PID_P_CV

This parameter sets the proportional gain factor for constant voltage regulation loop.

2.5.18 PID_I_CV

This parameter sets the integral gain factor for constant voltage regulation loop.

2.5.19 PID_I_CC

This parameter sets the integral gain factor for constant current regulation loop.

2.5.20 Jitter_m_index

This parameter manages jitter outside burst for spread spectrum functionality. The value is expressed as % of maximum Ipeak range.

$$CF[\%\ of\ Ipk] = 1.56,\ doubled\ at\ each\ step$$

2.5.21 Iout_OCP_th

This parameter sets the threshold for triggering secondary side Overcurrent Protection, expressed in mA.

$$CF[mA] = 0.001$$

2.5.22 Vout_OV/UV_th

This parameter sets the proportional factor for computing the OVP and UVP threshold according to the formula:

$$V_{ThOVP}[V] = V_{tgt}[V] + Vout\_OV/UV\_th \cdot V_{tgt}[V] + Vout\_OV/UV\_msk[V]$$
$$V_{ThUVP}[V] = V_{tgt}[V] - Vout\_OV/UV\_th \cdot V_{tgt}[V] - \text{Vout\_OV/UV\_msk}[V]$$

Where V_{tgt} is the target voltage set by the user or protocol.

$$CF[\%\ of\ Vout] = 0.386$$

2.5.23 Vout_OV/UV_msk

This parameter sets the absolute value for computing the OVP and UVP threshold according to the formula:

$$V_{ThOVP}[V] = V_{tgt}[V] + Vout\_OV/UV\_th \cdot V_{tgt}[V] + Vout\_OV/UV\_msk[V]$$
$$V_{ThUVP}[V] = V_{tgt}[V] - Vout\_OV/UV\_th \cdot V_{tgt}[V] - \text{Vout\_OV/UV\_msk}[V]$$

Where V_{tgt} is the target voltage set by the user or by protocol.

$$CF[mV] = 2.92$$

2.5.24 Ipeak_clmp_V-SKIP

This parameter sets the minimum primary side peak current for valley skipping mode. When the peak current reaches this value, the valley skipping control loop starts regulating the switching frequency instead of the peak current.

The value is expressed as % of maximum Ipeak range.

Note: The internal value derived by this parameter is updated dynamically depending on operating conditions.

$$CF[\%\ of\ Ipk] = 0.952$$

2.5.25 Tsw_ph21_V-SKIP_hyst_in

This parameter sets the positive hysteresis for changing skipping mode.

The value is expressed as % of maximum Ipeak range.

Note: The internal value derived by this parameter is updated dynamically depending on operating conditions.

$$CF[\%\ of\ Ipk] = 0.952$$

2.5.26 Trep_min_BRST

This parameter sets the time threshold for exiting burst mode. If the time between two bursts is less than this threshold, the system exits burst.

Note: There is a filter on the detection so its effect is not immediate.

$$CF[ms] = 0.01515$$

2.5.27 Trep_min_BRST_PPS

This parameter has the same effect as Trep_min_BRST but it is valid only when the USB PD mode is enabled and an APDO is requested.

$$CF[ms] = 0.01515$$

2.5.28 Trep_max_BRST

This parameter sets the time threshold for entering and exiting deep burst. If the time between two burst slots is more than this threshold, the system enters deep burst mode, otherwise the system exits deep burst, entering in normal burst mode.

Note: There is a filter on this time so its effect is not immediate.

$$CF[ms] = 0.01515$$

2.5.29 Ipeak_th_BRST

This parameter sets the minimum primary side peak current for entering burst mode. When the peak current reaches this value, the controller enters burst mode.

The value is expressed as % of maximum Ipeak range.

Note: The internal value derived by this parameter is updated dynamically depending on operating conditions.

$$CF[\%\ of\ Ipk] = 0.0004648$$

2.5.30 Ipeak_th_BRST_PPS

This parameter has the same effect as Ipeak_th_BRST but valid when the USB PD mode is enabled and an APDO is requested, or in FixpowerCC mode.

The value is expressed as % of maximum Ipeak range.

$$CF[\%\ of\ Ipk] = 0.0004648$$

2.5.31 PID_I_pre_BRST

When exiting burst, the value of the control loop integrator, and by consequence I_{pk}, is initialized according to the formula:

$$\mathrm{I_{pk}} = PID\_I\_pre\_BRST * V_{out} * I_{out}$$

2.5.32 Burst_settings

2.5.32.1 *Hysteresis*

This parameter sets the hysteresis setpoint of the comparator used by burst mode. It is valid only at 5 V, 9 V, 12 V, 15 V, and 20 V (hardware thresholds).

2.5.32.2 *Threshold*

This parameter sets the threshold for starting a new burst slot.

$$CF[\%\ of\ V_{out}] = 1$$

2.5.33 Ipeak_clmp_BRST

This parameter sets the primary side peak current used during burst mode.

The value is expressed as % of maximum Ipeak range.

$$CF[\%\ of\ Ipk] = 0.952$$

2.5.34 N-Tsw_gain_BRST

This parameter sets the gain factor used to calculate the number of pulses to be generated during each burst, depending on the output voltage.

The number of pulses is equal to:

$$n_{pulses} = \max\left[\text{N\_Tsw\_min\_BRST} + \left(\text{N\_Tsw\_gain\_BRST} \cdot \frac{V_{Tgt}[V] - 2.9V}{12V}\right), N\_Tsw\_max\_BRST\right]$$

$$CF[pulses/V] = 0.0833$$

2.5.35 N-Tsw_min_BRST

This parameter sets the minimum number of pulses for each burst slot.

2.5.36 N-Tsw_max_BRST

This parameter sets the maximum number of pulses for each burst slot.

2.5.37 Tdly_HS-off_LS-on_D-BRST

This parameter sets an additional deadtime used in deep burst mode.

$$CF[ns] = 7.52$$

2.5.38 Max current burst

This parameter sets a current threshold at secondary side for forcing burst entering. Set to 0 if not used.

$$CF[\%\ of\ Isec] = 0.0122$$

2.5.39 Toff_BLEEDER

This parameter sets the OFF-time for active bleeding mode.

$$CF[ns] = 7.52$$

2.5.40 Ton_BLEEDER_gain

This parameter sets the gain for computing active bleeding ON-time, according to the formula:

$$T_{ONBLEED}[ns] = \text{Ton\_BLEEDER\_Gain} \cdot \frac{Vcc}{20V}$$

$$CF[ns] = 7.52$$

2.5.41 Tmsk_I2-ZCD

This parameter sets the mask time from LS turn-ON to ZCD12 detection for the first HS & SR turn-ON. It is useful to mask ringing and avoid a spurious comparator trigger.

$$CF[ns] = 7.52$$

2.5.42 Tmsk_V2-ZCD

This parameter sets the mask time from HS turn-OFF to ZCD0 detection for the second HS turn-ON. It is useful to mask ringing and avoid a spurious comparator trigger.

$$CF[ns] = 7.52$$

2.5.43 V_CDC_max

This parameter sets the maximum voltage allowed for Cable Drop Compensation. It fixes the maximum V_{tgt} (see R_Cable) above which the Cable Drop Compensation is disabled. Cable Drop Compensation is disabled in PPS mode.

$$CF[V] = 1$$

2.5.44 R_Cable

This parameter sets the resistance of the cable, expressed in mΩ. This value is used for computing the Cable Drop Compensation. It increases the V_{tgt} according to the formula:

$$V_{tgt} = V_{tgtset} + I\_out \cdot \mathrm{R\_Cable}$$

In USB PD applications, it is suggested to leave this parameter to 0 unless the cable is embedded in the application.

$$CF[m\Omega] = 5.72204$$

2.5.45 Cable_detection_thr_to_vSafe5V

Cable detection time limit in milliseconds, to switch to vSafe5V while debouncing cable insertion.

2.5.46 EN_foldback

This parameter enables the constant current regulation (also for PDOs) writing a value different from 0.

2.5.47 Foldback_thr_PDO

It sets the threshold that the output voltage can reach before protection is triggered, calculated as a percentage of the nominal PDO voltage.

2.5.48 W_LUVP_thr

Threshold for LUVP warning. If the Vout remains more than 330 µs under this threshold, the LUVP protection is triggered.

$$CF[V] = 1$$

2.5.49 LUVP_thr

Hard threshold for LUVP. If Vout is under this threshold, the LUVP protection is triggered.

$$CF[V] = 1$$

2.5.50 Ilim_excess

This parameter sets how much current is allowed in PDO mode before triggering OCP.

$$CF[\%\ \text{of PDO nominal current}] = 0.390625$$

2.5.51 Truncate_Hon

During skipping, if this parameter is different from 0, the second HON pulse can be truncated according to control loop requests, otherwise it employs the Ton_SR_ext value for the second HON. This behavior can help avoid truncation ringing to achieve a better EMI spectrum.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
16-Jul-2024	1	Initial release.

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