Getting started with STEVAL-A6983IV1 evaluation board based on A6983I, 38 V, 10 W synchronous iso-buck converter for isolated applications

Introduction

The STEVAL-A6983IV1 is an evaluation board based on ST A6983I, 38 V, 10 W synchronous iso-buck converter designed for isolated applications.

The primary output voltage can be accurately adjusted, whereas the isolated secondary output is derived by using a given transformer ratio. No optocoupler is required. The primary sink capability up to -4.5 A (even during soft-start) allows a proper energy transfer to the secondary side as well as enables a tracked soft-start of the secondary output. The control loop is based on a peak current mode architecture and the device operates in forced PWM. The 390 ns blanking time filters oscillations, generated by the transformer leakage inductance, making the solution more robust.

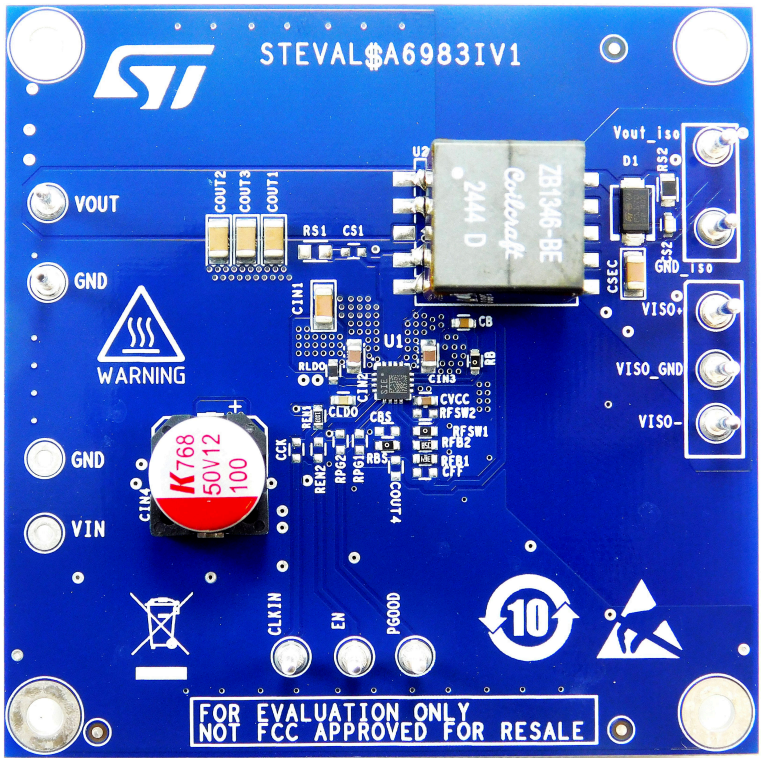
The compact QFN-16 3x3 mm package and the internal compensation of the A6983I help minimizing design complexity and size.

The switching frequency can be programmed in the 200 kHz - 1 MHz range with optional spread spectrum for improved EMC.

The EN pin provides enable/disable functionality. The typical shutdown current is 2 uA when disabled. As soon as the EN pin is pulled-up the device is enabled and the internal 1.3 ms soft start takes place. The A6983I features a power-good open collector that monitors the FB voltage. Pulse by pulse current sensing on both power elements implements an effective constant current protection and thermal shutdown prevents thermal run-away. Due to the primary reverse current limit, the secondary output is protected against short-circuit events.

The evaluation board generates an isolated unregulated voltage and provides the possibility to use a postregulation to generate a dual voltage (layout available on the bottom of the PCB, components not mounted).

Figure 1. STEVAL-A6983I



Notice: *For dedicated assistance, submit a request through our online support portal at **www.st.com/support**.*

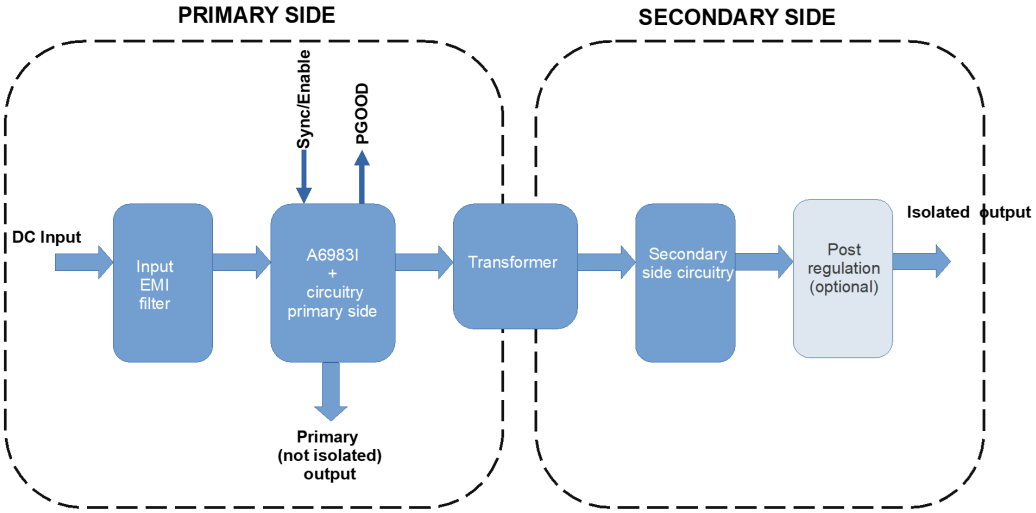
1 Getting started

1.1 Safety instructions

This board is intended for use by skilled technical personnel who are suitably qualified and familiar with the installation, use, and maintenance of power electronic systems. The same personnel must be aware of and must apply national accident prevention rules. The electrical installation shall be completed in accordance with the appropriate requirements (for example: cross-sectional areas of conductors, fusings, and GND connections).

1.2 Functional block diagram

Figure 2. STEVAL-A6983I block diagram



1.3 Features

- Designed for iso-buck topology
- 4 V to 38 V operating input voltage
- Primary output voltage regulation
- No optocoupler required
- 4.5 A source/sink peak primary current capability
- Peak current mode architecture in forced PWM operation
- 300 ns blanking time
- 25 µA operating quiescent current
- 200 kHz to 1 MHz programmable switching frequency. Stable with low ESR capacitor: min 2µF
- Internal compensation network
- 2µA shutdown current
- Internal soft start
- Enable
- Overvoltage protection
- Thermal protection
- Optional spread spectrum for improved EMC
- Power-good
- Synchronization to external clock
- QFN16 3x3mm package

2 How to use the board

The STEVAL-A6983IV1 is configured to deliver 5 V at the primary not isolated output and an unregulated voltage at the isolated output that varies with the applied load (see Section 7: STEVAL-A6983IV1 performance and waveforms). The switching frequency is set to 400 kHz.

To start any measurement with this board, the below mentioned steps should be followed.

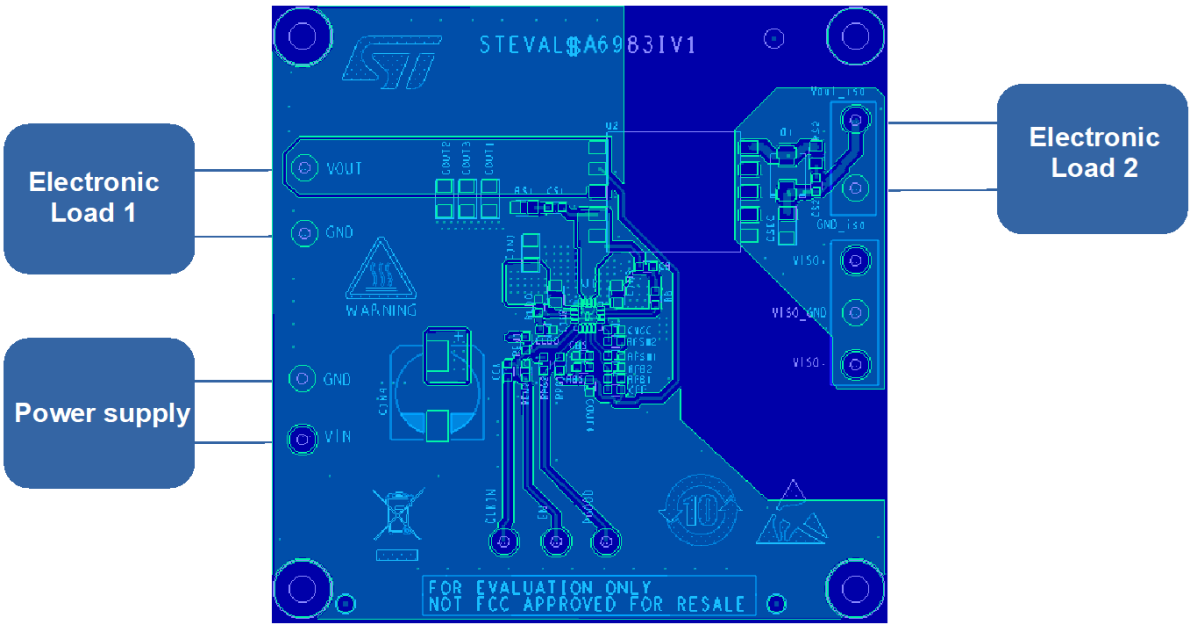
Step 1. Connect the power supply to the test points of VIN and GND.

Step 2. Connect the load to the primary not isolated output (if any) as well as to the secondary isolated output.

Step 3. Set the supply voltage VIN from 8 V to 38 V and switch the power supply on.

Step 4. Regulate both the active loads.

Figure 3. STEVAL-A6983IV1 basic testing setup



3 Connectors and test points

3.1 VIN - TPxx

This connector is for input supply voltage. This voltage is provided, through the input EMI filter, to the pin VIN of the device. A power supply ranging from 4 V to 38 V should be connected to this test point, setting a proper current limit.

The wire connection should be as short as possible to avoid or limits possible oscillations due to the parasitic inductance of the wire and the input capacitor.

3.2 GND1 and GND_{prim} - TPxx and TPxxx

GND1 and GND_{prim} are respectively the return path of the input and output capacitors. Wires used for this connection should be as short as possible.

3.3 V_{OUT1} - TPxx

This is the connector for the primary not isolated output voltage. If the primary output should be loaded, a resistor or an active load should be connected to this test point. Short wires are recommended.

3.4 EN/SYNCH - TPxx

The EN pin is by default pulled-up to the input voltage through the resistor R_{en1}, resulting in device always enabled. The same test-point can be used to apply an external signal for synchronization.

3.5 PGOOD - TPxx

This test point is directly connected to the PGOOD pin.

3.6 $VOUT_{iso}$ - TPxx

This test point provides the isolated output voltage (unregulated). Consider that the voltage at this pin, when completely unloaded, could be much higher than the theoretical value (N*VOUT1). Short wire connection from this test point to the load is recommended.

3.7 GND_{iso} - TPxx

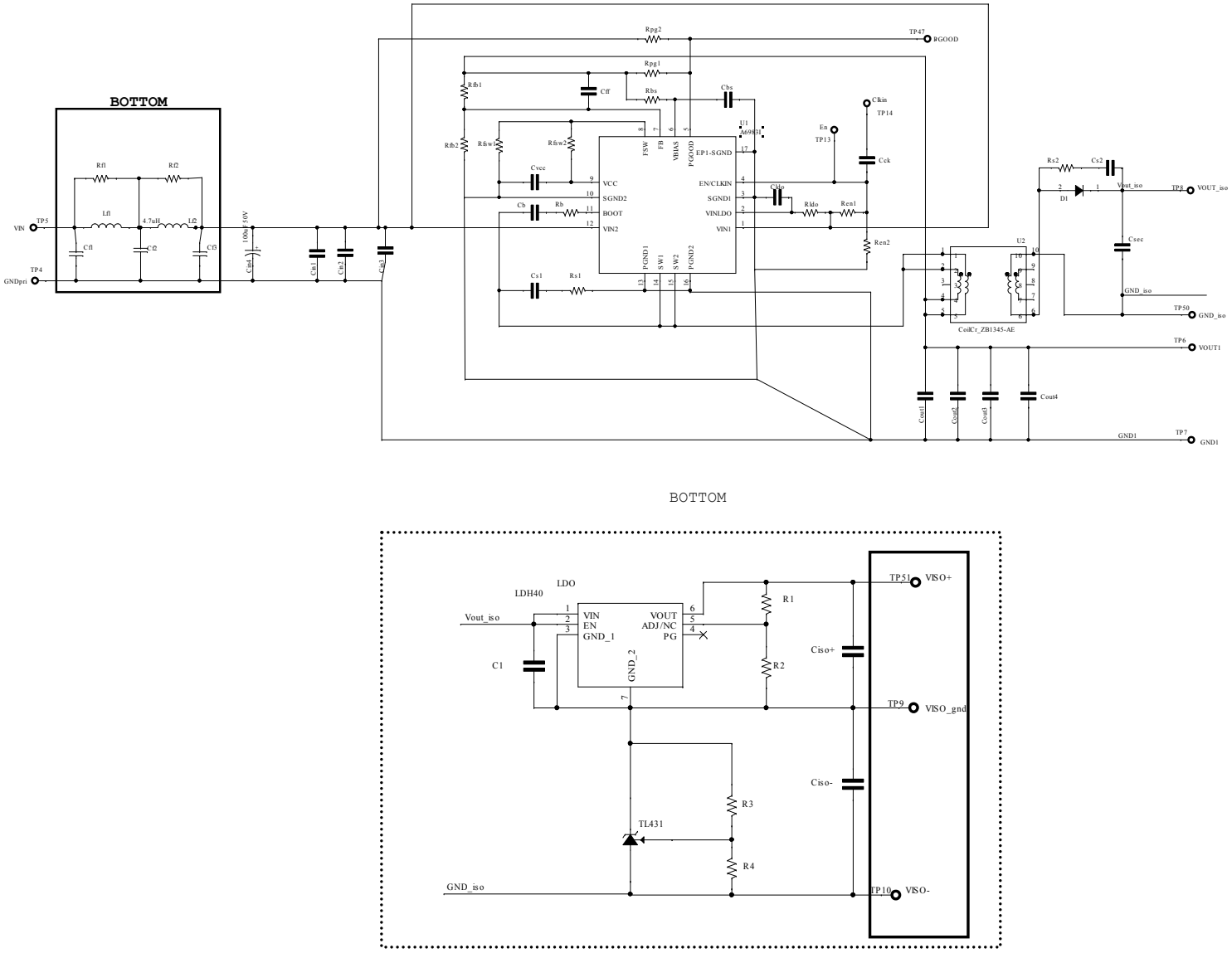
The voltage at this test point represents the reference for the isolated voltage. Short connection is recommended.

3.8 VISO+, VISO- and VISO_gnd – TPxx

The isolated output voltage can be post-regulated and used to generate a dual voltage. On the bottom side of the PCB, the layout for post-regulation is available (components to be assembled). If the components of the post regulation circuitry are assembled, the test points VISO+, VISO- and VISO_gnd provide a positive (VISO+) and negative voltage (VISO-), both referred to VISO_gnd.

4 Schematic diagrams

Figure 4. **STEVAL-A6983IV1 circuit schematic**



5 Bill of materials

Table 1. **STEVAL-A6983IV1 bill of materials**

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
1	1	U1, QFPN 3X3X0.80 16L PITCH 0.50		Isobuck converter A6983I	ST	A6983IQTR
2	1	U2		Transformer	Coilcraft	ZB1346-BE
3	1	LDO, DFN 6L 2X2X 0.75 PITCH0.65 AG		Linear regulator	ST	LDH40PURY
4	1	TL431, SOT23		Shunt voltage reference	ST	TL431BL3T
5	1	R1		SMD resistor		
6	1	R2		SMD resistor		
7	1	R3		SMD resistor		
7	1	R4		SMD resistor		
8	1	Rs1		SMD resistor		
9	1	Rb	0Ω	SMD resistor	YAGEO	RC0603FR-070RL
10	1	Rs2	300Ω	SMD resistor	Vishay	CRCW0805300RFKEAHP
11	1	Rf1		SMD resistor		
12	1	Rf2		SMD resistor		
13	1	Ren1	100kΩ	SMD resistor	YAGEO	AC0603FR-07100KL
14	1	Ren2		SMD resistor		
16	1	Rfb1	360kΩ	SMD resistor	YAGEO	RC0603FR-0775KL
15	1	Rfb2	75kΩ	SMD resistor		RC0603FR-07360KL
17	1	Rfsw1	0Ω	SMD resistor	YAGEO	RC0603FR-070RL
18	1	Rfsw2		SMD resistor		
19	1	Rpg2		SMD resistor		
20	1	Rpg1		SMD resistor		
21	1	Rbs	0Ω	SMD resistor	YAGEO	RC0603FR-070RL
22	1	Rldo	100Ω	SMD resistor	YAGEO	RC0603FR-10100RL
23	1	C1		MLCC		
24	1	Cldo	1uF	MLCC	Samsung Electro Mechanics	CL10A105KB8NNNC
25	1	Cff		MLCC		
26	1	Cb	100nF	MLCC	TDK	CGA3E2X7R1H104K080AA
27	1	Cs1		MLCC		
28	1	Cin1	10uF	MLCC	Samsung Electro Mechanics	CL31B106KBHNNNE
29	2	Cin2, Cin3	1uF	MLCC	TDK	CGA4J3X7R1H105M125AB

Item	Q.ty	Ref.	Part/value	Description	Manufacturer	Order code
30	1	Cin4	100uF	Aluminium Organic Polymer Capacitor	KEMET	A768MS107M1HLAV024
31	3	Cout1, Cout2, Cout3	22uF	MLCC	Taiyo Yuden	EMK316BB7226ML-T
32	1	Ciso+		MLCC		
33	1	Ciso-		MLCC		
34	1	Cs2	180pF	MLCC	Vishay	VJ0603A181FXAPW1BC
35	4	Csec, Cf1, Cf2, Cf3	10uF	MLCC	Samsung Electro Mechanics	CL31B106KBHNNNE
39	1	Cck		MLCC		
40	1	Cvcc	1uF	MLCC	TDK	CGA3E1X7R1C105K080AC
41	1	Cbs		MLCC		
42	1	Cout4		MLCC		
43	1	Lf1	220Ω	Ferrite bead	TDK	MPZ2012S221ATD25
44	1	Lf2	6.8uH	Inductor	Coilcraft	XGL4030-682MEC
45	1	D1, SMA Flat		Power Schottky diode	ST	STPS1170AF
48	12	TP1…TP12		Turret Solder	ETTINGER	13.14.239

Table 2. Main parameters of the transformer ZB1346-BE

Description	Value
Turn ratio	1:6
Magnetizing inductance	13.5 µH
Leakage inductance	140 nH
Primary winding resistance	60 mΩ
Secondary winding resistance	1.35 Ω

6 STEVAL-A6983IV1 layout

The STEVAL-A6983IV1 is a 2-layer PCB with 1 oz copper thickness.

Figure 5. PCB layout (top)

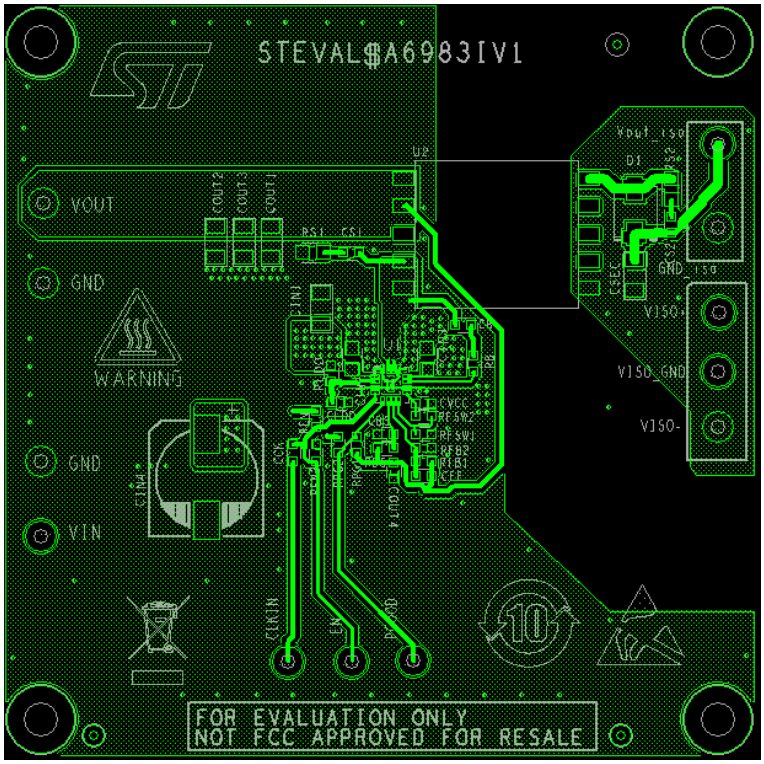
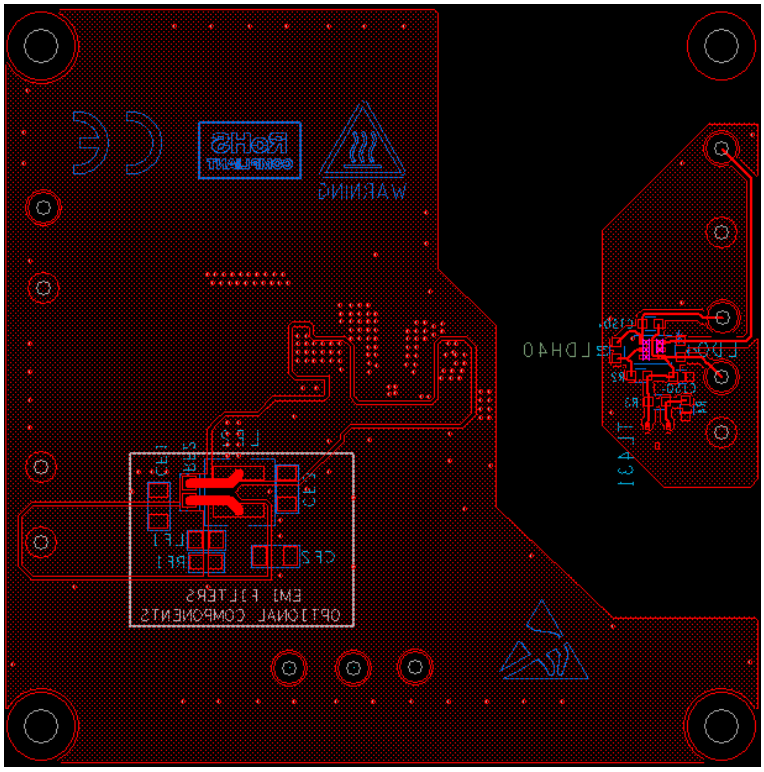


Figure 6. PCB layout (bottom)



7 STEVAL-A6983IV1 performance and waveforms

Efficiency

Figure 7. Efficiency at different VIN, f_{SW} = 400 kHz

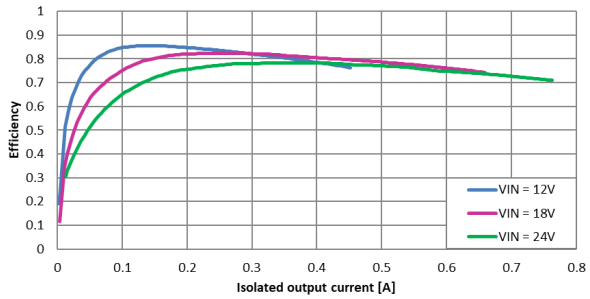


Figure 8. Efficiency vs f_{SW}, V_{IN} = 12 V

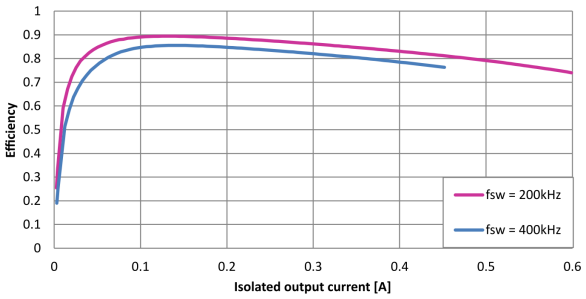


Figure 9. Efficiency vs f_{SW}, V_{IN} = 18 V

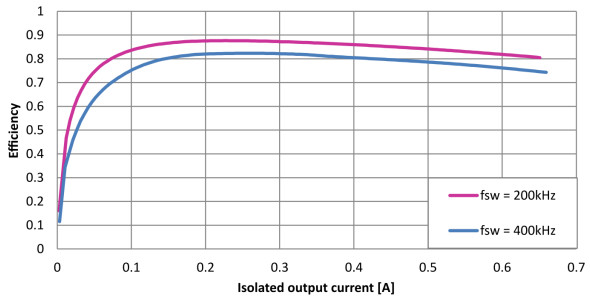
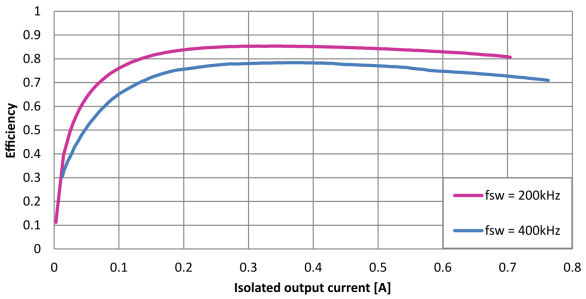


Figure 10. Efficiency vs f_{SW}, V_{IN} = 24 V



Load regulation

Figure 11. Load regulation at different V_{IN}, f_{SW} = 400 kHz

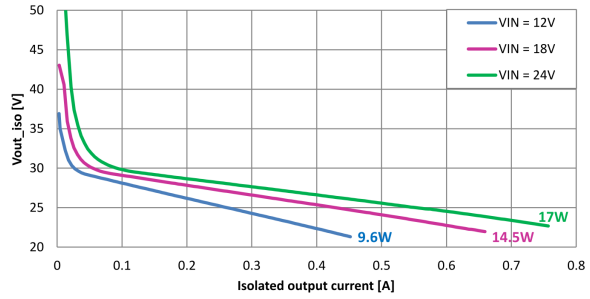


Figure 12. Load regulation vs f_{SW}, V_{IN} = 12 V

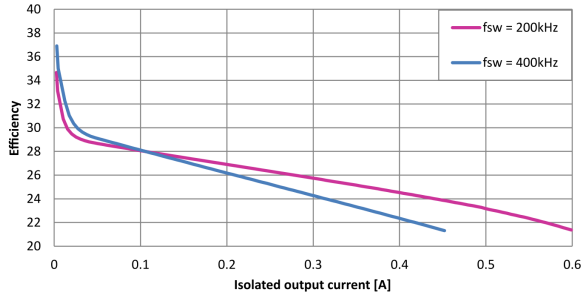


Figure 13. Load regulation vs f_{SW}, V_{IN} = 18 V

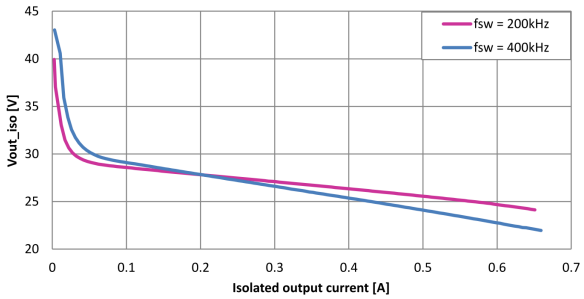
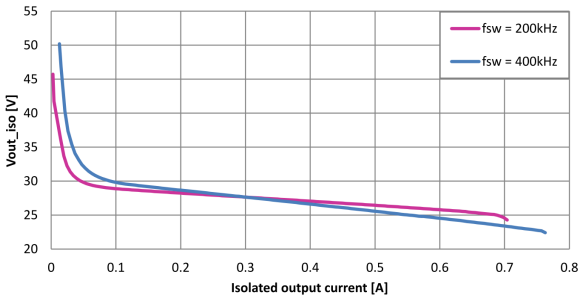


Figure 14. Load regulation vs f_{SW}, V_{IN} = 24 V



Winding currents

Figure 15. V_{IN} = 12 V, f_{SW} = 400 kHz, I_{OUTiso} = 450 mA

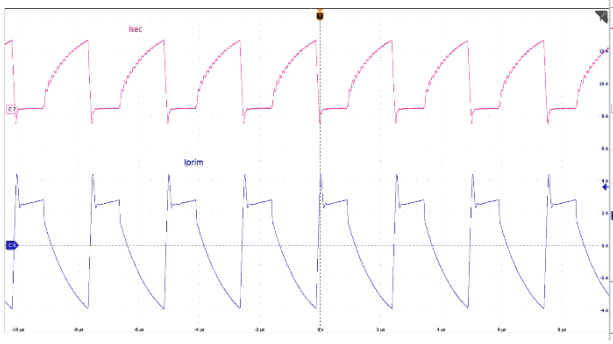


Figure 16. V_{IN} = 12 V, f_{SW} = 200 kHz, I_{OUTiso} = 600 mA

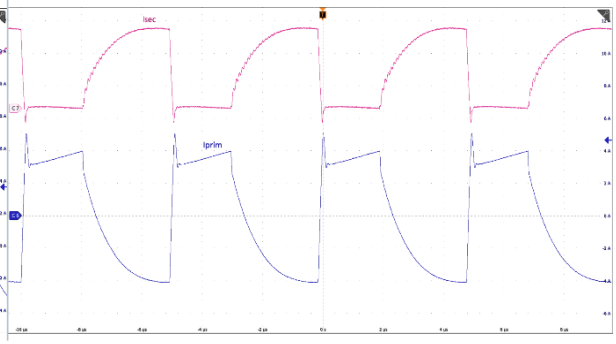


Figure 17. V_{IN} = 24 V, f_{SW} = 400 kHz, I_{OUTiso} = 750 mA

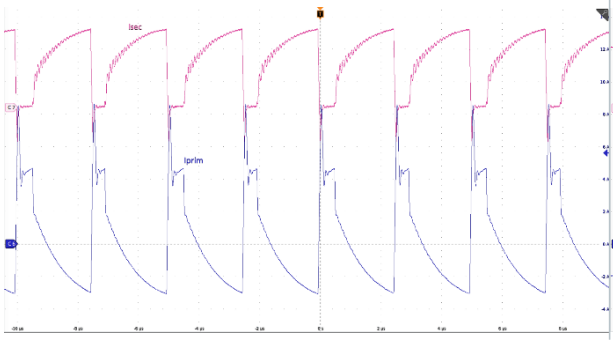
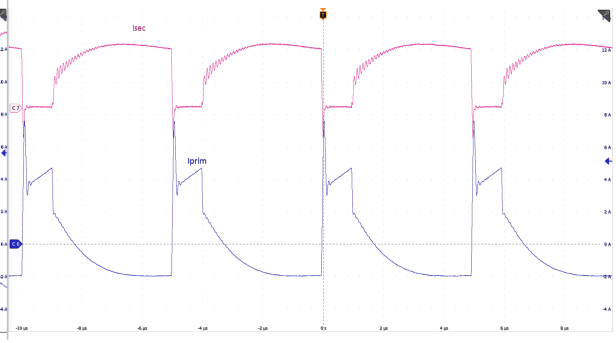


Figure 18. V_{IN} = 24 V, f_{SW} = 200 kHz, I_{OUTiso} = 700 mA



8 Input EMI filter

The STEVAL-A6983IV1 is compliant with CISPR16-4-2 due to the embedded EMI filter (bottom side).
The EMI filter consists of:

- A double pi filter with an inductor (Lf2).
- A ferrite bead (Lf1).
- Three MLCC capacitors (Cf1, Cf2, and Cf3).
- An electrolytic bulk capacitor used as bulk energy storage (Cin4).

9 STEVAL-A6983IV1 EMC compliance

The STEVAL-A6983IV1 is certified by an external supervisor company and Class A compliant with the following standards, for industrial use only:

Table 3. List of standards which the STEVAL-A6983IV1 complies with

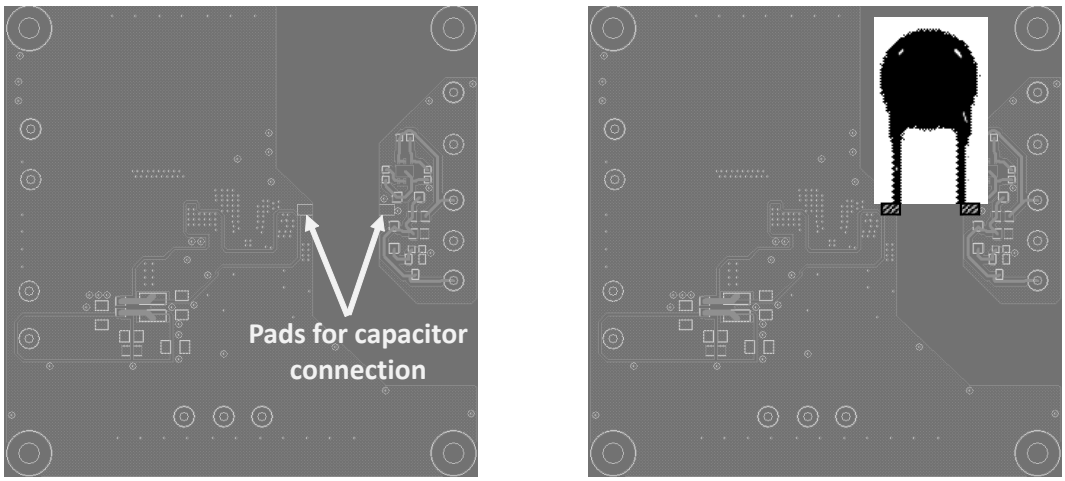
Reference standard	Standard application
CISPR 32:2015 +A1:2019 / EN 55032:2015 + A1:2020 CISPR 35:2016 / EN 55035:2017 + A11:2020 IEC 61000-3-2:2018 + A1:2020 EN IEC 61000-2-3:2019 + A1:2021 IEC 61000-3-3:2013 + A1:2017 + A2:2021 EN 61000-3-3:2013 + A1:2019 + A2:2021	Full
FCC CFR 47 Part 15 Subpart B	Full
ICES-003 Issue 7 (2020)	Full

The compliance is achieved by using a 4.7 nF capacitor (the one specified in the table below), soldered with a very short connection to the provided pads at the bottom of the STEVAL-A6983IV1 (see Figure 19)

Table 4. Capacitor used to achieve the compliance

Part number	Description	Manufacturer
CK45-B3DD472KYVNA	Ceramic Disc Capacitor, 4700 pF, 2 kV, ± 10%, B, 7.5 mm, Radial Leaded	TDK

Figure 19. Capacitor connection at the bottom of STEVAL-A6983IV1 for EMC compliance



The addition of the capacitor mentioned above implies an improvement of the EMC performances, with special reference to the radiated emissions in which a reduction up to 30 dBµV/m is achievable.

The results of the EMC tests are shown in the Figure 20 and Figure 21.

Figure 20. **Conducted EMC test results of the STEVAL-A6983IV1**

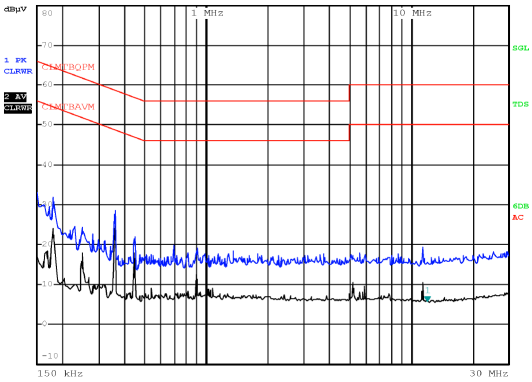
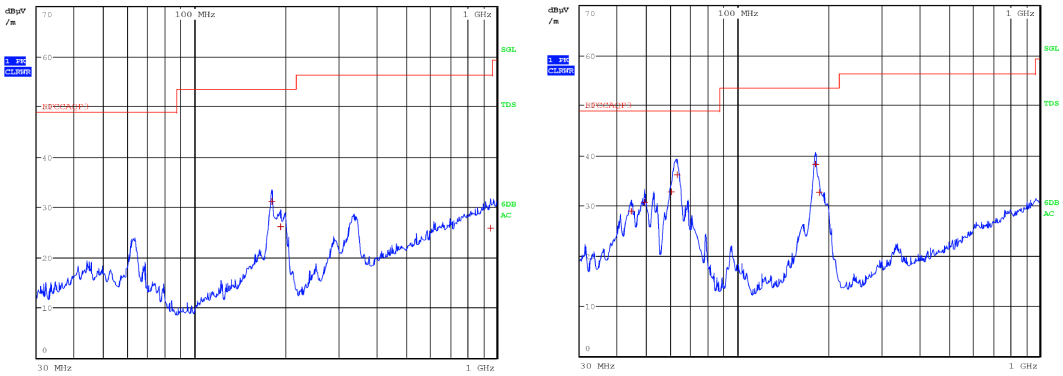


Figure 21. **Radiated EMC test results of the STEVAL-A6983IV1 (horizontal on the left, vertical on the right)**



10 Disclaimer

The certification of the STEVAL-A6983IV1 is fulfilled with the schematic, the layout and the BOM indicated in the sections Section 4: Schematic diagrams, Section 5: Bill of materials and Section 6: STEVAL-A6983IV1 layout.

Any drift from the schematic, the layout, and the BOM described in the sections Section 4: Schematic diagrams, Section 5: Bill of materials and Section 6: STEVAL-A6983IV1 layout, invalidates the certification and the EMC compliance of the STEVAL-A6983IV1 is no longer ensured.

Any change in the schematic, layout, and BOM implemented by the user of the STEVAL-A6983IV1 are under the user's responsibility.

The recommended changes in the BOM described in the next chapters should be considered as possible application ideas in case the user wish to adapt the board to other typical application requirements.

Although the recommended modifications can be considered as minor changes, the certification of the STEVAL-A6983IV1 remains valid only under the conditions mentioned in the sections Section 4: Schematic diagrams, Section 5: Bill of materials and Section 6: STEVAL-A6983IV1 layout.

11 Board setting capability

The STEVAL-A6983IV1 provides the possibility to change some setting in accordance with the application conditions.

Switching frequency

The Rfsw2 is by default equal to 0 Ω sets the switching frequency to 400 kHz and enables the dithering.

Changing the value of Rfsw1 sets a different switching frequency; using the Rfsw1 instead of Rfsw2 disables the dithering function (see Table 5).

Figure 22. Resistors on the PCB used to set the switching frequency and the dithering

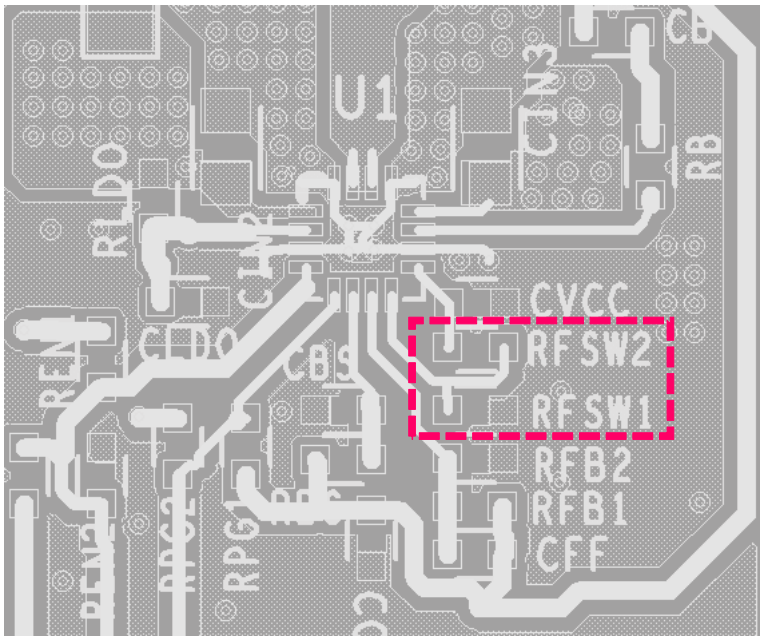


Table 5. Switching frequency and dithering setting

Symbol	Option	RVCC(KΩ)	RGND(KΩ)	Min.	Typ.	Max.	Unit
FSW	Dithering	1.8	N.C.		200		kHz
		0	N.C.		400		kHz
		3.3	N.C.		500		kHz
		5.6	N.C.		700		kHz
		10	N.C.		1000		kHz
	No dithering	N.C.	1.8		200		kHz
		N.C.	0	360	400	440	kHz
		N.C.	3.3		500		kHz
		N.C.	5.6	630	700	770	kHz
		N.C.	10	900	1000	1100	kHz

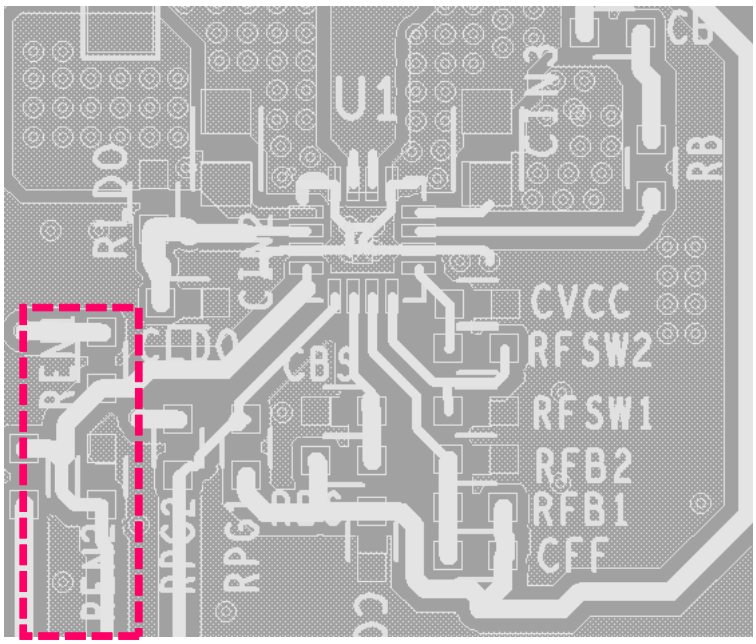
Enable thresholds

The STEVAL-A6983IV1 is equipped with the R_{EN1} = 100 kΩ as pull-up resistor to keep the device always enabled. The power-up threshold can be adjusted by the user with a proper selection of the R_{EN1} and R_{EN2}, according to the following equations:

$$V_{PowerUP} = 1.2 \cdot \left(1 + \frac{R_{EN1}}{R_{EN2}}\right)$$

$$V_{PowerDown} = 1.0 \cdot \left(1 + \frac{R_{EN1}}{R_{EN2}}\right)$$

Figure 23. Resistors enable for thresholds setting

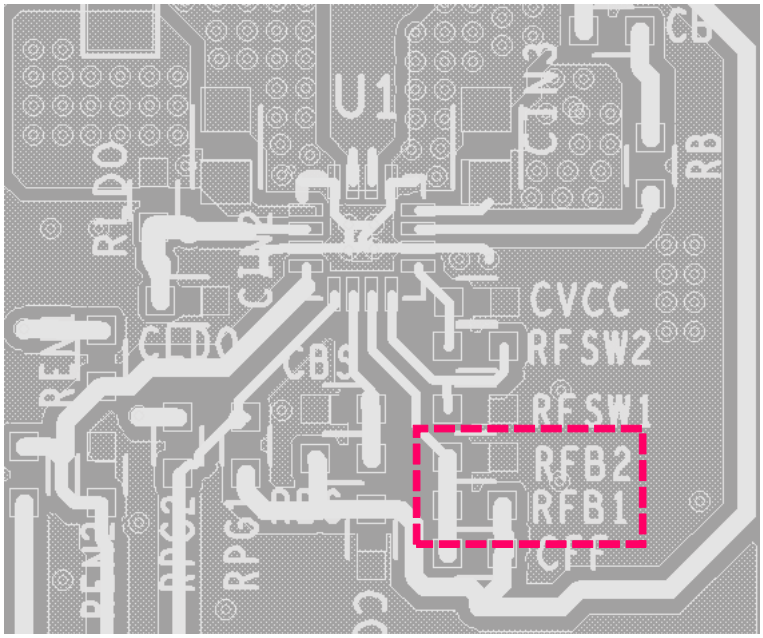


Primary output voltage

The primary (not isolated) output voltage is set to 5 V. If a different voltage is desired, the output resistor divider should be adjusted according to the following equation:

$$V_{OUT\_prim} = 0.85 \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Figure 24. **Resistors of the primary output divider**



Note: Changing the value of the primary output voltage implies the variation of the isolated output voltage too.

12 eDesignSuite

The eDesignSuite software available on the www.st.com website helps in the selection of the devices as well as in the design of the external components suitable for a certain application.

After inserting the application conditions, the device can be selected and the design of the external components is automatically carried out.

13 Application idea

13.1 Post regulation circuitry

A post regulation circuitry is foreseen in the layout at the bottom of the STEVAL-A6983IV1. No components are embedded.

Table 6 proposes the possible components that can be mounted according to the desired post-regulated voltage(s).

Table 6. Post regulation options for various applications

Desired isolated voltage(s)	R1	R2	R3	R4	TL431	C1	Ciso+, Ciso-	Other notes
18 V/-5 V	11.5 kΩ	825 Ω	10 kΩ	10 kΩ	TL431BL3T	1 µF	1 µF→10 µF	
15 V/-8 V	11.5 kΩ	1 kΩ	22 kΩ	10 kΩ	TL431BL3T	1 µF	1 µF→10 µF	
12 V	7.5 kΩ	825 Ω	n.m.	n.m.	n.m.	1 µF	1µF →10 µF (only Ciso+)	• Use a transformer with a lower turn ratio (e.g. ZD2087-AE, see next section) • Adjust the primary output voltage accordingly (e.g. R_{FB1} = 420 kΩ) • VISO- and GNDiso shorted
6 V/-3 V	3.3 kΩ	825 Ω	2 kΩ	10 kΩ	TL431BL3T	1 µF	1 µF→10 µF	• Use a transformer with a lower turn ratio (e.g. ZD2087-AE, see next section) • Adjust the primary output voltage accordingly (e.g. R_{FB1} = 330 kΩ)

The last two solutions foresee a different primary output voltage and a different transformer that better match the reduced voltage required at the secondary side for those applications.

More details about the proposed transformer are provided in the next section.

13.2 Transformer optimization example

The BOM described in Table 7 implies that the primary output voltage is regulated to 5 V and the transformer is optimized for that voltage in order to provide a secondary isolated output voltage (around 30V) suitable for a possible post-regulation that generates 18 V/-5 V or 15 V/-8 V.

If a different isolated voltage should be regulated or a 24 V bus is used as input voltage, an optimized solution can be derived with some changes in the BOM (e.g. transformer, primary side resistor divider).

The Table 8 shows an example how to change the primary output resistor divider in case a 12 V primary output is regulated from a 24 V input voltage. It is also proposed a different transformer with a lower turn ratio (N=2.55, see Table 8) that ensures a secondary output voltage around 30 V too.

Table 7. Comparison between STEVAL-A6983IV1 BOM and optimized solution for V_{IN} = 24 V

		Solution of the STEVAL-A6983IV1	Optimized solution for V_{IN} = 24 V regulating 12 V at the primary output
Transformer		ZB1346-BE	ZD2087-AE
Primary output resistor divider	R_{FB1}	360 kΩ	120 kΩ
	R_{FB2}	75 kΩ	9.1 kΩ

Characteristic of the transformer for this solution are summarized in the table below.

Table 8. Main parameters of the transformer ZD2087-AE

Description	Value
Turn ratio	1:2.55
Magnetizing inductance	13.
Leakage inductance	150 nH
Primary winding resistance	30 mΩ
Secondary winding resistance	293 mΩ

Here below some performance curves and waveforms relative to this application.

Figure 25. Efficiency vs f_{SW}, V_{IN} = 24 V

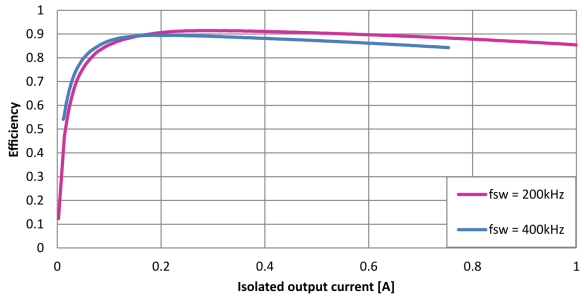


Figure 26. Load regulation vs f_{SW}, V_{IN} = 24 V

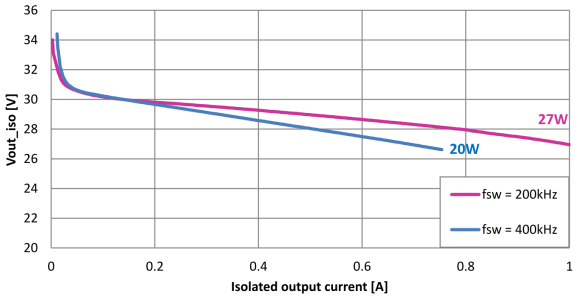


Figure 27. V_{IN} = 24 V, f_{SW} = 400 kHz, I_{OUTiso} = 750 mA

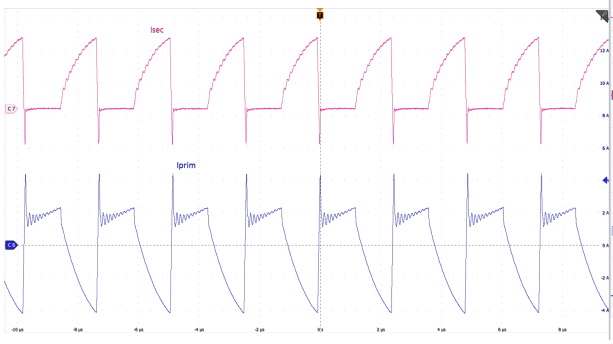
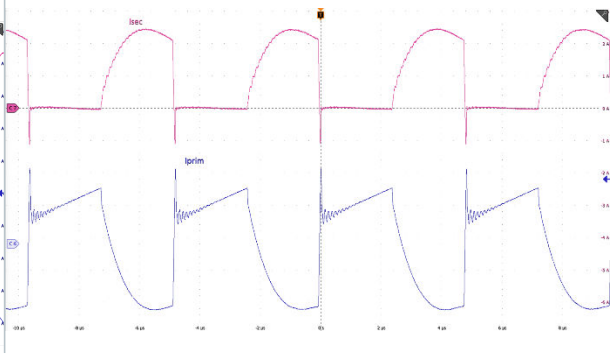


Figure 28. V_{IN} = 24 V, f_{SW} = 200 kHz, I_{OUTiso} = 1 A



14 Thermal performance

The picture below shows the thermal performance of the STEVAL_A6983IV1 detected by an infrared camera under the specified conditions.

Figure 29. **VIN = 12 V, f_{SW} = 400 kHz, I_{OUTiso} = 450 mA (hotspot around 74°C)**

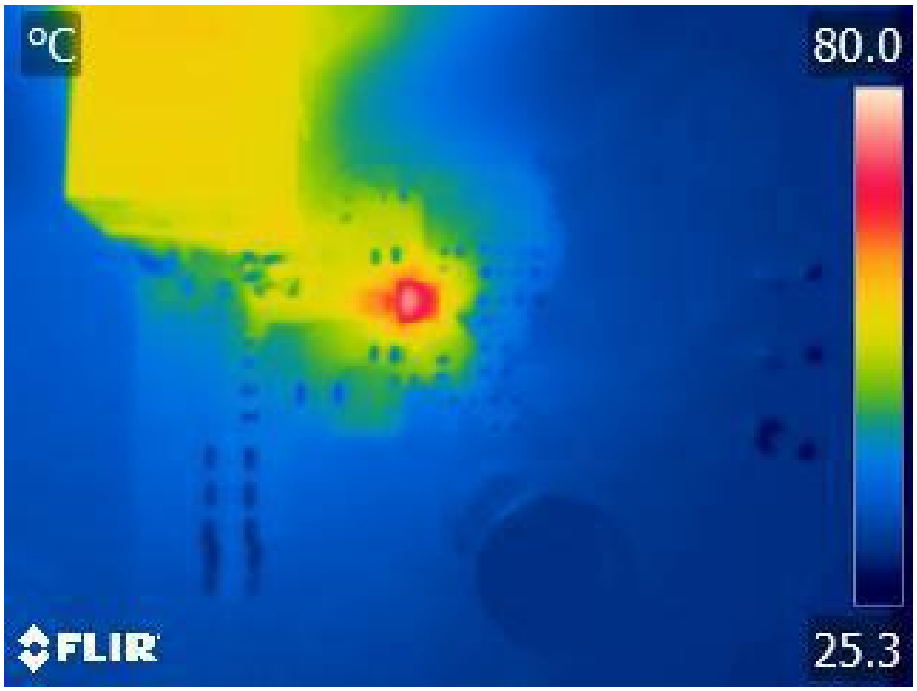
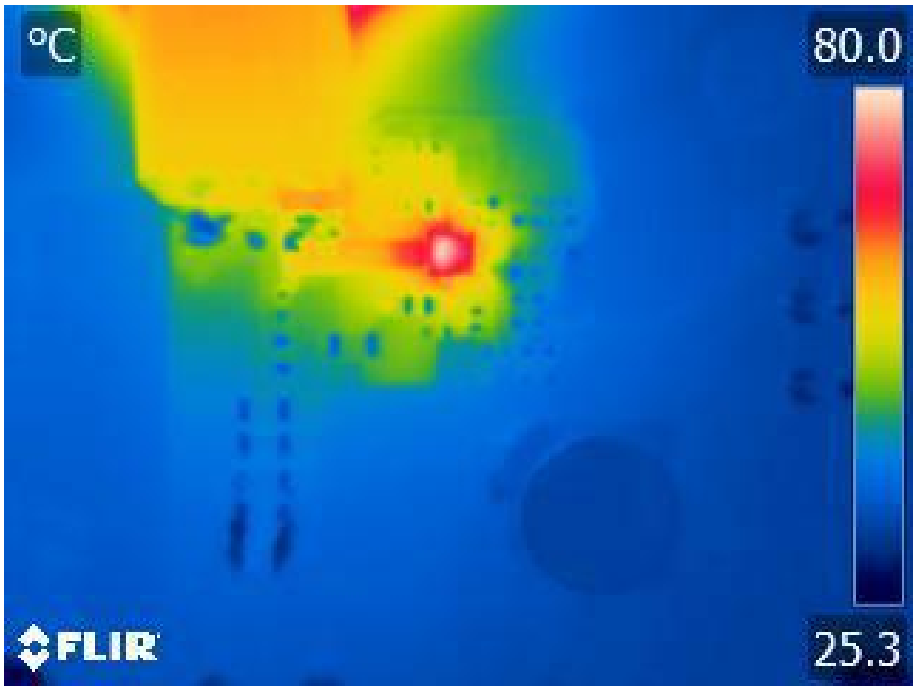


Figure 30. **VIN = 24V, f_{SW} = 400 kHz, I_{OUTiso} = 750 mA**



15 Board versions

Table 9. **STEVAL-A6983IV1 versions**

Finished good	Schematic diagrams	Bill of materials
STV$A6983IV1A (1)	STV$A6983IV1A schematic diagrams	STV$A6983IV1A bill of materials

1. *This code identifies the STEVAL-A6983IV1 evaluation board first version.*

16 Regulatory compliance information

Notice for US Federal Communication Commission (FCC)

For evaluation only; not FCC approved for resale

FCC NOTICE - This kit is designed to allow:

(1) Product developers to evaluate electronic components, circuitry, or software associated with the kit to determine

whether to incorporate such items in a finished product and

(2) Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter 3.1.2.

Notice for Innovation, Science and Economic Development Canada (ISED)

For evaluation purposes only. This kit generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to Industry Canada (IC) rules.

À des fins d'évaluation uniquement. Ce kit génère, utilise et peut émettre de l'énergie radiofréquence et n'a pas été testé pour sa conformité aux limites des appareils informatiques conformément aux règles d'Industrie Canada (IC).

Notice for the European Union

This device is in conformity with the essential requirements of the Directive 2014/30/EU (EMC) and of the Directive 2011/65/EU (RoHS II), including subsequent revisions and additions, as well as amended by the Delegated Directive 2015/863/EU (RoHS III). Compliance to EMC standards in Class A (industrial intended use).

Notice for the United Kingdom

This device is in compliance with the UK Electromagnetic Compatibility Regulations 2016 (UK S.I. 2016 No. 1091) and with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations 2012 (UK S.I. 2012 No. 3032). Compliance to EMC standards in Class A (industrial intended use).

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
11-Feb-2025	1	Initial release.
21-Aug-2025	2	Changed the order of the sections to improve readability.

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