How to select the right thyristor (SCR) for your application

Introduction

This document provides some guidelines about how to select the right thyristor, also referred to as "SCR" (semiconductor controlled rectifier), according to the different applications. Some very specific cases could require a higher level of expertise to ensure reliable and efficient operation.

1 SCR parameter reminder

The main parameters, defined in an SCR datasheet, are reported below (refer to AN2703 for a more exhaustive list).

Absolute ratings are the first parameters to be specified in any datasheet; they should not be exceeded to avoid the device is damaged.

These parameters are:

- V_{DRM} / V_{RRM}: repetitive peak off-state voltage (50 - 60 Hz)
  This is the allowed maximum peak voltage across the device. This parameter is specified up to the maximum junction temperature. I_{DRM} / I_{RRM} leakage currents are specified under this voltage value.
- $I_{T(RMS)}$: RMS on-state current (refer to Section 2.1: Classical topologies for power control using SCR and Section 2.2: Specified RMS and average currents in an SCR datasheet)
  This is the allowed maximum RMS current in the device for a specified case temperature (T_c), or ambient temperature (T_a) or lead temperature (T_l), depending on the type of package.
- $I_{T(AV)}$: average on-state current (refer to Section 2.1: Classical topologies for power control using SCR and Section 2.2: Specified RMS and average currents in an SCR datasheet)
  This is the allowed maximum average current in the SCR at a specified case temperature (T_c), or ambient temperature (T_a) or lead temperature (T_l), depending on the type of package.
- I_{TSM}: non-repetitive surge peak on-state current
  This is the allowed maximum peak current in the device under pulse conditions. Concerning SCRs, it is defined for a single half-cycle sine wave of 10 ms corresponding to 50 Hz mains, and 8.3 ms for 60 Hz mains.
- dI/dt: critical repetitive rate of rise of on-state current (refer to Section 2.3: Relation between SCR RMS current and load RMS current)
  During turn-on, the maximum rate of rise of current should not exceed this maximum value. Above this limit, SCR may be damaged.
- I^2t: recommended value for fuse-protection (10 ms overcurrent duration)
- T_{stg}, T_J: storage and operating junction temperatures
- I_{GM}: peak gate current
  This is the maximum peak current allowed through gate and cathode, defined for 20 µs pulse duration.
- V_{RGM} or V_{RG}: peak reverse gate voltage
  This is the maximum reverse voltage that can be applied across gate and cathode terminals, without damaging the gate-to-cathode junction.

Other electrical characteristic parameters are given to help designers to implement correctly a device in their application. The parameter limits usually reflect the semiconductor process dispersion.

These parameters are:

- I_{GT}: triggering gate current
  This is the current to be applied between gate and cathode to turn on the device. This parameter defines the sensitivity of the component.
- V_{GT}: triggering gate voltage
  This is the voltage to be applied across gate and cathode to reach the IGT current and then to trigger the device.
- I_H: holding current
  This is the current level circulating through the anode and cathode under which the device turns off, in case no gate current is applied.
- I_L: latching current
  This is the current level circulating through anode and cathode to keep the conducting of the device after the gate current has been removed.
- dV/dt: critical rate of rise of off-state voltage (refer to Section 4.2: Immunity improvement)
  This is the maximum value of the rate of the rising voltage that can be applied across the anode and cathode of the SCR without turning it on spuriously.
- V_{TO} / R_D: threshold voltage / dynamic on-state resistance
  These two parameters are used to calculate the instantaneous voltage drop according to the relation $V_T = V_{TO} + R_D \times I_T$ (refer to Section 2.2: Specified RMS and average currents in an SCR datasheet).

- V_{TM}: peak on-state voltage drop
  This is the voltage across the device while it is on-state. It is specified at the peak current corresponding to the $I_{T(RMS)}$ current of the device.
- I_{DRM} / I_{RRM}: maximum forward and reverse leakage currents
  This is the current flowing through the device when it is in the off-state, at the specified V_{DRM} or V_{RRM} value.
- t_q: turn-off time (refer to Section 3.3: SCR turn-off and tq parameter)
  After this time, a positive voltage rate can be applied across the anode and cathode without causing any spurious firing. This parameter defines the maximum operating frequency of the SCR.

2 SCR current rating selection

2.1 Classical topologies for power control using SCR

The thyristor device works as a silicon-controlled rectifier (SCR) so it can only conduct current to one direction (see AN4607), while triac can be considered as two back-to-back SCRs and can conduct a power current to both directions.

In the following four figures there are mainly four application circuits referring to the SCR used to control the power sunk from the AC line. For each topology, the load and SCR currents can be different and the simplified waveforms are given for a resistive load, so that the load current is in phase with the line voltage. t_d is the turn-on delay of the SCR, also called "turn-on angle" because it allows power setting in phase-control circuits. If t_d is equal to half-a-cycle (10 ms or 8.3 ms respectively for 50 Hz or 60 Hz line frequency), or in other words for 180 ° turn-on delay, the load is totally off. On the contrary, for 0 ° t_d angle or for 0 ms t_d time, SCR conducts during a full half-cycle, during 180 ° conduction angle. In ST's datasheet, the conduction angle is called α.

Figure 1. Half-wave rectified load control: simplified schematic (a) and waveforms (b)

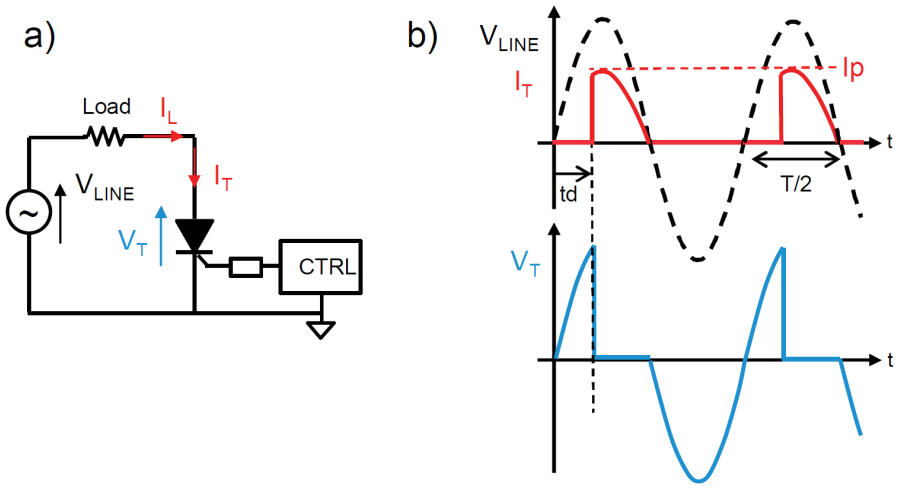


Figure 2. Full-wave load control: simplified schematic (a) and waveforms (b)

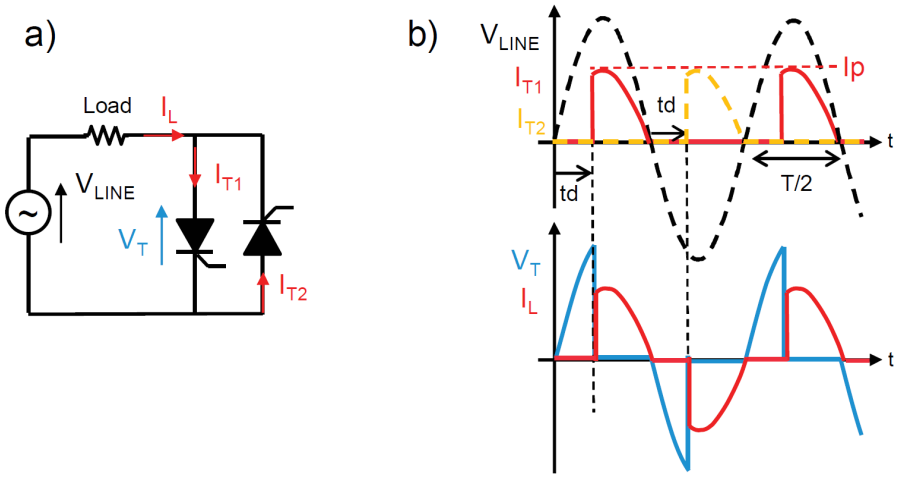


Figure 3. **Mixed bridge (full-wave rectifier with two SCRs): simplified schematic (a) and waveforms (b)**

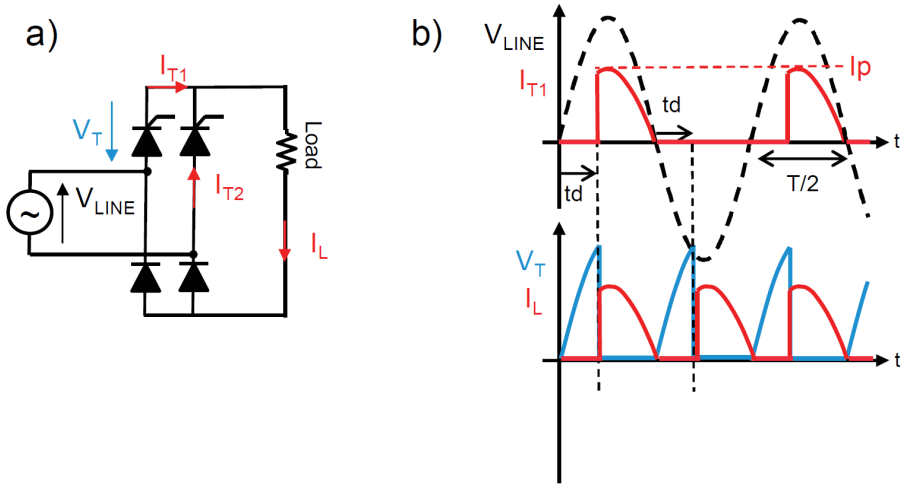
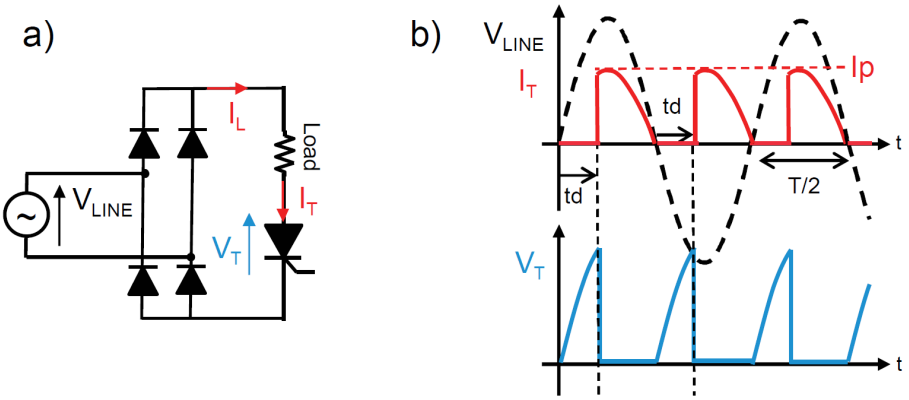


Figure 4. **Full-wave rectified load control: simplified schematic (a) and waveforms (b)**



2.2 Specified RMS and average currents in an SCR datasheet

Two different parameters define the maximum current capability of a thyristor:

- $I_{T(AV)}$ is the maximum average current allowed in the SCR at a specified case temperature (T_c), or ambient temperature (T_a) or lead temperature (T_l), depending on the type of package
- $I_{T(RMS)}$ is the maximum RMS current allowed in the device for a specified case temperature (T_c), or ambient temperature (T_a) or lead temperature (T_l), depending on the type of package.

As explained in Section 2.3: Relation between SCR RMS current and load RMS current, SCR can handle a maximum current only limited by the maximum allowed junction operating temperature, 125 °C for most of the devices, or 150 °C for high-temperature devices. In ST's datasheet, $I_{T(RMS)}$ and $I_{T(AV)}$ currents are defined by assuming an SCR half-wave 180 ° conduction. Such definitions correspond to the application topologies shown in the first three figures, but with 0 ms td time.

Specified current limits: $I_{T(RMS)} = \pi/2.I_{T(AV)}$.

Peak current of the half-wave current: $I_p = 2.I_{T(RMS)}$.

The I_P current value is used to define the V_{TM} (peak on-state voltage drop) parameter.

2.3 Relation between SCR RMS current and load RMS current

The following table gives the equations for the load and thyristor currents according to the different load controls available in the previous figures in Section 2.1: Classical topologies for power control using SCR.

Load current equations ($I_{L(RMS)}$ and $I_{L(AV)}$) are given as functions of SCR currents ($I_{T(RMS)}$ and $I_{T(AV)}$) of the same application (so the same line) to simplify the table.

For each equation of this table:

- I_p is the peak value of the load current assuming a sinusoidal waveform and 180 ° conduction angle
- T is the line period (20 ms or 16.6 ms respectively for 50 Hz or 60 Hz line frequency)
- t_d is the delay time between line zero voltage and SCR turn-on (in ms)

Table 1. Load and thyristor average and RMS currents for different load controls

Load control		Thyristor current		Load current	
		$I_{T(RMS)}$	$I_{T(AV)}$	$I_{L(RMS)}$	$I_{L(AV)}$
Half-wave rectification (Figure 1)	t_d = 0 °	I_p / 2	Ip / π	= $I_{T(RMS)}$	= $I_{T(AV)}$
	$t_d \neq 0$	$\frac{I_P}{2}\sqrt{1-\frac{2\cdot t_D}{T}+\frac{1}{2\pi}\cdot\sin\left(\frac{4\cdot t_D\cdot\pi}{T}\right)}$	$\frac{I_P}{\pi}\cdot\cos^2\left(t_D\cdot\frac{\pi}{T}\right)$		
Full-wave AC (Figure 2) Mixed bridge (Figure 3)	t_d = 0 °	I_p / 2	Ip / π	= √2 $I_{T(RMS)}$	= 0 or 2 x $I_{T(AV)}$ per half-cycle
	$t_d \neq 0$	$\frac{I_P}{2}\sqrt{1-\frac{2\cdot t_D}{T}+\frac{1}{2\pi}\cdot\sin\left(\frac{4\cdot t_D\cdot\pi}{T}\right)}$	$\frac{I_P}{\pi}\cdot\cos^2\left(t_D\cdot\frac{\pi}{T}\right)$		
Full-wave rectification (Figure 4)	t_d = 0 °	I_p / √2	2Ip / π	= $I_{T(RMS)}$	= $I_{T(AV)}$
	$t_d \neq 0$	$\frac{I_P}{\sqrt{2}}\sqrt{1-\frac{2\cdot t_D}{T}+\frac{1}{2\pi}\cdot\sin\left(\frac{4\cdot t_D\cdot\pi}{T}\right)}$	$\frac{2I_P}{\pi}\cdot\cos^2\left(t_D\cdot\frac{\pi}{T}\right)$		

In figure 1 and figure 4, the SCR current is the same as the load current, therefore SCR is able to control a maximum $I_{T(RMS)}$ load current. The maximum RMS load current has to be defined according to the $I_{T(RMS)}$ level specified in the SCR datasheet (here: $I_{T(RMS)DS}$) and by assuming that SCR works at its maximum allowed junction temperature, this load current depends on the application case:

- Half-wave rectification (see figure 1), as the SCR current is the same as the load current: $I_{L(RMS)}$ = $I_{T(RMS)DS}$
- Full-wave AC conduction or mixed bridge (see figure 2 and figure 3): $I_{L(RMS)}$ =√2. $I_{T(RMS)DS}$. Here, a load with RMS current 41% higher than the SCR $I_{T(RMS)DS}$ could be used. As the load current is split between the two back-to-back SCRs, each SCR sees $I_{T(RMS)DS}$ current level only.
- Full-wave rectification (see figure 4): $I_{L(RMS)}$ is between $I_{T(RMS)DS}$ / √2 and $I_{T(RMS)DS}$. The following equation gives the exact $I_{L(RMS)}$ value (where the dissipated power due to full-wave rectification in a single SCR is equal to the allowed losses for $I_{T(AV)}$ and $I_{T(RMS)}$ values specified in the datasheet).

$$P_d = 2\sqrt{2}/\pi \cdot V_{to} \cdot I_{L(RMS)} + R_D \cdot {I_{L(RMS)}}^2 = V_{to} \cdot I_{T(AV)DS} + R_D \cdot {I_{T(RMS)DS}}^2 = 2/\pi \cdot V_{to} \cdot I_{T(RMS)DS} + R_D \cdot {I_{T(RMS)DS}}^2 \quad (1)$$

The result of this equation is:

$$I_{L(RMS)} = -\frac{\sqrt{2}}{\pi \cdot R_D} \cdot V_{to} + 2\sqrt{\frac{2 \cdot V_{to}^2}{(\pi \cdot R_D)^2} + \frac{2 \cdot V_{to}}{\pi \cdot R_D} \cdot I_{T(RMS)DS} + {I_{T(RMS)DS}}^2} \quad (2)$$

2.4 Steady-state current versus operating temperature

SCR can handle a maximum current limited by the maximum allowed operating temperature only, except for specific applications where the turn-off capability can also become a limiting factor (refer to Section 3.3: SCR turn-off and tq parameter).

For most applications, the maximum SCR current depends on the operating temperature and the device power losses only.

In the SCR, as the switching times (around 100 ns) are lower than the switching period (50 Hz or 60 Hz for most cases), the device power losses are linked to the conduction losses only.

The equation below give the junction temperature (refer to AN533 for further information):

$$T_j = T_A + P_d \cdot R_{th(j-a)}$$
$$Or \quad (3)$$
$$T_j = T_C + P_d \cdot R_{th(j-c)}$$

With respectively:

- T_J: junction temperature
- T_A: ambient temperature
- T_C: case temperature
- P_d: conduction losses

The dissipated power losses in the SCR are given as follows:

$$P_d = V_{to} \cdot I_{T(AV)} + R_D \cdot I_{T(RMS)} \quad (4)$$

This where V_{TO} and R_D are respectively the threshold voltage and the dynamic resistance of the SCR on-state voltage drop.

For a sinusoidal load RMS current ($I_{L(RMS)}$) split into two back-to-back SCRs, the dissipated power losses in each SCR are the following:

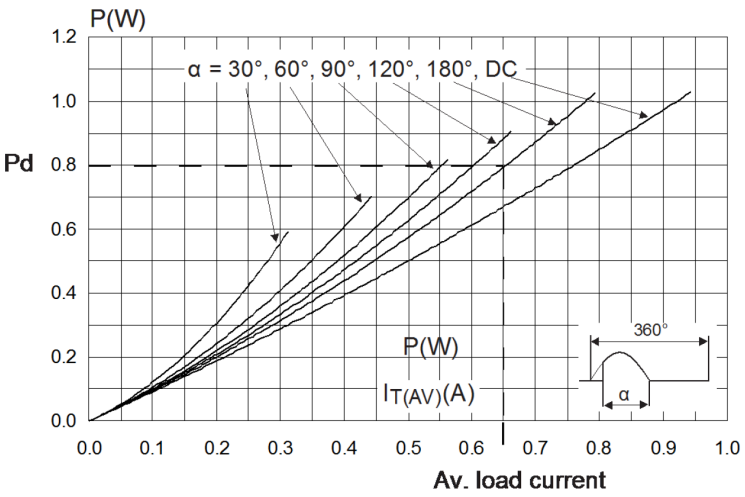
$$P_d = \frac{\sqrt{2}}{\pi} \cdot V_{to} \cdot I_{L(RMS)} + R_D \cdot \frac{I_{L(RMS)}^2}{2} \quad (5)$$

Eq. (5) refers to Figure 2 and Figure 3 circuits. As Figure 1 and Figure 4, refer to Table 1 equations for SCR average and RMS currents and use Eq. (4) to evaluate the conduction losses.

To simplify SCR circuit design, ST's datasheets give the P_d dissipated losses versus the average current (using Eq. (4) with $I_{T(RMS)} = \pi/2 \cdot I_{T(AV)}$) since the SCR current is half- wave rectified current. Figure 5 shows the TS110 curve (1.25 A 700/1250 V SCR). Power losses are calculated in relation to different conduction angles. Since the worst case occurs with 180 ° conduction angle, most curves are given just at 180 °.

For example, as shown in Figure 5, α = 180 °, the TS110 conduction losses with 0.65 A average current (or 1 A RMS current) = 0.8 W.

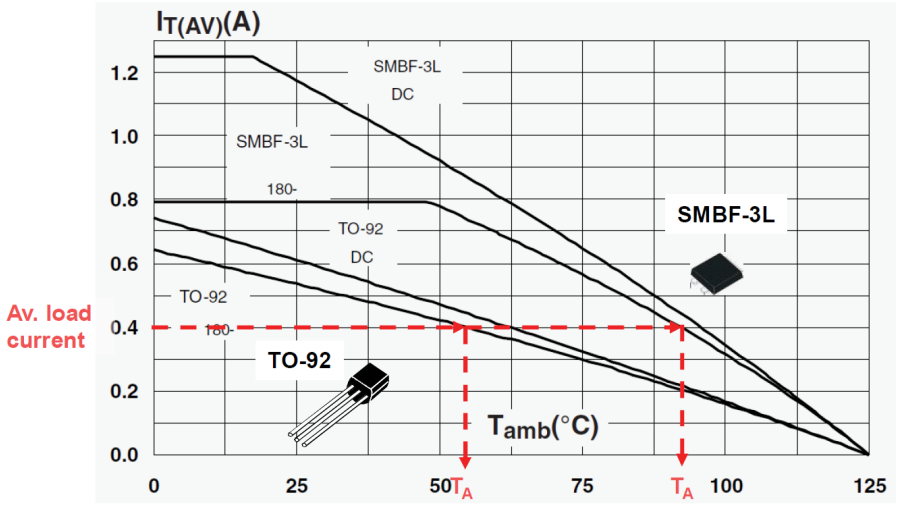
Figure 5. Maximum power dissipation versus RMS on-state current for the TS110



For each device, the datasheet gives the maximum allowed current. This current is calculated so that the associated power losses (with Eq. (4)) keep the junction temperature below the maximum operating temperature (with). This maximum temperature is usually 125 °C or 150 °C for high temperature devices. Figure 6 and Figure 7 give the examples of such datasheet curves for the TS110 and the TN1205H-6T respectively. As the TS110 is available in a TO-92 or SMBF-3L package, case temperature cannot be limited by adding an external heatsink to the device to evacuate its power losses. That is the reason why the curve is given versus the operating ambient temperature.

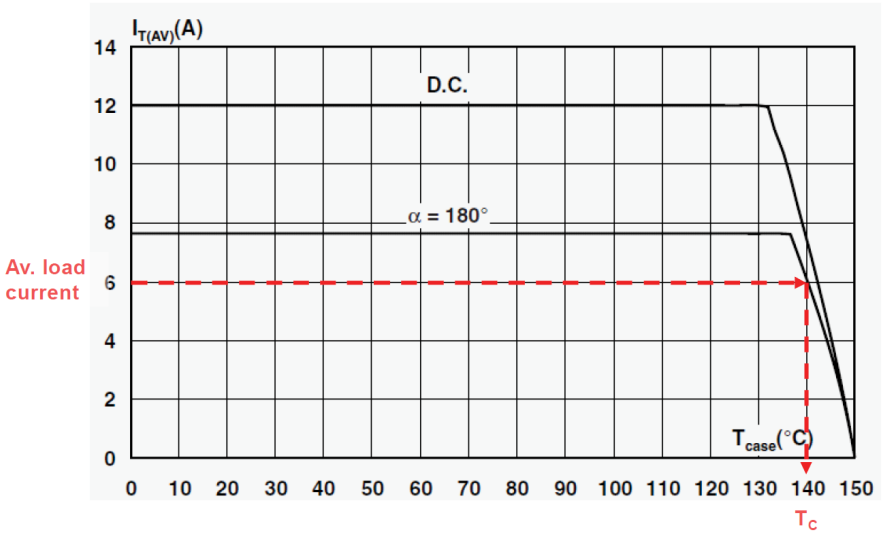
For example, consider 0.4 A average load current, this device has to work with a maximum ambient temperature lower than approximately 55 °C for a TO-92 package, or 92 °C for a SMBF-3L package. In other words, up to 92 °C ambient temperature, the TS110 in SMBF-3L can control a maximum average current of 0.4 A.

Figure 6. Maximum average current versus ambient temperature for the TS110



Referring to the TN1205H-6T (12 A 600 V 150 °C SCR), since the package of the device is a TO-220AB, and as this device can handle up to 12 A RMS current for 150 °C junction temperature, a heatsink is used in most of the cases. The curve is then given versus the operating case temperature as shown by the figure below. This figure shows: with 6 A average current (180 ° conduction angle), the package case temperature has to be lower than 140°C to keep the junction temperature below 150 °C. So, the heatsink has to evacuate the power conduction losses (P_d = 7.46 W for 12 A average current) while the case temperature is below 140 °C.

Figure 7. **Maximum average current versus case temperature for the TN1205H-6T**



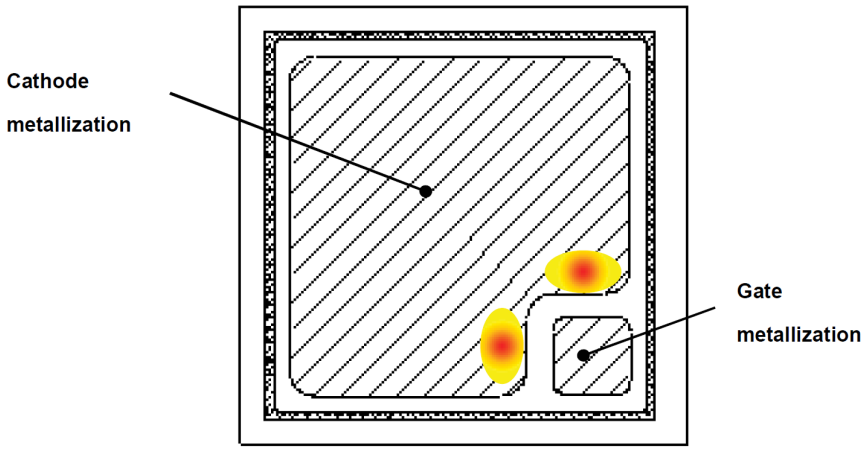
2.5 Maximum dI/dt rate at turn-on

To turn the thyristor on, a current is first applied through its gate-to-cathode junction. This current causes minority carrier injections to the silicon substrate.

For most thyristors, the gate area is in one corner of the die (see Figure 8). The current injection begins close to the gate area, and the power current (circulating from anode to cathode) starts to conduct to the restricted area shown in yellow in Figure 8. The carrier plasma takes some time to spread out along the whole die area (this time could be in the range of 10 to 150 µs depending on the die surface). The thyristor die can indeed be considered as a set of many small SCRs in parallel. The active area of the SCR, closer to the gate, first turns on, and the active area of the SCR placed on the opposite corner is the last to turn on. If the anode current increases too fast, this means that the conductive area has not enough time to spread out along the whole die area, and the power current is focused on a restrictive area shown on the Figure 8. The resistance of this area is necessarily higher than that of the whole die area, so the dissipated power is higher if the whole die conducts. These higher power losses heat up the restricted conducting area, leading to a resistance decreasing on the hot points. These hot points conduct preferably the anode current as their resistance is lower. This runaway phenomenon could lead to an excessive silicon temperature and localized silicon melting. The default modes in the case of melting could be:

- Off-mode: the silicon melting could lead to an I_{GT} increase so that the SCR could require a higher gate current level to be turned on than that applied by the control circuit. SCR remains off.
- Diode-mode: the silicon melting has damaged the silicon junction, which holds the forward voltage, but the bottom junction, which holds the negative voltage is not damaged. The SCR then behaves like a diode and turns on as soon as a high-enough positive voltage (which could be higher than 1 V) is applied between its anode and cathode terminals.
- Short-circuit mode: the silicon melting has damaged the two silicon junctions. The SCR is then not able to withstand any positive or negative voltage. The device turns on as soon as a voltage is applied. The junction damage could be more or less severe, and the SCR could turn on for a voltage higher than 1 V.

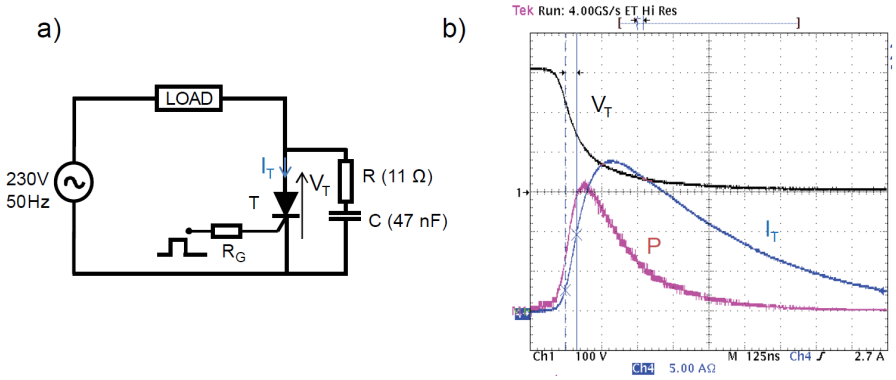
Figure 8. Schematic top view of the thyristor die and turn-on area



In SCR applications, a risk of high applied dI/dt mainly occurs if the SCR is turned on at non-zero voltage with a snubber circuit connected in parallel to the device as shown in the Figure 9 (a) schematic. The Figure 9 (b) shows the dI/dt rate, which is applied through the SCR, which is the TN1610H-6x thyristor (600 V, 16 A, 10 mA high-temperature device), when triggered at peak line voltage. This figure also shows that the power dissipated through the die presents a high peak value at the beginning of the conduction because the die resistivity and so its voltage drop is still high. The applied dI/dt rate is here 175 A/µs with 11 Ω – 47 nF RC snubber, which is above the allowed limit. To keep the dI/dt below the datasheet limit, a higher resistor value has to be selected, such as 47 Ω.

Most thyristors are specified to withstand a 50 A/µs maximum dI/dt rate at turn-on. Values up to 200 A/µs are specified for high-power SCRs (such as the TN5050H) or for SCRs dedicated to capacitive discharge ignition circuits (such as the FLC10).

Figure 9. Example of dI/dt at peak voltage turn-on



2.6 Transient overcurrent

SCR, thanks to its NPNP layer silicon structure, features the best overcurrent capability among semiconductor switches. For example, the AC switch can withstand a maximum peak current during a line cycle (10 ms for 50 Hz frequency) usually 6 or 10 times higher than its nominal RMS current ($I_{T(RMS)}$). This maximum peak current, defined for a half-cycle conduction, is called I_{TSM}. The non-repetitive I_{TSM} occurs rarely and with a limited number of occurrences during the service life of the device, as stated in the JESD77C.01 standard.

In the SCR datasheet, the overcurrent capability is given by this I_{TSM} parameter and also by two curves giving the variation of the I_{TSM} (repetitive or non-repetitive) versus the pulse duration. The Figure 10 (a and b) gives two curves, in "a" picture, pulse duration on the I_{TSM} curve is shorter than 10 ms, and on the other curve pulse durations are longer than a line cycle.

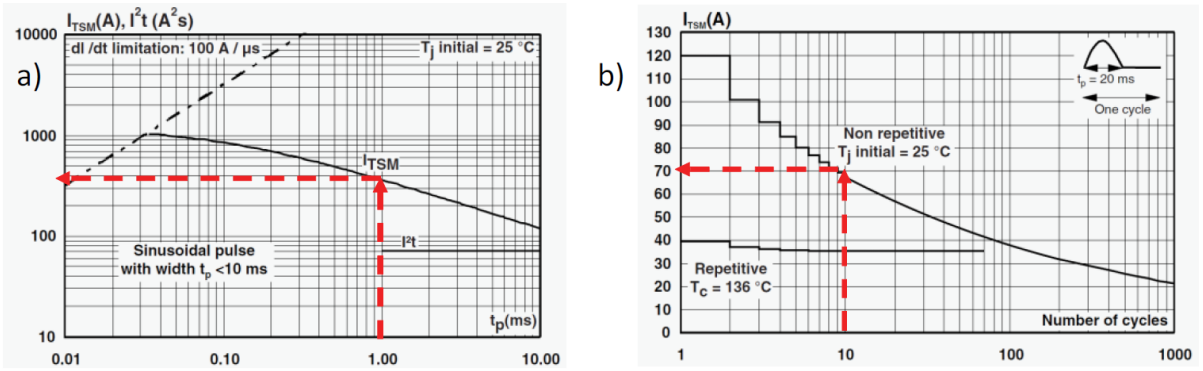
For 1 ms pulse length, the SCR non-repetitive overcurrent capability can be 20 to 40 times higher than the device current rating ($I_{T(RMS)}$). The Figure 10 (a) gives the non-repetitive I_{TSM} current for a pulse width shorter than 10 ms for the TN1205H. For 1 ms pulse, the maximum peak current applied is 360 A, which is 30 times higher than the $I_{T(RMS)}$ of this device (12 A for the TN1205H).

Figure 10 (b) gives the allowed current versus the number of cycles. One cycle is defined as a half-wave current (180 ° conduction time). So, a cycle defines here a time duration and not a number of operations as it is usually understood in terms of reliability. For example, 10 line cycles of 20 ms long mean 200 ms time length. For this 200 ms duration, the maximum non-repetitive peak current of the sinus half-wave can reach up to 70 A. If a higher peak current is applied during the 10 line cycles, the device may be damaged.

This Figure 10 also gives the maximum repetitive I_{TSM} current. This value is calculated according to the time conduction and to the case temperature to keep the junction temperature below the maximum allowed value (150 °C here for the TN1205H example). Before applying once again a new current equal to the allowed value, the junction temperature has to decrease to the initial condition where it is equal to the case temperature given in the curve. The case temperature has also to remain below the indicated value during the whole current conduction. These two I_{TSM} curves allow users to know if the selected part number fits their applications, particularly if overcurrent due to inrush currents or stalled rotor operation can occur.

These curves demonstrate that the current SCR rating should not be overrated in a motor control application.

Figure 10. TN1205H repetitive and non-repetitive I_{TSM} current capability versus pulse time



3 SCR voltage rating selection and turn-off capability

3.1 Peak line voltage

SCR is used in series with the load and the line voltage in most applications. This means that at the off-state, the SCR has to withstand at least (√2) per peak line voltage.

For single phase voltages, the power grid with the highest RMS level is 277 V. This leads to 390 V peak voltage applied across the SCR. If a 15% increase of the nominal grid voltage is assumed, the applied voltage is lower than 448 V. This is the reason why 600 V devices fit most single-phase applications (except those listed in Section 3.2: Overvoltage protection). For a 3-phase power grid, the line-to-line voltage is SQRT(3) times higher than the line-to-neutral voltage. The table below gives the standard values according to the different power grids.

Table 2. Nominal voltages for 3-phase grids

Single-phase voltage V_{LN} (V)	Phase-to-phase voltage U_{KL} (V)
220	380
230	400
240	415
277	480

The maximum voltage applied across the switch depends on the load configuration. As the switch is in series with the load, the maximum applied voltage is:

- For DELTA configuration (see Figure 12): $V_{Tmax} = U_{Peak}$
- For STAR configuration (see Figure 11): $V_{Tmax} = (U_{Peak} \times \sqrt{3})/2$ (the worst case for floating load neutral)

Figure 11. STAR connection

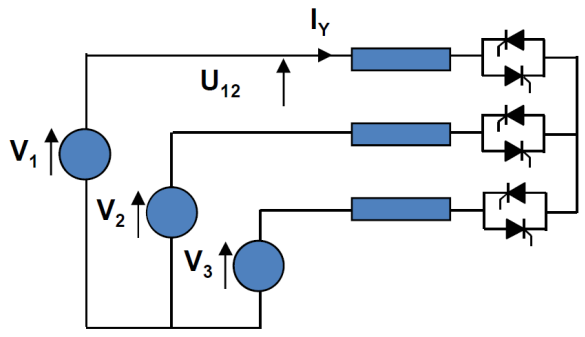
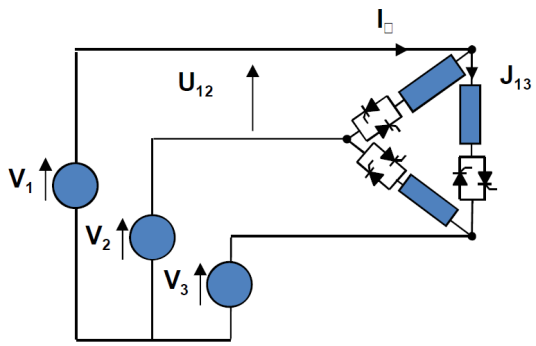


Figure 12. DELTA connection



The highest voltage across the SCR is then: U_{Peak} (peak line-to-line voltage). This voltage, according to the table values indicated above, is very close to or above 600 V. For such applications, SCRs withstand at least 800 V. For motor control, due to the back electro-motive force (BEMF) that can be added to the voltage held by the SCR at off-state, 1000 V, or 1200 V devices are preferred.

3.2 Overvoltage protection

As SCR is most of the case used in series with a load and the line voltage, any surge or transient voltage applied to the grid is seen by the SCR if it is in the off-state. If the SCR conducts, the surge results in a supplementary current through the device. This surge current can damage the device if it is higher than the SCR I_{TSM} capability.

There are mainly two solutions to protect an SCR when a voltage surge is applied across the device at off- state. The former consists of adding a metal-oxide varistor (MOV) in parallel to the SCR terminals. Any MOV presents an internal resistance, which causes the clamping voltage to increase with the applied surge current. Therefore, MOV should be placed in parallel to the SCR (see Figure 13 (a)) and not to the line input, to limit the MOV current with the help of load impedance.

If the load power is high, the load impedance is low and the surge current applied to the MOV can be very high, a high voltage is applied across the SCR.

The example of Figure 13 (a) refers to a half-wave rectification circuit. It can be noted that if another SCR is connected back-to-back to the first SCR to implement a full-wave AC power control (see Figure 2), MOV protects both devices since MOV has a bidirectional clamping capability. The latter is to use a Transil™ connected across anode and gate terminals as shown in Figure 12 (b). This allows a crowbar protection to be implemented.

This solution allows a more accurate control of the maximum voltage applied to the device (especially for high power applications) but it leads to a spurious triggering of the device if a surge is applied. Refer to AN1966 for more information on this solution. Figure 11 (b) shows a resistor (R1 or R2) connected between each SCR gate and cathode terminals.

This resistor helps to improve the SCR immunity as explained in Section 4.2: Immunity improvement.

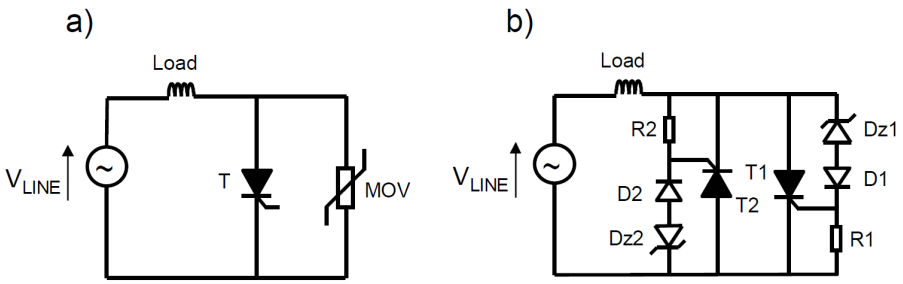
Two diodes (D1 and D2) are used in series with the unidirectional TRANSIL (D_{Z1} and D_{Z2}) as the alternating voltage is applied to the SCR in this schematic. If a DC positive voltage is applied, these diodes can be removed. Please also note that the D1 and D2 breakdown voltage has to be chosen higher than the D_{Z1} and D_{Z2} V_{CL} levels. Indeed, if a positive overvoltage is applied, D_{Z1} provides SCR T1 with a gate current. This device so turns on and the voltage applied to both SCRs suddenly falls down to T1 on-state voltage drop.

If the D2 breakdown voltage is lower than D_{Z1} V_{CL}, the surge is clamped by D2 and no current is applied to the T1 gate. As T2 cannot be triggered for a negative voltage, the whole surge energy is dissipated through D2 leading to D2 failure. For a 230 V application, the devices used to protect 600 V SCRs are usually:

- D_{Z1} and D_{Z2}: BZW04-376 or 1.5KE400C
- D1 and D2: STTH110
- R1 and R2: 50 to 100 Ω, ¼ W

More information on this solution can be found in the application note AN1966.

Figure 13. SCR overvoltage protection with a MOV (a) or with a TRANSIL (b)



3.3 SCR turn-off and tq parameter

SCR turns off when its anode current decreases and reaches zero. A reverse voltage is then usually applied across the anode and cathode terminals. This negative biased helps the recombination of the minority carriers still present in the SCR substrate. The SCR is completely off only after all these carriers are definitely disappeared.

If the reverse voltage level or duration is not sufficiently high, the SCR could turn on once a positive voltage is applied across the anode and cathode terminals.

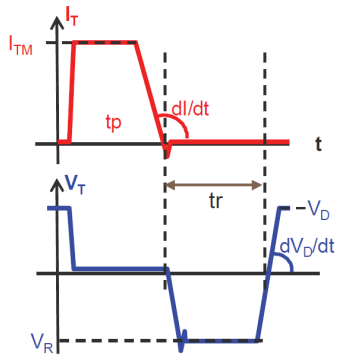
This is the reason why a t_q parameter is defined for SCRs. This tq time is the minimum time that a negative voltage has to be applied across the SCR, after zero-current switching, before applying again a positive voltage. This parameter is usually in the range of a few microseconds to hundreds of microseconds.

Concerning online frequency applications, SCR remains off most of the time at least half a cycle (more than 8.3 ms). t_q parameter does not need to be specified. For higher operating frequencies, the tq parameter can become relevant.

To define the SCR t_q capability, the test sequence shown in the Figure 14 is applied to a DUT (device under test). This sequence is the following:

1. First, I_{TM} peak current is applied during a t_p time.
2. This current is then decreased with a $(dI/dt)_{OFF}$ rate down to zero.
3. After zero-current crossing point, VR reverse voltage is applied during tr variable time.
4. After this tr time, a positive V_D voltage is applied with a dV_D/dt increasing rate.
5. At the first sequence, tr time is chosen long enough so that DUT remains off. The test sequence is then repeated starting from point 1, but with shorter tr time applied to point 4.
6. If DUT remains off, the whole sequence is repeated, reducing t_r time every new cycle, up to the SCR turn on when the positive voltage is applied. The last applied (and minimum) t_r time, for which the DUT was still off, is defined as the DUT t_q parameter.

Figure 14. SCR test sequence to characterize t_q parameter



t_q parameter increases, SCR needs more time to turn off:

- The applied I_{TM} current increases, if the $(dI/dt)_{OFF}$ decreasing rate increases
- If the V_R applied reverse voltage absolute value decreases
- If the V_D applied forward voltage increases
- If the dV_D/dt increasing rate increases
- If the junction temperature increases

As some parameters cannot be set by the user (such as applied current and voltage), the only ways to improve SCR turn-off capability in one application are:

- Adding a low R_{GK} resistor
- Decreasing T_j (by adding a heatsink)
- Decreasing $(dI/dt)_{OFF}$ (by adding a serial inductor)
- Decreasing dV_D/dt (by adding the RC snubber circuit in parallel to the SCR)

4 Triggering circuits

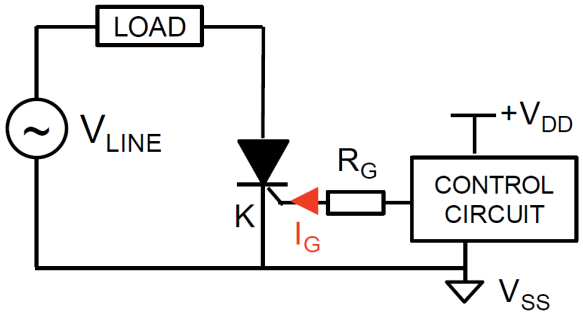
4.1 Gate control circuit

4.1.1 Non-insulated control circuit

There are many applications where the MCU has not to be insulated from the mains voltage. This can actually be implemented as the end-user usually does not have a direct access to any conductive parts connected to the MCU (for example end-used interfaces are most of the time non-conductive).

MCU can be connected to the line as shown in the Figure 15. The reference of the control circuit is directly related to the SCR cathode. This solution is called "positive power supply" as the voltage supply V_{DD} is above the drive reference (V_{SS}), which is connected to the mains terminal (line or neutral). If the supply is a 5 V power supply, then V_{DD} is 5 V above the mains.

Figure 15. SCR direct non-insulated control circuit



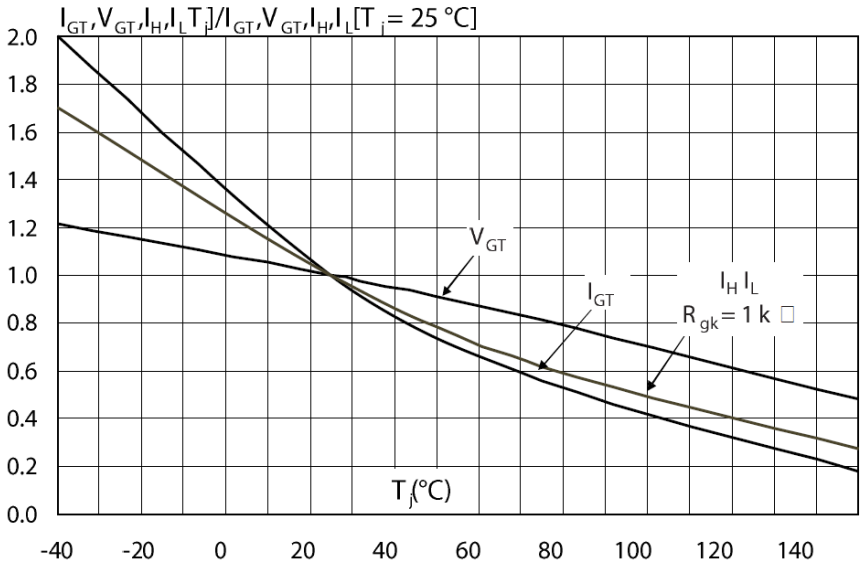
Please refer to AN3168 to adapt the gate control circuit to negative power supplies.

4.1.2 Gate resistor calculation (for non-insulated control circuit)

The minimum gate current (I_{GT}), required to trigger SCR, increases as the junction temperature (T_j) decreases (as well as V_{GT}, I_H, and I_L, see Figure 16). The worst case appears when T_j is equal to the minimum ambient temperature. For appliance systems, the minimum ambient temperature is generally 0 °C.

For example, the TN1205H I_{GT} level is given lower than 5 mA with T_j = 25 °C. When T_j = 0 °C, the maximum I_{GT} = 1.36 times the I_{GT} value specified at 25 °C. This means I_{GT} at 0 °C can reach 6.8 mA.

Figure 16. I_{GT}, V_{GT}, I_H, and I_L variation with junction temperature for TN1205H SCR



In the following, we assume that the device gate is directly connected to a microcontroller (MCU) output pin, through a gate resistor (R_G) as shown in Figure 13. To ensure that the MCU always delivers "I_{GT} (0 °C)", the maximum gate current to 0 °C, the gate resistor (R_G) must be calculated for the minimum available voltage. This means that the minimum supply voltage and the maximum voltage drop of the gate junction (V_{GT}) should be taken into account.

Furthermore, the resistance definition depends on its tolerance. Typically, 5% precision resistors are used.

The microcontroller output port resistor ($R_{DS(on)}$) maximum value also plays a role in the current limitation.

R_G is given by the following formula:

$$\frac{V_{DD\min} - V_{GT\max}}{R_{DSon\max} + R_G \cdot 1.05} > I_{GT}\left(0°C\right) \quad (6)$$

Example:

Given a 20 mA output pin of a microcontroller, the worst $R_{DS(on)}$ could be typically 50 Ω (1.5 V for 30 mA for 85 °C junction temperature).

If the T1205H SCR is used, its I_{GT} increases by 36% for 0 °C junction temperature as previously said. V_{GT} is given at 1.3 V for 25 °C T_j. Its value increases as T_j decreases as shown in the Figure 16. With a minimum supply voltage of 4.5 V and V_{GT} = 1.4 V (at 0 °C), R_G is given by the following formula for the T1205H device:

$$R_G \leq \left(\frac{4.5 - 1.4}{0.068} - 50\right)/1.05 = 386\ \Omega \quad (7)$$

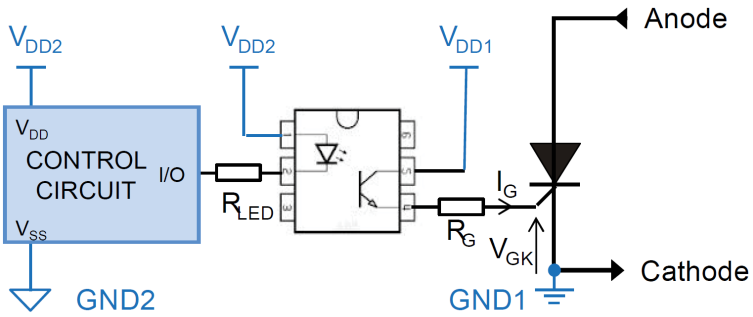
The normalized standard value, the closest to 386 Ω, and lower than the calculated value, can be 360 Ω.

4.1.3 Insulated control circuit

The Figure 17 gives a typical example of how an optotransistor can be used to develop the SCR triggering circuit insulated from the control unit (which is usually the MCU). SCR cathode is then connected to the high voltage (usually line, neutral, or DC bus), while its anode is connected either to the load, or to the line or to the neutral for a mixed bridge application. V_{DD2} is the supply of the control circuit. V_{DD1} is the supply used to provide SCR with a gate current. V_{DD1} and V_{DD2} supplies have to be insulated from each other.

V_{DD2} supply can easily be implemented using a secondary winding added to a flyback transformer (refer to AN4606 and AN4564).

Figure 17. SCR insulated control circuit with an optotransistor



4.1.4 Gate resistor calculation (for an insulated control circuit)

R_G gate resistor has to be selected to apply a current higher than SCR I_{GT}. This resistor has to satisfy the equation below, where $V_{CE(sat)}$ is the optotransistor collector-emitter saturation voltage and V_{GT} is the gate-to-cathode SCR voltage (see the Figure 17).

$$R_G \leq \frac{V_{DD1} - V_{CE(sat)} - V_{GT}(T_j)}{I_{GT}((T_j)} \quad (8)$$

As explained in Section 4.1.2: Gate resistor calculation (for non-insulated control circuit), the V_{GT} and I_{GT} worst case to be taken into account is when the junction temperature of the application is at the lowest ambient working value. To ensure SCR is well-triggered whatever the conditions are, the worst case for each parameter has to be considered. This means:

- V_{DD1} is at its lowest level (10% below its nominal value of 5 V)
- $VC_{E(sat)}$ = the maximum specified value (which is usually 0.4 V for a photo transistor)
- V_{GT} = the maximum V_{GT} for 0 °C junction temperature
- I_{GT} = the maximum I_{GT} for 0 °C junction temperature
- The selected resistor is a 5% accuracy resistor; so the worst case occurs when R_G is 5% higher than its standard value

The TN1205H device is considered for calculation purpose and the gate resistor to select has to be lower than:

$$R_G \leq \frac{V_{DD1\,\min} - V_{CE(sat)\,\max} - V_{GT}(0°C)}{I_{GT}(0°C) \cdot 1.05} = \frac{4.5 - 0.4 - 1.4}{6.8 \cdot 10^{-3} \cdot 1.05} = 378\ \Omega \quad (9)$$

The closest standard is 360 Ohms for 5% accuracy series.

Concerning the LED resistor (refer to R_{LED} in Figure 15), the minimum current to apply to the LED is linked to the gate current to apply and to the current transfer ratio (CTR) of the photocoupler.

For most photocouplers, CTR can be considered as constant from 25 °C to –10 °C, therefore the minimum specified CTR of the datasheet match our calculations.

By using a photo transistor (not a photodarlington) then the minimum CTR is 50%.

LED resistor ha to satisfy the following equation, where V_F is the optotransistor emitter LED forward voltage and V_{OL} the MCU I/O pin low-level output voltage.

$$R_{LED} \leq \frac{V_{DD2\,\min} - V_F - V_{OL}}{I_{GT}(T_j)/CTR} \quad (10)$$

To apply at least a current higher than the required I_{GT} to the photocoupler output, the worst case is taken into account here:

- V_{DD2} is at its lowest level (10% below its nominal value of 5 V)
- V_F = the maximum specified value of the LED (which is usually 1.5 V)
- Maximum low output level for the MCU pin, which sinks the LED current (0.8 V for the LED current level sunk by this I/O)
- T_j = the minimum ambient temperature of the application (0 °C as considered previously)

The selected resistor is a 5% accuracy resistor; so the worst case occurs when R_G is 5% higher than its standard value.

This gives the equation below:

$$R_{LED} \leq \frac{V_{DD2\,\min} - V_F\max - V_{OL}\max}{I_{GT}(0°C)/CTR\ \min \cdot 1.05} = \frac{4.5 - 1.5 - 0.8}{6.8 \cdot 10^{-3}/50 \cdot 1.05} = 15406\Omega \quad (11)$$

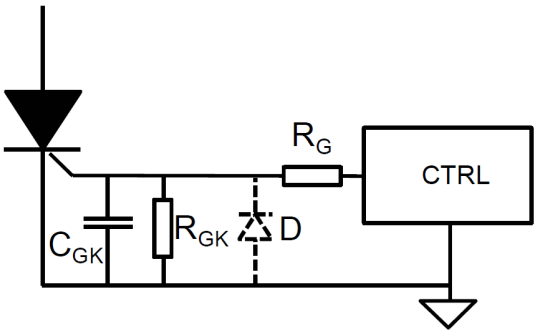
The closest standard is then 15 kΩ for the 5% accuracy series. The nominal current applied to the LED (V_{DD2}, V_{OL}, V_F, and R_G values) is then in the range of 0.2 mA. This is well below the maximum advised current, which is usually in the range of 10 mA. So, the photocoupler reliability is ensured and the CTR ratio should not decrease too much during the application lifetime.

4.2 Immunity improvement

The Figure 18 shows how to improve SCR immunity. SCR, due to its sandwich structure of several silicon layers, embeds an internal parasitic capacitor. Each time a dV/dt voltage transient is applied between anode and cathode terminals, a capacitive current is injected to the gate due to this internal SCR capacitor. This parasitic current may trigger the device. This is the reason why added C_{GK} or R_{GK} components, like shown in theFigure 18, allow this capacitive current to come from the gate and improve SCR dV/dt withstanding (refer to AN4030).

Diode D shown in the dashed line is used if a negative voltage above VRGM could be applied by the control circuit. Such a case cannot occur with MCU direct control, but it can happen with the opto triac control (refer to AN4607).

Figure 18. SCR gate-circuit for immunity improvement



All SCRs, presenting an I_{GT} level higher than 1 mA, embed an internal R_{GK} resistor about = 0.6 V divided by I_{GT} level. An external resistor does not always improve SCR dV/dt withstanding. To get a good result, the external R_{GK} resistor value has to be lower than the internal R_{GK} resistor. For 15 mA SCR, the internal R_{GK} is about 40 Ω, so to get an impact, an external resistor at least 40 Ω has to be added. The drawback is that a supplementary current has to be provided by the control circuit to trigger the SCR, as from the external R_{GK} comes a current equals to the V_{GT} divided by the R_{GK} (so 32.5 mA for 1.3 V V_{GT} and 40 Ω resistor).

Better performance can be reached by a C_{GK} capacitor. A capacitor indeed behaves like a short-circuit during transients. Adding a C_{GK} means 0 Ω resistor. Moreover, the advantage of C_{GK} is that this component does not draw any current from the control circuit output as long as the output signal is consistently applied, allowing the CGK capacitor to charge. This is the reason why C_{GK} is used with sensitive SCRs (with I_{GT} lower than 1 mA).

A C_{GK} has always to be used with the R_{GK} in parallel. If C_{GK} is charged to the V_{GK} voltage, any current can flow; so it has to be discharged each time the SCR is turned off. The discharge can be ensured by an external R_{GK} (which can have 1 kΩ value for example). If the SCR is directly driven by the MCU, the MCU I/O pin has to be configured in push-pull mode. At SCR off-state, the MCU I/O is at low-level. The bottom MOSFET of the MCU I/O pin discharges the C_{GK} capacitor through its $R_{DS(on)}$. Working with an I/O pin configured in push-pull and using non-sensitive SCRs (with I_{GT} levels above 15 mA) allow high immunity levels to be reached and external R_{GK} and C_{GK} components are not required.

5 Conclusion

This paper has dealt with the fundamental parameters to select the SCR:

- Current rating, mainly linked to the operating temperature
- Voltage rating, according to the load to control and the mains voltage
- Triggering current depends mainly on the application control circuit output current capability and the desired dV/dt immunity level

Further information can be found in the following application notes:

- AN302 and AN303: handle in detail the latching and holding current parameters
- AN392: gives basic information about triac control with a microcontroller (given information could be adapted to the SCR device)
- AN533: lists precautions for the correct mounting and cooling of SCR/Triac devices
- AN1966: explains how to protect triac against overvoltage (given information could be adapted to the SCR device)
- AN2703: gives the definition of triac, ACST, ACS, SCR datasheet parameters
- AN3168: gives tips about how to design an SCR control circuit according to the supply polarity
- AN4030: analyzes the impact of a capacitor connected between the device gate and drive reference

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
25-Mar-2016	1	First release
30-Jan-2024	2	Document reworked to improve readability. No content changes.

Contents