E-mode GaN technology: tips for best driving

Introduction

The major challenge of power electronics today is to deal with the growing need for power and efficiency improvements and at the same time, the constant pursuit of cost and size reduction. The introduction of wide band gap materials (WBG) devices moves in this direction, thanks to their electrical features and considering that Si devices have achieved their theoretical limits with the increased switching frequency.

Among the WBG semiconductors, Gallium Nitride (GaN) technology is increasing its importance and diffusion in power conversion applications, becoming at the same time also commercially available. GaN power devices have better figure-of-merit (FOM, $R_{DS(on)} \cdot Q_G$) than silicon counterparts: in fact, this technology shows low specific $R_{DS(on)}$ and leakage, a high breakdown voltage, zero reverse recovery charge and very low intrinsic capacitances. This leads to better efficiency, higher power density and increased maximum frequency in power converters.

Rather than discussing only device physics or converter design principles, this work aims to bridge the gap between the two, providing the background necessary for a power electronics engineer to begin a project in GaN-based converter design. The challenges encountered in GaN-based converter design are also considered, such as the consequences of faster switching on gate driver design and board layout.

This paper basically investigates the driving requirements of discrete Power GaN devices when used in half-bridge circuits. In Section 1 Overview of the gallium nitride technology, there is a brief overview of the GaN technology and the structure of commercial GaN devices in both cascode and HEMT technology. Section 2 GaN drive circuits: main characteristics reviews the main characteristics of GaN Drive circuits, while Section 3 GaN drive circuit: different topologies analyses different topologies of GaN drive circuit.

1 Overview of the gallium nitride technology

The following table describes the relevant physical and electronic properties of gallium nitride (GaN) compared with silicon (Si) and silicon carbide (4H – SiC). As shown below, GaN has a very high critical electric field (>10x than Si technology): so, gallium nitride is more capable of sustaining high voltage before failing. Higher electric field means also compact high voltage switches compared to silicon, thus far surpassing state-of-the-art silicon transistors in terms of all relevant figures of merit (FOM). The high breakdown field and the superior mobility of the 2-dimensional electron (2DEG) gas allow to fabricate transistors with low resistive and switching losses, improving the efficiency of switching mode power converters beyond 99 %.

Table 1. Si vs. SiC vs. GaN (physical and electronic comparison)

Property	Si	4H-SiC	GaN
Bandgap (eV)	1.12	3.2	3.4
Critical field Ecr (MV/cm)	0.25	3	4
Dielectric constant ε	11.8	9.7	9.5
Saturation velocity (10^7cm/s)	1	2	3
Electron mobility μ (cm^2/Vs)	1350	800	2000
Thermal conductivity k (W/cm K)	1.5	4.9	1.3

Of course, when designing switched-mode power supplies (SMPS), the main figures of merit (FOM) are cost, size, and efficiency. These three FOMs are coupled and require that many factors be taken into consideration.

For example, increasing switching frequency can reduce the size and cost of the magnetics, but it will increase losses in the magnetics and switching losses in the power devices. This has been the main blocking point for higher switching frequencies with traditional Si switches. Because of low terminal capacitances and no diode reverse recovery, GaN HEMTs have the potential to significantly lower losses compared to MOSFETs and IGBTs.

Moving from Si to gallium nitride, for the above-mentioned reasons, strong improvement of overall performance can be achieved considering the “entire system” (power devices, magnetics, driver and so on). In other words, it is misleading to compare only the electrical features and the cost of the power switches, because other system components or sections can benefit from gallium nitride selection.

In the following table, there is a brief comparison between Silicon and GaN from electrical point view:

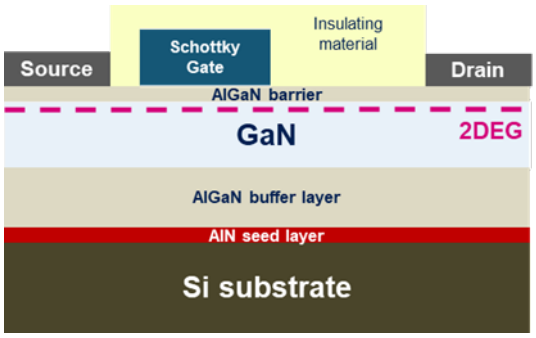
Table 2. Si vs. GaN (electrical comparison)

Parameters	Silicon	GaN	Comments
On-resistance ($R_{DS(on)}$)	Larger	Smaller	GaN: lower conduction losses and higher current capability
Gate charge (Q_g)	Larger	Smaller	GaN: faster switching speed and better performance in hard-switching and high frequency applications
Reverse recovery charge (Q_{rr})	From nC to μC	Zero	GaN: zero recovery losses and the best choice for half-bridge/bridgeless TP applications
Third quadrant conduction	Lower	Higher	Higher reverse conduction losses for a GaN, dead-time optimization is mandatory
V_{GS} rating	Wider	Narrower	GaN: lower immunity vs. gate ringing/bouncing (driving stage layout to be optimized)
Avalanche breakdown	YES	NO	No “reversible” avalanche mechanism for GaN, even if there is margin vs. BV rating

1.1 GaN HEMT physical structure

The figure below shows the basic structure of GaN HEMT (high electron mobility transistor). The principle feature of this structure is the AlGaN/GaN heterojunction. At the interface between these two layers, a layer of high-mobility electrons called “two-dimensional electron gas” (2DEG) forms as a result of the crystal polarity, and is also augmented by piezoelectric crystal strain due to the lattice mismatch between AlGaN and GaN. The 2DEG forms a native channel between the source and drain of the device.

Figure 1. Basic structure of depletion-mode lateral GaN HEMTs



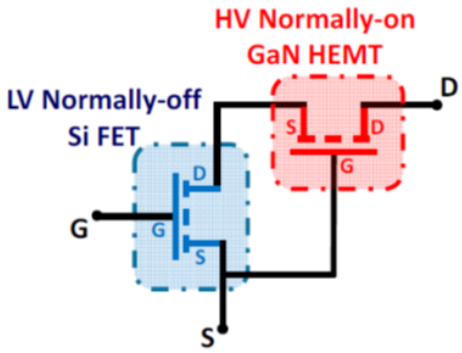
The substrate is typically Si, but other materials such as SiC, sapphire, and diamond can be used. To deposit the GaN layer on the substrate, a buffer layer must be deposited that provides strain relief between the GaN and the foreign material. This buffer often includes several thin layers of GaN, AlGaN, and AlN.

Because of the native 2DEG channel, the HEMT is inherently a depletion-mode (normally-on) device. This is not desirable for voltage-source converters, because of the potential for shoot-through during startup or loss of control power. Several methods have therefore been used to fabricate normally-off GaN HFETs.

1.2 Cascode HEMTs

A normally-off GaN device can be made with the so-called “cascode” configuration, consisting in the series connection of a low voltage silicon MOSFET with a high voltage normally-ON GaN HEMT.

Figure 2. Basic structure of cascode HEMTs



A cascode device requires co-packaging of the depletion-mode HEMT with a low-voltage enhancement-mode MOSFET. The two dies are connected in such a way that the output (drain-source) voltage of the MOSFET determines the input (gate-source) voltage of the HEMT. Both devices share the same channel current while on, and the blocking voltage is distributed between them while off.

When a positive gate-source voltage, higher than the threshold voltage, is applied to the low voltage silicon device, the normally-ON GaN HEMT gate voltage is close to zero and the device is turned on. Hence, the current can flow through the series of the normally-ON GaN and the low voltage Si MOSFET, as both are in on state. Vice versa, if the Si device is turned off, an applied bias to the drain terminal will generate a negative voltage between gate and source of the GaN HEMT. So, any further increase of the applied drain voltage will be sustained by the GaN HEMT. The two dies are connected inside the package with wire bonding or in a planar architecture.

One of the main advantages for cascode solution is the simple driving circuit needed to turn on and off the device: in fact, common MOSFET drivers can be used to switch on and off the low voltage Si device. Moreover, cascode configuration has higher gate drive safety margin: in fact, the difference between the gate-source absolute maximum ratings and the typical gate driving voltage is quite large to ensure good ruggedness against spurious glitches. Finally, as the threshold voltage is in the range of 3 V- 4 V, there is no need for negative off voltage to improve device immunity against gate drive noise.

The first major drawback of cascode is the increased package complexity, due to the series connection GaN-Si devices. Then, the switching performance of the cascode device relies heavily on the parasitic inductances in the package, especially between the two dies, and on how well the junction capacitances of the two are matched. If the inductances are too high, or the capacitances are not well matched, the switching losses can increase significantly. Another drawback is the limited breakdown range covered by this technology: the lower is the targeted breakdown, the higher is the GaN contribution on the overall RDSon. So, cascode configuration is effective only for breakdown voltages higher than 300V.

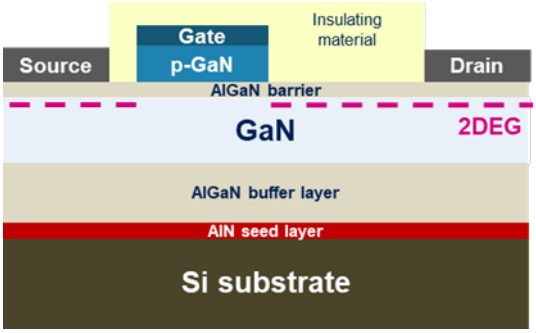
STMicroelectronics will include cascode GaN devices (G-FET) in its product portfolio.

1.3 Enhancement-mode HEMTs

Although the 2DEG makes the lateral HFET natively depletion-mode, the gate can be modified to shift the threshold voltage positively and thereby make an enhancement-mode (or E-mode) device.

There are many techniques used to deplete the 2DEG carriers beneath the gate when no voltage is applied. A positive voltage above the threshold is then required to enhance this depleted 2DEG beneath the gate and complete the channel.

Figure 3. Basic structure of enhancement-mode lateral GaN HEMTs, p-GaN gate structure

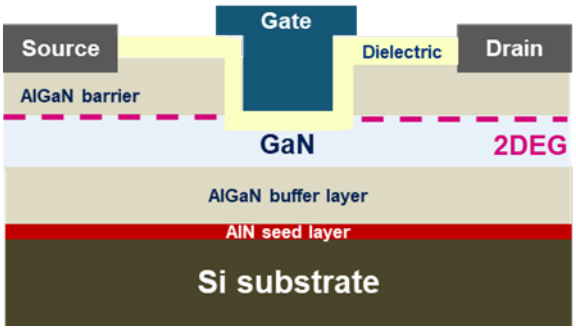


STMicroelectronics uses a p-doped layer of GaN beneath the gate (**p-GaN gate**) as shown in Figure 3. Basic structure of enhancement-mode lateral GaN HEMTs, p-GaN gate structure, which creates a diode-like characteristic on the gate that shifts the threshold up by the magnitude of the diode voltage drop. P-GaN approach is probably the most common normally-OFF HEMT solution in the semiconductor market. The main advantages of the p-GaN gate structure are low resistance under the gate and the absence of dielectric issues, while, as drawbacks, the trapping effect due to the p-GaN dopant and the limited positive gate voltage swing can be mentioned.

G-HEMT is the name of p-GaN gate HEMT series that STMicroelectronics has actually under development.

Recessed gate (Figure 4. Basic structure of enhancement-mode lateral GaN HEMTs, recessed gate structure) is another gate structure needed to build a normally-OFF device. It is less popular among GaN suppliers, but interesting R&D progress and enhancements have been reached in the latest years. The most important benefits of the recessed gate are the higher gate breakdown (≈ 9 V) and lower gate leakage current, because of the presence of the gate dielectric.

Figure 4. Basic structure of enhancement-mode lateral GaN HEMTs, recessed gate structure



Larger series resistance of the recessed gate below the gate region is one of the major drawbacks of this approach: in fact, comparing with a comparable p-GaN device, recessed gate one has lower output current. Furthermore, gate channel resistance makes recessed gate structure not suitable for low voltage application.

2 GaN drive circuits: main characteristics

For all the power devices, the right gate drive circuit choice and its proper design are mandatory to achieve the best performance and enhance the overall systems. Considering a GaN HEMT, this design step is somewhat tricky, as some electrical parameters are more critical for GaN technology. There is good literature on understanding the driving requirements for GaN HEMTs and designing novel gate drives for these devices, but most of them are focused on certain aspects of GaN drive issues and do not always cater to the commercial feasibility of these drives.

The right selection and combination of layout, driver choice, external components are the main keys for a successful design and high-performance application (next figure).

Some of the below aspects are of course less crucial for Si devices (i.e. V_{GS} off-voltage, V_{GS} maximum ratings).

Figure 5. Key factors for GaN driving

Both e-mode and cascode GaN devices are controlled by supplying or removing the voltage bias from the gate electrode. Gate drive design for cascode device is identical to the Si devices and it is not the focus of this application note. However, driving e-mode devices is more complex and needs special considerations. Main issues of driving high speed e-mode GaN devices are:

- Low threshold voltage (V_{th}): the device Is more sensitive to spurious gate bouncing.
- Very small margin of allowable gate voltage: gate signal must be as clean as possible to avoid any overvoltage or spike exceeding the absolute maximum ratings.
- dv/dt and di/dt constraints: as GaN HEMTs are very fast devices, high dV/dt and dI/dt can affect seriously the device switching behavior.
- Layout considerations: due to the previous statements (gate voltage ratings and fast switching speed), the layout optimization is a fundamental step for GaN devices.

In the next chapters, we will analyze the following aspects:

1. V_{GS} maximum ratings
2. Parasitic inductances, layout, and driver placement

3. High dV/dt and spurious turn-on
   a. External gate resistance selection
   b. Negative V_{GS} off voltage ($V_{GS, OFF}$)

trying to define some guidelines for a robust and effective gate driving circuit.

To better understand the above-mentioned aspects, dedicated pSpice simulations on a single-phase synchronous buck converter are performed (Figure 6. Buck converter schematic); the impact of each circuit parameter is hence deeply analyzed through simulation results.

Figure 6. Buck converter schematic

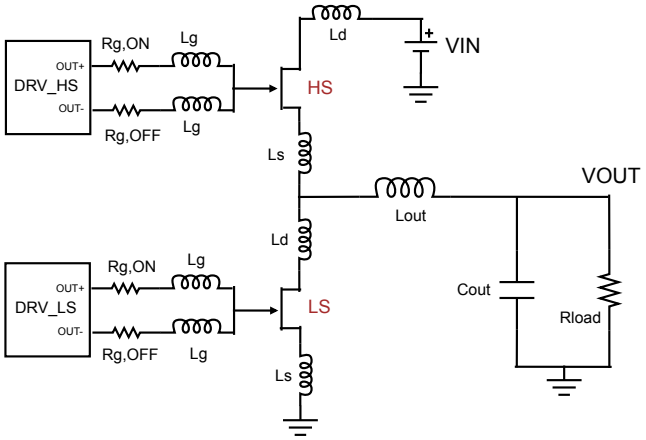


Table 3. Schematic parameters

Parameter	Value
V_{in}	400 V
V_{out}	200 V
I_{out}	10 A
f_{sw}	300 kHz

In this circuit, L_s is the source inductance, L_d is the drain inductance while L_g is the gate inductance.

2.1 VGS maximum ratings

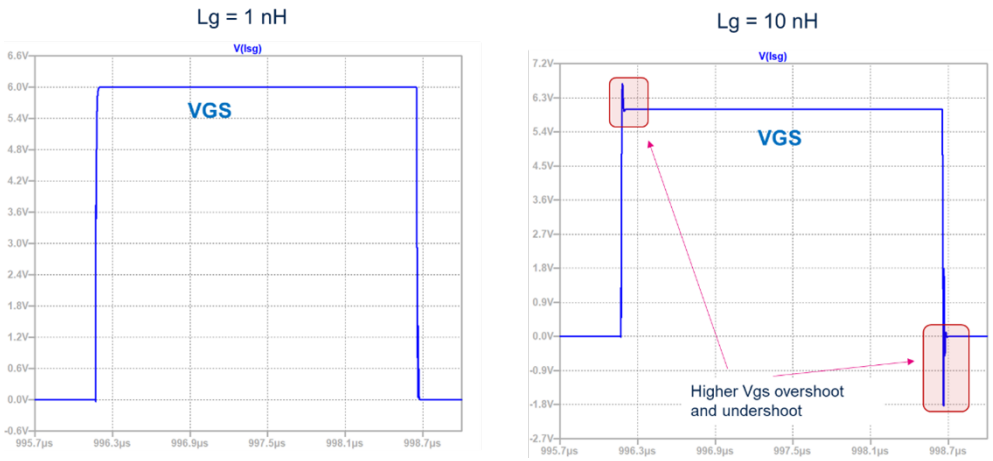
For enhancement-mode devices, the maximum allowable Gate to Source voltage (V_{GS}, max) is normally 5 V or 6 V but the devices require 4 to 5 Volts to be fully turned on, resulting in a very narrow margin. Vice versa, Si MOSFETs have much higher V_{GS} absolute maximum ratings (20 V). Useless to say, the Cascode GaN have higher VGS ratings, because of it has a low voltage Si FET as input FET.

The threshold voltage, $V_{GS(th)}$ of GaN HEMT device is very low, (from 1 to 2 V), increasing the device sensitivity to undesired switch-on when it is used in high dV/dt applications.

The gate drive design for GaN HEMT is therefore quite awkward, due to the low V_{GS} margin and low $V_{GS(th)}$. The gate-source driving signal must be very clean, without any overvoltage or undesired ringing exceeding gate maximum ratings. These requirements can be achieved in different ways:

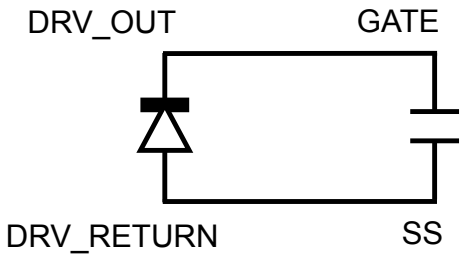
- **Very stable driver supply voltage** (i.e LDO regulator)
- **Miller effect and spurious gate noise must be avoided**
  – Design optimization to reduce gate inductance (L_g): driver must be placed as close as possible to power GaN device (next figure)

Figure 7. Overvoltage and undervoltage generated by L_g (gate inductance)



- **Simple overvoltage clamp circuit** (Zener diode and/or ceramic capacitors) helps to cut potential risky spikes (next figure)

Figure 8. Overvoltage clamping circuit



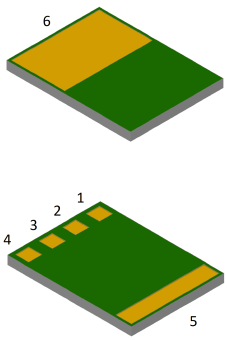
2.2 Parasitic inductances, layout and driver placement

Because GaN devices are capable of very fast switching, thanks to lower intrinsic capacitances, the parasitic inductances associated with the package and pcb, are extremely important. In certain cases, they can severely limit the device performance.

The package for a PowerGaN (see Figure 9. 2SPAK package silhouette) device must combine very low parasitic inductances with an excellent thermal behavior (Section 2.2). If by thermal point of view, the reason is quite simple to be understood, let us add more details on the main effect of parasitic inductances:

- Power losses: at high frequency, power losses due to interconnections parasitic resistances and inductance are relevant
- Power ringing (L_{stray}): drain and source package inductances contribute to generating output voltage or current oscillations and consequent HF EMI disturbances
- Gate ringing: gate and source package inductances contribute to generating oscillations on the gate, with risk of false turn-on/turn-off and damage of the device

Figure 9. **2SPAK package silhouette**



2SPAK

Table 4. **2SPAK package RLC parasitic contributions**

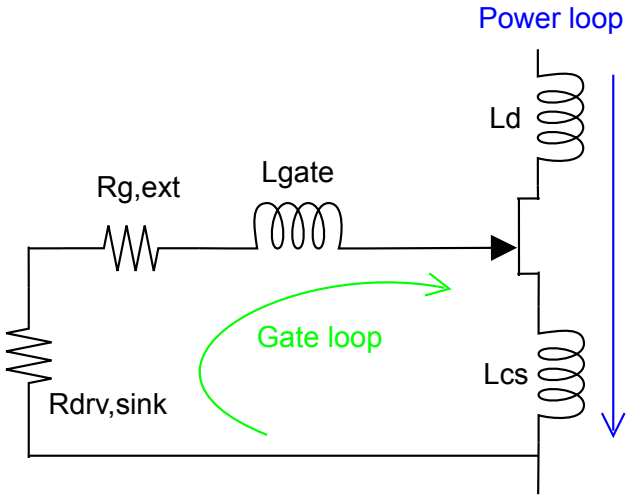
Terminal	RL DC		RL AC @1GHz		Capacitance
	R [mΩ]	L [nH]	R [mΩ]	L [nH]	C [pF]
Source	0.11	0.02	2.29	0.01	0.21
Kelvin	1.2	0.13	10.54	0.07	0.01
Drain	0.54	0.93	13.22	0.51	0.07
Gate	0.54	0.05	6.36	0.03	0.01

Among all parasitic elements, common source inductance (CSI, Lcs) is the most significant because of its effects on electrical performance. The overall CSI is the sum of the source inductance internal to the package and the lead inductance of the package itself. CSI has the potential to create ringing across the drain-to-source and gate-to-source voltage due to the presence of high di/dt in the drain-to-source circuit, resulting in increased losses and false switching. In e-GaN devices, the V_{GS} ringing can even result in breakdown of the gate, as the safety margin is limited.

Said that, to minimize parasitic inductances, SMD wire bonding free package for sub nH parasitic inductances are preferred and well used (check values on Section 2.2).

Another solution is to provide a Kelvin source connection to remove CSI from the gate loop. While this can address the false switching problem, drain-to-source ringing can still be present.

Figure 10. **Parasitic inductances: driver and power loop**



Parasitic inductances may affect GaN switching behavior, in particular (Figure 10. Parasitic inductances: driver and power loop):

- L_{cs} (common source inductance) is shared between drive loop and power loop; high dI/dt across it can produce voltage drop, affecting turn-on and turn-off time and causing unwanted ringing. Kelvin pin is very useful to improve switching behavior and clean gate-source signal from undesired ringing (following figures)

Figure 11. Impact of common source inductance @ LS turn-off with and without Kelvin Source

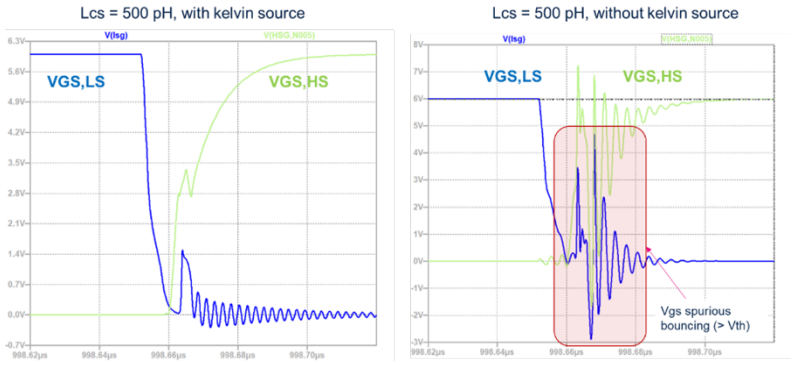
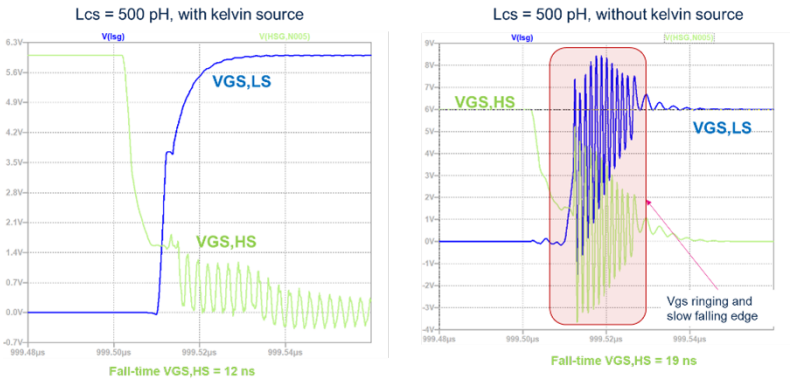
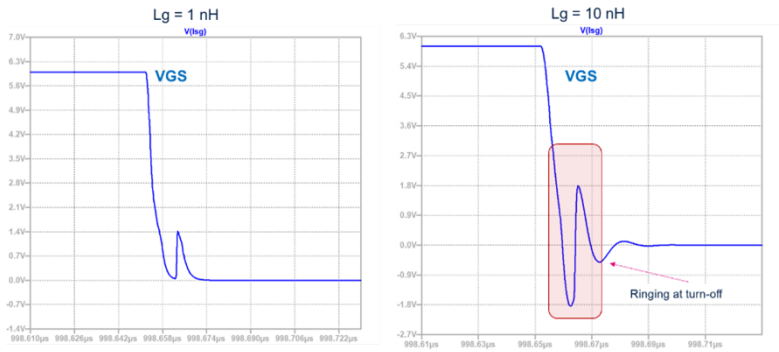


Figure 12. Impact of common source inductance @ LS turn-on with and without Kelvin Source



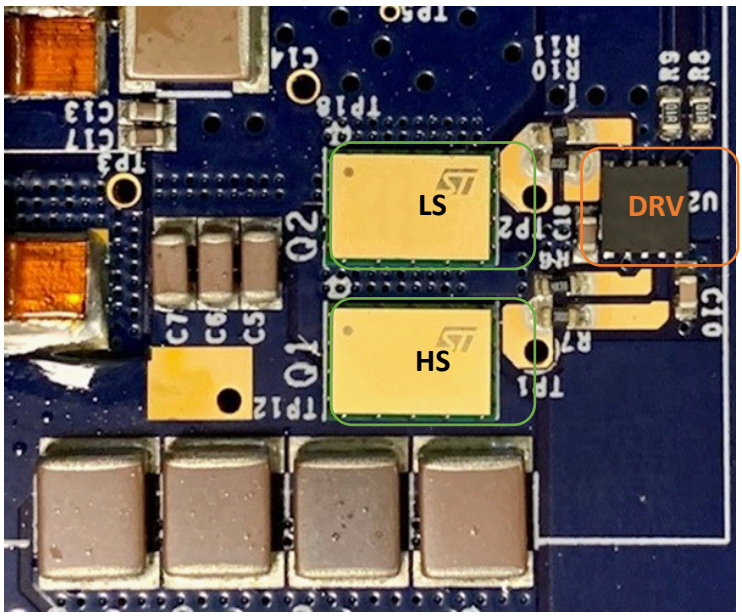
- L_g affects gate-source signal, increasing spurious ringing (next figure)

Figure 13. L_g (gate inductance) impact on gate-source voltage (V_{GS})



To minimize parasitic inductances, a well noted and used rule is to have driver, external gate resistors and power GaN device be located as close as possible.

Figure 14. **Example of driver and power GaN placement**



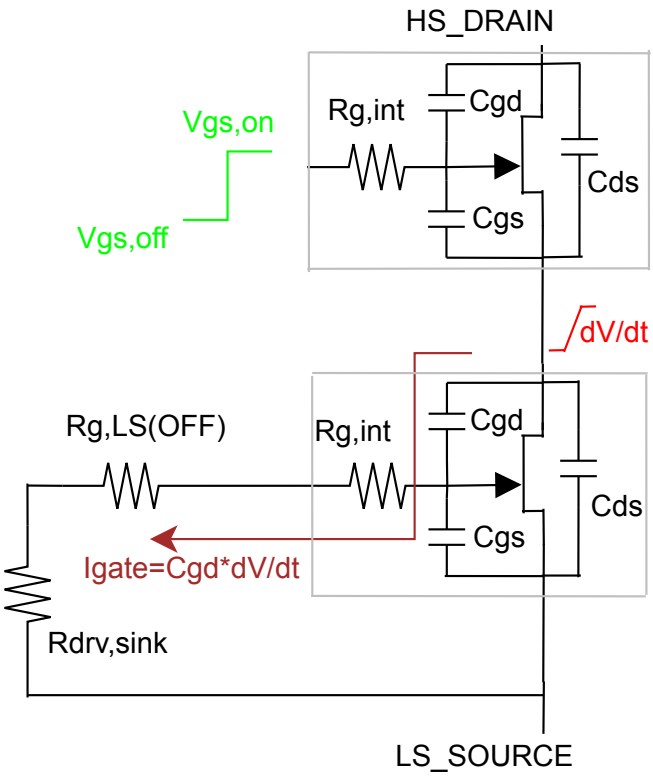
2.3 High dV/dt and spurious turn-on

Another major constraint in driving GaN high speed switches is the dV/dt effect.

The voltage slew rate (dV/dt) of power-switching devices is caused by the interaction between the various parasitic capacitances and gate-drive circuit impedances and it is determined by the charge and discharge rate of the Miller capacitance. High slew rates are typically common in bridge topologies with high voltages buses and this phenomenon is exacerbated by the high switching speed of the Gallium Nitride technology.

In bridge topologies, when the high side device is turned on (see next figure), a current is injected towards the gate by the Miller capacitance of low side switch. If the current injection into the gate is large enough to bring the gate voltage above the device threshold voltage, parasitic turn-on can be observed resulting in lower efficiency or even device failure.

Figure 15. dV/dt effect during high side turn-on

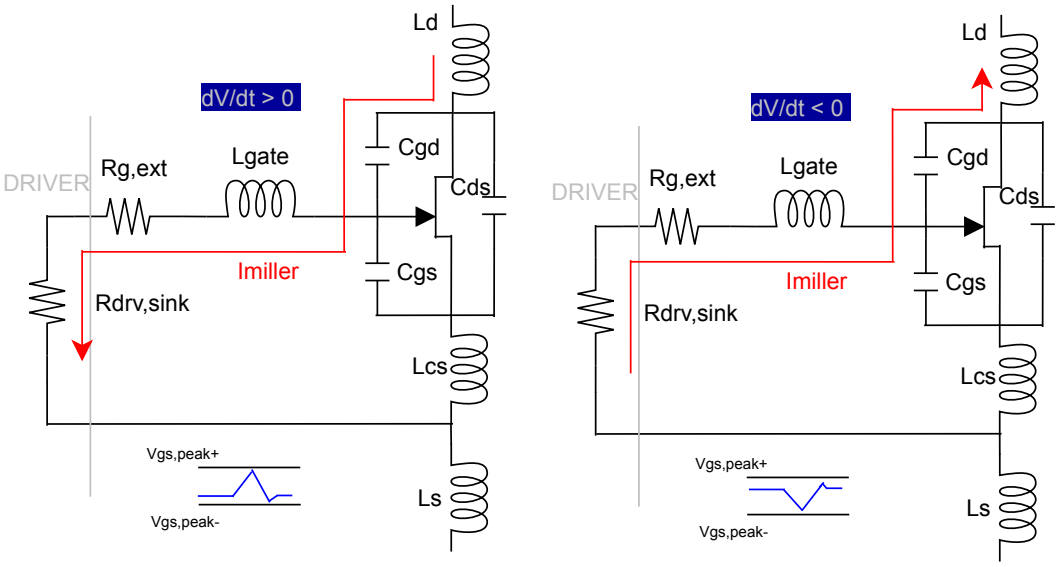


If a positive dV_{DS}/dt occurs across the low side device, the spurious voltage spike seen at device gate can be approximated as follows:

$$V_{GS,spike} = \left(R_{G,INT} + R_{G,LS(OFF)} + R_{DRV,SINK}\right) \cdot C_{GD} \cdot \frac{dV_{DS}}{dt} \quad (1)$$

Spurious voltages between gate and source can appear in both transient edges due to the applied positive or negative dV/dt on the phase node of a bridge topology.

Figure 16. **Miller effect generated by positive dV/dt (on the left) and negative dV/dt (on the right)**



The Miller effect can be mitigated by minimizing the parasitic gate loop inductance, selecting driver with low sink resistance and applying a negative bias to the gate pin. The goal of the Miller effect turn-on mitigation techniques is to keep the gate voltage below a desired threshold when a current spike through the Miller capacitance occurs.

Here below we will just highlight different strategies to improve dV/dt ruggedness:

- External gate resistor selection
- Active miller clamp
- Negative off-voltage
- Driver selection

2.3.1 External gate resistance selection

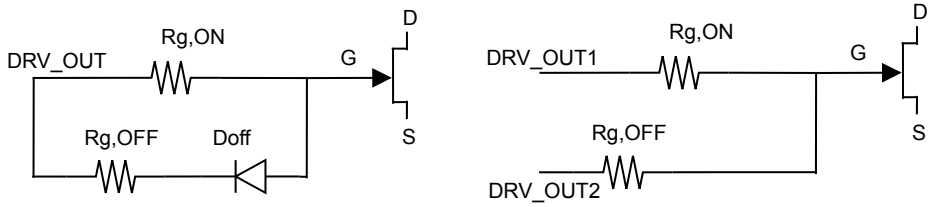
External gate resistor impacts device switching behavior (slew rate, switching losses, Miller effect, EMI).

R_g selection is a tradeoff between fast switching (low R_g) and dV/dt control (high R_g) : for instance, the value of the external gate resistors can be increased to slow down dv/dt but this can increase the switching losses. So surely an optimization of gate resistance selection is required.

Gate drive circuit should have different turn-on and off resistors, to adjust both switching edges; different paths for turn-on and off can be achieved as follows:

- Select driver with separate outputs
- Use asymmetrical driving for drivers with single output

Figure 17. **External gate resistors usage in single and 2-output driver**



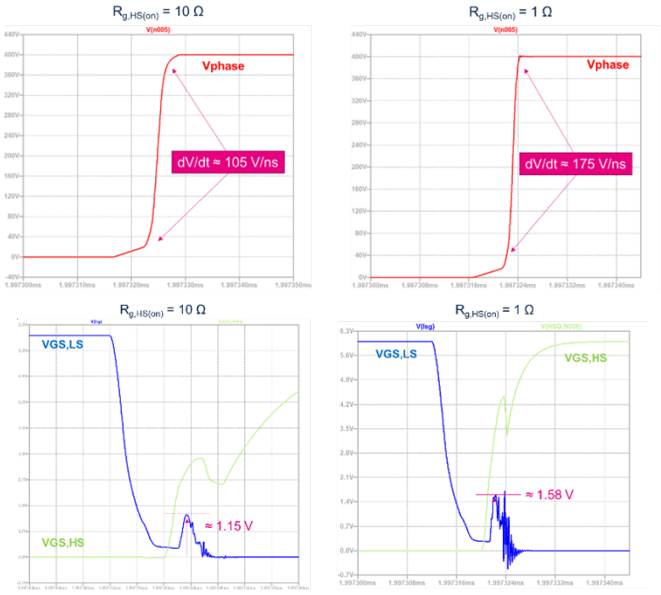
The following table shows a possible selection of turn-on and off resistors, both for high voltage and low voltage GaN HEMTs:

Table 5. External gate resistor selection

	Turn-on resistor	Turn-off resistor
HV GaN	10 Ω - 20 Ω	< 2 Ω
LV GaN	2.2 Ω – 4.7 Ω	< 1 Ω

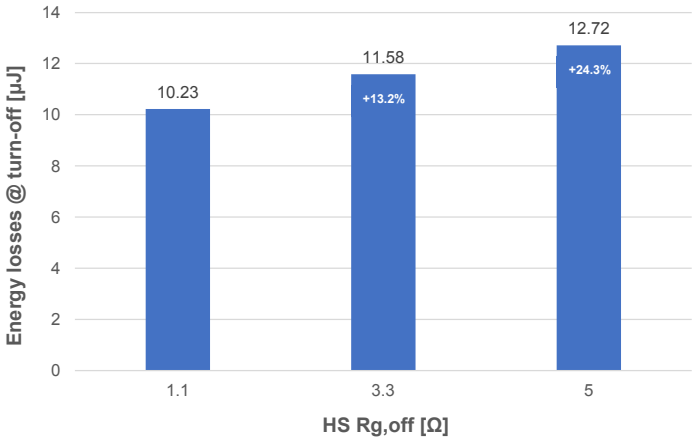
In a bridge topology, high side turn-on resistor affects the phase node slew rate (dV/dt): increasing $R_{G,\ HS(on)}$, dV/dt decreases reducing also the capacitive current and the Miller effect on low side device.

Figure 18. Impact of high side turn-on resistor on dV/dt and low side Miller effect



As previously mentioned, high side turn-off resistor should be as low as possible to reduce the switching losses.

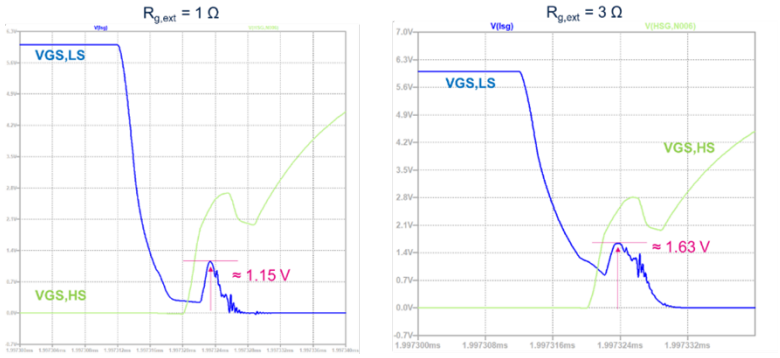
Figure 19. Impact of high side turn-off resistor on turn-off losses



Two last pictures highlight that separate outputs are mandatory to achieve the best performance with GaN HEMT, allowing dV/dt control and switching losses minimization.

Low side turn-off resistor directly impacts the device immunity to Miller effect (see Eq. (1)). As shown in the following figure, increasing the low side resistor from 1 Ω to 3 Ω (see Figure 6. Buck converter schematic), the spike level rises with higher risk of shoot-through.

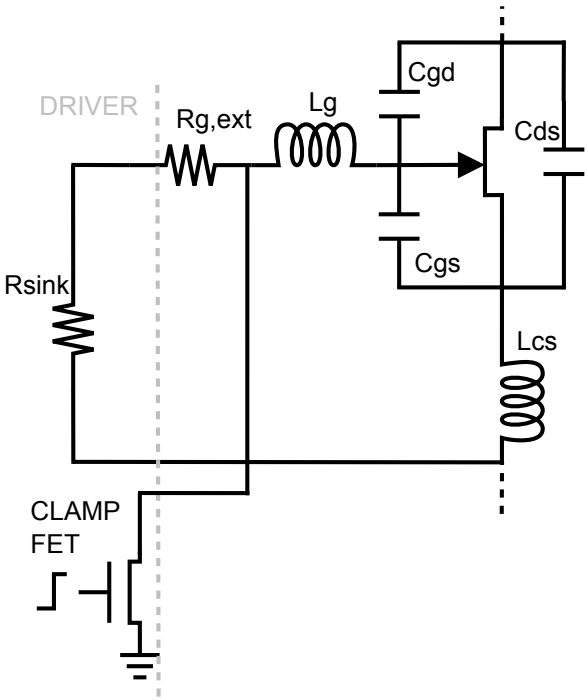
Figure 20. **Impact of low side turn-off resistor on G-S spurious bouncing**



2.3.2 Active Miller clamp

The active Miller clamp is realized by N-channel MOSFET connected between gate and source. If a high dV/dt induces Miller current through C_{gd}, this additional switch keeps the GaN HEMT totally off by shorting the gate to source path when a certain threshold is reached. It practically works supplying an additional low impedance path to further decrease the total sink resistance and it is only effective during HEMT turn-off (NMOS turns off at PWM rising edge) and does not affect HEMT turn-on.

Figure 21. **Active Miller clamp**



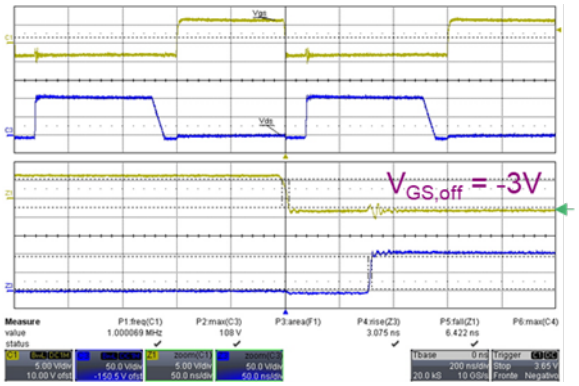
Some drivers with active Miller clamp integrated are available in the market.

2.3.3 Negative $V_{GS,off}$ voltage ($V_{GS,off}$)

Negative gate-source voltage can help to increase ruggedness against Miller effect, enlarging the safety margin between the maximum spike value and the threshold of the device ($V_{GS(th)}$). However, the negative gate bias must be properly selected, as too low values increase the risk of exceeding the negative absolute maximum ratings on the gate when negative spikes occur.

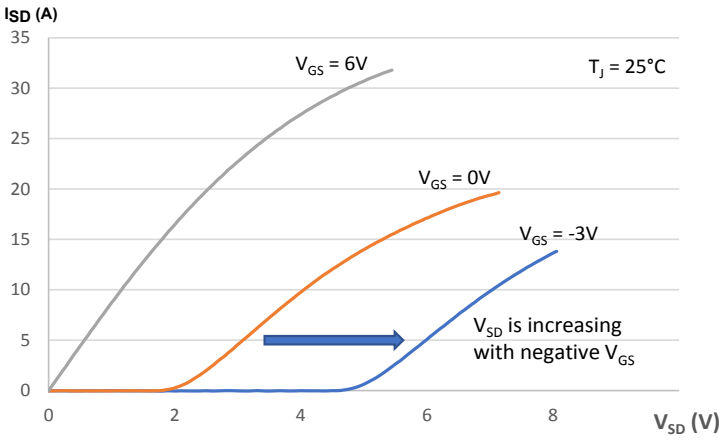
Here below you can see an example of gate driving using negative V_{GS} ($V_{GS,off}$ = -3 V).

Figure 22. Example of negative gate bias



In the next chapter we will show how a bipolar gate drive circuit is used to generate negative voltage. The major disadvantage using negative V_{GS} is the increase of reverse voltage drop across the device ($V_{SD} = V_{th} + V_{GS,off}$) and hence also the reverse conduction losses ($P_{rev} = 2*V_{SD}*I_D*t_{DEAD}$).

Figure 23. Impact of negative gate bias on V_{SD}



Next 2 figures show simulation results without negative gate bias and with V_{GS} = - 3 V.

Figure 24. V_{SD} with V_{GS} = 0 V

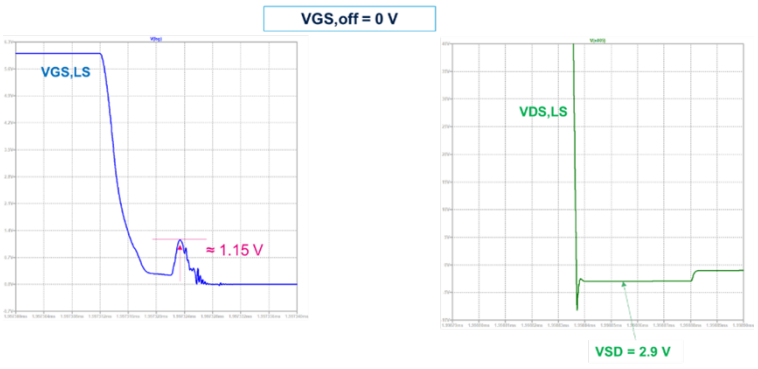
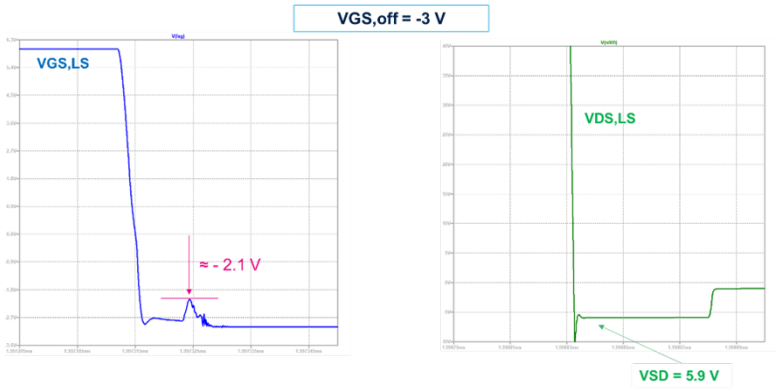


Figure 25. V_{SD} with V_{GS} = -3 V



2.3.4 Driver selection

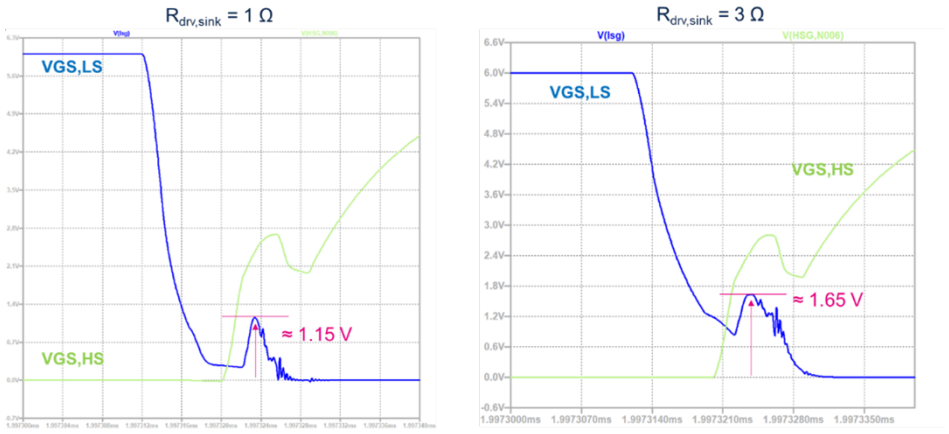
The right driver selection is another key step during drive circuit design and can help to improve the immunity to CdV/dt spurious turn-on (see Eq. (1)). As GaN HEMTs have high switching speed, the driver must be able to turn-on and off the GaN HEMT very quickly to improve the overall performance.

The main driver parameters (at least one of these parameters is always reported in the datasheet) are:

- I_{sink} (or $I_{pull-down}$), which is the sink or pull-down current (during the device turn-off)
- R_{sink} (or $R_{pull-down}$): during turn-off, R_{sink} is in series to the external gate resistor, closing the path to GND.

To reduce the Miller effect, the GaN driver should have high sink current values (today in the market, are available driver with 7 A as sink current peak) to quickly turn-off the device. Alternatively, the sink resistance should be as low as possible, because of it affects the spurious bouncing between gate and source.

Figure 26. Impact of driver sink resistance on V_{GS}



3 GaN drive circuit: different topologies

In this section, we analyze the main topologies used to create a GaN Drive circuit:

- Single supply gate drive
- Bipolar gate drive

The first one refers to an isolated gate driver operating with single positive supply voltage: the gate voltage swings from 0 V to V_{CC}.

Certain power device types even require a negative voltage to be fully off, necessitating negative voltage drive coming from the gate driver. Device manufacturers that recommend negative gate drive voltage include standard silicon MOSFETs, IGBTs, SiC, and GaN devices.

One method to overcome this lack of negative gate drive devices is to offset the gate driver from the power device, thereby creating a negative gate drive relative to the source or drain of the power device, while the gate driver IC still only sees a unipolar supply (see Figure 29. V_{CC}/-V_{CC} generation (with a 6.2 V Zener diode)).

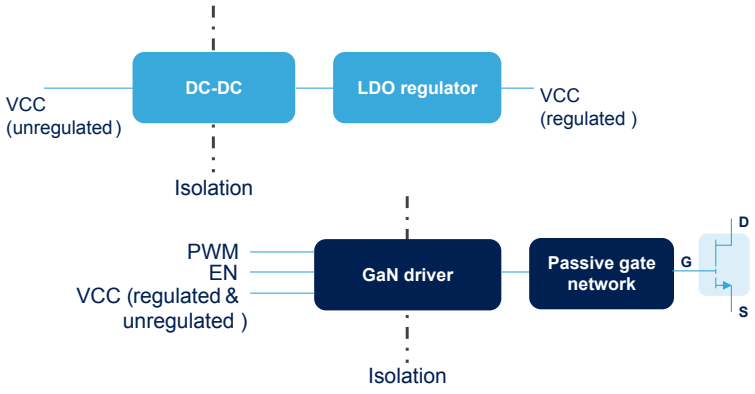
3.1 Single supply gate driving (isolated)

In the following figure, is reported a simplified block diagram of a single supply gate drive circuit, which is a simple and cost-effective solution. DC-DC converter guarantees electric isolation while low drop-out IC generates stable and regulated supply voltage (V_{CC}).

The gate voltage swings between 0 V and V_{CC}. As there is not negative gate bias, this driving solution can be used with GaN HEMTs with kelvin pin, which have higher immunity to gate noise even with 0 V as off-voltage, and suits high frequency zero-voltage switching (ZVS) application requirements.

This configuration needs optimized layout (gate loop, power loop) to limit undesired switching noise.

Figure 27. Single supply gate drive (isolated)



3.2 Bipolar gate driving (isolated)

The following figure shows the basic block diagram of a bipolar gate drive circuit for GaN. Here, the unregulated V_{CC} is converted by DC-DC block, becoming the input of a simple passive circuit needed to generate the supply voltages, V_{CC} and -V_{CC} (Figure 29. V_{CC}/-V_{CC} generation (with a 6.2 V Zener diode)).

The negative gate bias increases the circuit immunity to spurious gate bouncing and shoot-through. Consequently, it is the best configuration for hard-switching, high-power applications, when high dV/dt occurs during switching transients.

It requires more passive components than previous solution, even if there is no need of an LDO IC.

Because of negative gate voltage ($V_{GS,OFF}$) increases reverse conduction losses (power losses during dead time, see Section 2.3.3 Negative VGS,off voltage (VGS,off)), designers must choice the right dead time value for a trade-off between robust switching behavior and power losses minimization.

Figure 28. Bipolar Gate driving (isolated) example

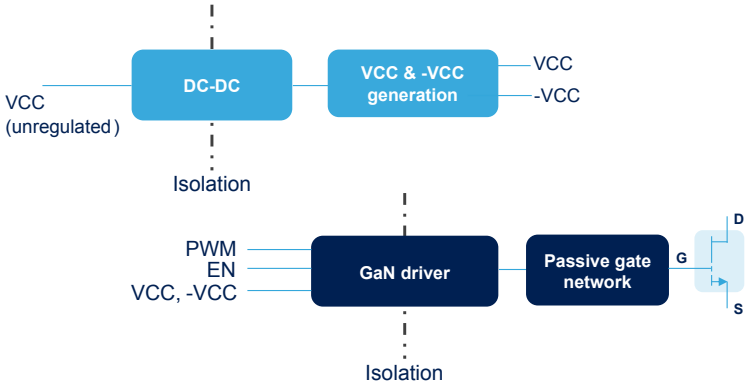
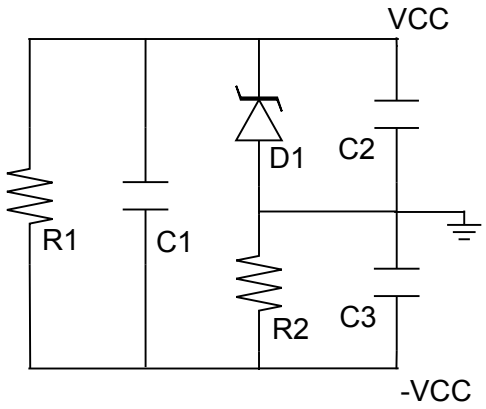


Figure 29. V_{CC}/-V_{CC} generation (with a 6.2 V Zener diode)

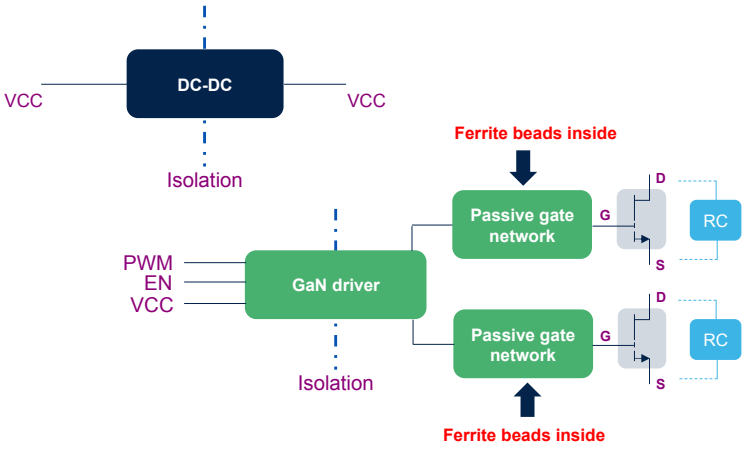


3.3 Unipolar gate driving for cascode

As already mentioned (Section 1.2 Cascode HEMTs), cascode GaN devices have much easier drive topology as a low voltage MOSFET can be switched on and off. So, common MOSFET drivers are used to drive cascode devices, because of negative gate bias is not necessary and the gate absolute maximum ratings are wider ($V_{GS,max}$ = +20 V, $V_{GS,min}$ = -20 V). The standard gate circuit is hence a cost-effective configuration, as passive components are limited and there is not additional voltage regulator.

Passive gate network includes ferrite beads to smooth gate voltage ringing and additional RC snubber circuit is often used to reduce over voltages across the device.

Figure 30. **Gate driving circuit for cascode**



3.4 GaN drive circuit: summary table

Here below a summary table of the GaN Drive different topologies we just described:

Table 6. **Gate driving circuit comparison**

	Single supply drive	Bipolar drive	Cascode
Negative drive voltage	NO	YES	NO
Immunity to cross/conduction and gate bouncing	Medium	**High**	**High**
Cost effectiveness	**High**	Medium	**High**
Sensitivity to layout parasitics	**High**	Low	Low

3.5 GaN driver: main features

There is already a wide selection on the market of gate drivers for power GaN devices. Here below there are reported the main parameters of commercial gate drivers and STM recommended value for each of them.

Table 7. Overview of main gate driver parameters

Parameter	Recommended value	Explanation
R_{sink} (R_{pull_down})	< 1.5 Ω	dV/dt ruggedness improvement (Miller effect)
I_{sink} (IOL)	> 3 A (peak)	
t_{rise}, t_{fall}	< 20 ns @ CLoad = 2 nF	Switching behavior improvement and switching losses reduction
$V_{GS,ON}$	6 V (± 2%)	
$V_{GS,OFF}$	0V / -3 V (± 2%)	• Negative $V_{GS,OFF}$ improve noise immunity • Trade-off between switching and dead-time loss
Dead-time	50 ns	Minimize third-quadrant conduction
Isolation	YES	Safety; protection of low voltage electronics/controller
Split outputs (OUT1, OUT2)	YES	Turn-on/off resistor separation without any external components
CMTI (Common mode transient immunity)	> 150 kV/µs	High CMTI means capability to withstand fast dV/dt without dangerous glitches, jitter or short-circuit (mandatory for HV GaN and HB topologies)

4 Conclusions and scope for future work

The main motivation for this work was to provide a thorough user-focused description of GaN power devices for an audience of application-focused power designers. It was deeply investigated the driving requirements of discrete HEMT devices with a particular focus on faster switching on gate driver design and some tips on board layout too.

It was quite evident that driving an HEMT device to get the advantage of this brilliant technology (better efficiency, higher power density and increased maximum frequency in power converters) is something feasible and easy just following the simple rules we here descripted and highlighted.

STM intention is to proceed actual analysis in 2 different directions: third quadrant operation of PowerGan devices and design considerations of paralleled GaN HEMT.

5 References

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[2] AN5355 “Mitigation technique of the SiC MOSFET gate voltage glitches with Miller clamp”

[3] *Performance evaluation of ST’s new HEMT GaN vs SJ Si MOSFETs in resonant converters*: Domenico Nardo, Agatino Palermo, Filadelfo Fusillo, Rosario Scollo, Simone Buonomo. (STMicroelectronics, Catania), PCIM 2020

[4] *Investigation of gate drive strategies for high voltage GaN HEMTs:* Nikita Hari, Teng Long, Edward Shelton, 2017

[5] *Review and Characterization of Gallium Nitride Power Devices: Edward Andrew Jones (Thesis)*

Revision history

Table 8. **Document revision history**

Date	Version	Changes
10-Dec-2020	1	Initial release
22-Feb-2021	2	Modified Figure 21. Active Miller clamp and Figure 29. V_{CC}/-V_{CC} generation (with a 6.2 V Zener diode).

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