Application note

Automotive 3-Phase Motor Gate Driver Unit

Introduction

L9908 is a gate driver unit (GDU) capable of controlling 6 N-channel FETs for 3-phase motors in automotive applications.

Each one of the 3 half bridge drivers channels (HS/LS couples) can be independently configured allowing different load driving and is able to withstand -14 V to 95 V excursion on motor`s pins.

Through 6 dedicated parallel inputs, the pre-driver stages can be controlled independently supporting duty cycle operations from 0% to 100% and allowing to implement all kinds of electric motor control strategy.

A dedicated combination of regulators, charge pumps and bootstrap circuits allows L9908 to be suitable to operate in single/ double (12 V/24 V) or high supply (48 V) voltage systems.

Safe operation of half bridges is ensured by shoot-through diagnosis, dead-time, short to battery, short to ground and open load detection plus a real time phase voltage monitoring.

L9908 is equipped with 3 independent high accuracy current monitor channels with SPI-configurable gain and offset for ground referenced current measurements.

Current monitors can also be used in synergy with a microcontroller, to develop a precise phase over-current monitoring and protecting.

L9908 implements diagnostics on external and internal supply, ground level, internal temperature.

A 32-bit out of frame SPI-slave interface is implemented for communication up to 10 MHz between L9908 and µC. SPI communication is safe-guarded by 5-bit CRC, 1bit frame counter, frame length check and an SPI-configurable Window Watchdog.

1 Application circuit

Figure 1. **Application circuit, 12 V/24 V systems**

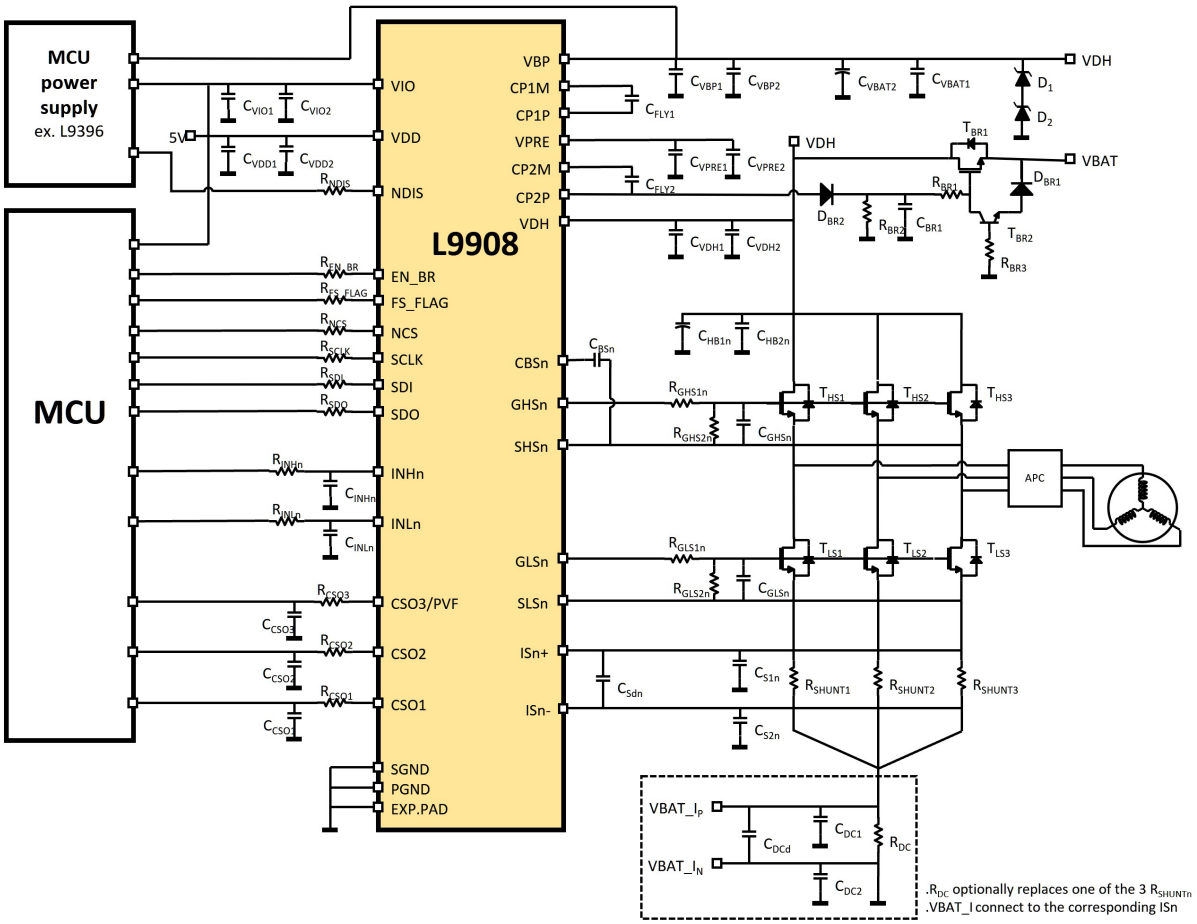


Figure 2. **Application circuit, 48 V systems**

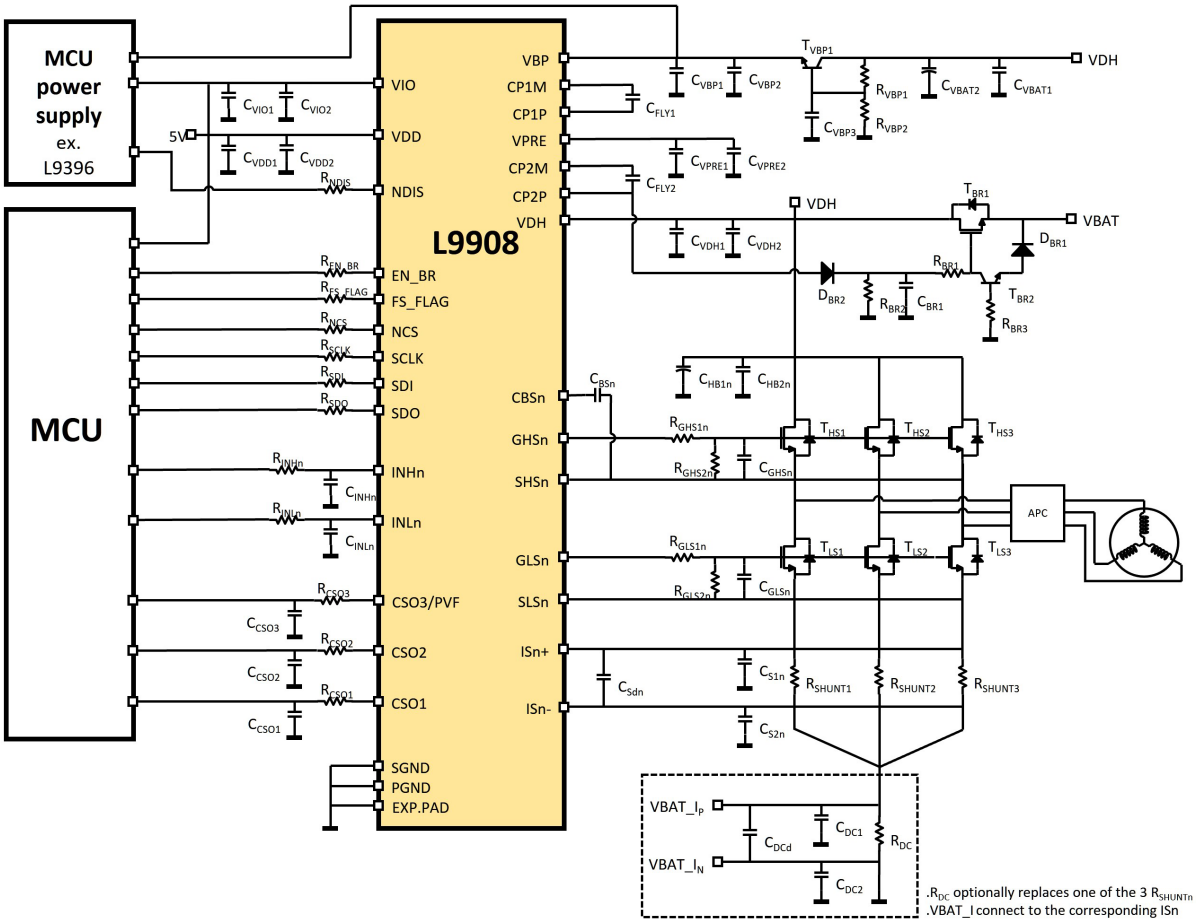


Table 1. Bill of material

Component	Min	Typ	Max	Unit	Minimum requirement			Comment
					12 V systems	24 V systems	48 V systems	
C_{BR1}	-	390	-	nF	50 V	100 V		-
C_{BSn}	-	1	-	µF	25 V			-
C_{CSO1}	-	220	-	pF	6.3 V			With $R_{CSO1,2,3}$, is mandatory for CSO signal stability
C_{CSO2}	-	220	-	pF	6.3 V			
C_{CSO3}	-	220	-	pF	6.3 V			
C_{DC1}	-	10	-	nF	6.3 V			Max tolerance ± 5% to be mounted close to R_{DC}
C_{DC2}	-	10	-	nF	6.3 V			Max tolerance ± 5% to be mounted close to R_{DC}
C_{DCd}	-	220	-	nF	6.3 V			To be mounted close to pin
C_{FLY1}	-	1	-	µF	50 V	100 V		-
C_{FLY2}	-	1	-	µF	50 V	100 V		-
C_{GHSn}	-	-	-	-	16 V			Optional
C_{GLSn}	-	-	-	-	16 V			Optional
C_{HB1n}	-	100	-	nF	50 V	100 V		-
C_{HB2n}	-	220	-	µF	50 V	100 V		-
C_{INHn}	-	10	-	pF	6.3 V			Optional
C_{INLn}	-	10	-	pF	6.3 V			Optional
C_{S1n}	-	10	-	nF	6.3 V			Max tolerance ± 5% to be mounted close to R_{SHUNTn}
C_{S2n}	-	10	-	nF	6.3 V			Max tolerance ± 5% to be mounted close to R_{SHUNTn}
C_{Sdn}	-	220	-	nF	6.3 V			To be mounted close to pin
C_{VBAT1}	-	100	-	nF	50 V	100 V		-
C_{VBAT2}	-	10	-	µF	50 V	100 V		-
C_{VBP1}	-	1	-	µF	50 V	100 V	16 V	-
C_{VBP2}	-	100	-	nF	50 V	100 V	16 V	To be mounted close to pin
C_{VBP3}	-	100	-	nF	n.a.		50 V	-
C_{VDD1}	-	1	-	µF	6.3 V			-
C_{VDD2}	-	100	-	nF	6.3 V			To be mounted close to pin
C_{VDH1}	-	100	-	nF	50 V	100 V		To be mounted close to pin
C_{VDH2}	-	1	-	µF	50 V	100 V		-
C_{VIO1}	-	1	-	µF	6.3 V			-
C_{VIO2}	-	100	-	nF	6.3 V			To be mounted close to pin
C_{VPRE1}	-	4.7	6.8	µF	16 V			Max tolerance: ± 20%
C_{VPRE2}	-	100	-	nF	16 V			To be mounted close to pin
D_1	-	-	-	-	SMA6T39AY	SMA6T56AY	n.a.	-
D_2	-	-	-	-	short	SMA6T6V7AY		-

Component	Min	Typ	Max	Unit	Minimum requirement			Comment
					12 V systems	24 V systems	48 V systems	
D_{BR1}	-	-	-	-	STPS3L60			-
D_{BR2}	-	-	-	-	STPS0520Z			-
R_{VBP1}	-	22	-	kΩ	-			-
R_{VBP2}	-	22	-	kΩ	-			-
R_{BR1}	-	1	-	kΩ	-			-
R_{BR2}	-	39	-	kΩ	-			-
R_{BR3}	-	22	-	kΩ	-			-
R_{CSO1}	-	1	-	kΩ	-			With $C_{CSO1,2,3}$, is mandatory for CSO signal stability
R_{CSO2}	-	1	-	kΩ	-			
R_{CSO3}	-	1	-	kΩ	-			
R_{DC}	-	4	-	mΩ	WSL10204L000FEA			-
R_{EN_BR}	-	100	-	Ω	-			Optional
R_{FS_FLAG}	-	100	-	Ω	-			Optional
R_{GHS1n}	-	47	-	Ω	-			-
R_{GHS2n}	-	100	-	kΩ	-			-
R_{GLS1n}	-	47	-	Ω	-			-
R_{GLS2n}	-	100	-	kΩ	-			-
R_{INHn}	-	100	-	Ω	-			Optional
R_{INLn}	-	100	-	Ω	-			Optional
R_{NCS}	-	100	-	Ω	-			Optional
R_{NDIS}	-	100	-	Ω	-			Optional
R_{SCLK}	-	100	-	Ω	-			Optional
R_{SDI}	-	100	-	Ω	-			Optional
R_{SDO}	-	100	-	Ω	-			Optional
R_{SHUNTn}	-	4	-	mΩ	WSL10204L000FEA			-
T_{BR1}	-	-	-	-	STL225N6F7AG	STH275N8F7		-
T_{BR2}	-	-	-	-	BCP56-16			-
T_{VBP1}	-	-	-	-	BCP56-16			-
T_{HSn}	-	-	-	-	STL225N6F7AG	STD105N10F7AG		-
T_{LSn}	-	-	-	-	STL225N6F7AG	STD105N10F7AG		-

2 Block diagram and pin description

Figure 3. **Block diagram**

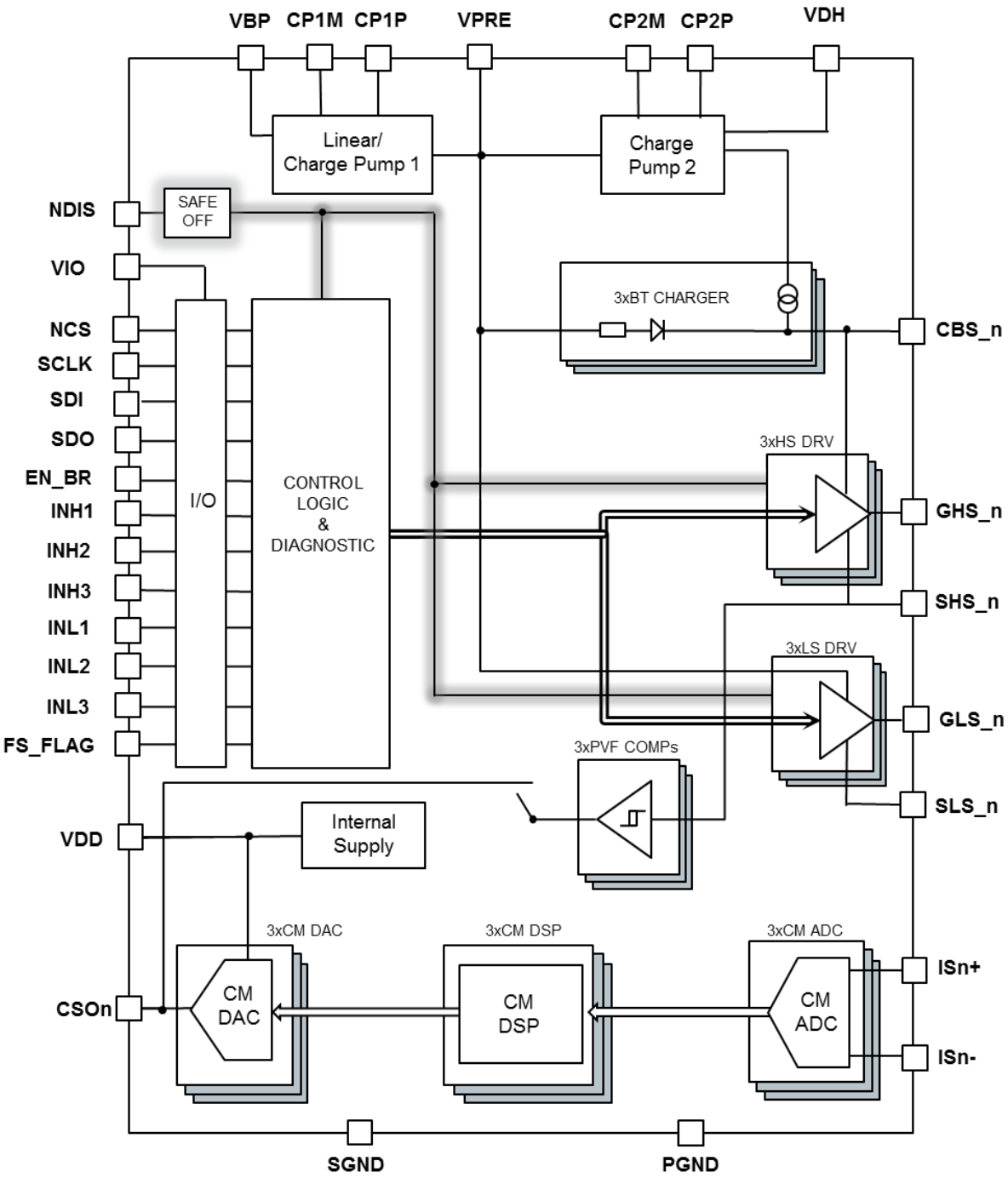
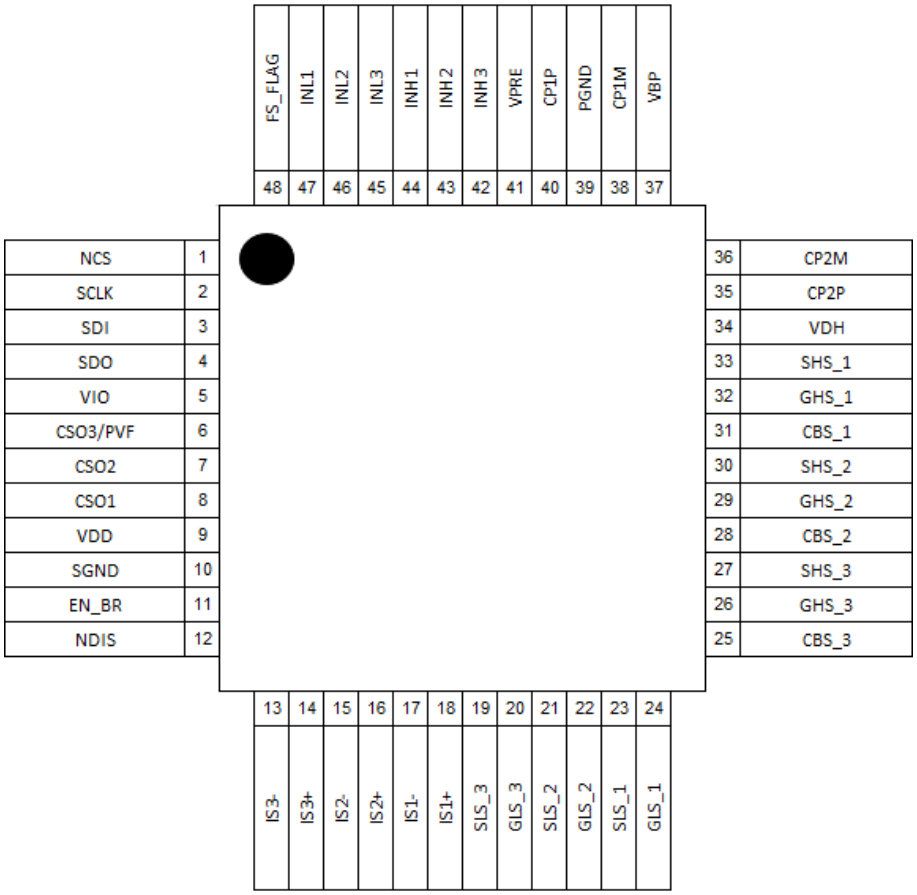


Figure 4. **Pin connection diagram (top view)**



Legenda: I = Input, O = Output, P = Power Supply, G = Ground, I/O = Input/Output

Table 2. **Pin list description**

Pin #	Pin name	Description	Pin type	Class
1	NCS	SPI Chip Select Input (Active LOW)	I	Local
2	SCLK	SPI Serial Clock Input	I	Local
3	SDI	SPI Serial Data Input	I	Local
4	SDO	SPI Serial Data Output	O	Local
5	VIO	Power supply for digital output	P	Local
6	CSO3/PVM	Current monitor 3 analog output. Phase voltage feedback output	O	Local
7	CSO2	Current monitor 2 analog output	O	Local
8	CSO1	Current monitor 1 analog output	O	Local
9	VDD	Power supply input for internal circuitry and current monitors analog output (CSOn)	P	Local
10	SGND	Signal Ground (Analog, Digital, Reference)	G	Local
11	EN_BR	Bridge Enable Input (Active HIGH)	I	Local
12	NDIS	Safe switch-off activation Input (Active LOW)	I	Local
13	IS3-	Current monitor 3 negative input	I	Local
14	IS3+	Current monitor 3 positive input	I	Local

Pin #	Pin name	Description	Pin type	Class
15	IS2-	Current monitor 2 negative input	I	Local
16	IS2+	Current monitor 2 positive input	I	Local
17	IS1-	Current monitor 1 negative input	I	Local
18	IS1+	Current monitor 1 positive input	I	Local
19	SLS_3	Source connection of LS FET, phase 3	I/O	Local
20	GLS_3	Gate connection of LS FET, phase 3	I/O	Local
21	SLS_2	Source connection of LS FET, phase 2	I/O	Local
22	GLS_2	Gate connection of LS FET, phase 2	I/O	Local
23	SLS_1	Source connection of LS FET, phase 1	I/O	Local
24	GLS_1	Gate connection of LS FET, phase 1	I/O	Local
25	CBS_3	Bootstrap capacitor of HS, phase 3	I/O	Local
26	GHS_3	Gate connection of HS FET, phase 3	I/O	Local
27	SHS_3	Source connection of HS FET, phase 3	I/O	Global
28	CBS_2	Bootstrap capacitor of HS, phase 2	I/O	Local
29	GHS_2	Gate connection of HS FET, phase 2	I/O	Local
30	SHS_2	Source connection of HS FET, phase 2	I/O	Global
31	CBS_1	Bootstrap capacitor of HS, phase 1	I/O	Local
32	GHS_1	Gate connection of HS FET, phase 1	I/O	Local
33	SHS_1	Source connection of HS FET, phase 1	I/O	Global
34	VDH	Drain connection of HS FETs	P	Global
35	CP2P	Charge Pump 2 positive input of fly capacitance	I/O	Local
36	CP2M	Charge Pump 2 negative input of fly capacitance	I/O	Local
37	VBP	Pre-regulation stage power supply	P	Global
38	CP1M	Charge Pump 1 negative input of fly capacitance	I/O	Local
39	PGND	Power Ground (Charge Pump 1 and 2)	G	Local
40	CP1P	Charge Pump 1 positive input of fly capacitance	I/O	Local
41	VPRE	Pre-regulated voltage for HS/LS Vgs driving	I/O	Local
42	INH3	PWM command for HS, phase 3 (Active HIGH)	I	Local
43	INH2	PWM command for HS, phase 2 (Active HIGH)	I	Local
44	INH1	PWM command for HS, phase 1 (Active HIGH)	I	Local
45	INL3	PWM command for LS, phase 3 (Active HIGH)	I	Local
46	INL2	PWM command for LS, phase 2 (Active HIGH)	I	Local
47	INL1	PWM command for LS, phase 1 (Active HIGH)	I	Local
48	FS_FLAG	Fault status flag output (Active LOW)	O	Local
-	Exp. PAD	Cooling pad not electrically connected. Connect to GND plane on PCB	-	-

3 Evaluation system

L9908 evaluation system is a complete hardware/software system designed to evaluate 3-phase motor control application by using L9908 gate driver. The system is made of the L9908 Evaluation Board, and it works with 12 V, 24 V and 48 V battery applications.

The custom pin strip allows the connection of the board to any microcontroller board via simple jumper cable to speed up the system evaluation. When the L9908 Evaluation board is used with SPC570-DISP MCU evaluation board, a dedicated GUI is available as a ready software environment to fully control L9908.

Figure 5. L9908 application board overview

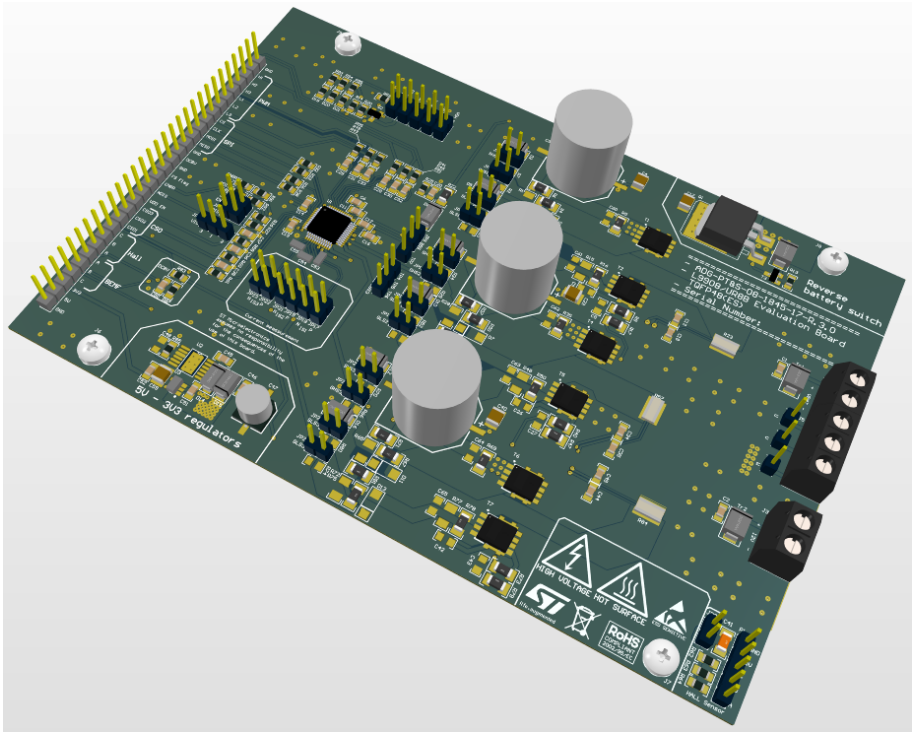
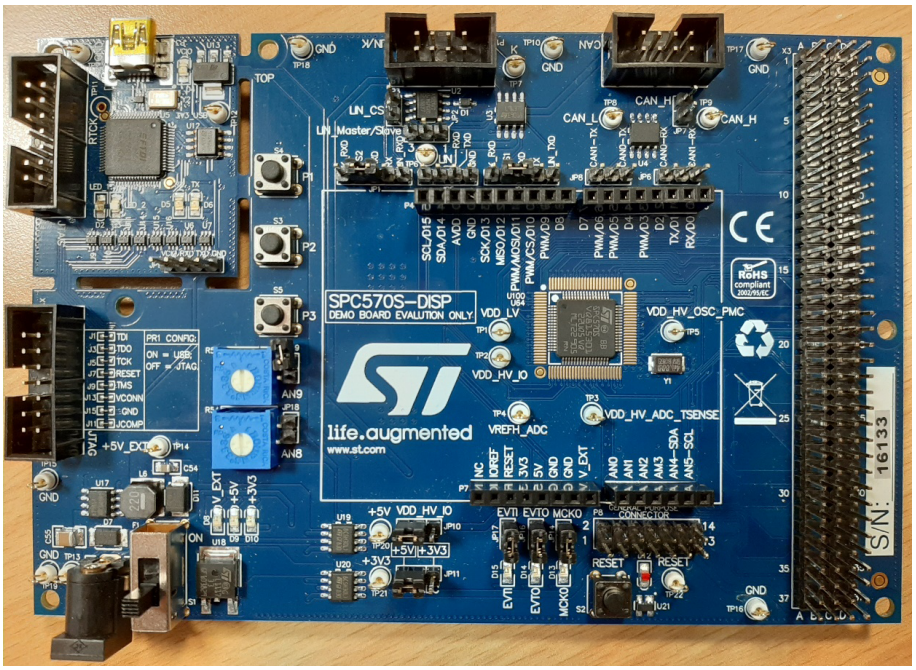


Figure 6. **SPC570S microcontroller board**



4 Layout suggestions

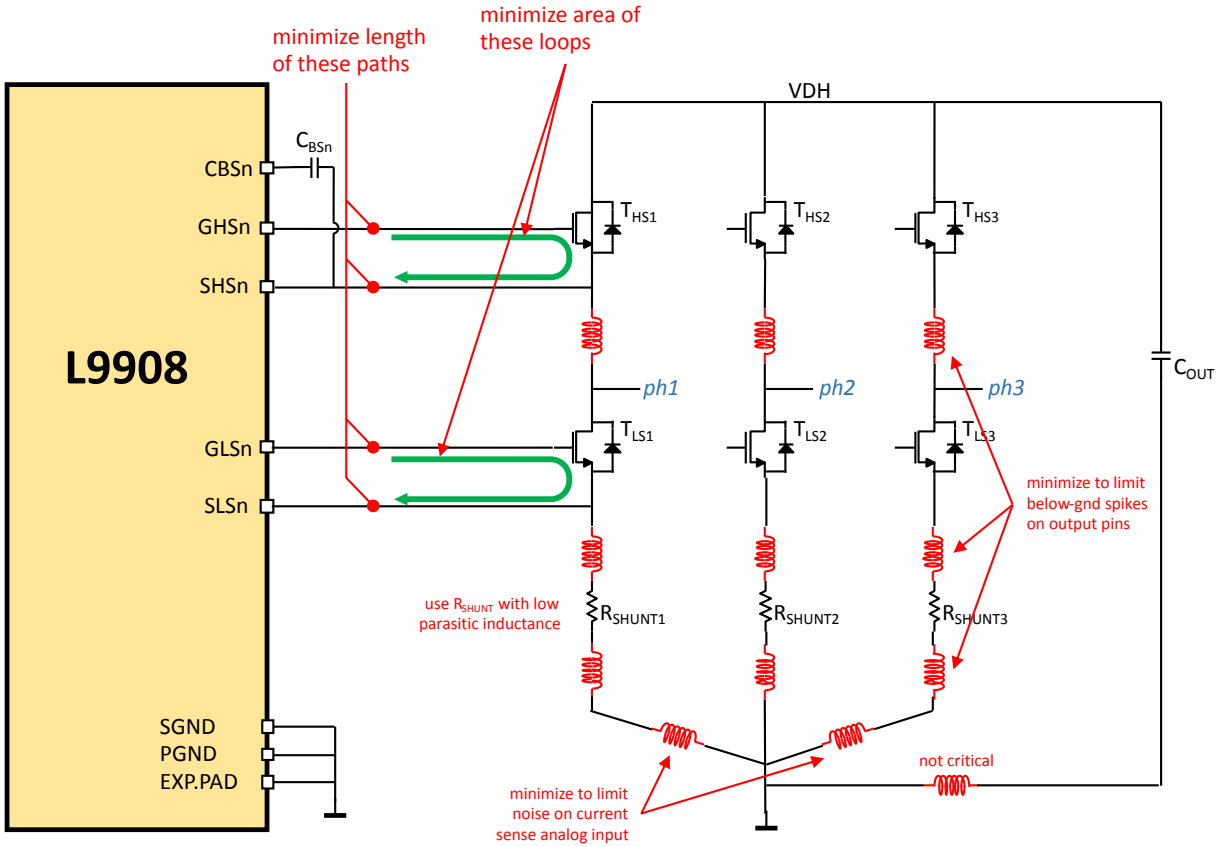
Typically, for power applications using high voltages and large load currents, the board layout of all circuits related to the power stage is important. Board layout includes several aspects, such as track dimensions (length and width), circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements and power sources in the PCB area. The reasons to pay particular attention to the PCB layout are:

- EMI issues (both induced and perceived by the application);
- over-voltage spikes due to parasitic inductances along the PCB traces;
- proper connection of sense blocks, logic inputs and analog outputs of the device.

In fact, L9908 IC not only has the function to drive the power stage, but also embeds analog sensing blocks such as comparators and op-amps. For example, especially regarding multi-phase power stages, it is important to keep the current reading from ground noise.

Figure 7 shows a simplified version of application diagram, with some layout guidelines and suggestions.

Figure 7. Layout suggestions for a 3-phase system



Gate driving PCB traces should be designed to be as short as possible, and the area of the loop formed by the gate line and its return line should be minimized to avoid the sensitivity of such structures to the surrounding noise. Typically, a good power system layout keeps the power MOSFETs of each half-bridge as close as possible to the related gate driver.

In Figure 7 a set of parasitic inductances related to the different circuit tracks is shown. The various groups of inductances may have undesired effects which should be limited as much as possible. Moreover, note that Figure 7 emphasizes parasitic inductances located on the lines usually managing high voltages and fast current transitions, which are very noisy analog signals. In fact, each phase of the bridge causes high currents (with high dI/dt) to flow on these paths, resulting in voltage noise which drops between the gate driver ground and the controller ground. This noise is directly added to all logic and analog voltage signals between the gate driver and the microcontroller, included the input logic signals and the analog output of the related gate driver. It is recommended to minimize this noise by reducing the distance between the signal ground and the driver ground (for each gate driver in the system) as much as possible. Generally, it is recommended to connect the signal ground to the three driver grounds through a star connection, in order to improve the balancing and symmetry of the 3-phase driving topology.

Note: it is very important to avoid any ground loop; only a single path must connect two different ground nodes.

The parasitic inductance between the negative terminal of the bulk capacitor and the signal/power ground is usually not critical; spikes on this parasitic element minimally influence other nodes of the system.

Another useful suggestion is to ensure some distance between the lines switching with high voltage transitions, and the signal lines sensitive to electrical noise. Specifically, the tracks of each phase (ph1, ph2, ph3 in Figure 7), bringing significant currents and high voltages should be separated from the logic lines and analog sensing circuits of op-amps and comparators.

5 Logic input/output

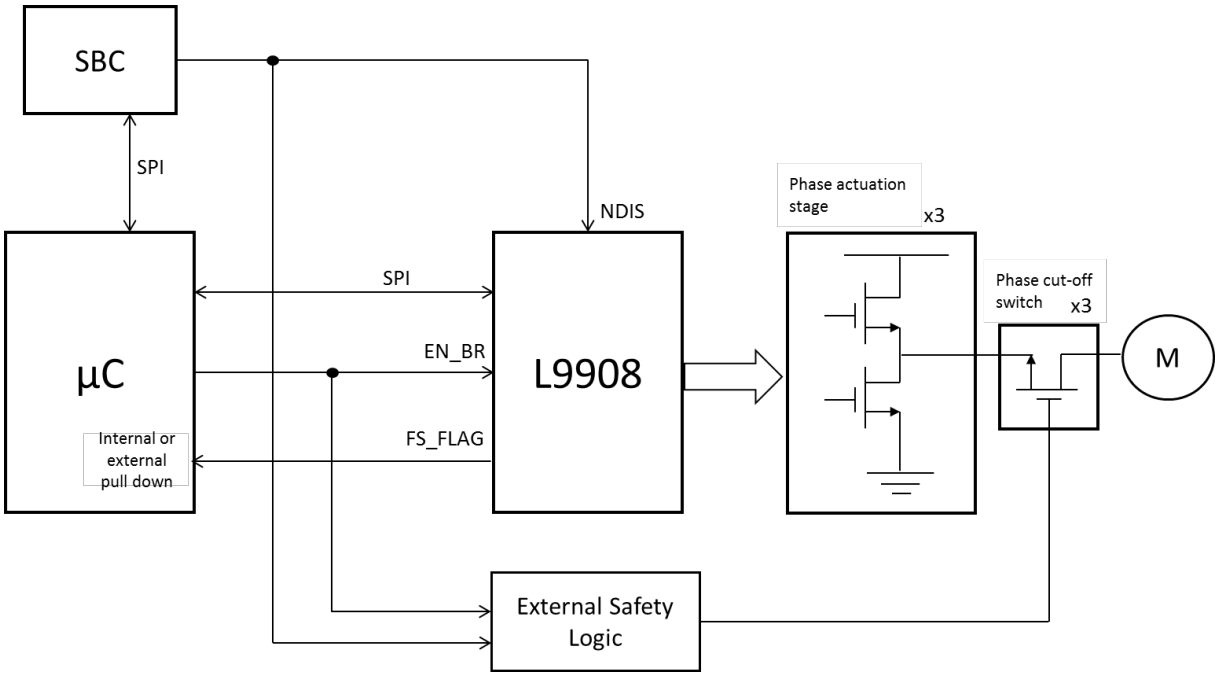
All digital I/O pins of L9908 can be grouped in three main categories:

- All the parallel input pins that control the external FETs (INLx, INHx);
- The SPI signals;
- All the I/O pins having a direct control on the status of L9908 inside the device operation State Machine (NDIS, EN_BR and FS_FLAG).

These last I/O pins have also a huge relevance on the safety targets of the application where L9908 is used.

Figure 8 shows how the safety architecture of L9908 is implemented. Users shall follow it, in order to exploit at the maximum level the safety concepts considered during the product development.

Figure 8. Safety architecture for L9908



As showed, L9908 implements redundant paths to bring the system in a safe state. For the application environment of L9908, safe state means the interruption of motor actuation if a malfunction is detected.

The former path comes from NDIS pin, which is intended to be connected to the fault pin available on the system basis chip (SBC), which generates the supply voltage and monitors the MCU through the watchdog function.

A second switch off path comes from MCU, which can acknowledge the status of the bridge driver, monitoring the fault status flag output from L9908.Once a fault is detected by L9908, the FS_FLAG assertion shall trigger the proper action at system level by generating a warning condition for the MCU, which, in turns, controls EN_BR input.

Finally, a third path is introduced in order to guarantee the transition to a safe state also in case L9908 is not working properly, and cannot control the driving of the external FETs. At this purpose, Phase Cut-Off switch transistors are introduced in series to each phase output. If switched OFF, the connections with the load get opened, making possible the interruption of the actuation.

6 Fault management

The fault set is divided in two main categories based on the required corrective actions:

- STD (Shutdown Faults): this set include faults which are highly dangerous for the IC or the application and that need a quick corrective action to avoid harming;
- WRN (Warnings): this set includes all those faults against which the application and the device are tolerant and the corrective action can be waived or delayed.

L9908 allows a certain degree of fault management customization; a subset of available enabled faults can be configured by setting the proper FHC registers.

Table 3. Fault summary

Fault flag	Source diagnosis	Self-Check	Failure reaction	Fault description
INT_RST=1	Internal Supply Monitor	Yes	RESET	Under-voltage on V3V3_ANA
INT_RST=1	Internal Supply Monitor	Yes	RESET	Under-voltage on V3V3_DIG
INT_RST=1	Internal Supply Monitor	Yes	RESET	Over-voltage on V3V3_ANA
INT_RST=1	Internal Supply Monitor	Yes	RESET	Over-voltage on V3V3_DIG
INT_RST=1	VDD Monitor	Yes	RESET	Under-voltage on VDD
VDD_OV=1	VDD Monitor	Yes	SAFE-OFF	Over-voltage on VDD
INT_RST=1	ICM	Yes	RESET & SAFE_OFF	Main clock stuck violation
CLK1_ERR=1 CLK2_ERR=1 CLK2_TIME_OUT=1	ICM	No	Flag only (NORMAL)	Oscillators mismatch or auxiliary clock stuck violation
PGND_LOSS=1 AGND_LOSS=1 DGND_LOSS=1	GLM	Yes	Flag only (NORMAL)	Loss of power or signal grounds
OTM_SD=1	OTM	No	SAFE-OFF	Thermal shutdown
OTM_WR=1	OTM	No	Flag only (NORMAL)	Thermal warning
STDn_PWM =1 [n=1,2,3]	STD on PWM	No	Ignore overlapping PWM command	Shoot through on half bridge n (PWM input)
STDn_VGS =1 [n=1,2,3]	STD on VGS	No	Configurable	Shoot through on half bridge n (Ext. FET Vgs)
HSn_STG = 1 [n=1,2,3]	OND	Yes	Configurable	Short to ground on SHS_n
LSn_STB=1 [n=1,2,3]	OND	Yes	Configurable	Short to battery on SHS_n
HS2_OFD=1 LSn_OFD=0 [n=1,2,3]	OFD	Yes	Flag only (NORMAL)	Short to ground on one or multiple motor phase
HS2_OFD=0 LSn_OFD=1 [n=1,2,3]	OFD	Yes	Flag only (NORMAL)	Short to battery on one or multiple motor phase

Fault flag	Source diagnosis	Self-Check	Failure reaction	Fault description
HS2_OFD=0 LSn_OFD=011,101,100 [n=1,2,3]	OFD	Yes	Flag only (NORMAL)	Open connection on motor phase 1,2,3
VDH_UV=1	MBM	Yes	Configurable	Under-voltage at VDH pin
VDH_OV=1	MBM	Yes	Configurable	Over-voltage at VDH pin
VPRE_UV=1	VPRE Monitor	Yes	Auto-retry	Under-voltage at VPRE pin
VPRE_OV=1	VPRE Monitor	Yes	SAFE-OFF	Over-voltage at VPRE pin
VCP_UV=1	VCP Monitor	Yes	Flag only (NORMAL)	Under-voltage at CP2 output
VCP_OV=1	VCP Monitor	Yes	Flag only (NORMAL)	Over-voltage at CP2 output
VBP_UV=1	VBP Monitor	Yes	Configurable	Under-voltage at VBP pin
VBP_OV=1	VBP Monitor	Yes	Configurable	Over-voltage at VBP pin
WDT_DATA_fail=1	WDT	NA	SAFE-OFF	Watchdog reset failure
WDT_OVF_fail=1	WDT	NA	SAFE-OFF	Watchdog time-out failure
SPI_ERR=1	SPI CRC Check	NA	Ignore Frame	SPI CRC Check failure
SPI_ERR=1	SPI FC Check	NA	Ignore Frame	SPI FC Check failure
SPI_ERR=1	SPI Clock Counter Check	NA	Ignore Frame	SPI Clock Counter Check failure
NVM_CRC_FAIL=1	NVM Data CRC Check	NA	SAFE-OFF Load default values	NVM Data CRC Check
CFG_CRC_FAIL=1	SRR Data CRC Check	NA	SAFE-OFF	SRR Data CRC Check
BIST_STATUS=11	BIST	NA	SAFE-OFF	BIST Failure

6.1 Fault Reaction Configuration (FRC)

For each one of the fault listed in Table 3 two configuration bits allow to define whether the corrective action shall be automatically developed by the device itself or it can be waived.

Table 4. Fault Reaction Configuration bits

<FLT_REF>_REACT_CFG1	<FLT_REF>_REACT_CFG0	Description
0	0	Full SW Off – disable all HB drivers and CPs, device goes in SAFE-OFF mode (Default)(1)
0	1	Reduced Operation Mode – disable failing HB only, device remains in NORMAL mode(2)
1	0	Flag only – down-rate fault to simple warning, device remains in NORMAL mode(3)
1	1	Flag only – down-rate fault to simple warning, device remains in NORMAL mode(3)

1. *Fault danger for the application is considered high, the corrective action shall be taken as soon as it is detected by the device itself by disabling all half bridges and charge pumps.*
2. *Fault danger for the application is considered high, the corrective action shall be taken as soon as it is detected by the device itself by disabling only the half bridge on which the fault is present still allowing a reduced performance operation.*
3. *Fault danger for the application is considered low, the fault can be ignored with no corrective action applied nor internal or external.*

The following table details the Fault Reaction Configurations available for the different Fault events.

Table 5. Internal Managed Faults reaction details

Fault Flag	Device Fault	Half Bridge Fault	FRC Available
STD_VGS_n=1	-	X	(1)(2)(3)
HSn_STG = 1	-	X	(1)(2)(3)
LSn_STG=1	-	X	(1)(2)(3)
VDH_UV=1	X	-	(1)(3)
VDH_OV=1	X	-	(1)(3)
VBP_UV=1	X	-	(1)(3)
VBP_OV=1	X	-	(1)(3)

1. *Fault danger for the application is considered high, the corrective action shall be taken as soon as it is detected by the device itself by disabling all half bridges and charge pumps.*
2. *Fault danger for the application is considered high, the corrective action shall be taken as soon as it is detected by the device itself by disabling only the half bridge on which the fault is present still allowing a reduced performance operation.*
3. *Fault danger for the application is considered low, the fault can be ignored with no corrective action applied nor internal or external.*

Note:
- *While other configurations are available for all FHC faults the configuration 01 is available only on a limited subset. In Faults that don't support such a FRC the configuration 01 is reserved.*
- *For VDH_UV, VDH_OV, VBP_UV, VBP_OV and CFG_CRC_FAIL the configuration 01 has the same effect as configuration 10 and 11.*

6.2 Register lock mechanism

Depending on their Safety relevance, registers are divided in 3 types, each of them requiring different procedure to grant writing access.

- *NSR – Non Safety Registers:* the content of these registers has no impact on device Safety and registers are immediately accessible for reading and writing.
- *SLR – Safety Latent Registers:* the content of these registers has a limited impact on device Safety, registers are normally accessible for reading and can be accessed to write with a one-step lock mechanism.
- *SRR – Safety Relevant Registers:* the content of these registers has a significative impact on device Safety and cannot be modified in any functional state of the device. Registers are always readable but writing access is available upon a two-steps lock mechanism.

Lock mechanisms indicated above, allow the transition of the device from its functional NORMAL mode to CONFIG mode, during which SLR and SRR are writable; only NSR are writable in NORMAL mode.

6.2.1 One-step lock mechanism

Write unlocking keys in the correct sequence into the dedicated register, as follows:

- device is in NORMAL MODE
  - write reg CFG_EN_UNLOCK = **0x55**
  - write reg CFG_EN_UNLOCK = **0x33**
- device is now in CONFIG MODE
  - **< perform SLR write operations >**
  - write reg CFG_EN_UNLOCK = **0xAA**
- device back to NORMAL MODE with SLR values stored

Configuration mode is also left automatically after the CONFIG mode time-out expiration: if no correct lock SPI frame is detected within T_cgf_time_out (typical value 100 ms), CONFIG mode is left.

6.2.2 Two-step lock mechanism

Increases the protection of one-step locking system by furtherly masking it with a hardware signal:

- device is in NORMAL MODE
  - set pin **EN_BR = 0** or **HBn_DIS = 1** (n = 1,2,3)
  - write reg CFG_EN_UNLOCK = **0x55**
  - write reg CFG_EN_UNLOCK = **0x33**
- device is now in CONFIG MODE
  - **< perform SRR write operations >**
  - write reg CFG_EN_UNLOCK = **0xAA**
  - set pin **EN_BR = 1** or **HBn_DIS = 0** (n = 1,2,3)
- device back to NORMAL MODE with SRR values stored

Configuration mode is also left automatically after the CONFIG mode time-out expiration: if no correct lock SPI frame is detected within T_cgf_time_out (typical value 100 ms), CONFIG mode is left.

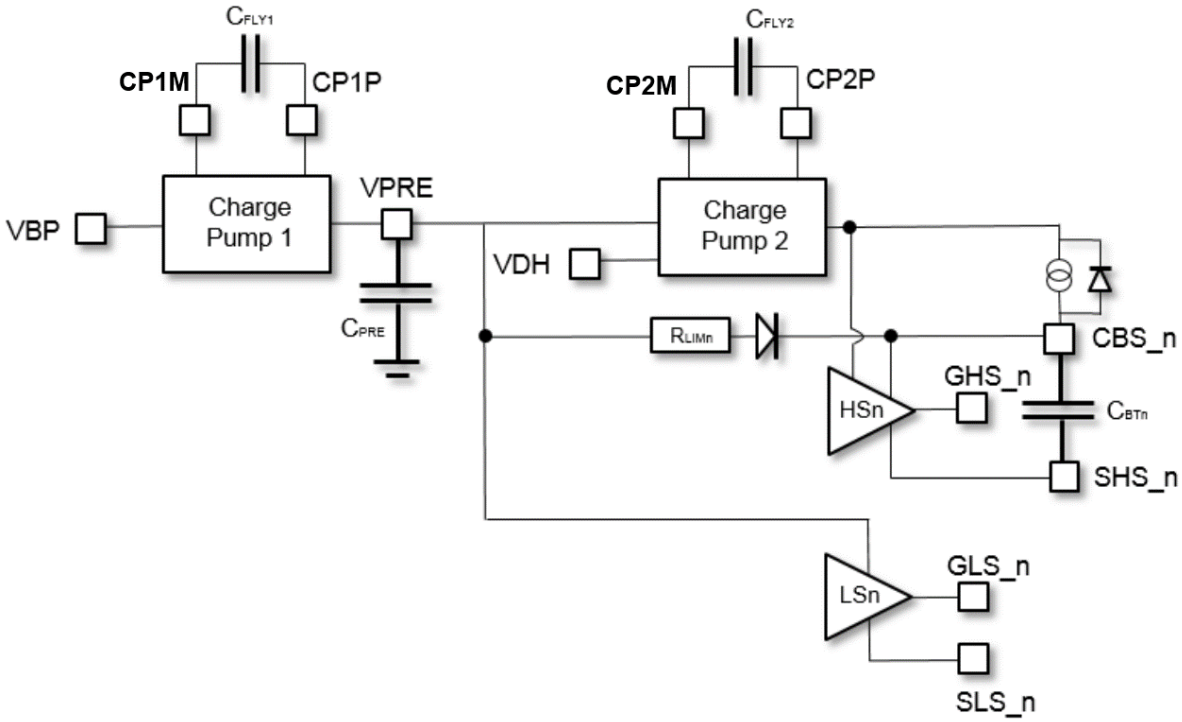
7 Gate driver output

7.1 Principle of operation

The stage of external FETs pre-drivers is mainly composed, for both LS and HS case, by a push-pull stage that, alternatively, charges and discharges the gate terminal.

Figure 9 represents these push-pull stages with the blocks HSn and LSn, and shows how the entire stage is supplied, starting from VBP supply.

Figure 9. Simplified block diagram of external FETs gate supply



There is a cascaded connection between the two charge pump stages:

- The first one generates VPRE voltage, which is an intermediate supply rail to be used as reference level for the stage immediately after, but it is also the supply rail for the stages driving Low Side gates and it has a key role on the charge of bootstrap capacitors;
- The second charge pump provides the supply rail for the stages driving the High Side gates, but it is also used, as explained in the following paragraphs, to sustain the charging of bootstrap capacitors.

7.2 External components

7.2.1 Fly capacitors choice

For both fly capacitors C_{FLY1} and C_{FLY2} the value of 1 µF is recommended, considering the internal structure of charge pump stages, and typical values of other external capacitors, such as C_{PRE} and C_{BTn}.

For both, user shall be taking care of the maximum voltage they can withstand.

For fly capacitance for VPRE regulator (connected between CP1P and CP1M) maximum voltage is VBP.

For fly capacitance for charge pump (connected between CP2P and CP2M) maximum voltage depends on the system: it shall be equal to maximum battery voltage VDH.

7.2.2 Capacitor on VPRE and bootstrap capacitors

The value of capacitance suggested for VPRE depends on which ripple is acceptable on regulator output:

- In normal condition, with VBP=12V, regulator operates in linear mode and the output VPRE does not show any ripple.
- With low VBP voltage(<9V), VPRE regulator operates as a charge pump, therefore on the output a ripple is expected.

To minimize this ripple a value of 4.7 µF has been proposed.

To calculate the ripple, the current consumption due to charge/discharge external FET shall be evaluated:

$$\mathrm{I_{load}} = (\text{number of ext FET}) \times (\text{PWM frequency}) \times \mathrm{Qgate} \quad (1)$$

Our charge pump works with 200 kHz clock frequency, hence for half a period (2.5 µs) output load current is fed by CPRE capacitance.

Your ripple will be:

$$\text{VPRE Ripple} = 2.5\,\mu s \times \frac{\mathrm{I_{load}}}{C_{pre}} \quad (2)$$

Once C_{PRE} is chosen, it is important to keep a certain ratio between VPRE capacitance and bootstrap capacitance because the charging current of bootstrap capacitances comes from C_{PRE}.

For example:

- Choosing CPRE = 4.7 µF, CBT 1 µF are recommended.
- Choosing CPRE =1 µF, we suggest using CBT = 220 nF.

In the next paragraph a more detailed explanation about charging of bootstrap capacitor is provided, impacting also C_{PRE} value.

7.2.3 Bootstrap capacitor charging

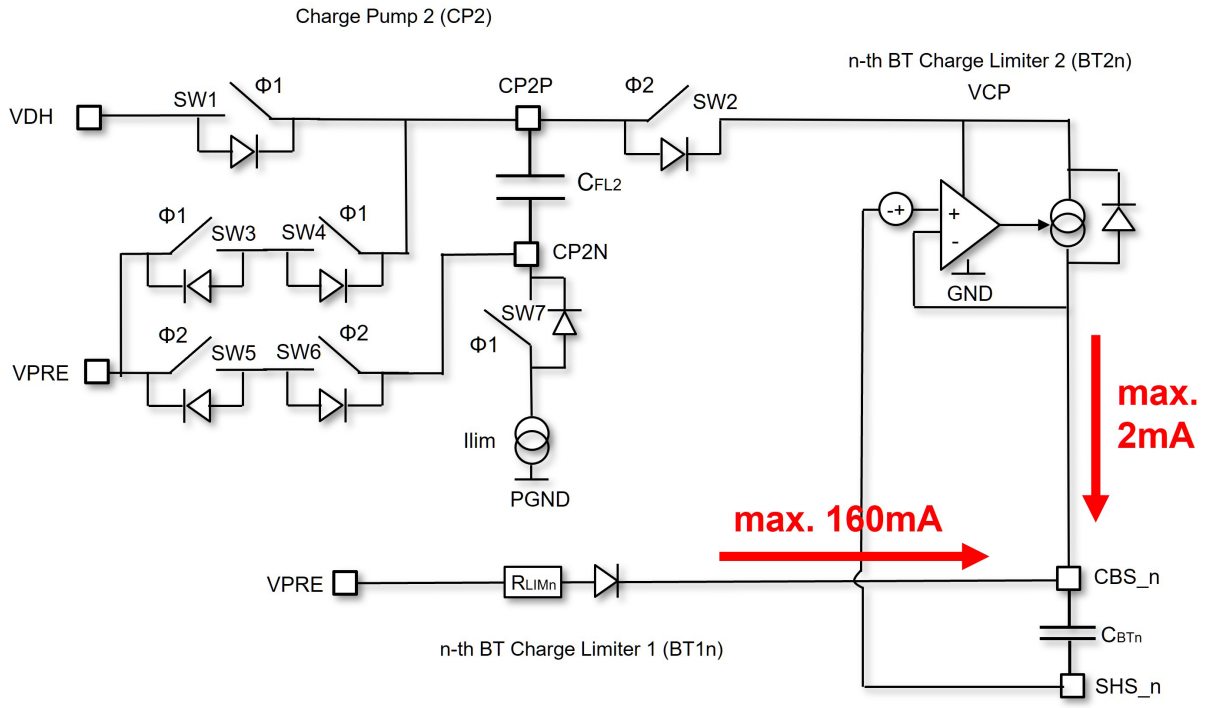
Bootstrap capacitors are very important because they allow to generate the overdrive voltage necessary to bring High Side gates voltage above the battery level.

There are two sources allowing to keep Bootstrap capacitors to a good level of charge (see Figure 10):

- VPRE: it is the main contribution, because the current availability is higher (typically 118 mA). But, to have an efficient bootstrap capacitor charging, its negative terminal (SHS_n) must be fixed to GND level. This happens whenever the Low Side FET of the phases, is switched ON.
- Charge pump 2: this contribution is lower (about 2 mA) and is active only when INH = 1. However, in case the phase is driven with a 100% of duty cycle (meaning High Side FET permanently ON), node SHS_n never goes to GND level, and the contribution from VPRE is not useful. The charge pump is, therefore, the only contribution to support bootstrap capacitors charge unless an external CBS charging system is present.

Note: At every start-up, it is necessary, before motor actuation, to switch ON the three Low Side FETs for a period, in order to fix SHS_n at GND level and charge effectively all bootstrap capacitors. To avoid VPRE undervoltage events it is recommended to avoid the simultaneously turn on of all three Low Side FET.

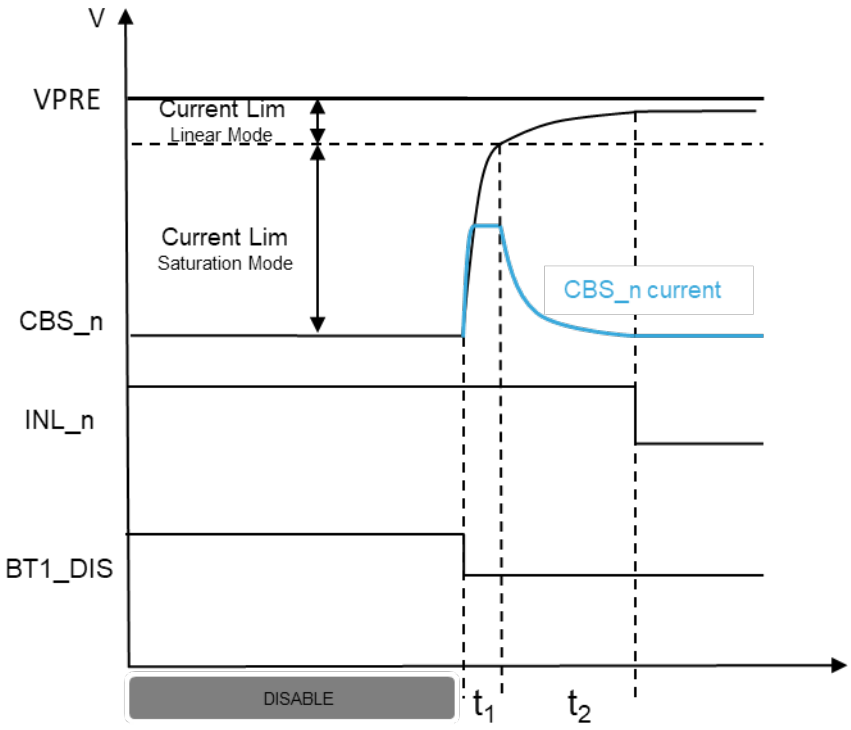
Figure 10. Charge pump 2 and bootstrap capacitors charging



The first CBS charge at startup is composed of two stages as shown in Figure 11: the first at constant current, the second with a resistive-like behavior.

$$\Delta t = t_1 + t_2 \approx \frac{C_{BT} \times (\Delta V - 1.3V)}{BT_{LIM1\_CURR}} + \left(4 \times BT_{LIM1_{RES}} \times C_{BT}\right) \approx 740\,\mu s \quad (3)$$

Figure 11. Bootstrap capacitor charging at startup from VPRE



Doing a worst-case evaluation, the peak current drained from VPRE for CBT charging can be as high as 480 mA if all three capacitors are charged simultaneously, leading to a potential VPRE undervoltage detection due to excessive CPRE discharge; it is therefore strongly suggested to charge each capacitor individually.

In case of bigger CBT it is possible to further increase the CPRE capacitor value up to 6.8 µF to avoid undervoltage events on VPRE. In case a CPRE of 6.8 µF is not enough to avoid undervoltage events during CBT charge, it is recommended to deactivate CP1 regulator and provide VPRE from external power supply with enough current capability to charge the CBTs.

7.2.4 Gate lines: external components and layout suggestions

The gates of the power switches and the gate driver outputs can be connected directly, but usually some gate resistors are placed in series on the gate lines in order to limit the gate current during commutations. The final target is to control the dV/dt of each half-bridge output and then reducing the EMI. A typical value for gate resistor series is in the range 50-100 Ω.

It is also useful the insertion of a high value resistor between gate and source terminals (100 kΩ typically), helping the gate capacitor discharge in case of passive switch-off, when the gate node is not pulled down by the activation of the low side of the pre-driving stage.

Figure 1 and Figure 2 show as example the resistors R_{GHS1n}, R_{GHS2n}, R_{GLS1n} and R_{GLS1n}.

Regarding the layout of such gate lines, it is always strongly recommended to place the external FETs very close to the gate driver. It is important to reduce as much as possible the lengths of such line paths as well as the areas included in the gate circuits, because these areas can act as weak antennas and could capture noise from the surrounding environment. The larger these areas, the higher the gain of such undesired antenna circuits.

7.3 Gate charge driving capability

It is important that the device can generate a good level of voltage difference between gate and source of external FETs in order to switch them in the proper way.

A series of bench tests were done in order to check which Vgs voltage levels is possible to guarantee even in worst case condition.

The test conditions having a strong impact on the gate charge capability are listed below.

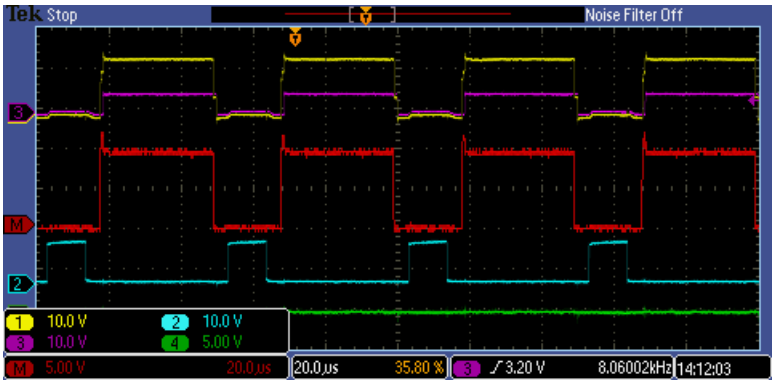
1. High side predrivers were tested. They are more critical than the corresponding Low side stages, because the charging of bootstrap capacitor is needed;
2. High level of duty cycle (higher than 95% but not 100%). In this case the low side driver of the same phase remains switched on for short time, and bootstrap capacitors cannot reach a proper level of charge. On the other hand, it is not possible to rely on the contribution from CP2 output, as in the case of 100% of duty cycle;
3. Low values of VBP supply (4,5 V or near to lower limit threshold). In this case VPRE regulator stage works as Charge Pump with higher current consumption, with reduced capability of sustaining bootstrap capacitors charging;
4. Increasing of gate capacitance, in order to increase the total amount of gate charge Q_g. To reach this condition, additional capacitors between gate and source of external FETs were connected (C_{GHSn} and C_{GLSn} capacitors shown in Figure 1 and Figure 2);
5. Hot temperature.

Referring to point 4, 22 nF capacitors were added in order to approach the condition to have an equivalent Q_g = 300 nC.

In the figures below, the test findings are shown.

Bench tests give the demonstration that even in worst case conditions (external FETs with high Q_g, high temperature, very high duty cycle, low VBP) the device can guarantee a minimum VGS of 7 V.

Figure 12. Gate charge driving capability bench tests: condition 1

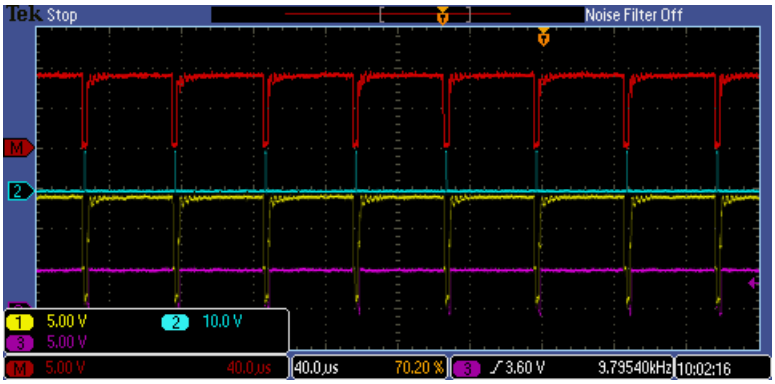


Conditions:

- VBP = 12 V; VDH = 4.75 V
- Q_g increased in order to approach 300 nC
- Load motor driven with f_pwm = 20 kHz
- Room Temperature

We can obtain VGS = 9 V for HS and LS.

Figure 13. **Gate charge driving capability bench tests: condition 2**

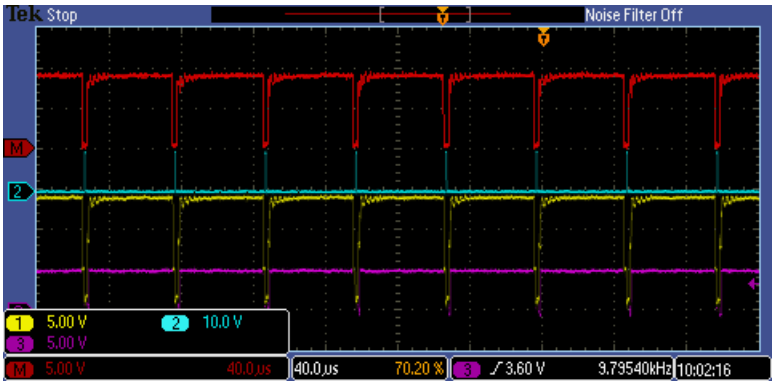


Conditions:

- VBP = 12 V; VDH = 4.75 V
- Q_g increased in order to approach 300 nC
- Load motor driven with f_pwm = 20 kHz
- Room Temperature

We can obtain VGS = 9 V for HS and LS also increasing the motor speed and reducing the duty cycle of Low Sides to 1.2% (Ton = 600 ns with T = 50 µs).

Figure 14. **Gate charge driving capability bench tests: condition 3**

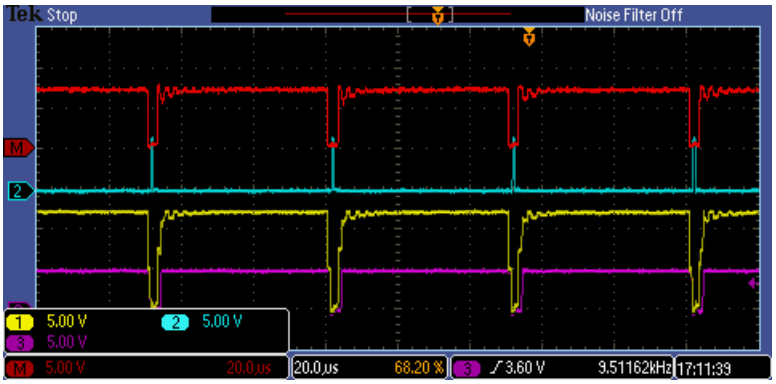


Conditions:

- VBP = 12 V; VDH = 4.75 V
- Q_g increased in order to approach 300 nC
- Load motor driven with f_pwm = 20 kHz
- Room Temperature

Decreasing also VBP to 4.75 V (keeping very low duty cycle values for the Low Sides), VGS becomes smaller (about 8 V for High Sides and 7 V for Low Sides).

Figure 15. **Gate charge driving capability bench tests: condition 4**



Conditions:

- VBP = 12 V; VDH = 4.75 V
- Q_g increased in order to approach 300 nC
- Load motor driven with f_pwm = 20 kHz
- Room Temperature

Hot temperature is the worst case. After a comparison with the waveforms taken at RT, VGS for the High Sides is a little smaller (about 7 V).

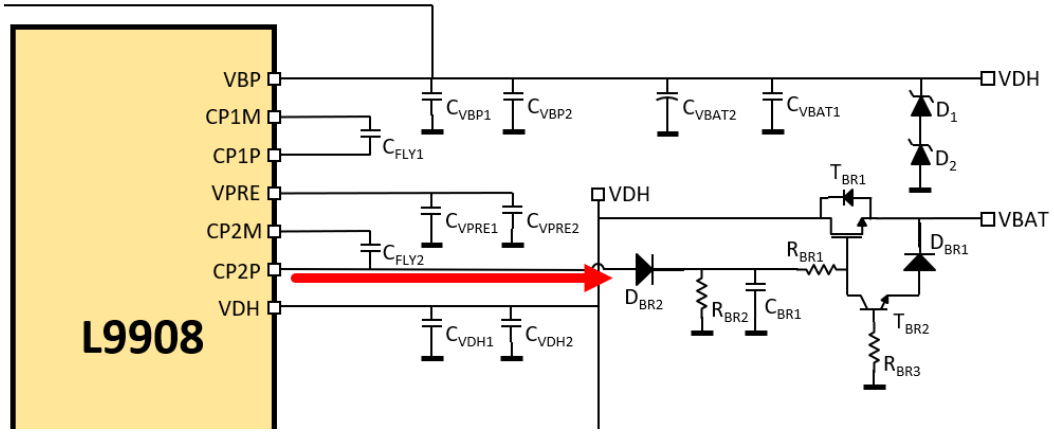
7.3.1 Current load on CP2

In the suggested Application Circuits, CP2 output pin has been used to bias the reverse battery protection circuitry (see Figure 16). In some customer's applications, an additive current load might be requested to CP2 to drive, as an example, a phase cut-off circuit or other functions. In these cases, user must take into accout that charge pump 2 block hasn't been designed specifically for the purpose of driving external loads with a DC current request, and its current capability is limited to 1.5 mA.

In case of such usage, the main drawback the user shall encouter will be a reduction of the minimum guaranteed V_{GS} on high-side mosfets L9908 is able to provide. This drawback shall be mostly evident the longer the high-side duty cycle is.

As a general margining rule, a V_{GS} reduction of 150 mV per each extra mA requested to CP2 can be considered.

Figure 16. **External load on CP2**



7.4 Methods for increasing gate charge driving capability

User can, in any cases, overcome the limits shown in the previous paragraph, and adopt strategies to increase the gate charge driving capability, because in certain applications, it may be required.

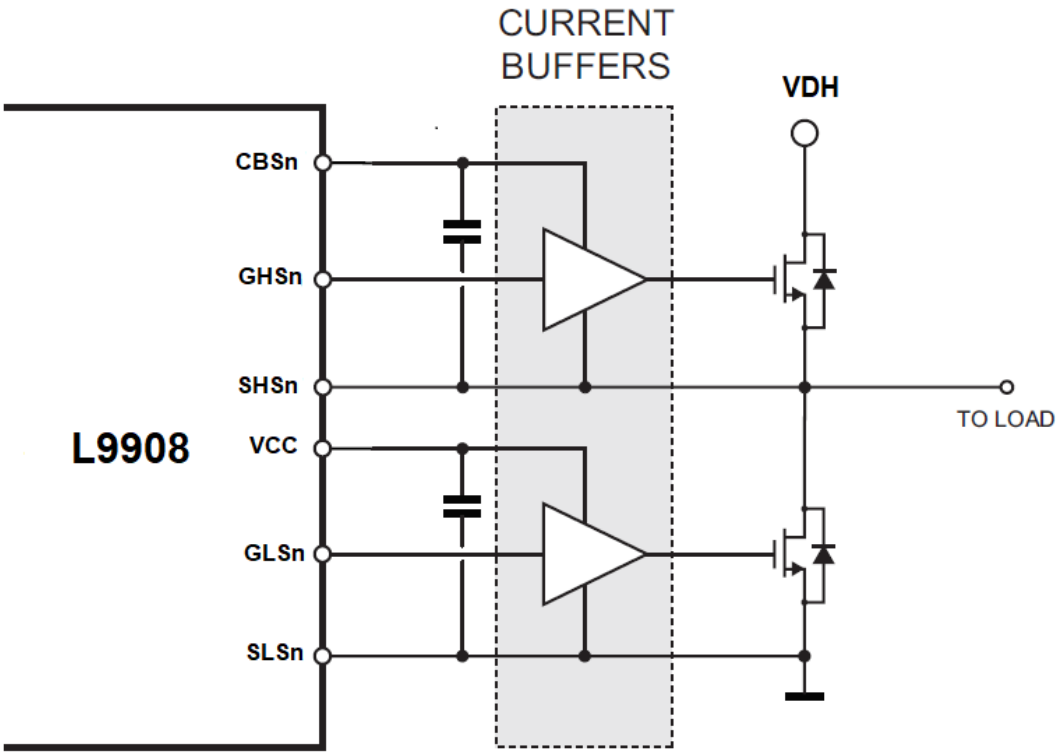
This requirement could be found in systems having a power rating higher than about 1 kW. In those applications, in fact, typically the external FETs have a large gate charge which contributes to a slowing down of the power switch transition (the dVOUT/dt), increasing the power dissipation during each commutation. Note that also in applications with power rating higher than 1 kW, the output current capability of L9908 could be enough if the power dissipation for commutation is acceptable (the power dissipation due to RDS(on) or VDSSAT is not dependent on the gate current). But if the limitation of this power contribution is a constraint, the dVOUT/dt of each transition must be increased by enhancing the current capability of the gate driver.

7.4.1 Using external current buffers

A simple way to increase the current capability of the gate driver outputs is to insert, in series with the gate lines of every half-bridge gate driver IC, two external current buffers.

A simplified block diagram is shown in Figure 17.

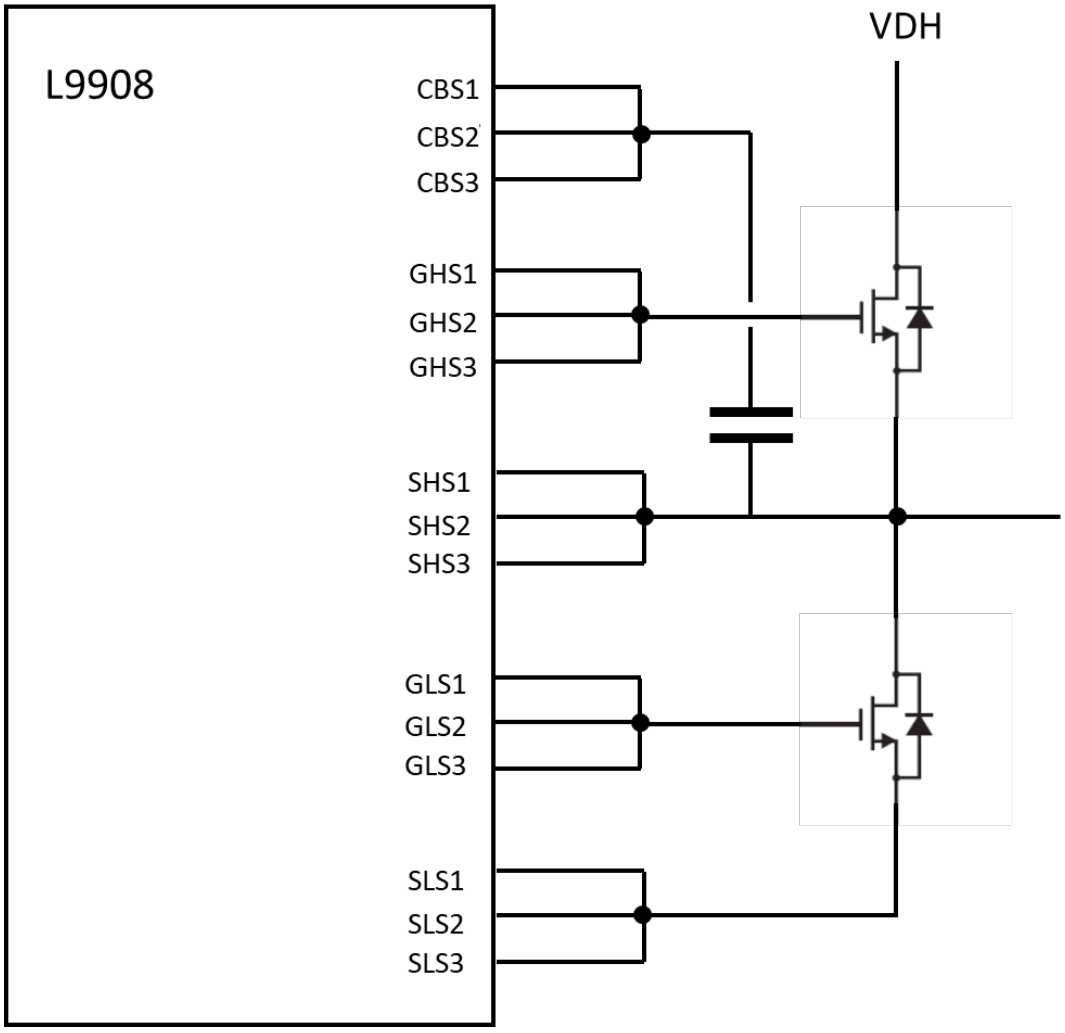
Figure 17. External current buffers



7.4.2 Pre-driver parallelization

Another way to increase the current capability of the gate driver outputs is the connection of all the three high-side pre-driver outputs of L9908 to a single external High-Side FET, and all the three low-side pre-driver outputs to a single Low-Side FET.

Figure 18. Pre-driver parallelization solution



The advantage of this solution is having the gate charge driving capability increased by 3 factors.

In case of a three-phase motor driving application however, the main drawback of this solution is the need for 3x L9908 devices, one for each phase of the motor, with the consequent BOM cost impact.

8 Current measurement

8.1 Principle of operation

L9908 is equipped with a stage for phase current measurement. The principle of the operation is the acquisition of the voltage across an external shunt resistor, and, after elaboration, this measurement is made available in two different formats:

- A digital conversion, 11-bit resolution (sign included), readable via SPI (rescaled at 15-bit resolution).
- An analog conversion, available on CSOn output pin.

The user can select among the shunt configurations shown in Figure 19. From left to right we have: a) DC-Link, b) 2xSingle Leg + DC-Link, c) 3xSingle Leg.

Figure 19. External shunt configurations

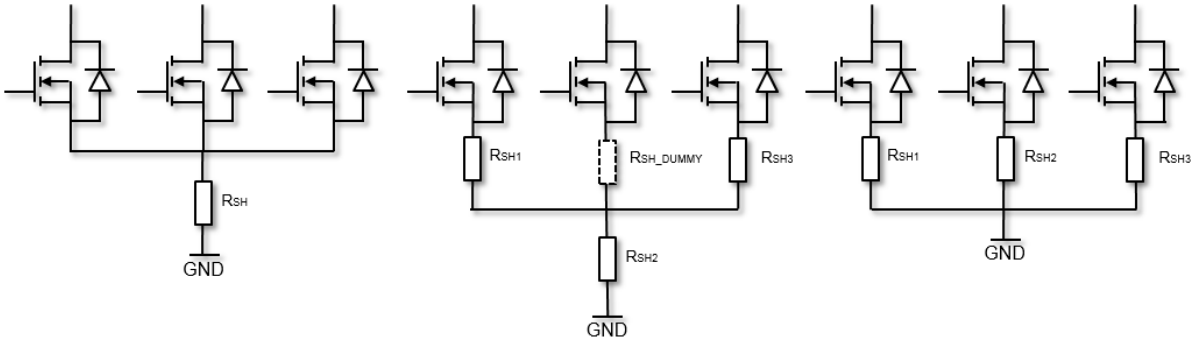
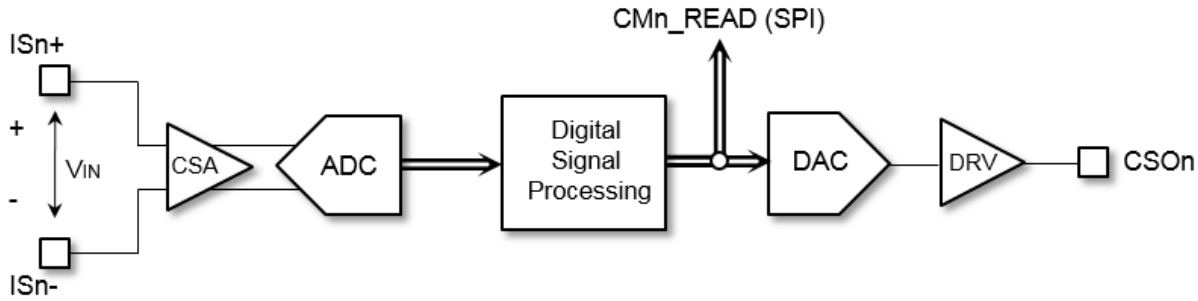


Figure 20 shows the block diagram of the current monitor for the n-th phase. The incoming signal (analog voltage across the shunt resistor) is, at first, converted to digital, with 11-bit resolution (and 4-bit after a SINC decimator filter is added to improve the S/N ratio), for the elaboration of the digital conversion.

After that, the signal is again converted to analog, and can be acquired on CSOn output (it can be adjusted to µC ADC input range, being compatible with 3.3 V and 5 V).

Figure 20. Current monitor channel simplified block diagram



Depending on the kind of application and, consequently, the current range, user can configure by SPI the Current Monitor input range (see Table 6), in order to obtain the best resolution. V_{IN_MAX} is the input range for which all parameters are guaranteed.

For example, in EPS application, typically 0.5 mΩ shunt resistance at each inverter leg is used, and in the range of ±14 A a typical resolution of at least 18mA is required.

Selecting the finest resolution (V_{IN_MAX} = ±7 mV of input range):

$$I\_\max = \frac{7\ mV}{0.5\ \mathrm{m\Omega}} = 14\ A \quad (4)$$

with a resulting resolution:

$$resolution = \frac{14\ A}{2^{10}} = 13{,}7\ mA \quad (5)$$

Table 6. Current monitor input range configuration bit

CSMn_IN_RANGE_CFG2	CSMn_IN_RANGE_CFG1	CSMn_IN_RANGE_CFG0	Description
0	0	0	V_{IN_MAX} = ±7 mV
0	0	1	V_{IN_MAX} = ±18 mV
0	1	0	V_{IN_MAX} = ±36 mV
0	1	1	V_{IN_MAX} = ±90 mV
1	0	0	V_{IN_MAX} = ±160 mV
1	0	1	V_{IN_MAX} = ±300 mV (Default)
1	1	0	Ignored
1	1	1	Ignored

8.1.1 A/D conversion

The A/D conversion is performed using two different algorithms:

- Up/Down TRK algorithm. TRK logic increments/decrements by 1LSB at each clock cycle the DAC input depending on sign comparator assessment. This algorithm can guarantee a high conversion accuracy but along with a limited input slew rate given by 1LSB/Tclk.
- SAR algorithm. SAR logic increments/decrements by 2^{10} / 2^{N} at each *N* clock cycle. This algorithm is effective in following fast changing signal but lacks in accuracy.

The principle of operation relies on the fact that if the signal is stable, with slow level variations, TRK algorithm is used, since it is more appropriate to follow the signal and it is more accurate.

SAR algorithm is recalled when an applicative condition consequent to a fast signal variation occurs. It can be recalled in two ways:

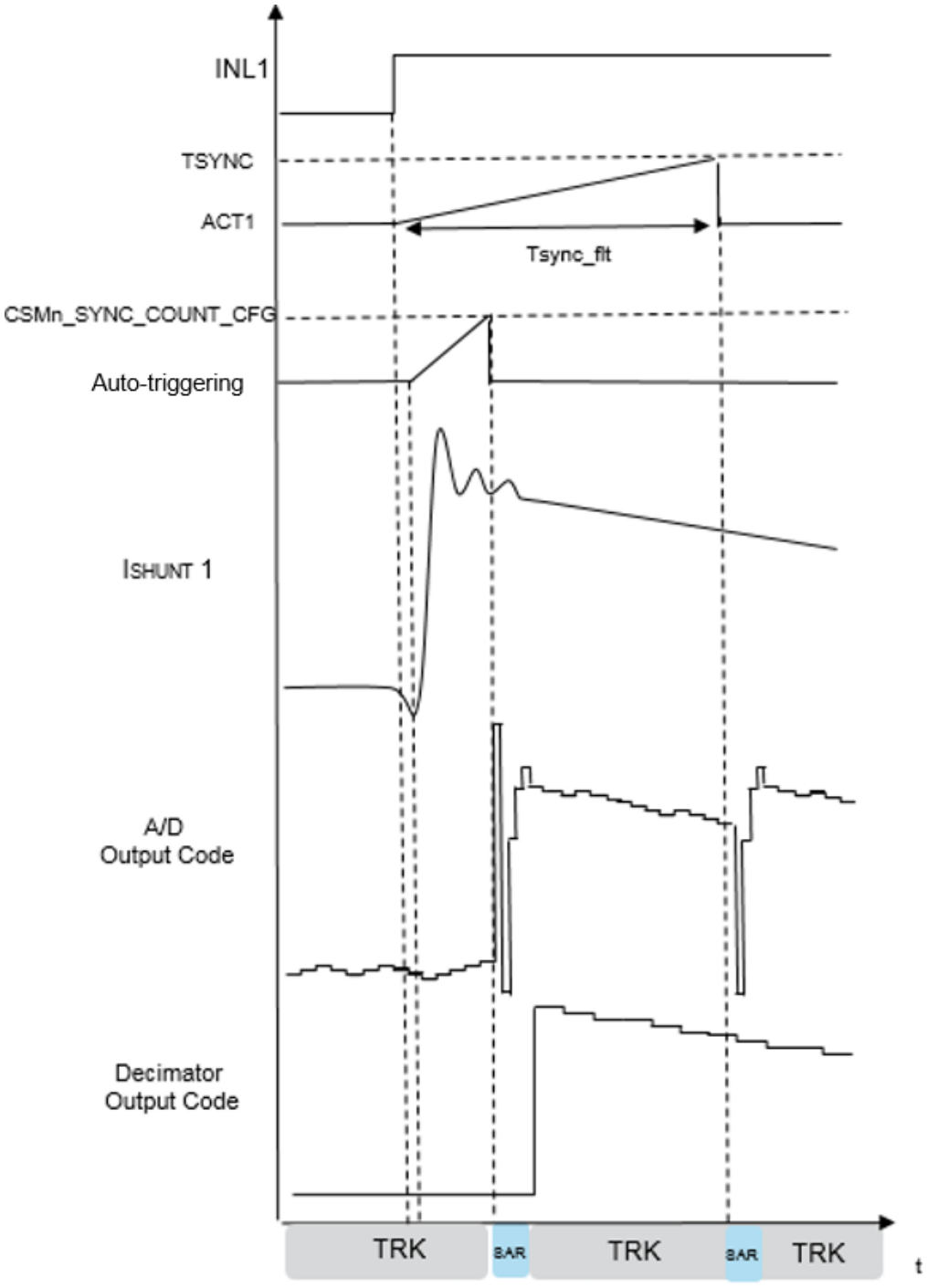
- Command edge. A synchronization mechanism is present, based on the edge of a signal related to a fast variation (INL or PVF).
- Auto-triggering. The SAR is executed when the number of clock cycles in which the Sign comparator has the same sign has reached a fixed value, set by SPI.

Figure 21 shows the two mechanisms.

First SAR event is recalled by Auto-triggering counter that is always active. In the example, the current has just been switched ON by INL1 command, and with TRK algorithm is not possible to quickly fit the new signal level. Having reached the maximum number of clock pulses with the same sign of the error, a SAR conversion is recalled.

The second SAR event, on the contrary, is synchronized with INL1 rising edge. After that a time programmable in TSYNCn register has elapsed, the SAR conversion is executed.

Figure 21. **Triggering of SAR**



Conversions synchronization

Command Edge Triggering criteria relies on ACT function: when the value stored in ACTn register equals the value configured in the TSYNCn register, a trigger pulse is generated, and SAR conversion is performed.

User can select the event triggering the start of the counter on ACTn register, programming the ACT_CFG bits (see Table 7).

Table 7. Actuation timers configuration bits

ACT_CFG1	ACT_CFG0	Description
0	0	PVF Negative Polarity (Default)
0	1	PVF Positive Polarity
1	0	INL Negative Polarity
1	1	INL Positive Polarity

SAR conversion is launched at the same time on all current monitors, synchronously.

The n-th ACT to be used for sampling reference can be configured by means of the following bits:

Table 8. Command edge triggering configuration bits

CSM_SSPV_PH_CFG1	CSM_SSPV_PH_CFG0	Description
0	0	No synchronization
0	1	TSYNC based on Phase 1 (Default)
1	0	TSYNC based on Phase 2
1	1	TSYNC based on Phase 3

The possibility to choose the phase on which SAR synchronization is based offers great advantages and flexibility.

In some applications environment, such as FOC controls, there are driving signals INLx never going too low. In this way it is not possible to implement a mechanism where the conversion is controlled independently on each phase, basing on the edge of the driving signals. Alternatively, a conversion on all the three phases, synchronized on the last driving signal having a transition too low.

In this way the user can choose the most appropriate phase to be used as a reference for the synchronization.

The most relevant advantage of this solution is given, anyway, by the synchronization of TSYNC with the starting of SAR conversion. User can program, in a deterministic way, the sampling time, having as reference the edge of the signal chosen as trigger for ACTn counter (see Figure 21, where the trigger is rising edge of INL input).

Moreover, the user has other options to choose which data conversion will be captured and used (both on SPI reading and on CSOn output).

All the possible options are programmed via SPI by setting CSM_n_SAMPLE_CFG bits.

Table 9. Current monitors sampling configuration bits

CSMn_SAMPLE_CFG3	CSMn_SAMPLE_CFG1	CSMn_SAMPLE_CFG0	Description
0	0	0	Free running – No T&H
0	0	1	T&H 1st data conversion from triggering
0	1	0	T&H 2nd data conversion from triggering (Default)
0	1	1	T&H 3rd data conversion from triggering
1	0	0	T&H 4th data conversion from triggering
1	0	1	T&H 5th data conversion from triggering
1	1	0	T&H 6th data conversion from triggering
1	1	1	T&H 7th data conversion from triggering

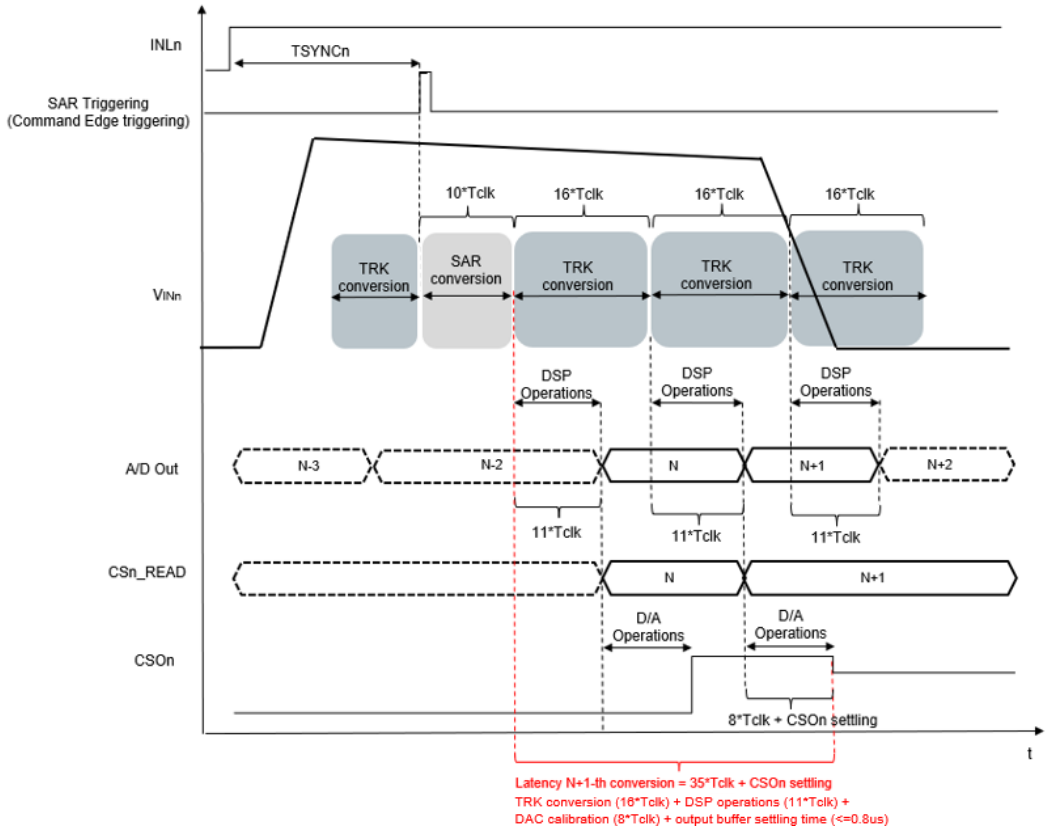
Choosing Free running option (CSM_n_SAMPLE_CFG = [000]), every time a conversion is done, it is available both on digital and analog output.

On the other options, a Track & Hold algorithm is used, and the conversion results are kept stable until the next triggering event occurs. In particular way the user can choose:

- CSM_n_SAMPLE_CFG = [001]: the data available on the outputs is the first conversion result after triggering. It is just the SAR conversion;
- CSM_n_SAMPLE_CFG = [010]: the data available on the outputs is the second conversion result after triggering. It is a TRK conversion, the first after SAR;
- CSM_n_SAMPLE_CFG = [011]: the data available on the outputs is the third conversion result after triggering. It is a TRK conversion, the second after SAR;

As shown in Figure 22, and explained below, the timing is totally under control because every conversion timing has its own reference to SAR conversion, whose start time is set by TSYNCn.

Figure 22. T&H sampling timing diagram



The user has different possibilities:

- Directly the SAR conversion (CSM_n_SAMPLE_CFG = [001]). In this case the conversion is faster, but less accurate (11-bit). The resulting waiting time is:
  - TSYNC + 21*Tclk = TSYNC + 1050 ns for SPI result;
  - TSYNC + 21*Tclk + 8*Tclk + CSOn setting (< 0,8 µs) = TSYNC + 1450 ns + CSOn setting.
- The first TRK conversion (CSM_n_SAMPLE_CFG = [010]). This is just the case shown in Figure 22. The conversion is slower, the waiting time is longer, but the results have better accuracy. The resulting waiting time is:
  - TSYNC + 37*Tclk = TSYNC + 1850 ns for SPI result;
  - TSYNC + 37*Tclk + 8*Tclk + CSOn setting (< 0,8 µs) = TSYNC + 2250 ns + CSOn setting.
- It is possible to choose other options (the third, the fourth data conversion from triggering, and so on) but there is not any gain in terms of conversion accuracy with respect to the solution shown in the previous point. User can, in any cases, take advantage from having more options to manage the delay on the conversion readings.

Timings above were calculated considering the following fixed timings (clock frequency = 20 MHz; Tclk = 50 ns):

- 10* Tclk for SAR conversion;
- 16* Tclk for TRK conversion;

- 11* Tclk for DSP operation (required to complete A/D conversion);
- 8* Tclk for DAC calibration (required to output D/A conversion on CSOn).

As mentioned, SAR conversion can be also activated by Auto-triggering mechanism. Auto-triggering criteria relies on an internal counter which counts the number of clock cycles in which the Sign comparator has the same sign. When the number of counted pulses equals the value configured in the CSMn_SYNC_COUNT_CFG register, a trigger pulse is generated, and SAR conversion is performed.

When activated by Auto-triggering, SAR conversion is launched independently of each current monitor, asynchronously.

Auto-triggering is always active and cannot be disabled. Its purpose is allowing A/D to promptly react in front of input voltage sharp transitions also in case Command Edge Triggering is not enabled.

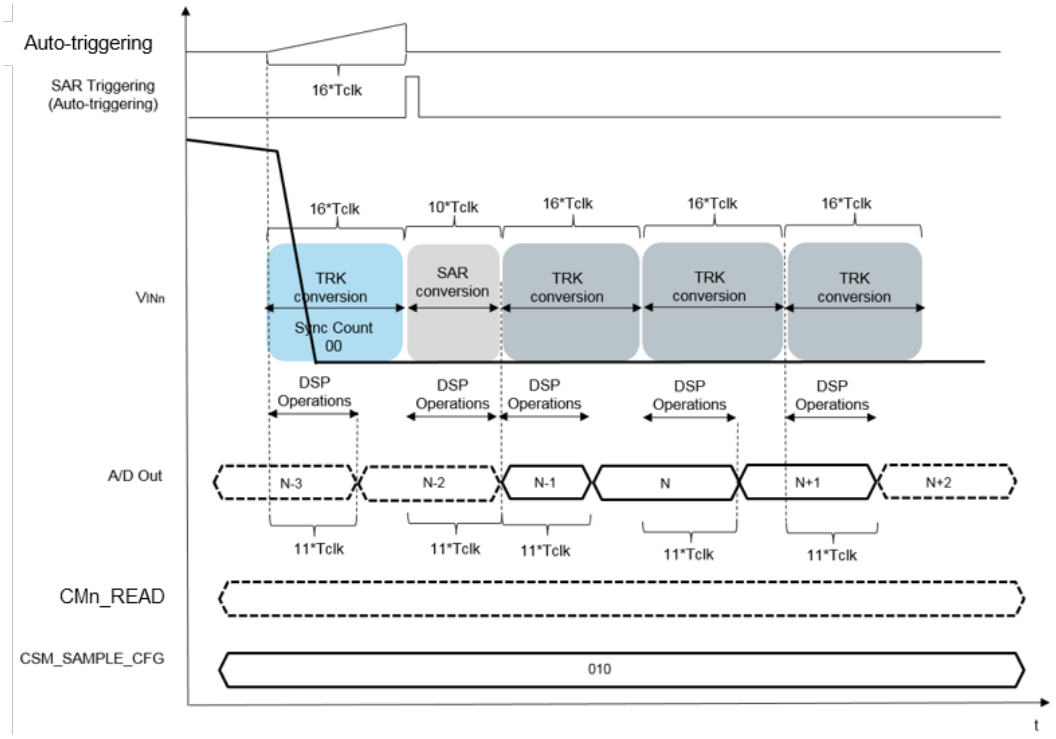
Zero current conversion

In many cases user can be interested to perform an A/D conversion in case of zero current. This can be interesting, for example, for offset evaluation, that can be subtracted, by software options implementation, to non-zero current conversions, in order to obtain more reliable results.

L9908 current monitor architecture allows to do it.

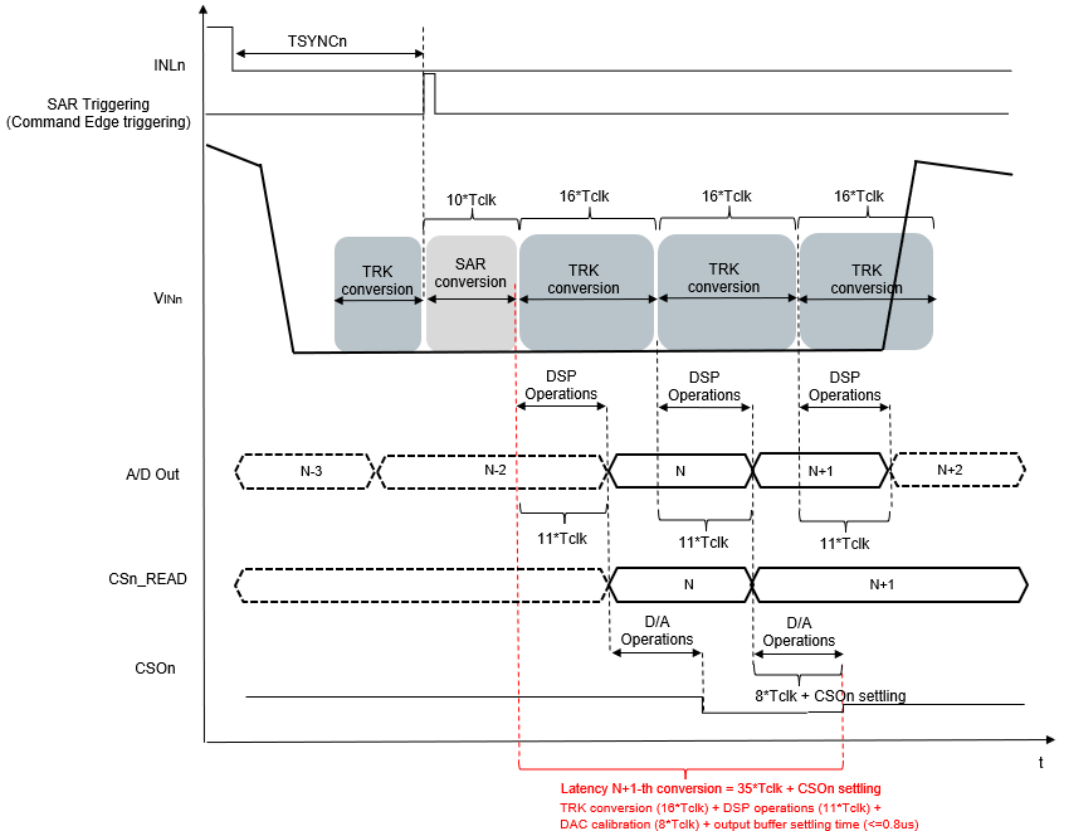
It is possible, of course, to trigger a SAR conversion with Auto-triggering mechanism, whenever the phase current goes to zero, because it is a case of sharp signal transition (see Figure 23).

Figure 23. Zero-current conversion + Auto triggering



However, user can also take advantage of the synchronization offered by Command Edge mechanism (see Figure 24).

Figure 24. **Zero-current conversion + Command Edge triggering**

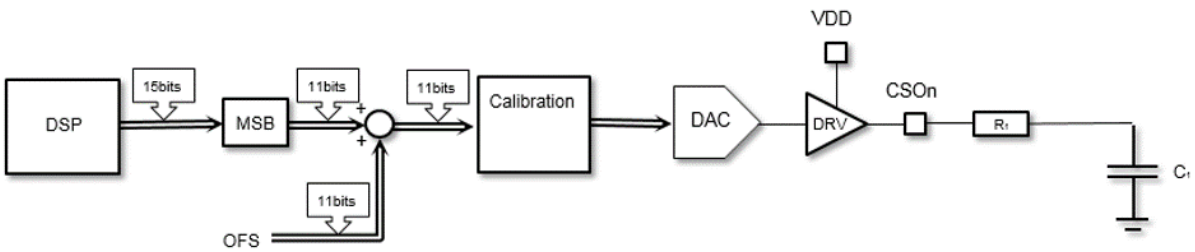


In this case, user should make sure to configure by SPI the actuation timer ACTn (where n is the phase chosen as sampling reference, see Table 8) choosing, as triggering event, the negative polarity of INLn signal (see Table 7).

8.1.2 D/A conversion

After DSP operations digital conversion is forwarded to analog output channel which makes available the processed current information also in the analog domain. In Figure 25 the simplified block diagram of D/A conversion is shown.

Figure 25. **D/A conversion simplified block diagram**



In order to better fit dynamic range and maximize the output S/N with respect to the externally connected microcontroller A/D, two successive digital operations are performed.

The current measurement coded in a signed 15-bit word is firstly converted to a signed 11-bit word by taking the 11MSB.

From the resulting processed word, the 11MSB, without sign, are taken and a fixed selectable offset OFS is added (shift).

Shift amount for the specific channel can be configured by means of dedicated SPI bits in order to adjust the current monitor output range to uC ADC input range as follows (see Table 10):

Table 10. CM output offset configuration bits

CSMn_OFS1	CSMn_OFS0	Description
0	0	0LSB DAC
0	1	90LSB DAC
1	0	1024LSB DAC
1	1	1024LSB DAC (Default)

Where:

- 00 and 01 configurations are intended to be used when the current to be read is only positive (DC-LINK configuration);
- 10 and 11 configurations should be used when the current to be read is either positive or negative (Single Leg).

DRV gain can be configured by means of dedicated SPI bit (CSM_OUT_RANGE_CFG = 0 for 3.3 V range; 1 for 5 V range) in order to adjust the current monitor output range to µC ADC input range.

8.1.3 Current monitor gain

It is possible to summarize the gain of the entire conversion chain, from the input signal across the shunt resistor, to the analog signal available on CSOn output.

Depending on the current monitor input range, it is possible to obtain the gain values summarized in Table 11.

The full-scale range values are obtained multiplying CM input ADC LSB values (a precise value is defined for every CSM input range) by 2^{11}-1.

Table 11. Current monitor gain in case of OFS = 1024 LSB

CM input ADC LSB	CSM input range FULL SCALE	GAIN (output range: 0-3.3 V)	GAIN (output range: 0-5 V)
10.05 µV	±10.29 mV	160.3	242.9
20.11 µV	±20.59 mV	80.1	121.4
40.28 µV	±41.25 mV	40	60.6
100.7 µV	±103.12 mV	16	24.24
181.27 µV	±185.62 mV	8.89	13.47
322.26 µV	±329.99 mV	5	7.57

It is immediate to notice that the full-scale range values calculated from LSB are higher than the corresponding values of the input ranges listed in Table 6. The difference between these values is necessary for device calibration during production process and can't be relied on during real-life applications. Conversion parameters are guaranteed only within VIN_MAX ranges listed in Table 6.

As example, to evaluate the gain in case of the lowest input range, the total full-scale range (considering positive and negative values) is 10.29 * 2 = 20.58 mV.

As a result, for output range of 3.3 V

$$Gain = \frac{3.3V}{20.58\,mV} = 160.3 \quad (6)$$

More generally, the formula to calculate the gain is the following:

$$I_{LOAD}R_{shunt} = \left(\frac{V_{CSO\_n}}{\Delta_{CM\_out\_LSB}} - OFS\right)\Delta_{CM\_in\_LSB} \quad (7)$$

Where:

- VCSO_n is the voltage at pin CSO_n

- OFS is the selected shift value
- RSHUNT is the shunt resistance value
- ΔCM_in_LSB and ΔCM_out_LSB are respectively the A/D and D/A quantization steps

$$Gain = \frac{V_{out}}{V_{in}} = \frac{V_{CSOn}}{I_{LOAD} R_{shunt}} \quad (8)$$

In the case where OFS=0, the Gain becomes

$$Gain = \frac{V_{out}}{V_{in}} = \frac{\Delta_{CM\_out\_LSB}}{\Delta_{CM\_in\_LSB}} \quad (9)$$

Note: Values in Table 11 are valid only in case OFS=1024 LSB, that is the case where the values can be both positive and negative. As explained, OFS = 0 LSB and OFS = 90 LSB have to be used in case of DC-link configuration; in this case input voltage can be only positive and these gain values must be multiplied by 2. For example, in the case of the third input range, the total full-scale range is exactly 41.25 mV (it is not multiplied by 2 because there are not negative values).

The gain in the case of 5 V output is:

$$Gain = \frac{5V}{41.25\,mV} = 121.2 \quad (10)$$

That is exactly the gain we have in the case of OFS = 1024, multiplied by 2.

Gain values in case of OFS = 0 LSB and OFS = 90 LSB are then summarized in Table 12.

Table 12. Current monitor gain in case of OFS = 0 LSB and OFS = 90 LSB

CSM input range FULL SCALE	GAIN (output range: 0-3.3 V)	GAIN (output range: 0-5 V)
+10.29 mV	320.6	485.8
+20.59 mV	160.2	242.8
+41.25 mV	80	121.2
+103.12 mV	32	48.48
+185.62 mV	17.78	26.94
+329.99 mV	10	15.14

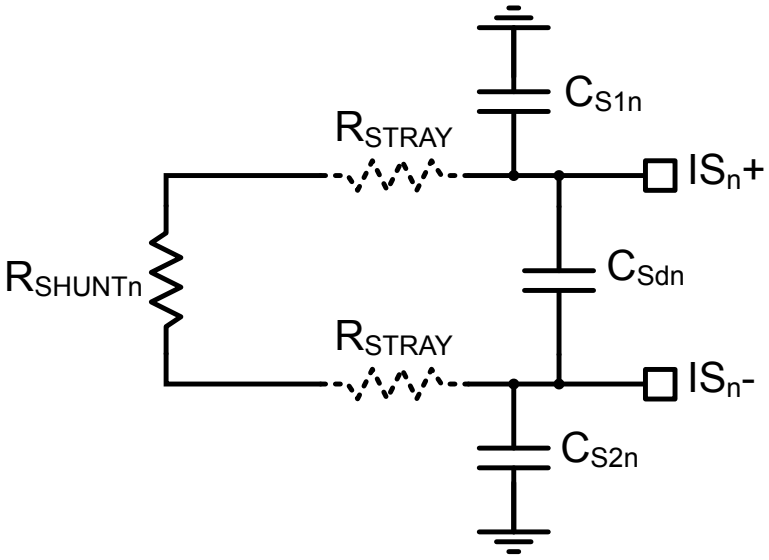
8.2 Applicative information

8.2.1 Input filter

User may evaluate the usage of a low pass RC filter between sense resistor and current monitor inputs, as illustrated in the application diagram (Figure 1 and Figure 2). C_{S1n} and C_{S2n} are for common-mode disturbances filtering, while C_{Sdn} is for filtering of differential disturbances.

Components selection must be performed by the user, who, knowing his own system should be aware about the minimum frequency above which noise is to be filtered. Components for this filter must be selected with the lowest tolerance; a mismatch between ISn+ and ISn- will result in a systematic error on current measurement. To prevent systematic gain error it is also recommended to avoid the use of resistors in series to the current monitor inputs due to the finite input resistance of the amplifier.

Figure 26. **Current monitor input filter**



Input filter sizing calculation example:

Assuming C_{S1n} = C_{S2n} << C_{Sdn}, we can estimate the frequency of the dominant pole for differential noise filtering as:

$$f_{p\_diff} \approx \frac{1}{2\pi C_{Sdn}(R_{SHUNTn} + 2R_{STRAY})} \quad (11)$$

While the common-mode cut-off frequency will be:

$$f_{p\_CM} = \frac{1}{2\pi C_{S2n} R_{STRAY}} \quad (12)$$

Where R_{STRAY} is the parasitic resistance of the PCB trace.

C_{Sdn}, should be selected in order to have the differential cut-off frequency 100 times bigger than PWM frequency and possibly smaller than half of CSA sampling frequency.

C_{S1n} and C_{S2n} should be the same value and at least 10 time smaller than C_{Sdn}.

8.2.2 Output filter

A low pass RC filter on CSOn pins is mandatory for signal stability. Suggested values are the following:

R_{CSOn} = 1 kΩ; C_{CSOn} = 220 pF; n = (1,2,3)

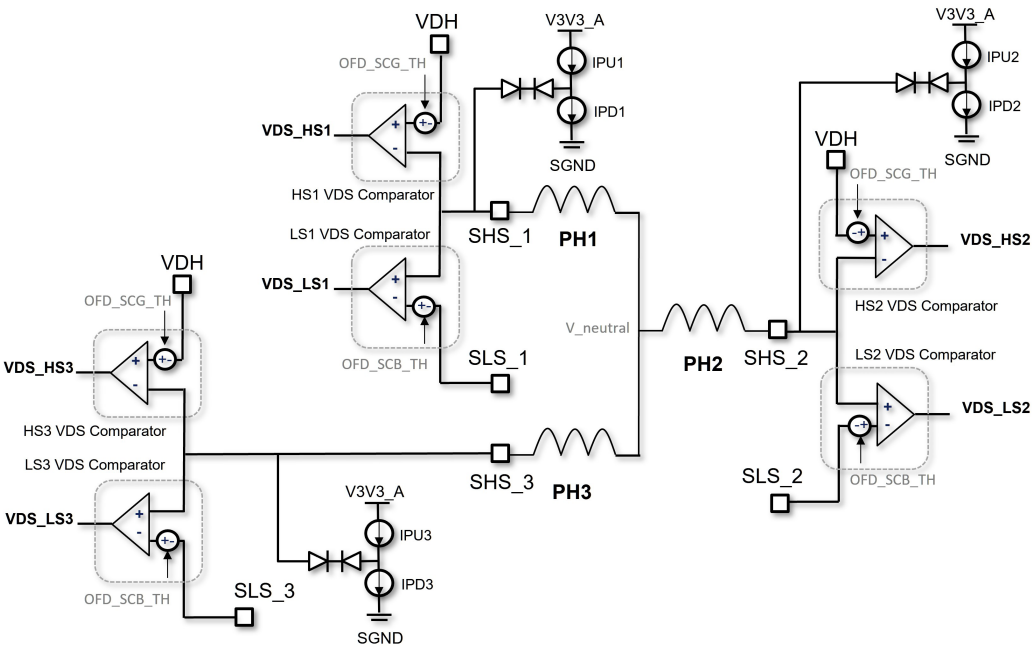
8.2.3 Shunt resistor selection

In high di/dt applications it is highly recommended to use a wide-terminal shunt resistor that shows minimum parasitic inductance with respect to a standard form factor. A small parasitic inductance helps reducing voltage under/over-shoot during current switching, therefore improving the CSA performance. With extremely high di/dt applications the usage of low inductance shunt resistor becomes mandatory to avoid CSA input pin AMR violation due to inductive under/overshoot.

9 Off state diagnosis (OFD)

The off-state diagnosis is available on L9908 by SPI request, provided that no actuation is in progress. During off-state diagnosis, multiple force stages and multiple monitor stages are activated. The principle of working is shown in Figure 27.

Figure 27. Off state diagnosis block diagram



To activate the diagnosis, user can choose the configuration, setting for each phase the bits, as summarized in Table 13. It means that, whenever OFD is enabled, on each phase, the pull-up or pull-down current generators referred to 3.3 V supply are activated, depending on the settings.

Table 13. Off state diagnosis enable bit

OFDn_EN1	OFDn_EN0	Description
0	0	Off State Diagnosis disabled (Default)
0	1	Pull-up current enabled, Pull-down current disabled
1	0	Pull-down current enabled, Pull-up current disabled
1	1	Off State Diagnosis disabled

The scheme works provided that:

- On one phase, the pull-up current generator is enabled
- On the other two phases, the pull-down current generators are activated

The levels at the outputs of VDS comparators are checked. Considering the threshold values for the detection of short conditions (see Figure 27), these outputs are at high level if:

- In case of VDS High-Side comparators, (VDH – 0.7 V) > SHSn
- In case of VDS Low-Side comparators, SHSn > SLSn + 1.7 V

In case of faulty conditions (phase shorted to battery or GND, open load), the outputs of these VDS comparators have voltage levels different from the expected values (all high levels in case of no-faults).

As an example, Table 14 shows the expected results when the pull-up current source is enabled on phase 2. The flag values reflect the voltage levels at the output of the corresponding VDS comparators.

Table 14. OFD fault detection table

Condition	OFD_EN[1:0]	Error flag	Description
3-Phase OFD [Three phase load]	OFD1 = 10 OFD2 = 01 OFD3 = 10	HS2_OFD = X(1) LS1_OFD = 0 LS2_OFD = 0 LS3_OFD = 0	Short to ground on one or multiple motor phase
		HS2_OFD = 0 LS1_OFD = 1 LS2_OFD = 1 LS3_OFD = 1	Short to battery on one or multiple motor phase
		HS2_OFD = X(1) LS1_OFD = 0 LS2_OFD = 1 LS3_OFD = 1	Open connection on motor phase 1 (SHS_1)
		HS2_OFD = X(1) LS1_OFD = 0 LS2_OFD = 1 LS3_OFD = 0	Open connection on motor phase 2 (SHS_2)
		HS2_OFD = X(1) LS1_OFD = 1 LS2_OFD = 1 LS3_OFD = 0	Open connection on motor phase 3 (SHS_3)
		HS2_OFD = 1 LS1_OFD = 1 LS2_OFD = 1 LS3_OFD = 1	No Fault

1. *Don't care.*

Particular attention deserves the case of “open” condition on the phase where the pull-up source is enabled (phase 2 in the example). In this case, the voltage on SHS2 is brought to a higher voltage level by the polarization currents acting on the stage of VDS monitor and High-Side pre-driver. On Figure 27, this contribution is represented by current generator ILEAK referred to CP_OUT.

In a condition where VBP = VDH = 12 V for example:

(VDH – 0.7 V) < SHS2 → the output of HS2 comparator goes low → HS2_OFD = 0.

The connection of a pull-down resistor between SHS and GND helps to decrease the voltage value on SHS below (VDH-0.7 V). In this case HS2_OFD = 1.

In any cases the user can consider that the combinations:

- HS2_ OFD = 0
- LS1_ OFD = 0
- LS2_ OFD = 1
- LS3_ OFD = 0

does not correspond to any other faulty condition and can codify unambiguously the fault of phase 2 disconnection.

10 Dual L9908 system

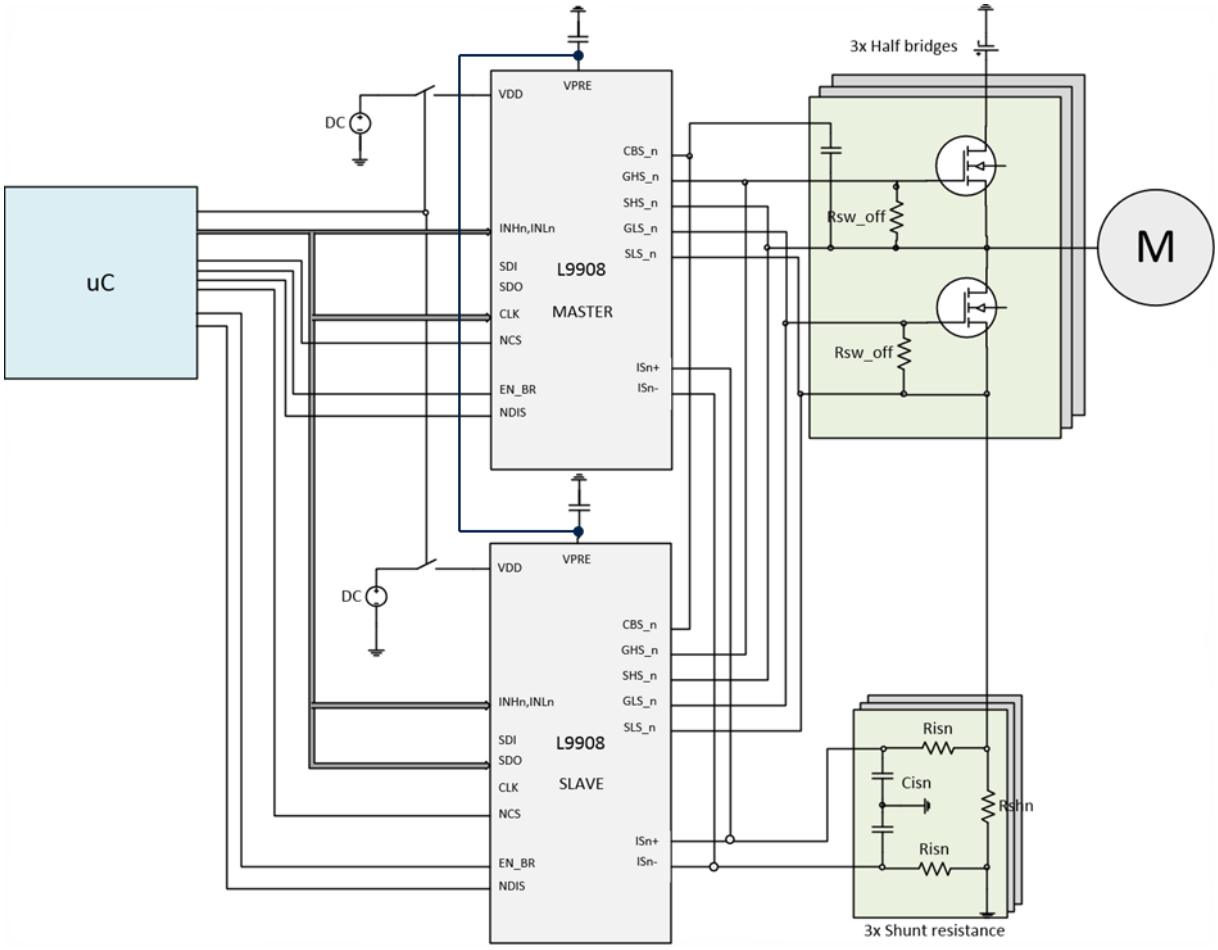
A possible application of L9908 is the Dual Device System, where 2 L9908 receive the same INL/INH driving signal from a microcontroller and are connected to the same power section.

Only one out of the two devices (Master) actively drives mosfets gates and provides current measurement feedback, while the second one (Slave), keeps its outputs in HiZ state, until it's commanded by the micro.

In case of Master's failure, as soon as the microcontroller detects the failure, it will disconnect Master L9908 from the mosfets by commanding it in HiZ; then it will command Slave L9908 out of HiZ. Such a system ensures almost seamless driving by switching from Master to Slave in less than 100 ms.

Dedicated Application Board and GUI had been developed to demonstrate and evaluate such system.

Figure 28. Dual L9908 system block diagram



In order that the system works correctly, Slave device (or Master, after the transition), must always be able to set predrivers in HiZ state. To do so, VDD must always be present. In case of lack of responsiveness from either the two devices, Microcontroller can toggle VDD to initialize the device and restore its HiZ state.

In case of VDD loss on Master, the device completely turns off and Slave device must be able to:

- Keep CPRE and CBSs capacitors charged.
- Keep pre-drivers in Hi-Z.

For these reasons, VPRE and CBSn pins of Master and Slave are shorted.

10.1 Master/Slave switching procedure

At startup phase both drivers are initialized, set to NORMAL mode, Master DRV_HIZ = 0, Slave DRV_HIZ = 1 and motor can be driven with Master unit.

Switching can be triggered by the following sources:

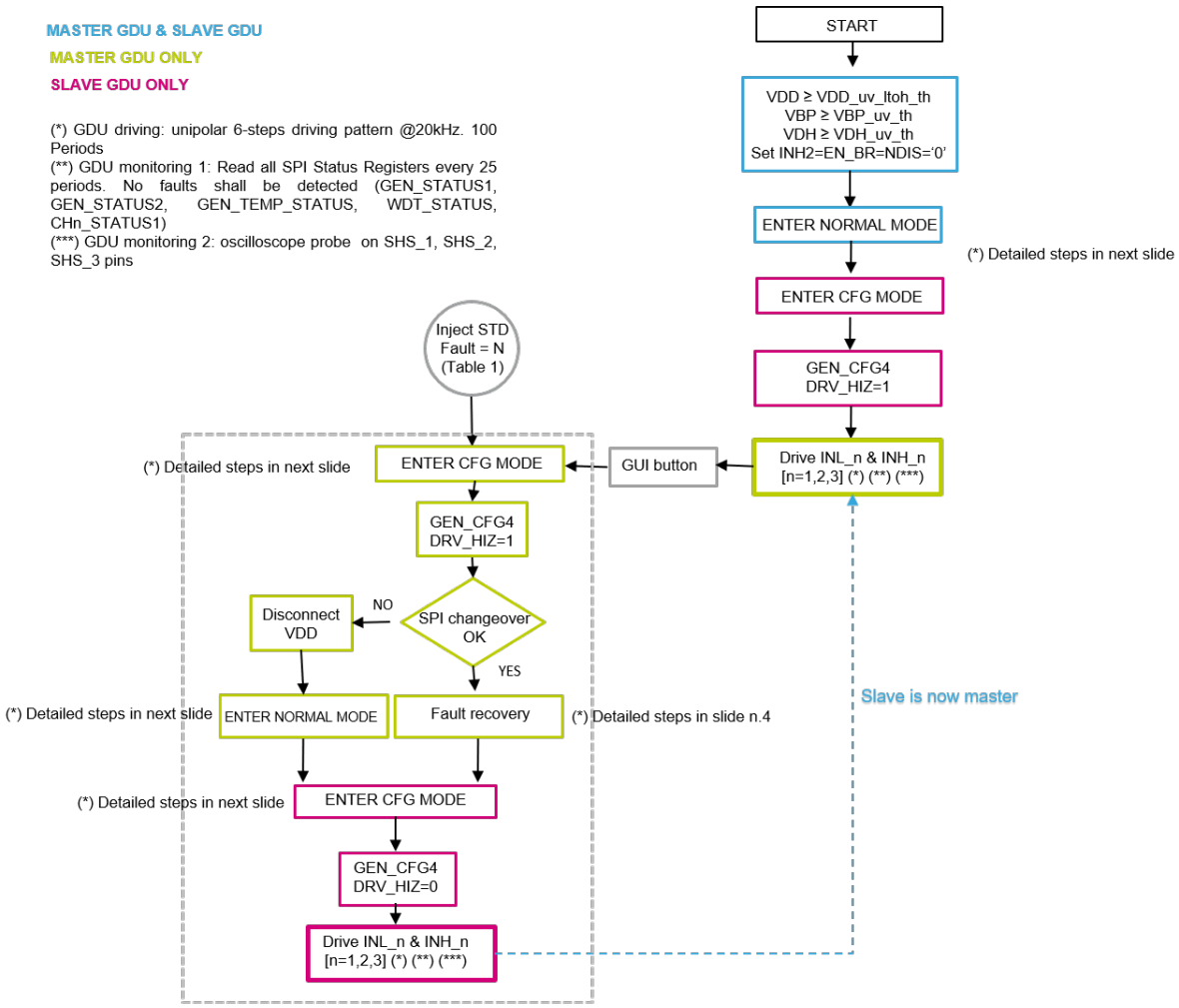
- by GUI through switching button
- by external fault (autoswitch)

When any of the two events occurs, microcontroller performs the Switching Procedure (detailed in Figure 29), supervising the following events:

- Set Master L9908 in CONFIG mode
- Set Master in HiZ
- Verify its SPI integrity - if not functional, power off the device
- Set Slave L9908 in CONFIG mode
- Bring Slave out of HiZ
- Set Slave L9908 in NORMAL mode

Now Slave is driving the motor, whereas inactive driver (previous Master) is performing fault recovery procedure.

Figure 29. Master/Slave switching flowchart



Next flowcharts detail “ENTER NORMAL MODE” and “FAULT RECOVERY” procedures mentioned above.

Figure 30. **Normal mode procedure**

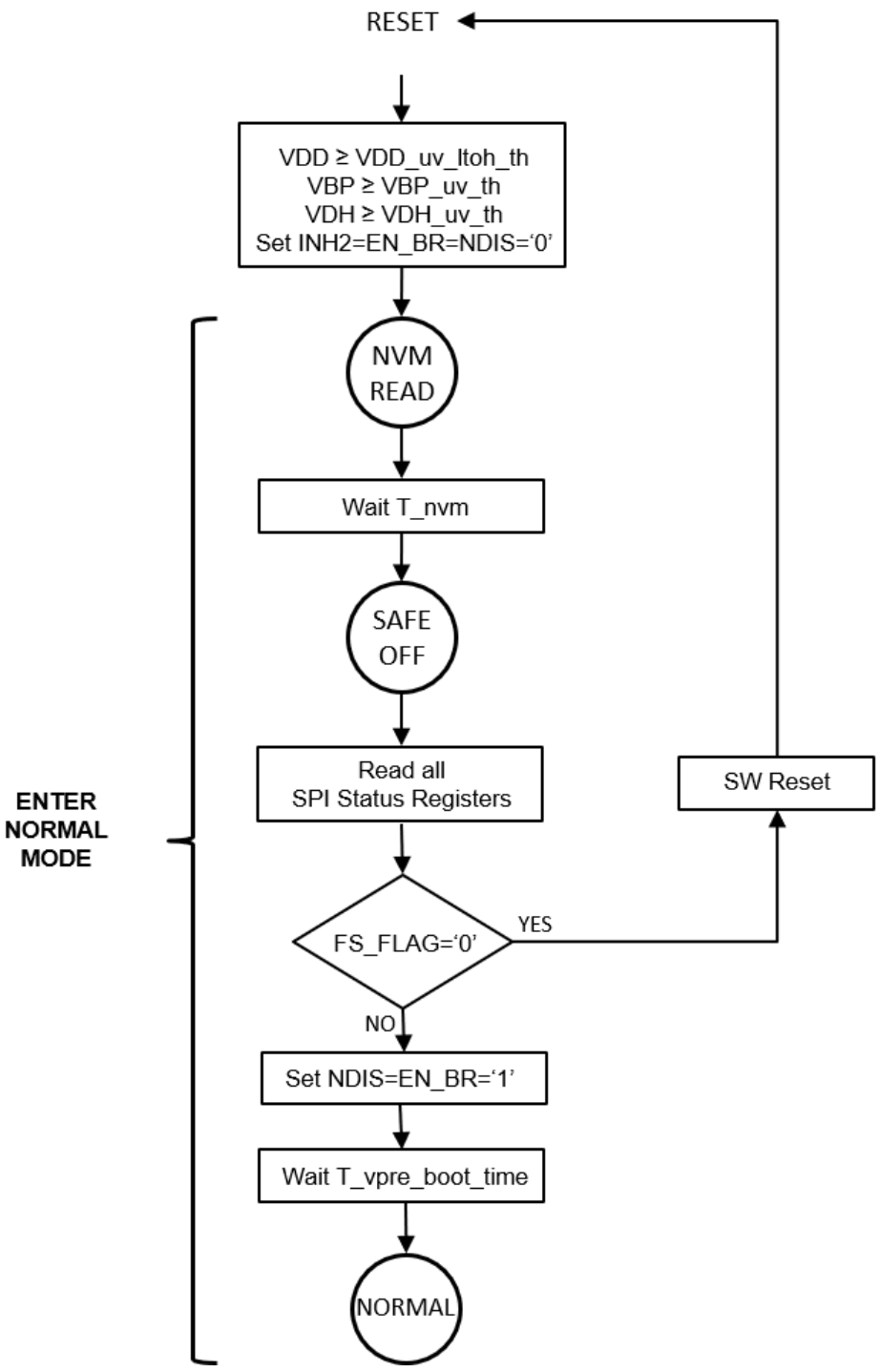


Figure 31. **Fault recovery procedure**

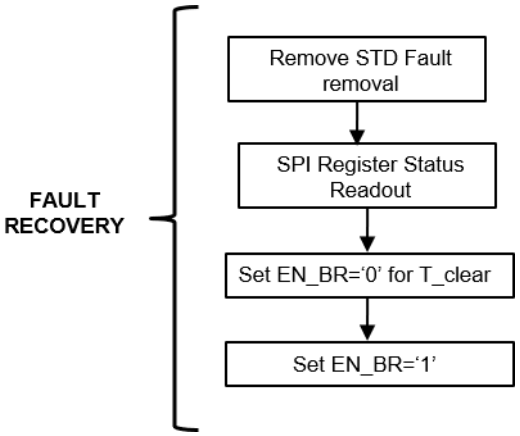
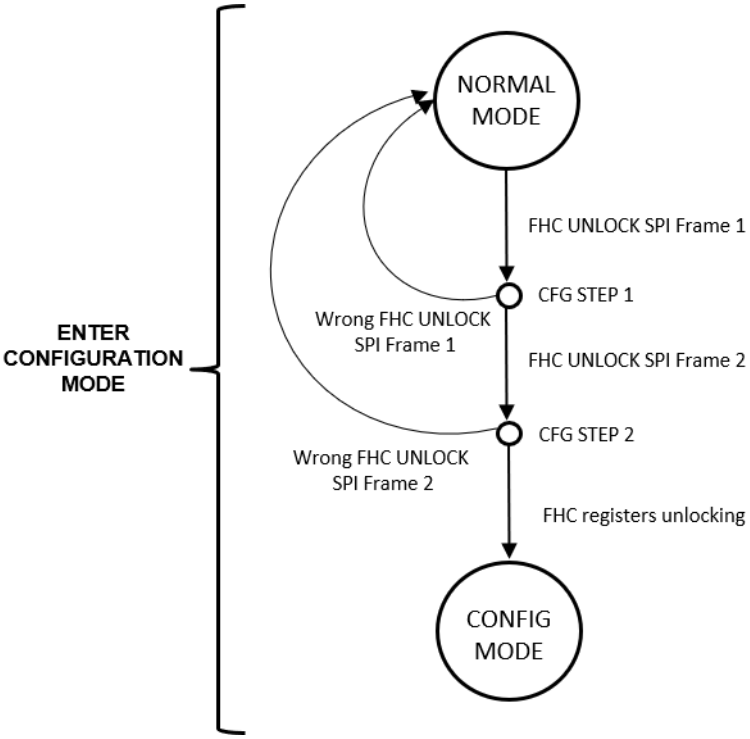


Figure 32. **Config mode procedure**



10.2 Demo board and GUI

A dual L9908 demo system based on SPC570S-DISP MCU eval board and a dedicated GUI has been developed to test the system.

Figure 33. Dual L9908 demo system

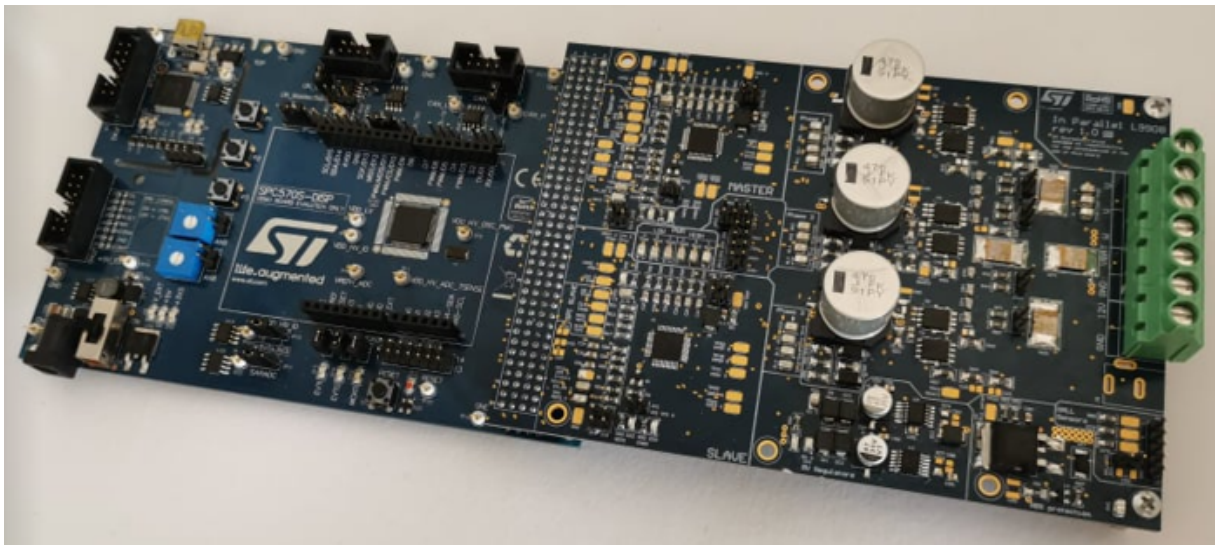
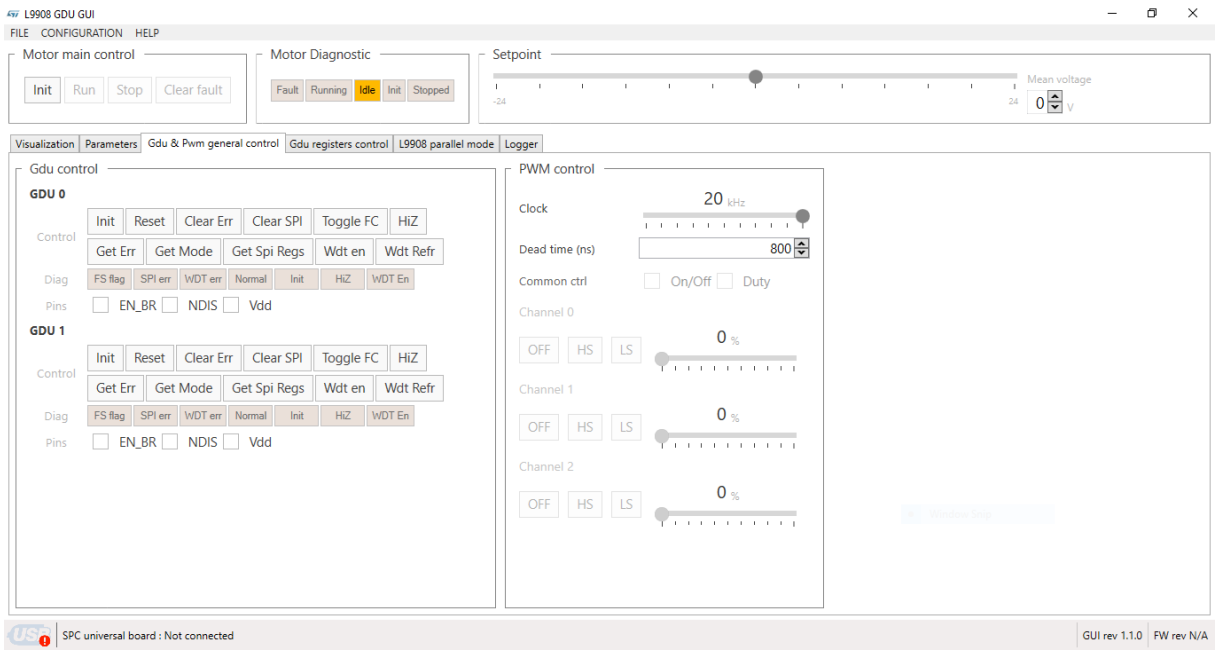


Figure 34. GUI main window



10.3 Test results

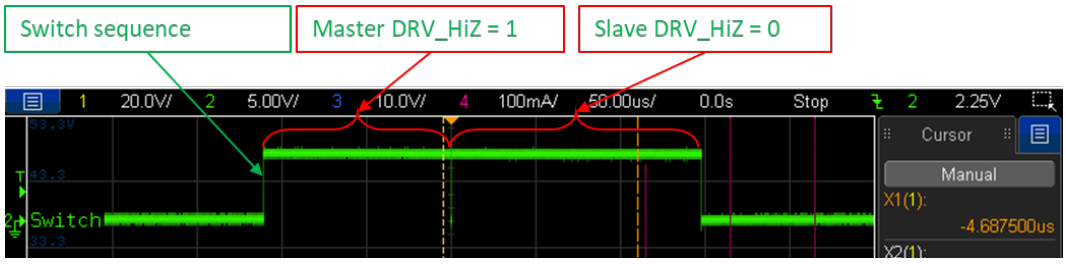
Using dual L9908 demo system and GUI, the following performances have been verified:

- Master/Slave transition time
- Phase current stability during transition

10.3.1 Master/Slave transition time

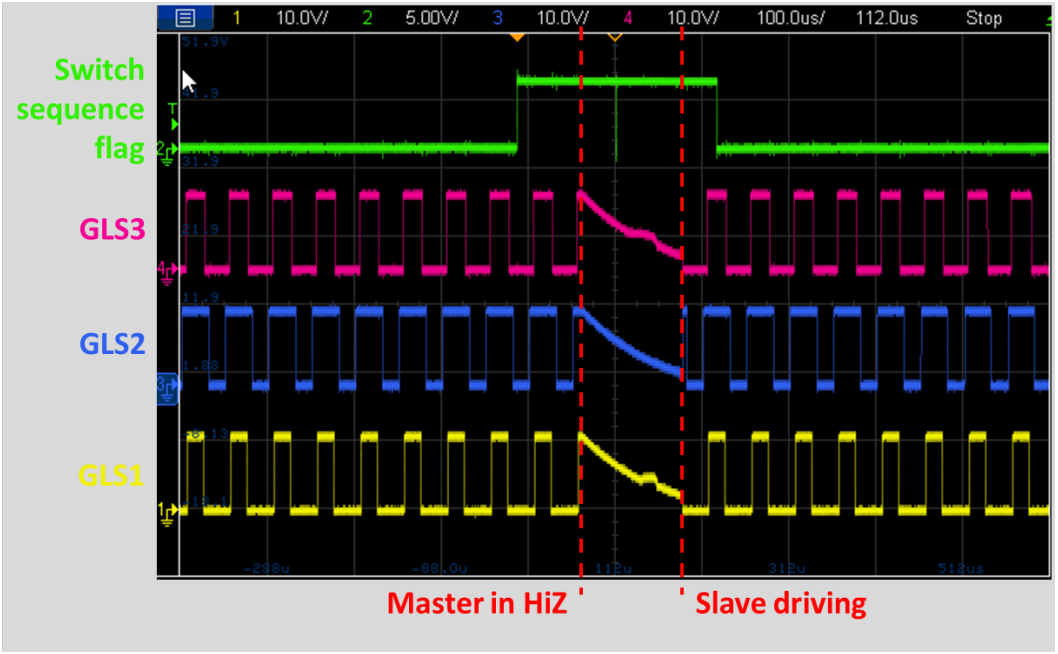
Transition time is defined as the interval between disconnection of Master predrivers from mosfets gates and engagement of Slave predrivers. For test purpose, the software switch sequence duration is flagged by a GPIO pin of the micro, so it can be probed with an oscilloscope; a quick toggling of this flag has been inserted in the instruction sequence to mark the instant when the SPI instruction to set Slave HiZ = 0 is issued by the micro.

Figure 35. Transition time probing



For this test, INLn / INHn inputs of both Master and Slave devices are provided by the micro with a fixed duty cycle, complementary pattern (i.e.: INH = not INL). Next figure shows the behaviour of gate lines during the transition:

Figure 36. Master to slave transition, gate lines

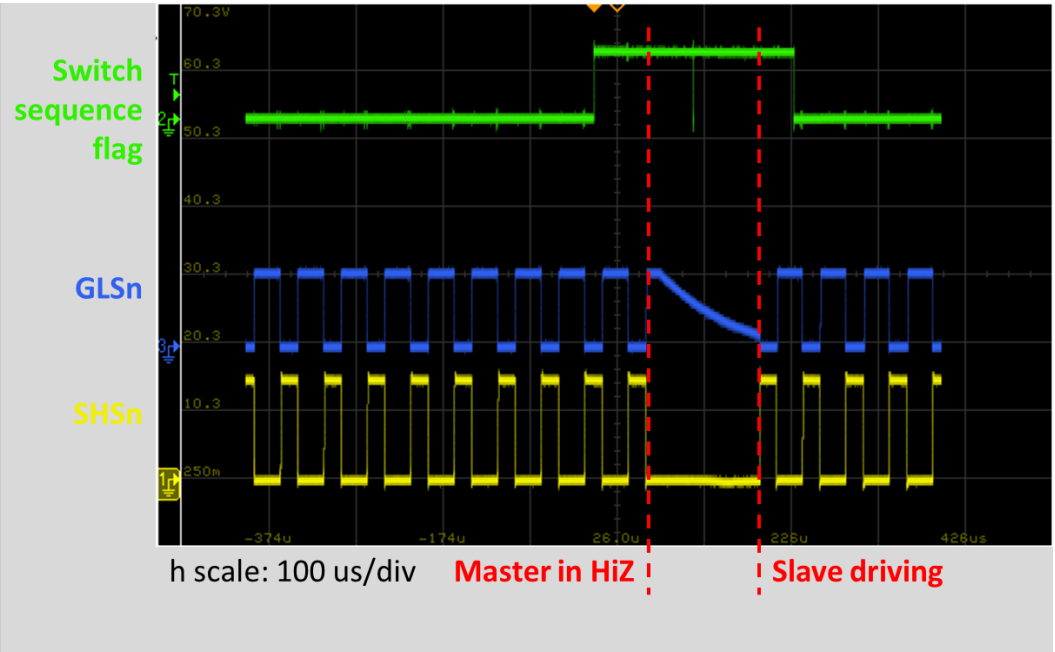


When GLSn signal stops toggling is the instant when Master's predriver has actually entered in HiZ mode. From that moment on, power mosfet gate isn't driven and starts discharging through the gate-source resistor present on the board. In the meanwhile, Slave predriver is commanded out of HiZ and starts driving mosfets according to the INL/INH pattern provided by microcontroller.

Actual transition time is shorter than the switch sequence flag duration and it's less than 200 µs.

Next figure shows a gate and a phase line during the transition.

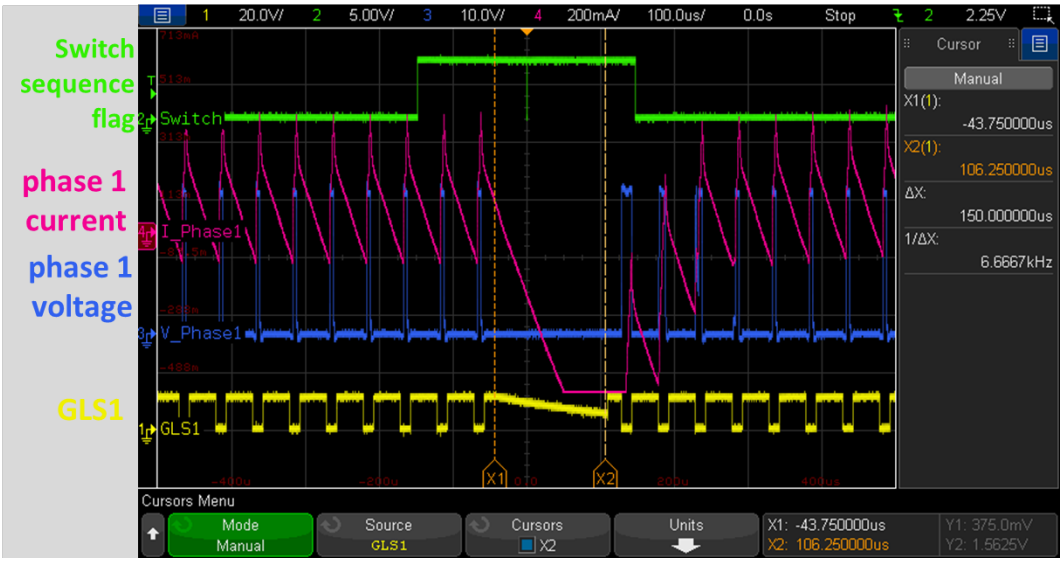
Figure 37. **Master to slave transition, gate and phase line**



10.3.2 Phase current during transition time

Possible deviance of motor output current during disconnection of Master driver and activation of Slave driver have been checked with the same setup.

Figure 38. **Master to slave transition, phase voltage and current**



10.3.3 Test conclusions

Bench tests have demonstrated the functionality of the dual L9908 system and its matching with expected performances. In particular:

- Transition time between Master and Slave of 300 µs full fills requirement (< 100 ms).
- The transition is reflected only by a very small voltage peak in the motor phase.
- Switching between Master and Slave doesn't affect smooth operation of the motor.
- Inactive driver doesn't affect behavior of active driver.

Revision history

Table 15. **Document revision history**

Date	Version	Changes
23-Mar-2021	1	Initial release.
28-Jun-2022	2	Added Section 8.2.3 Shunt resistor selection. Updated: • Figure 27. Off state diagnosis block diagram; • Figure 33. Dual L9908 demo system; • Section 1 Application circuit; • Section 3 Evaluation system; • Section 7.2.3 Bootstrap capacitor charging; • Section 8.2.1 Input filter. Minor text changes in Table 2. Pin list description.

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