SR5E1 line - 7 KW EV/HEV on-board-charger reference design

Introduction

The STDES-7KWOBC is an on-board charger (OBC) reference design based on SR5E1 (Stellar E) automotive microcontroller that allows charging the battery of electric vehicles (EV) via the electrical power grid supporting both residential and commercial AC charging methods.

The reference design incorporates two sections: an interleaved totem pole PFC with SiC and a dual galvanic isolated full bridge LLC DC-DC ZVS resonant converter, based on MDmesh DM6 superjunction power MOSFETs.

The power platform is a 7 kW module able to deliver a constant current (CC) or constant voltage (CV) on the output to be used as standalone (1 Ph+ N), in parallel or in 3-phase mode (3Ph + N) to reach 21 kW.

The underlying insulated metal substrate (IMS) on aluminum base plate enables very effective heat dissipation, and the design supports forced air or liquid cooling methods.

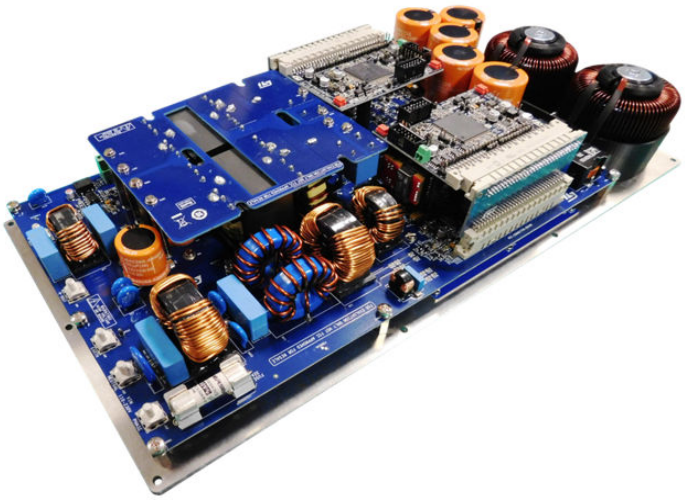
The design is modularized, making provision for scaling output power via simple interconnects between each power module.

This design places a high priority on both efficiency and power density, and this is made possible by a collection of semiconductor products tailored for power conversion applications. Among these are the SR5E1 automotive-grade microcontroller with Arm® architecture, gate drivers, SiC and SJ power MOSFETs, silicon and SiC diodes and SCR thyristors for inrush current limitation.

This reference design shows how it is possible to manage efficiently the two stages PFC and LLC either with two separated MCUs or single MCU thanks to the innovative timer capability and high performing ADC, comparator and high-resolution timer (HRTIM).

The STDES-7KWOBC is a fully assembled kit developed for performance evaluation only, and is not necessarily a production intent design that can be made available for sale.

Figure 1. STDES-7KWOBC reference design



Note: Fully assembled board developed for performance evaluation only, ***not available for sale***

1 System overview

1.1 STDES-7KWOBC

The STDES-7KWOBC features:

- Front-end PFC stage using 2-channel interleaved totem pole topology operating at 70 kHz
- Digital inrush current control
- DC-DC stage using FB LLC resonant topology with 140 kHz resonant frequency
- Constant current and constant voltage mode
- Control stage based on SR5E1
- 12 V input supply voltage galvanically isolated from output voltage GND (high-voltage battery)
- Bus bar interconnection possibility
- RoHs compliant
- PFC:
  - Key products: SR5E1 MCU controller
  - SCTH35N65G2V-7AG SiC power MOSFETs, TN3050H-12GY-TR SCRs, STBR3012G2Y bypass diodes, STGAP1AS gate driver
  - Input: 85 to 265 VAC, 45 to 65 Hz
  - Digital inrush current limiter
  - Max. input current: 32 Arms
  - Switching frequency: 70 kHz
  - Average current mode control in continuous conduction mode (CCM)
  - PID or 2p2z 2x independent current loop regulators
  - PID or 2p2pz voltage regulator
- DC-DC:
  - Key products: SR5E1 MCU controller
  - STB47N60DM6AG power MOSFET, STPSC20065GY-TR output diodes, A6387 gate driver

Output voltage: 250 to 450 VDC

- Switching frequency: 92 to 250 kHz with startup at 350 kHz
- Two independent current loops (CC)
- One voltage loop plus current balancing (CV)
- PID regulators

2 Safety and operating instructions

2.1 General precautions

Danger: *During assembly and operation, the STDES-7KWOBC poses several inherent hazards, including bare wires, and hot surfaces. There is danger of serious personal injury and damage to property if the DC-DC converter or its components are not used or installed correctly. All operations involving transportation, installation and use, and maintenance must be performed by skilled technical personnel able to understand and implement national accident prevention regulations. For the purposes of these basic safety instructions, "skilled technical personnel" are suitably qualified people who are familiar with the installation, use, and maintenance of power electronic systems.*

2.2 Reference design intended use

Refer to STDES-7KWOBC documentation for technical data and strictly observe them (see Appendix B Reference documents).

2.3 Electronics connection

Important: *The STDES-7KWOBC is intended for evaluation purposes only. Supply the reference design through an AC-DC source lab supply only. The electrical installation has to be completed in accordance with the appropriate requirements.*

2.4 Operating instructions

Warning: *Do not touch the reference design immediately after disconnection from the voltage supply as several parts and power terminals contain energized capacitors that need time to discharge. Do not touch the reference design after disconnection from the voltage supply as several parts like heat-sinks and transformers could still be very hot.*

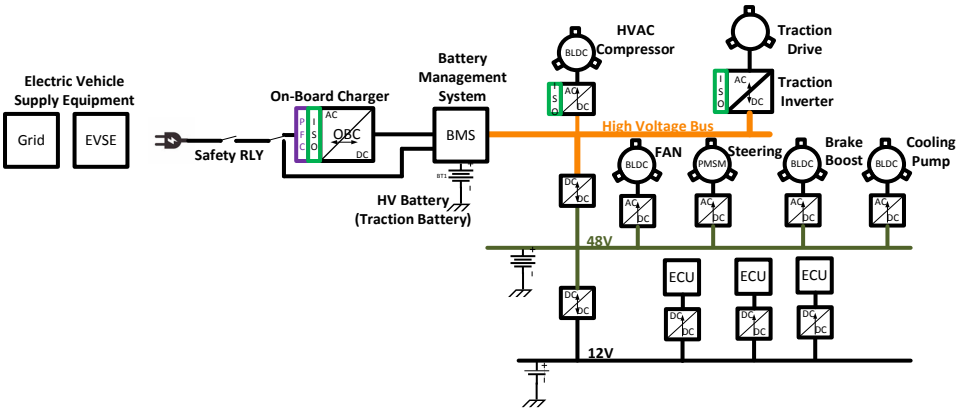
Important: *Always use the reference design with a plexiglass covering. Do not use the kit without the aluminum plate attached under the IMS. Always connect the earth ground connection to the input connector before you turn the reference design on.*

3 General description of OBC

A battery electric vehicle (BEV) transforms, stores, and consumes energy; and a typical representation of the systems associated with this energy flow is shown in the following figure. Electrical energy is provided by the 'grid' and is connected to the vehicle via electric vehicle supply equipment (EVSE). EVSE supplies either alternating current (AC) or direct current (DC). The vehicle incorporates an on-board charger (OBC); and its purpose is to convert AC to DC for use by the battery management system (BMS) to charge the battery pack. It is activated when the vehicle is connected to an EVSE that provides AC. AC chargers are less expensive; however, they typically require more time to charge the battery. The rate at which the battery is charged using alternating current is limited to either the power rating of the EVSE or the on-board charger (OBC), whichever is less.

The Stellar E (SR5E1) MCUs are designed to implement advanced digital power control that automotive applications demand; for more information, see SR5E1 documentation (see Appendix B Reference documents).

Figure 2. BEV electrical voltage domains



The term range anxiety stems from the idea that consumers compare their transportation experiences in BEVs with their long history of using internal combustion engine (ICE) based vehicles. ICE vehicles can travel for 300-600 miles on a single tank of fossil fuel. When the fuel tank needs to be filled, gas stations are prevalent, and once fueling is started the process requires about four minutes. Moreover, if the ICE car runs out of fuel in route, it is straightforward to use a container to transport fuel to the vehicle to enable it to travel 30 miles to the nearest gas station to fill it up. BEV engineers address range anxiety by:

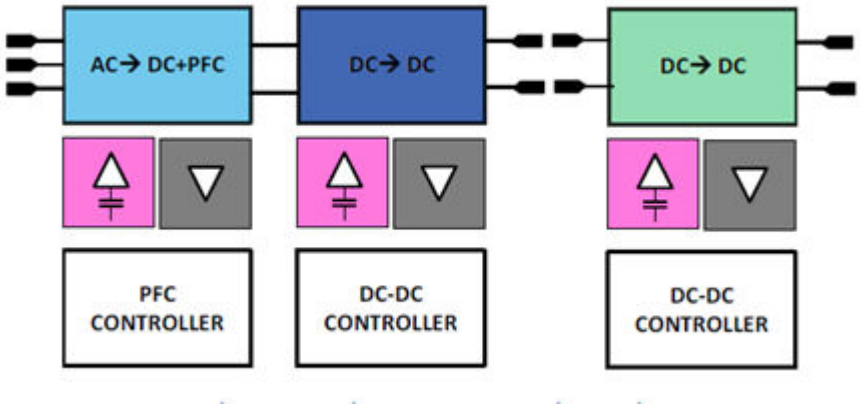
- Incorporating larger battery packs. This increases vehicle range; however, it requires substantially more charge time.
- Specifying higher ratings for the OBC. This reduces charge time if charging with an AC charger.
- Increasing maximum charge current accepted by the battery pack. This reduces charge time when charging with a DC charger.
- Optimize efficiency in systems that consume energy. The biggest consumers of energy in a BEV are the traction drive (which converts electricity into motion) and the compressor.
- Optimize power density (power delivered per m^2) and specific power (how much power per kg) for each system. Smaller and lighter systems can help increase vehicle range.

3.1 On-board charger

How the on-board charger (OBC) fits into the overall vehicle is mentioned in Figure 3. OBC and DC-DC converter integration example. Also discussed is the objective to increase the energy density and specific energy of vehicle systems (that is, designing things to be smaller and lighter to improve efficiency). The ability to charge the battery fully overnight is highly desired for most EV Level 1 and Level 2 chargers. With battery capacity increasing, the OBCs need to be designed for even higher power. With the increasing power capacity of the OBC, specifications such as power density and efficiency are even more important, due to limited space and cooling capacity in the car.

One approach is to combine systems that share common wiring and/or can leverage mechanization that may be required. BEVs include DC-DC converters to generate a different voltage domain to power certain ECUs. It is commonplace for a BEV to have three voltage domains: the DCLINK voltage that is typically 100s of volts, 48-Volts, and 12-Volts (used to power traditional legacy ECUs). One such approach to combine two systems is to implement an OBC and DC-DC converter into one module (in this way, certain electronic components can be shared, and other electromechanical systems leveraged (for example, the cooling system).

Figure 3. OBC and DC-DC converter integration example

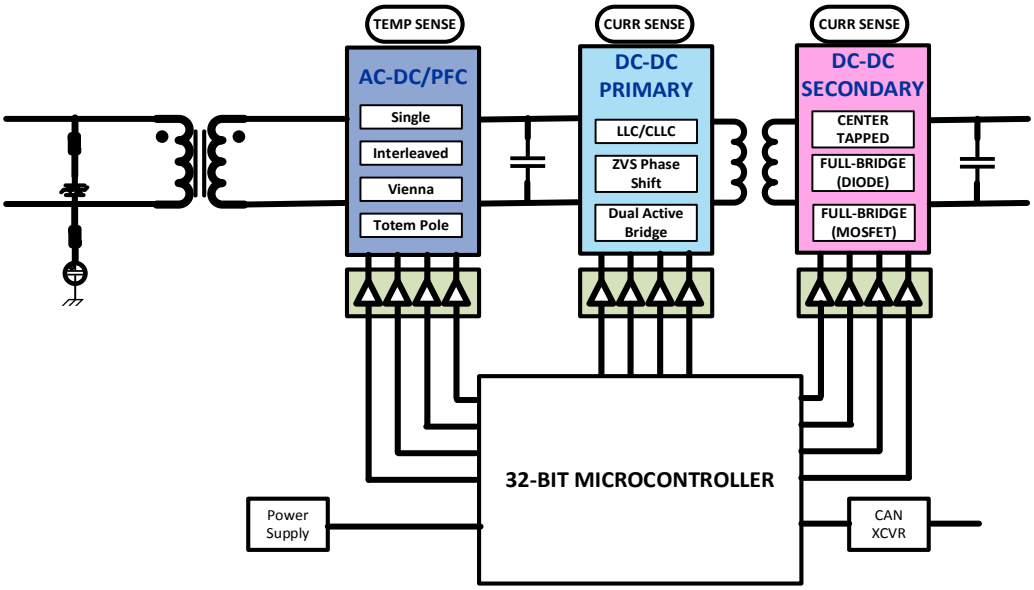


The figure above pictures the major sections on an OBC/BEV charger. There is a front-end that performs AC-DC conversion along with power factor correction (PFC). There is also a DC-DC converter section (primary and secondary side). This is not to be confused with the standalone DC-DC converter that is included in this applications example. Each section can be implemented using one of several architectural choices. These choices are determined by several considerations:

- Cost
- Size
- Efficiency
- Mono or bidirectional operation desired
- Single or poly-phase AC power input
- Thermal performance targets and budget
- Protection and diagnostics

In this application reference, as already mentioned, we cover the OBC (PFC+DCDC) case remanding to further application reference combined solution covering OBC+DCDC.

Figure 4. BEV charger architectures



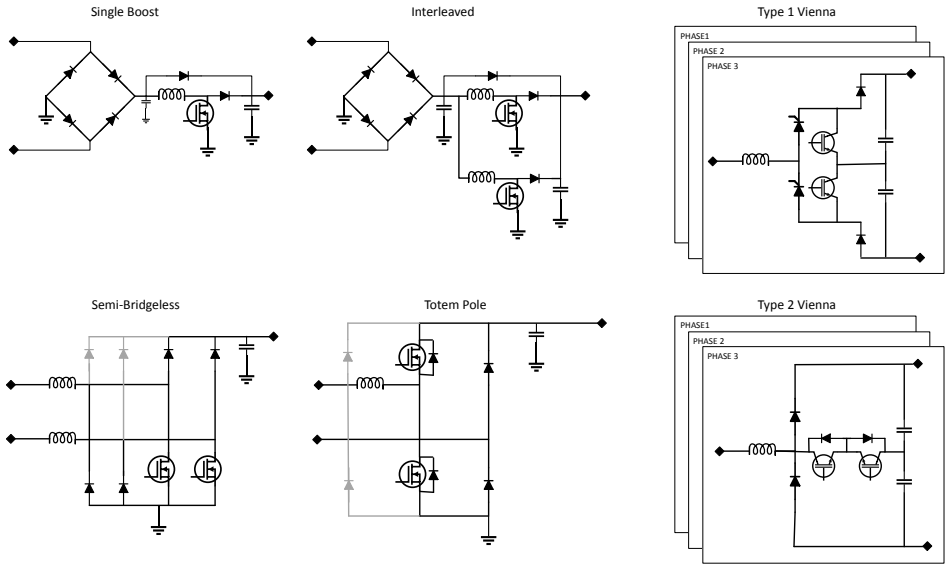
3.2 PFC: basic theory of operation for EV

Aside from emissions that are byproducts of power conversion in the OBC, harmonic distortion (and its associated emissions) is introduced as well. Any variation of the input impedance of the OBC that is a function of the voltage applied will cause distortion of the input current; and this reactance contributes not only to a degradation of power factor but also to an increase in conducted emissions. This non-linearity must be minimized to optimize power factor and minimize harmonic distortion.

PFC circuits employed in OBC typically incorporate a boost pre-regulator that forces the input current to track (that is, continuously be proportional to) the applied voltage. In theory, either the peak or the average current can be controlled by the PFC; however, in practice average current mode is generally used. The upper left side of Figure 5. Basic rectifier - PFC circuits shows a simplified block diagram of a boost pre-regulator that can implement PFC for a single phase and a 3-phase AC input. Note that on the single boosts topology the output of the rectifier lacks of a larger filter capacitor (it would normally be present in an AC-DC converter). Because PFC must continuously and quickly control the input current and output voltage; filter capacitors present are sized to attenuate ripple currents only. While this is a simplified representation, the fundamental operating principles are apparent. This approach has demonstrated very good (near unity PF) performance.

Power factor correction is employed due to the need to optimize efficiency and to comply with EMC requirements. In the United States, this entails FCC Part 15 Class A. For Europe, some of the relevant standards include IEC61000- 3-3, EN55011, and EN55022.

Figure 5. Basic rectifier - PFC circuits



3.3 Basic of boost converter

A boost converter steps up voltage (while stepping down current) from its input (supply) to its output (load).

Basic configuration (see Figure 6. Boost converter basic configuration) is composed by an inductor and a switch between a load(V_0) and a not regulated DC source (V_{NR}).

If the switch is in position 1 the input current flows to the ground. While in position 2 the input current flows on the load ($I=I_0$), if the capacitor is significant enough “to keep constant the output voltage during the commutation” we have the following conditions:

1. $$V_L = V_{NR} = L\frac{di_L}{dt} \Rightarrow \frac{di_L}{dt} = \frac{V_{NR}}{L}$$

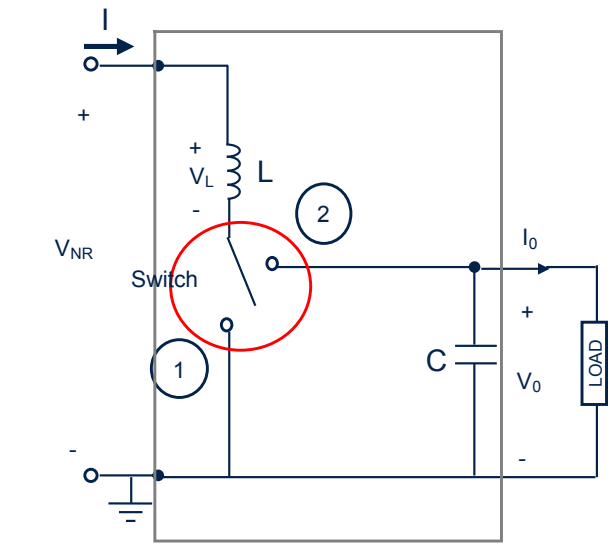
   L is charging and current grows linearly.

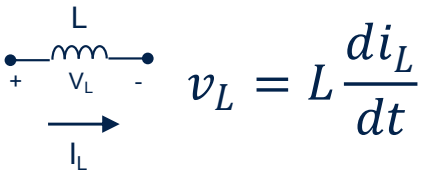
2. $$V_L = V_{NR} - V_0 = L\frac{di_L}{dt} \Rightarrow \frac{di_L}{dt} = \frac{V_{NR} - V_0}{L}$$

In the Hp of steady state, current is periodic. As shown in the plot the current ramp from B section has to reconnect to the ramp on the A section, therefore it is forced to decrease and L is discharging

$$\Rightarrow \frac{di_L}{dt} < 0 \Rightarrow V_0 > V_{NR}$$

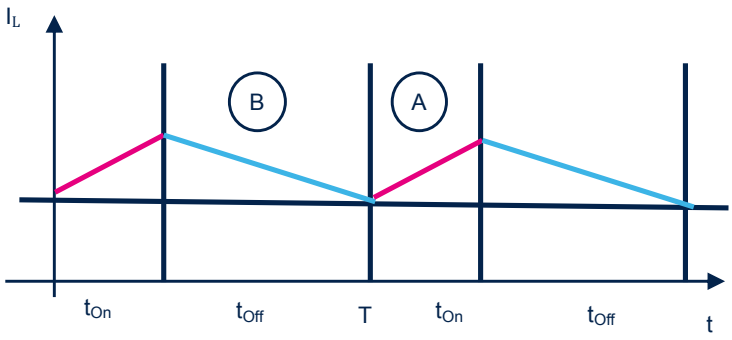
Figure 6. Boost converter basic configuration





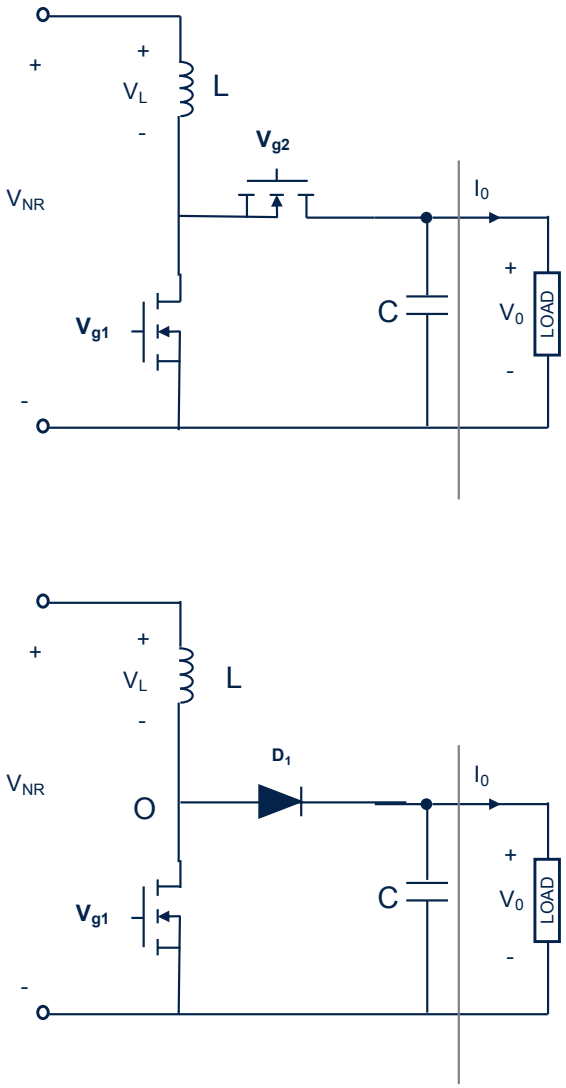
$$v_L = L\frac{di_L}{dt}$$

$V_L>0 \Rightarrow I_L \uparrow$
$V_L<0 \Rightarrow I_L \downarrow$



In electronic application instead of the switch we can use the below configuration (see the following figure).

Figure 7. Boost converter schematics



Let's try to determine a relation between input and output:
The average value of the voltage on the inductance is equal to 0,

$$\frac{1}{T}\int_0^T L\frac{di_L}{dt}dt = i(T) - i(0)$$

as per integral definition in the hypothesis of steady operations, current can be considered periodic, therefore:

$$i(T) = i(0)$$

$$\Rightarrow \int_0^T \frac{di_L}{dt}dt = 0$$

$$0 < D < 1 \Rightarrow \frac{V_0}{V_{NR}} > 1$$

the conversion ratio

$$\left({}^{V_0}/_{V_{NR}}\right)$$

is greater than 1

special cases are:

$$D = 0 \;\; V_0 = V_{NR}$$
$$D = 1 \;\; V_0 = \infty$$

3.4 PFC: Totem pole overview

Totem pole PFC is a bridgeless PFC that takes advantage of wide band gap devices (GaN or SiC) to reduce the number of components (body diode used as fast rectifier).

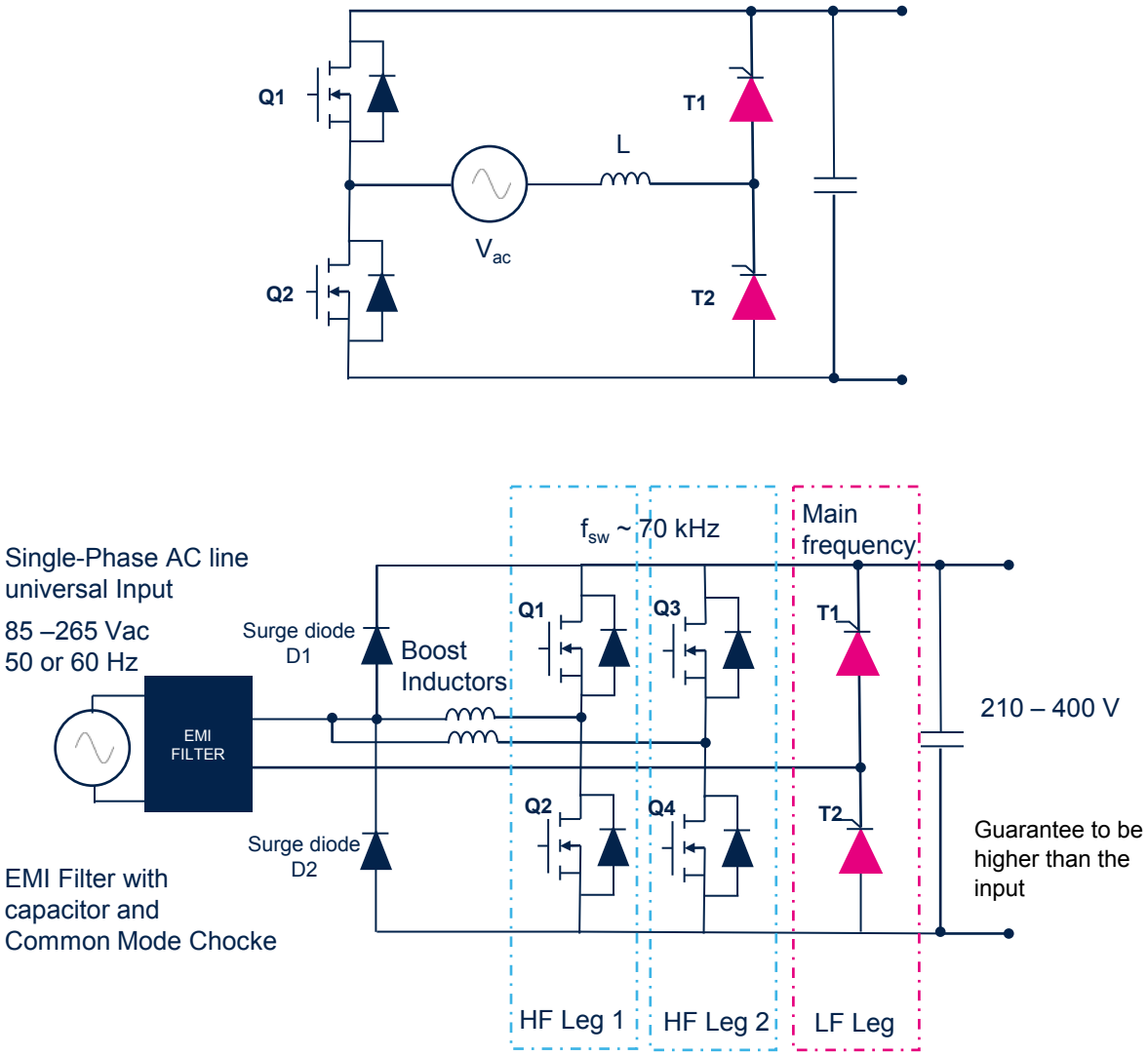
Totem pole PFC topology has a very high efficiency because:

- Do not have the rectifier bridge (less loss)
- Reduced number of components, wide band gap (SiC and GaN) is used not only as active device but also as synchronous rectifier of the boost diode (which must have a very good performance)
- This topology in continuous conduction mode (CCM), which is when the inductor current does not reach zero in the PWM period, requires wide band gap devices

Low frequency leg works at main frequency and can be composed of:

- Diodes
- SCRs (to limit the inrush current)
- MOSFET (to perform an SR increasing the efficiency)

Figure 8. **Totem pole: single and dual**



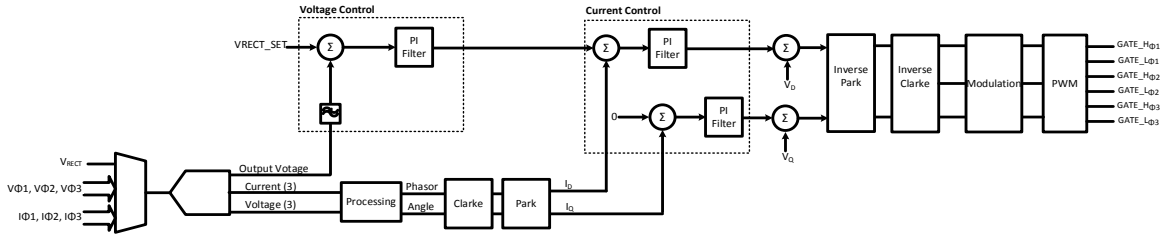
3.5 PFC: Control algorithm

The control algorithm must regulate the output voltage, attenuate reactive power and drive it to zero if possible. The Figure 20. PFC plant model comparison shows the inputs and outputs between the power electronics and the microcontroller. The measured parameters (inputs to the microcontroller) for the specific implementation shown in the Figure 9. Rectifier-PFC typical control loop example include:

- Phase currents (3)
- Line voltages (3)
- DC bus voltage

These measured values are used to calculate the voltage and current phasor and the angle between them. One possible control implementation is shown in Figure 29. Constant voltage with current control block. It takes advantage of PI loop control as well as employing field-oriented control to implement voltage control and power factor correction. The current is separated between real and reactive components and uses the loop to drive the reactive component to zero, thus accomplishing power factor correction.

Figure 9. **Rectifier-PFC typical control loop example**



What should not be lost here is that something that appears to be a simple function may require significant complexity in terms of control algorithms and computation. The control is typically tightly coupled to the hardware, which may require low latency and determinism. This has implications on the capabilities of the core, math acceleration, and peripherals in the microcontroller.

3.6 DCDC

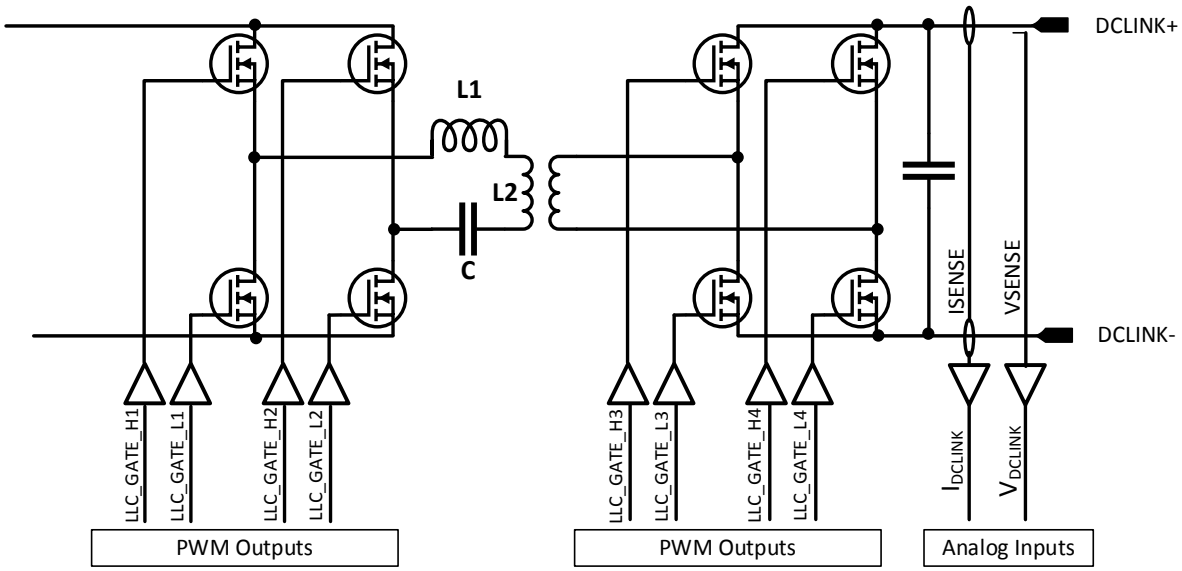
The Figure 10. DCDC converter shows a DCDC converter that generates the DCLINK voltage that is distributed throughout the vehicle to charge the battery and ultimately power the traction inverter and compressor. This specific implementation is called an LLC resonant converter because it incorporates two inductors and a capacitor as shown in the Figure 10. DCDC converter. DC-DC converter designs today operate at about 350 kHz, and efficiency targets give motivation for engineers to push this limit further.

Why LLC? Losses in power switches comprise two major components: switching and conduction losses. During switching times, the transistors pass through their linear region of operation and switching losses occur. It is intuitive, but faster switching transistors exhibit lower switching losses because they are in the linear region for less time. In addition, faster switching frequencies mean that smaller transformers, inductors, and filters may be used which helps address challenges to achieve power density design goals. The switching time is influenced by two primary factors: the characteristics of the transistor itself as well as the circuitry that drives the gate of the switch.

On the other hand, the OBC must address stringent requirements for emissions. Slamming the gate drive up and down generates harmonics and spurious that wreak havoc on emissions. Properly designed LLC resonant converters facilitate a compromise between switching frequency (which reduces switching losses and increases power density) and edge rate (which reduces emissions). The fundamental principle of operation is for the resonant frequency of the LLC circuit to coincide with the switching frequency of the power transistors; thus, the gates see a sinusoidal signal with a predictable and addressable emissions envelope instead of a pulse train with steep rise/fall times that generates spectral emissions that are more difficult and expensive to filter.

A key to the operation of the LLC resonant converter is that the inductance of the transformer is small enough that it affects the behavior of the resonant network at the desired switching frequency. Thus, the LLC resonant converter regulates its output well over a very wide range of load conditions.

Figure 10. **DCDC converter**



4 StellarE highlights - Key advantages

4.1 Description

The SR5E1x MCU family has been designed to meet the enhanced digital control and high-performance analog required by the new wide bandgap power technologies, silicon carbide and GaN, from power conversion applications such as on-board charger and DC/DC converters as well as advanced motor control like traction inverter applications.

SR5E1x also offers superior real-time and safe performance (including support for ASIL-D compliance), security cryptographic services (HSM) and high efficiency OTA reprogramming capability.

4.2 All features

- SR5 high-performance analog MCUs offering:
  - Digital and analog high-frequency control required by new wide-bandgap technologies (silicon carbide and gallium nitride)
  - Superior real-time and functional safety performance (ASIL-D capability)
  - Built-in fast and cost optimized OTA (over-the-air) reprogramming capability (with built-in dual image storage)
  - High-speed security cryptographic services (HSM)
- Cores
  - 2x 32-bit Arm® Cortex®M7 with double-precision FPU, L1 cache and DSP instructions
    - Split-lock configuration, allowing either two cores in parallel or one core in lockstep configuration
  - 2 DMA engines in lockstep configuration
- Memories
  - Up to 2 MB on-chip Flash memory with read while write support
    - 1920 KB code Flash memory split in two banks allowing 960 KB OTA reprogramming support
    - 160 KB HSM dedicated code Flash memory
  - 96 KB data Flash memory (64 KB + 32 KB dedicated to HSM)
  - 488 KB on-chip general-purpose SRAM:
    - 2x 32 KB instruction TCM + 2x 64 KB data TCM
    - 256 KB system RAM
    - 40 KB HSM dedicated system RAM
- Security: hardware security module (HSM)
  - On-chip high-performance security module with dedicated RAM and Flash
  - Based on Cortex®M0+ core
  - Hardware accelerator for symmetric cryptography
- Safety: comprehensive new generation ASIL-D safety concept
  - State of the art safety measures at all level of the architecture enabling an efficient implementation of ISO26262 ASIL-D functionality.
  - FCCU for collection and reaction to failure notifications with enhanced configurability
  - Memory error management unit (MEMU) for collection and reporting of error events in memories
  - Cyclic redundancy check (CRC) unit

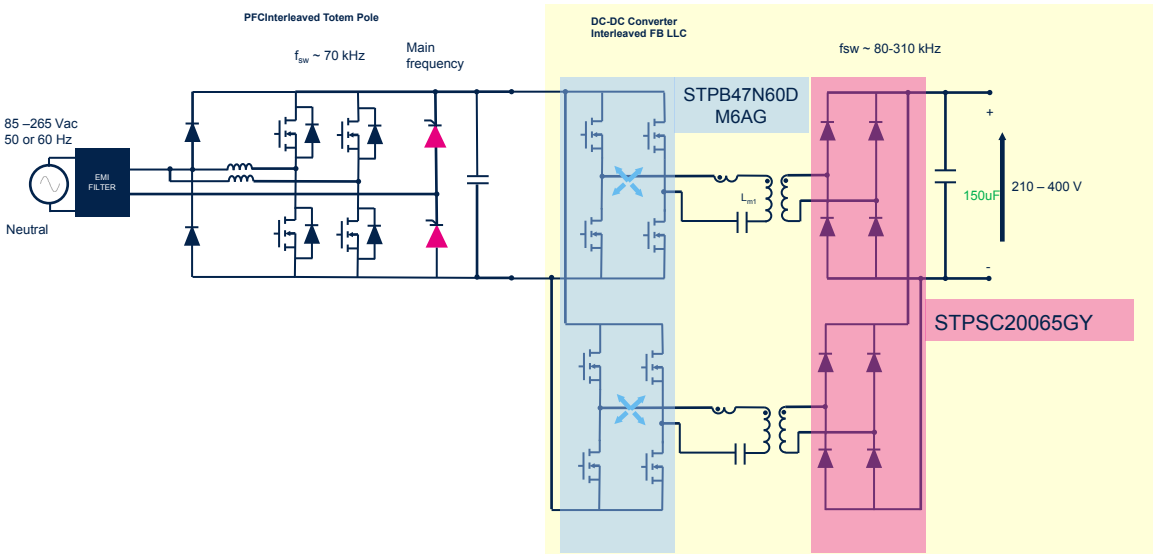
- Enhanced peripherals for fast control loop capability
  - 12 timers:
    - 2x HRTIM (high-resolution and complex waveform builder)
    - 2x advanced control timers
    - 2x 32-bit + 4x 16-bit general purpose timers
    - 2x basic timers
  - Enhanced analog-to-digital converter system with:
    - 5 SAR analog converters
    - 2 sigma-delta analog converters
  - Digital-to-analog converters (DAC)
    - 2 buffered external channels
    - 8 unbuffered internal channels
  - 8 comparators
  - Hardware accelerator
    - 1x CORDIC for trigonometric functions acceleration
- Communication interfaces
  - 4 modular controller area network (MCAN) modules, all supporting flexible data rate (ISO CAN-FD)
  - 3 UART modules with LIN functionality
  - 4 serial peripheral interface (SPI) modules, 2 multiplexed with I²S interfaces
  - 2 I²C modules
- Advanced debug and trace for high-performance automotive application development
  - Built around Arm® CoreSight™-600
  - Debug interface: Arm® CoreSight™ JTAG (IEEE 1149.1) or SWD
  - Embedded trace FIFO for both on- and off-chip tracing
  - Trace port for off-chip tracing: parallel trace port configurable from one to eight data lines

5 OBC reference design

5.1 System overview

The STDES-7KWOBC consists of an AC-DC totem pole PFC and a DC-DC LLC resonant converter as represented in the figure below.

Figure 11. STDES-7KWOBC topology



The switching frequency of the interleaved totem pole PFC is 70 kHz, whereas for the dual DC-DC LLC resonant converter is in the range of 80 to 310 kHz.

The interleaved totem pole features an inductor current balanced control while the DC-DC LLC features output current balance control. These functions ensure a balanced current of the parallel connection stages.

The AC-DC totem pole PFC section converts an input voltage of 85 V_{AC} to 265 VAC into 400 V. The maximum input current is 32 A at 50 Hz or 60 Hz.

The PFC works in continuous conduction mode (CCM). The TN3050H-12GY-TR SCR thyristors implement inrush current with a dynamic resistance of 14 mohm. PID or 2p2 controllers regulate the current via two independent current loop regulators. These controls are implemented on the SR5E1 MCU controller.

The second converter is the dual resonant DC-DC LLC based on superjunction MOSFETs.

The output DC-DC voltage is in the range of 250 V_{DC} to 450 V_{DC}. Two independent constant current loops (CC) and one constant voltage loop (CV) plus current balancing are implemented on a second SR5E1 MCU controller.

5.2 Specifications

Table 1. STDES-7KWOBC electrical specifications

Parameter	Value
Input voltage	85 to 265 V_{AC}
Input frequency	45 to 65 Hz
Max. input current	32 Arms
PFC switching frequency	70 kHz
Output voltage	250 to 450 V_{DC}

Parameter	Value
DC-DC switching frequency	92 to 250 kHz with startup at 350 kHz
Resonant frequency	140 kHz
DC-DC input	400 V
External input supply voltage	12 V

5.3 SR5E1 control board

The OBC requires two Stellar E1s (SR5E1) one for the PFC and one for DC-DC, which are connected to the driver board through a standard 64-pin DIN 41612 connector with a specific pin-out for DSMPS applications.

The SR5E1 control board has been designed following the adopted modular approach: the STMicroelectronics 64-pin DSMPS standard connector allows to save time in control board design and guarantees the reuse of control boards and code already developed.

The standard connector also allows the reuse of existing power boards to test the capabilities of new microcontroller families, like for the STDES-7KWOBC, initially designed for the SPC58 MCU and afterwards tested with SR5E1.

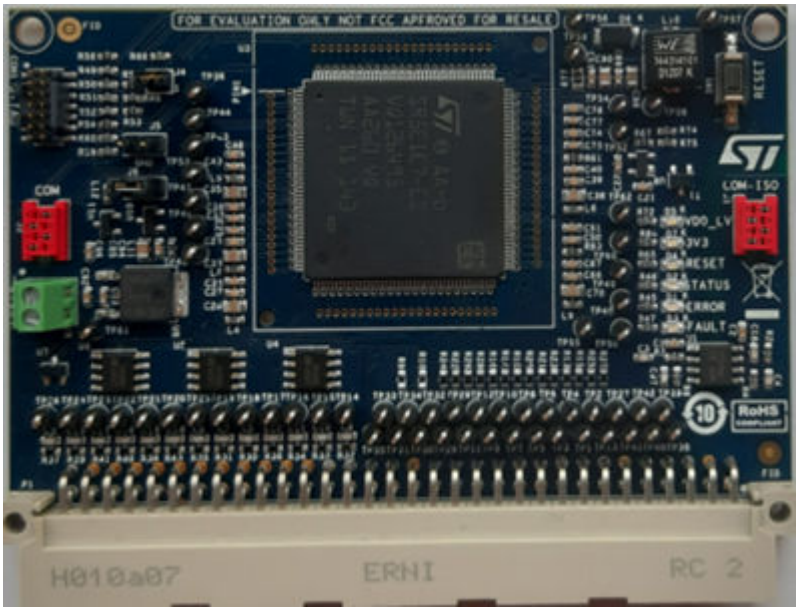
The SR5E1 control board is general purpose for DSMPS applications two of them have been used to control the PFC stage and DC/DC stage respectively, showing very good performances in control capabilities with a low CPU load.

At last, using a special connector, both PFC and DC/DC stages have been tested with a dual core microcontroller board, taking advantage of the SR5E1 multicore architecture see Section 5 OBC reference design.

The main features are:

- SR5E1 dual core MCU with 2x HRTIM V2 with Arm® architecture
- The same 64-pin DSMPS connector (DIN4162) as previous control boards (like for SPC58) for a modular approach
- Compatible with existing power boards
- Isolated UART for a board-to-board communication
- STD14 connector for programming and debugging with virtual COM support
- Connection for adapter board V2 to provide UART, CAN and SMBUS communication interfaces
- RC filters and clamps for analog signals
- Test point for each analog and digital signal
- Embedded 5 V/3.3 V voltage regulator
- LEDs for power-on, faults, errors, and status signaling
- ESD protections
- Embedded reset button
- MCU footprints: 176-pin, 176-pin with socket and 100-pin

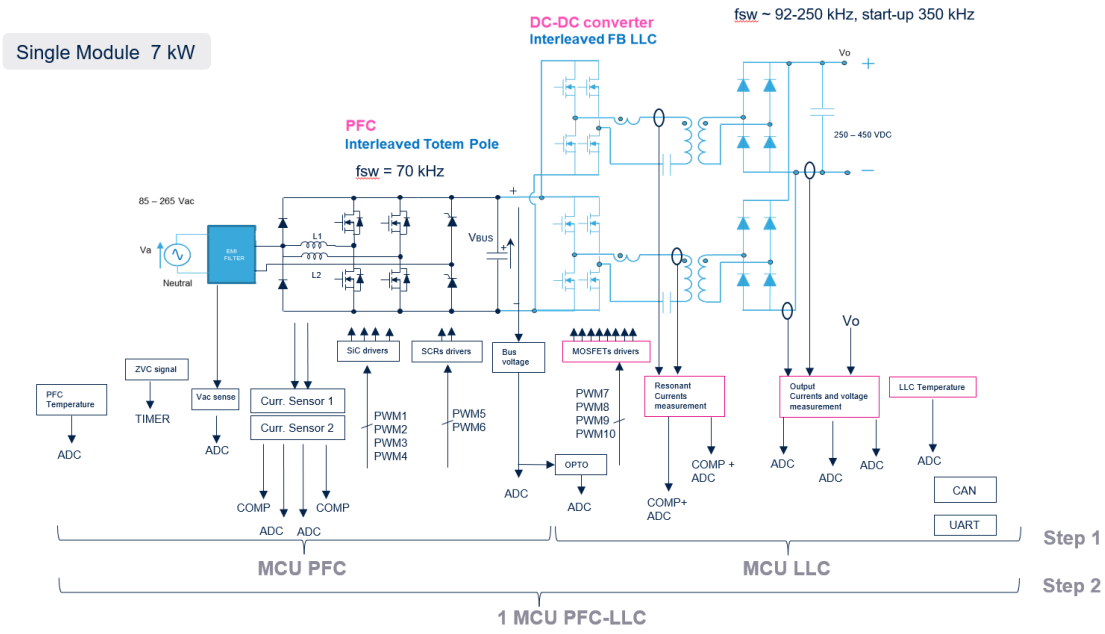
Figure 12. **SR5E1 control board**



5.4 MCU control signals

The following figure shows all the signals involved in the system.

Figure 13. **STDES-7KWOBC internal block schematic**



5.5 Power section functional area

The STDES-7KWOBC power section boards are based on insulated metal substrate (IMS) screwed on an aluminum base plate. This plate has a thickness of 3 mm for effective heat dissipation, forced air, or liquid cooling.

1. IMS thickness = 1.5 mm with 105 µm of copper; IMS substrate = 91 mm x 65 mm (DC-DC output diodes)
2. IMS: VT-4A1/VT-4A1; PP: thermal conductivity = 1.6 W/mK; ceramic filled aluminum thickness of 1.5 mm, dielectric layer of 100 µm, copper thickness of 105 µm
3. IMS substrate = 203 x 139 mm; PFC totem pole SiC MOSFETs plus LLC; DC-DC MOSFETs (PFC and DC-DC power part)
4. Aluminum baseplate thickness of 6 mm

Figure 14. STDES-7KWOBC - IMS positioning

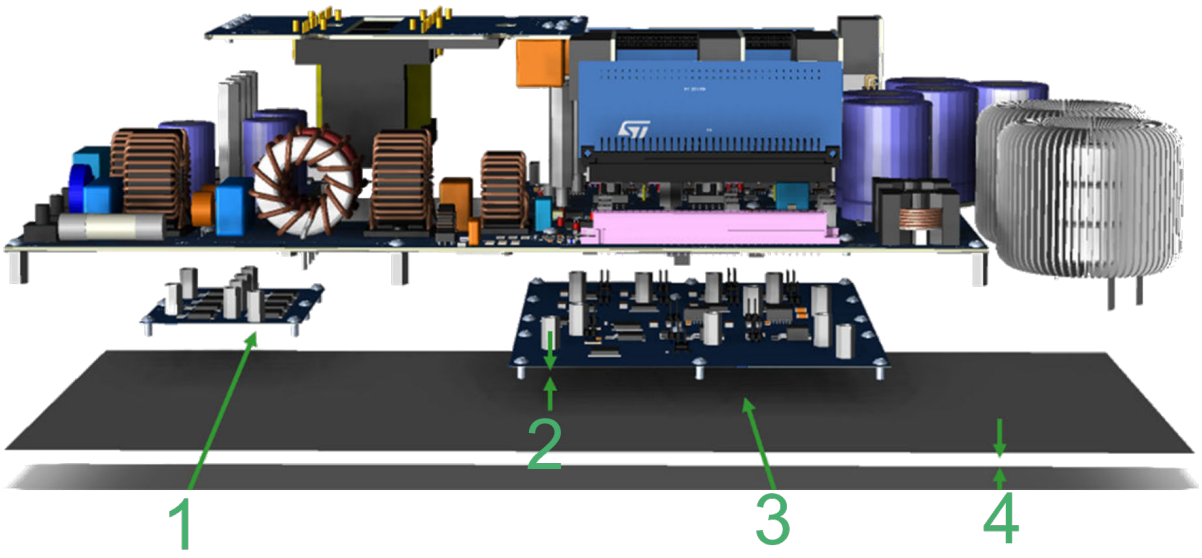
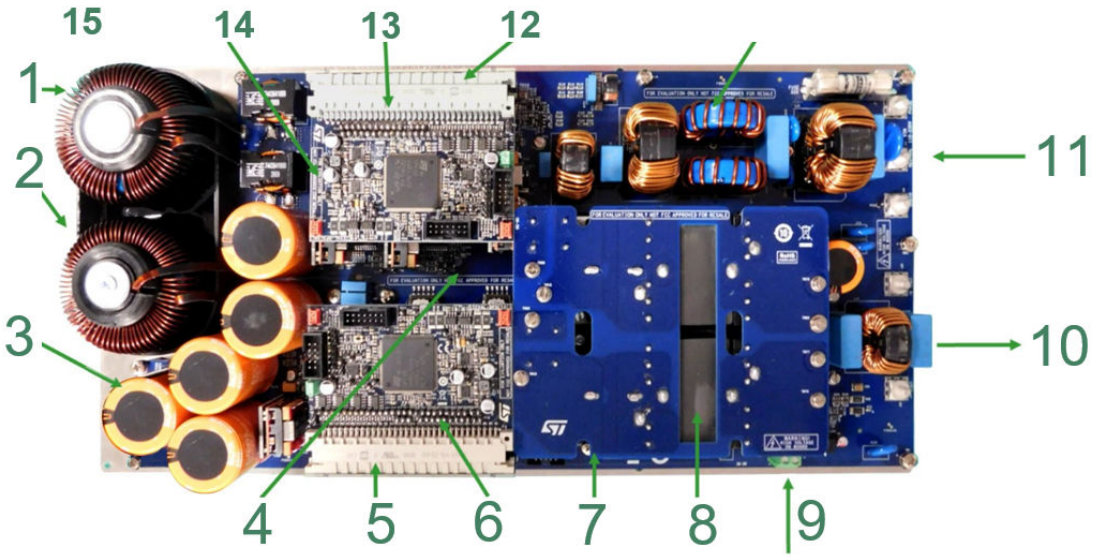


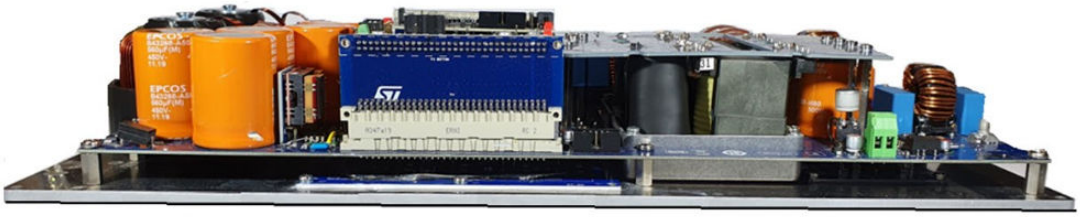
Figure 15. STDES-7KWOBC - functional areas (top view)



1. *PFC inductor*
2. *PFC inductor*
3. *Bulk capacitors*

4. *LLC current limit transformers*
5. *64-pin DSMPS connector*
6. *LLC control board*
7. *DC-DC resonant inductors*
8. *DC-DC transformers*
9. *External 12 V supply voltage*
10. *DC output voltage*
11. *AC input voltage*
12. *Input filter*
13. *64-pin DSMPS connector*
14. *PFC control board*
15. *DC-DC AUX supply*

Figure 16. STSTDES-7KWOBC functional areas (lateral view) - dimension: 200 x 420 x h 70



5.6 Control board and cable connections

The STDES-7KWOBC platform can manage up to 7 kW of power across the operating input voltage range. For functional and efficiency testing, use the following equipment:

- a 7500 W programmable AC voltage source
- 500 V max / 28 A DC electronic load
- a power analyzer (optional)
- a digital oscilloscope (optional)

Step 1. Connect the programmed control board to the 64-pin connector.
PFC section and LLC section work with different firmware.
The control boards of the platform are already programmed and ready to use, thus you do not need to load firmware.
To program a new control board, power it with an external 5 V supply through J3 connector of the control board.

Note: Do not connect the control board to the power board for this operation.

Note: Do not swap the control boards.

Step 2. Connect the programmable AC voltage source to the board AC input voltage, respecting the cross-section gauge to sustain 32 A.

Step 3. Connect the output load to J28-J29 connectors with a cable of appropriate cross-section to carry the desired load current (28 Amax.).

Note: Always connect the earth to the input connector.

Step 4. Ensure the STDES-7KWOBC is not powered.

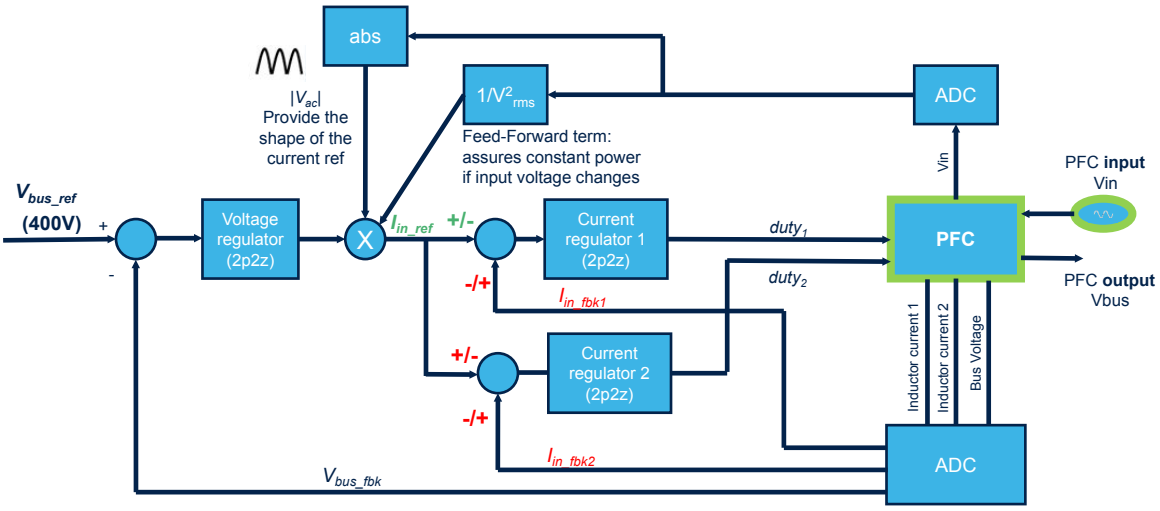
6 SW architecture and implementation

6.1 PFC control scheme

The PFC section is an interleaved totem pole that uses 2 x 510 µH inductors and 2240 µF bulk capacitors. The switching frequency is 70 kHz. The HF legs use SiC MOSFETs (STB47N60DM6AG) and the low frequency leg is SCR-based (TN3050H-12GY-TR).

This PFC is designed to work in continuous conduction mode (CCM) using average current control with two independent current loops (type II or PID), mains voltage feedforward, PWM startup at zero-crossing to avoid current spikes.

Figure 17. Average current control - block diagram



6.2 Voltage feedforward

The RMS mains voltage value (Vrms) allows calculating the input current reference:

$$i_{ref} = V_{reg\ out} \cdot \frac{|V_{mains}|}{V_{rms}^{2}}$$

Being the V_{rms} value proportional to mains average value, the last one is calculated using a digital low pass filter with 10.6 Hz cutoff frequency and 0.011 gain, in order to limit the third harmonic content at 0.75%, on current reference. TheFigure 18. Absolute sampled value of V_{mains} shows the result of the digital filter on a 6 kHz sampled test signal (red stars) comparing the result given by MATLAB® (blue squares) and what computed by the MCU (black dots).

Figure 18. **Absolute sampled value of V_{mains}**

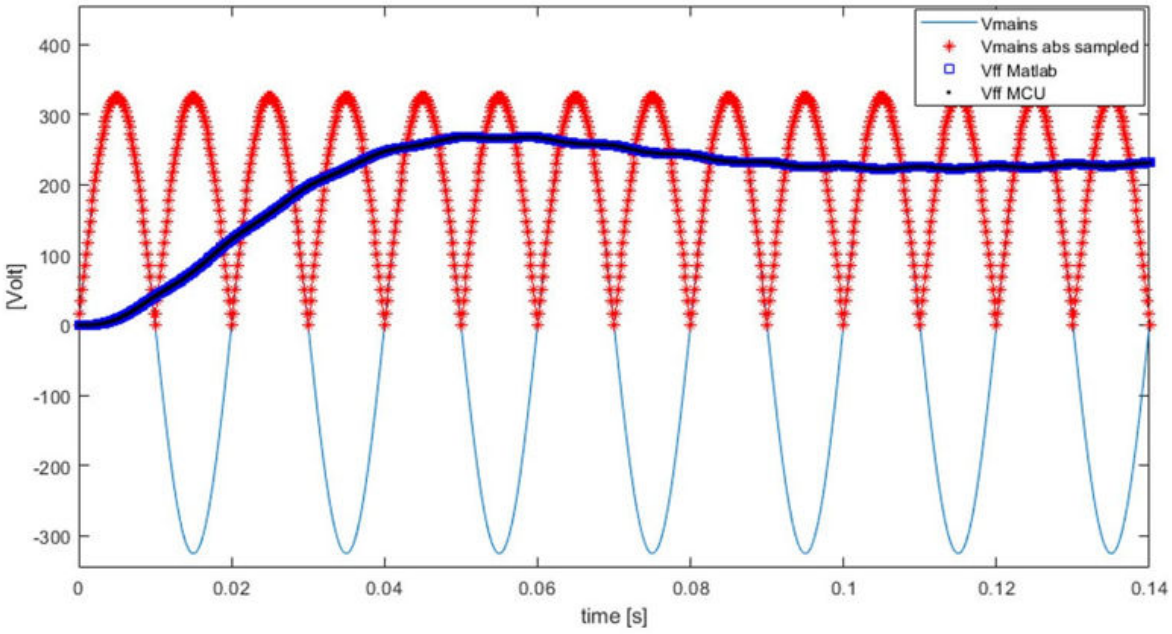
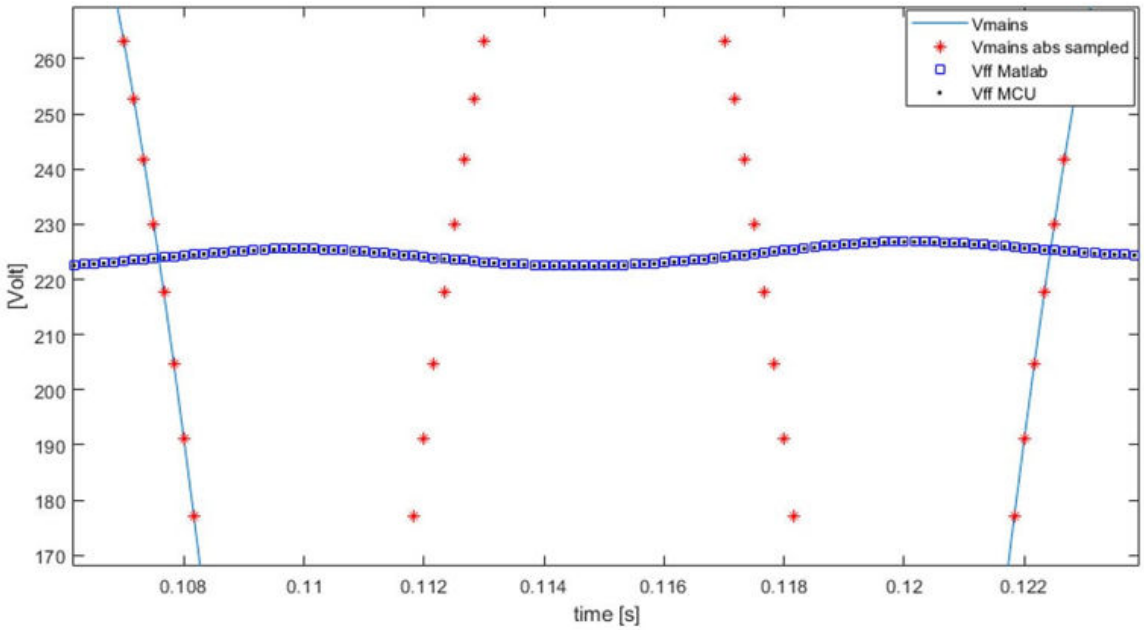


Figure 19. **Filter output comparison**



Note: $\frac{1}{V^2_{rms}}$ *assures constant power if input voltage changes;*

Note: *A low pass digital filter calculates Vrms to limit the second harmonic distortion, and then the third harmonic content of line current, in order to meet the EN-61000-3-2 standard;*

Note: *Digital filter parameters: mains voltage sampled at 6 kHz, third harmonic = 0.75%, gain = 0.011, cutoff frequency = 10.61 Hz;*

Note: *The filter is designed through MATLAB®; the output of the MATLAB® filter and the MCU results using a test signal ($V_{test} = 2\sqrt{.230}.\Pi(.50.t)$are the same.*

6.3 Type II digital controller

Used mostly for current controllers:

$$H(s) = \left(\frac{\omega_{p0}}{s}\right) \times \frac{\left(\frac{s}{\omega_{z1}} + 1\right)}{\left(\frac{s}{\omega_{p2}} + 1\right)}$$

Applying bilinear transformation

$$s = \frac{2}{T} \cdot \frac{1 - z^{-1}}{1 + z^{-1}}$$

we obtain a two-pole, two zero digital controller:

$$H[z] = \frac{y[z]}{x[z]} = \frac{B_2 z^{-2} + B_1 z^{-1} + B_0}{-A_2 z^{-2} + A_1 z^{-1} + 1}$$

Linear differential equation (LDE):

$$y[n] = A_1 y[n-1] + A_2 y[n-2] + B_0 x[n] + B_1 x[n-1] + B_2 x[n-2]$$

6.4 PFC current controller

Independent controllers for each HF leg executed cycle by cycle at PWM frequency (70 kHz).

Selectable PID or two-pole, two-zero controller.

Designed in frequency domain to satisfy the stability criteria of phase margin and crossover frequency ($\varphi m \geq 45°$), with Fx between 2 and 10 kHz.

LDE coefficient calculation executed in MATLAB® and pasted in C code.

Same results using exact or simplified plant model (at high frequency the exact model plot converges to the simplified plot).

Figure 20. PFC plant model comparison

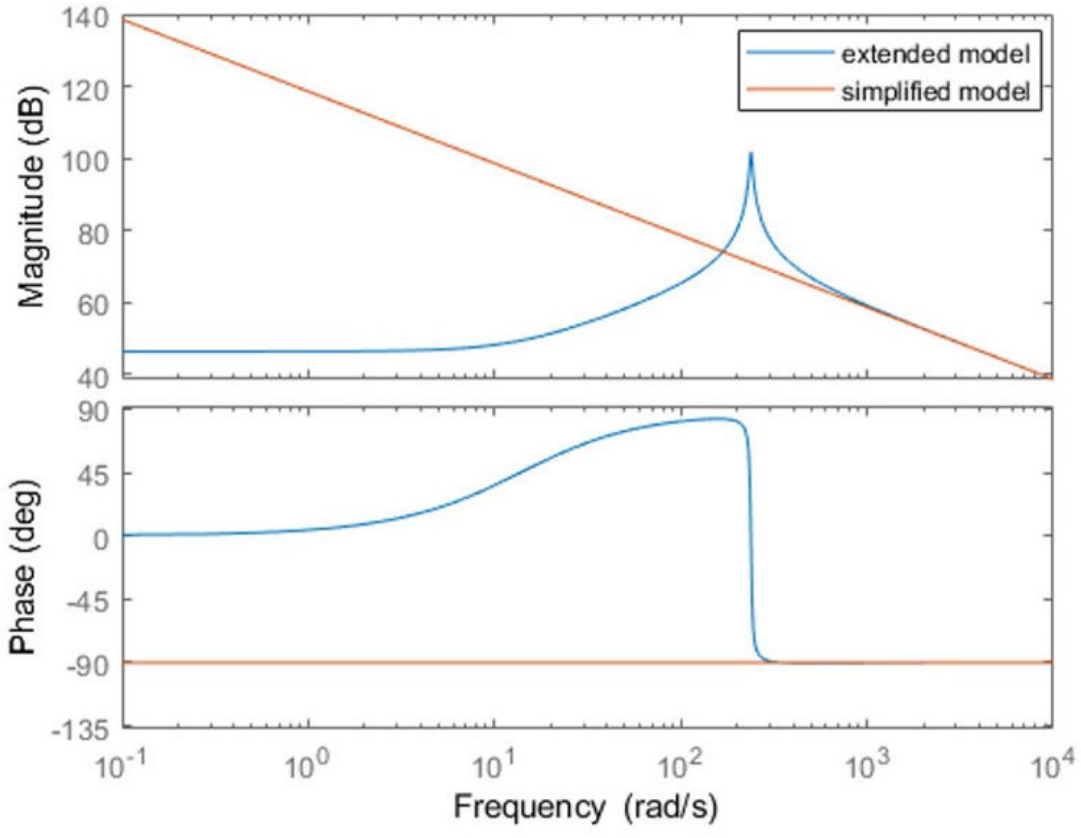
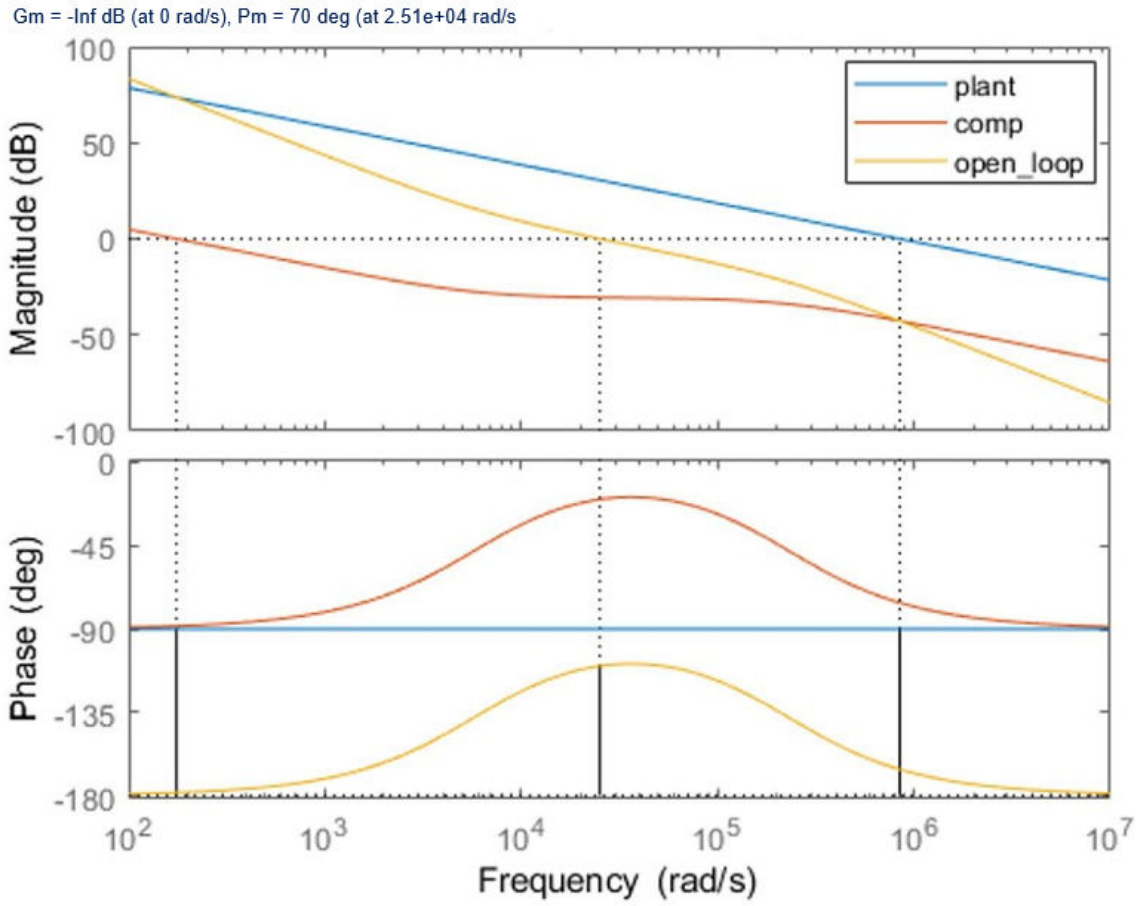


Figure 21. **Current loop design**



6.5 PFC voltage controller

Voltage control loop executed at 6 kHz (same frequency of feedforward calculation).

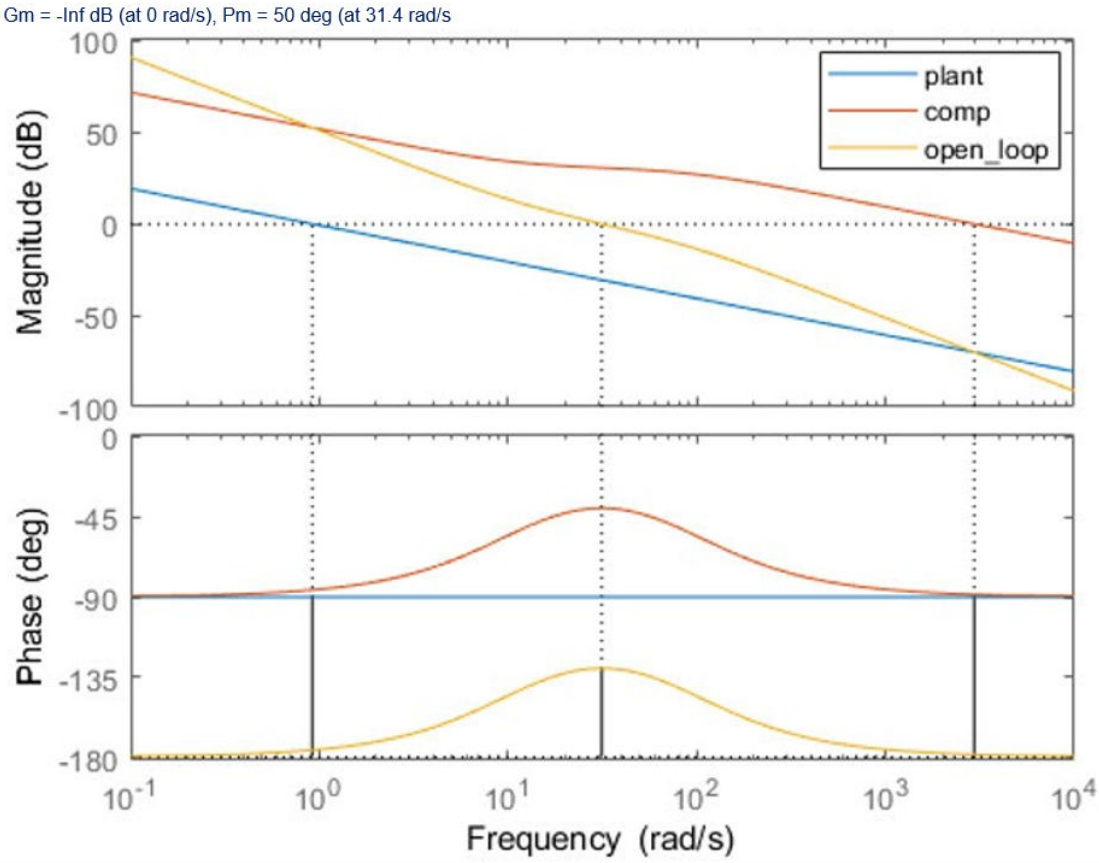
Selectable PID or two-pole, two-zero controller.

Designed in frequency domain to satisfy the stability criteria of phase margin and crossover frequency (*φm* around 50 or 60°), with Fx between 5 and 10 kHz .

LDE coefficient calculation executed in MATLAB® and pasted in C code/

After calculating the amplitude current reference (from voltage regulator output and feed forward), the current reference (iref) is built using the last V_{mains} value to shape the mains voltage.

Figure 22. **Voltage loop design**



6.6 Inrush current limiter

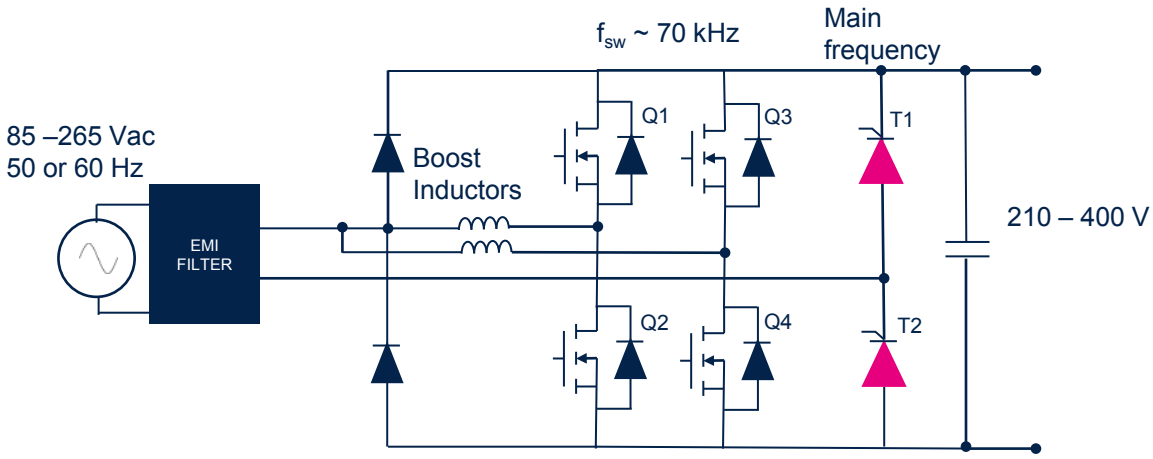
At startup, when DC bus capacitors are discharged, the mains might absorb a high current. Usually, an NTC resistor and a bypass relay can limit the inrush current.

Using SCRs in PFC low frequency leg and adopting a progressive phase control at board startup, you can limit inrush current without the need of NTC and relay.

At steady state, SCRs are driven with 50% duty cycle, and with a safe dead time, synchronized with the mains.

With the totem pole PFC using the SCRs, the bus capacitor can be smoothly charged with a progressive phase control, avoiding the use of an NTC or a resistor.

Figure 23. **Interleaved PFC totem pole topology with SCRs**



As long as the SCRs are not driven, the bridge does not conduct the current, and the DC bus capacitors are not charged. To start charging the DC capacitors, semiconductor controlled rectifier T1 and semiconductor controlled rectifier T2 have to be turned on according to the AC line voltage polarity (T1 is turned on when the AC line polarity is negative and T2 is turned on when the AC line polarity is positive).

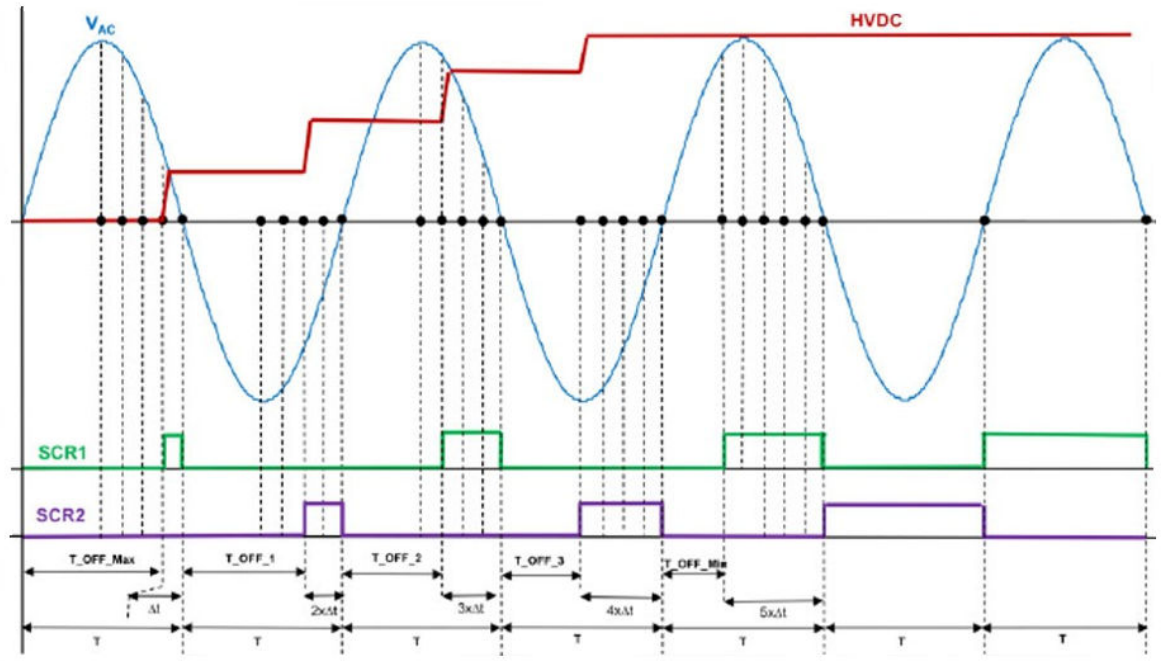
To reduce the inrush current, the SCRs are alternatively triggered at the end of the half line voltage cycle, just a few hundreds of microseconds before the line zero voltage. This allows the output capacitor to be charged to a low level (around 10 to 30 V) and not directly to the peak line voltage. The current driven from the line is then much lower than in the case of a direct full charge of the DC capacitor.

This soft start solution can work only when an inductor is present on the line side, as the rate of the current increase has also to be limited to prevent semiconductor controlled rectifier damage. The inductor is already present for most applications where the EMI filter usually embeds a common-mode choke, which has a differential mode parasitic inductor due to the copper turns of the windings.

To control the inrush current at PFC board startup with the SCRs, a solution has been implemented in the MCU firmware: the variable SCRs on the delays allow a complete charge of this capacitor to the peak line voltage.

SCRs have to be triggered on the subsequent half cycle with a shorter turn-on delay than the one used to start charging.

Figure 24. **SCRs driving signals and DC bus charging**



By reducing the semiconductor controlled rectifier turn-on delay by few tens or hundreds of microseconds from half-cycle to half-cycle, the output capacitor is progressively charged while the line current is kept low. The step of the SCR turn-on delay reduction is constant from one half-cycle to the following one.

The SCR1 and SCR2 TON start at 30 µs and 60 µs, respectively. Each TON is incremented step-by-step by a ΔT (30 µs) until reaching a quarter of the mains period. When the mains voltage reaches its peak value, then the ON time is equal to the half mains period, with a short time interval, before and after the mains zero-crossing, in which both devices are not driven (see the figure above).

6.7 SCR control signals

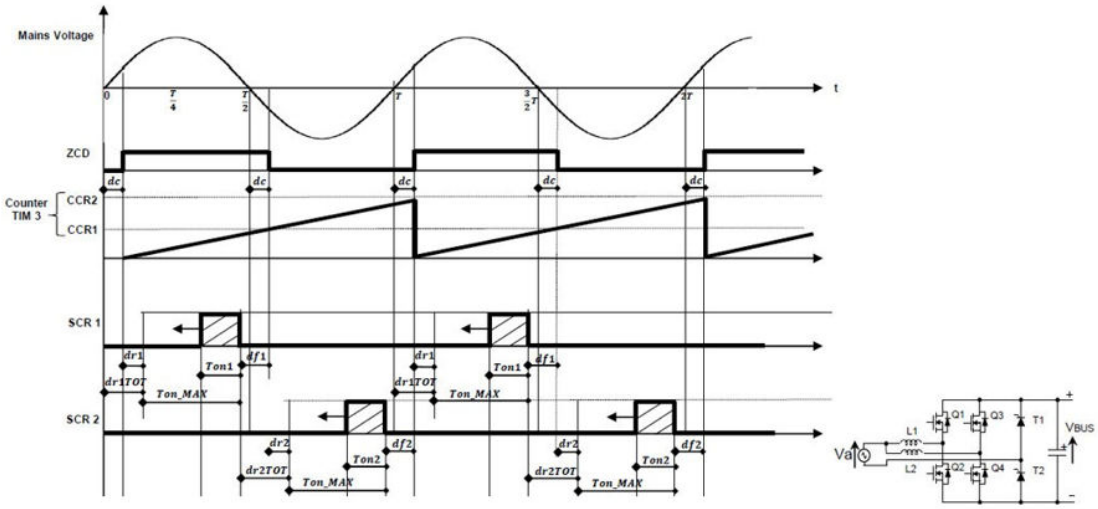
A zero-crossing detection (ZCD) signal, which gives the mains polarity and comes from a comparator, detects both the mains frequency and the duty (it should be around 50%) using a timer in input mode, and synchronizes low frequency PWM signals (that is the synchronization of another timer).

The Figure 25. SCR driving signals and DC bus charging shows:

- dc that represents the delay of the comparator output;
- dr1 that is the delay rising of the SCR1 turn-on with respect to the rising edge of ZCD in steady state (when the inrush procedure is completed);
- df1 is the falling delay of the same signal with respect to the falling edge of ZCD with one programmable value
- dr2 and df2 are rising and falling delays of SCR2 driving signal with respect to ZCD. All these delays are defined and can be changed in the control firmware.

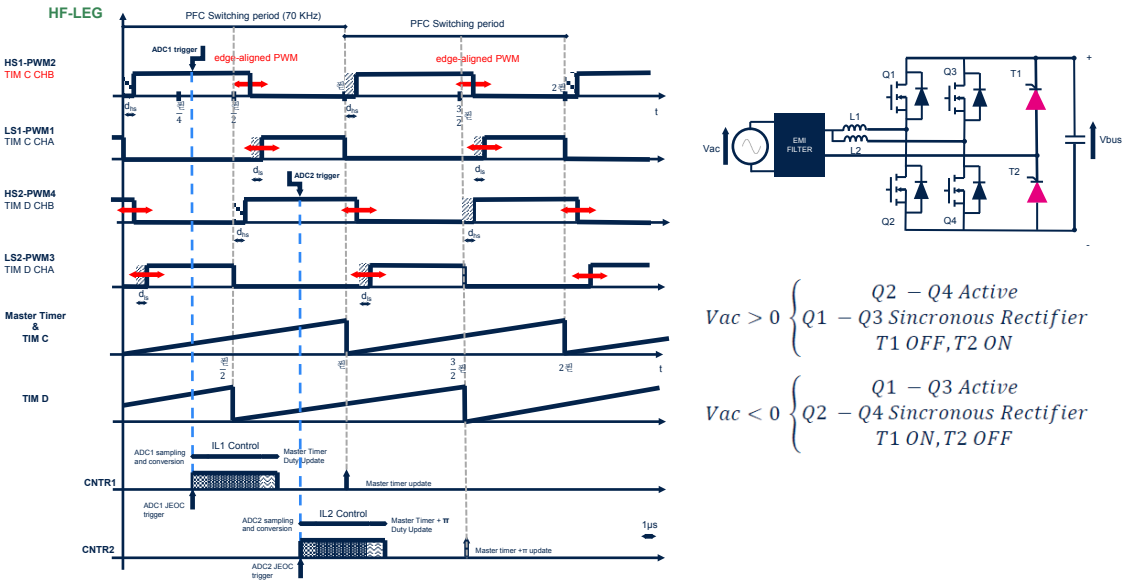
Figure 25. **SCR driving signals and DC bus charging**

- dc = delay comparator
- dr1 = delay rising with one programmable value
- df1 = delay falling with one programmable value
- dr2 = delay rising with two programmable values
- df2 = delay falling with two programmable values
- T_{on1} = SCR1 T_{ON} variable
- T_{on2} = SCR2 T_{ON} variable



6.8 PFC control signals

Figure 26. **Interleaved totem pole PFC signals**



$$Vac > 0 \begin{cases} Q2 - Q4\ Active \\ Q1 - Q3\ Sincronous\ Rectifier \\ T1\ OFF, T2\ ON \end{cases}$$

$$Vac < 0 \begin{cases} Q1 - Q3\ Active \\ Q2 - Q4\ Sincronous\ Rectifier \\ T1\ ON, T2\ OFF \end{cases}$$

Current sampling is performed in the middle point of the T_{ON} PFC switching period.

In the bridgeless totem pole PFC, the roles of the switches in the high frequency legs depend on the mains polarity: when the mains voltage is positive, Q2 and Q4 (low side) are the active switches, whereas Q1 and Q3 (high side) are driven in a complementary way with a fixed dead time. In the latter case, the current can circulate, in the low frequency leg, through T2, whereas T1 is off.

During the negative mains voltage half cycle, Q1 and Q3 (high side) are the active switches, whereas Q2 and Q4 (low side) are driven in a complementary way with a fixed dead time. In the latter case, the current circulates through T1 in the low frequency leg.

To generate the necessary four PWMs signals, two different timers, with the phase shifted by 180°, are used to obtain an interleaving driving and to minimize the input current ripple.

At the T_{ON} period midpoint of each active switch, an injected acquisition of the related inductor current is triggered by the ADC. At the end of each conversion, once obtained the last current measure, the current control algorithm is executed and the new duty cycle value is written in the timer registers before the end of the actual period becomes effective at the next PWM cycle.

6.9 MCU PFC tasks

Table 2. PFC tasks

Task name	Priority	Frequency	Description
Current control loop X2	Very high	70 kHz	There are two independent current loops: one sinusoidal current reference calculation and two PID or 2p2z regulators; one duty cycle computation and actuation.
Voltage control loop	High	6 kHz	A PID or 2p2z regulator calculates the amplitude of current reference.
Mains voltage rms and feedforward computation, enable/ disable SR	High	6 kHz	Computes rms value of input voltage using a low pass digital filter, and feedforward term for input current reference calculation.
Mains frequency computation	Medium	45-65 Hz	Computes mains frequency from a ZVD external signal (slow timer configured in input capture to measure the time between two consecutive rising edges).
Inrush current algorithm	Medium	2*(45-65) Hz	Drives SCRs at twice mains frequency to charge slowly the bus voltage at startup. The algorithm drives SCRs also in steady state.
Duty cycle soft-start at zero-crossing	Medium	2*(45-65) Hz	At mains zero-crossing, the duty cycle is slowly changed from the max. to the required value to avoid current spikes.
Slow protection checks	Low	-	Compares the measured values with high and low thresholds, and manages the state machine: • Input under/over voltage; • Input under/over frequency; • Output under/over voltage; • Overtemperature • Current sensor calibration error; • Startup failed protection.
Fast protection checks	Very high	Immediately after ADC conversion delay	Fast protection based on ADC AWD: • Inductor 1 overcurrent; • Inductor 2 overcurrent.
Serial communication	Very low	5 Hz or immediately after a fault on the primary side	Manages primary to secondary side opto-coupled communication in a two-MCU solution.

6.10 DC-DC LLC section

The DC-DC LLC section features:

- Dual full bridge LLC with CC/CV control mode:

- Two independent current loops (CC)
- One voltage loop plus current balancing (CV)
- Transformers:

– Turn ratio = 1.1:1 ±1%

– Llk= 5.5 µH, Lp = 62.40 µH, Isat = 40 A

- Resonant inductors:

– 17.3 µH, 13.5 A

- Output capacitors:

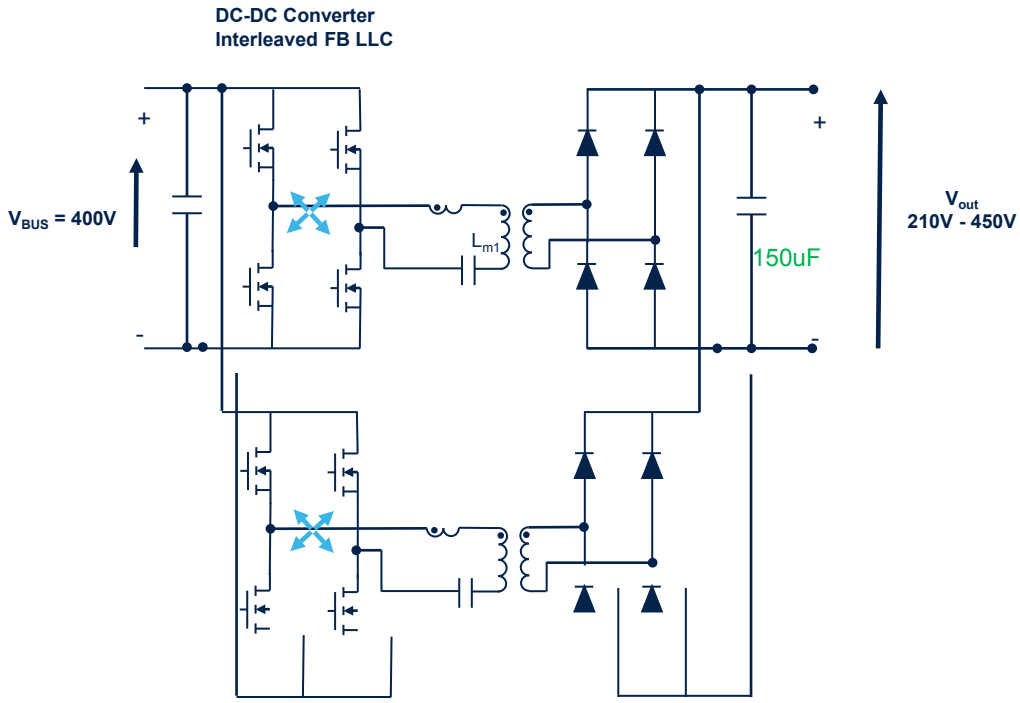
– 150 µF, 500 V

- Switching frequency: 80 – 310 kHz
- Primary side MOSFETs: STB47N60DM6AG
- Secondary side diodes: STPSC20065GY

The DC-DC converters section consists of two LLC converters in parallel supplied by the same voltage output PFC bus.

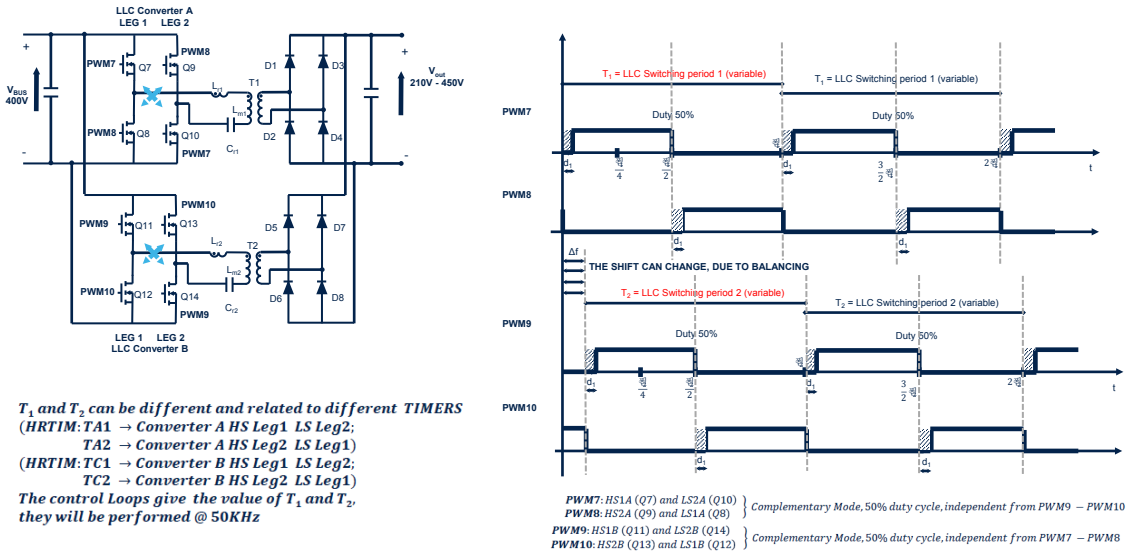
The transformers provide the galvanic isolation from the mains. The gain is given by the resonant tank and depends on the switching frequency.

Figure 27. DC-DC LLC main schematic



6.11 FB LLC control signals

Figure 28. **LLC main schematic and switching periods**



T_1 *and* T_2 *can be different and related to different TIMERS*
(HRTIM: TA1 $\rightarrow$ *Converter A HS Leg1 LS Leg2;*
TA2 $\rightarrow$ *Converter A HS Leg2 LS Leg1)*
(HRTIM: TC1 $\rightarrow$ *Converter B HS Leg1 LS Leg2;*
TC2 $\rightarrow$ *Converter B HS Leg2 LS Leg1)*
The control Loops give the value of T_1 *and* T_2*, they will be performed @ 50KHz*

***PWM7**: HS1A (Q7) and LS2A (Q10)*
***PWM8**: HS2A (Q9) and LS1A (Q8)*
} *Complementary Mode, 50% duty cycle, independent from PWM9 – PWM10*

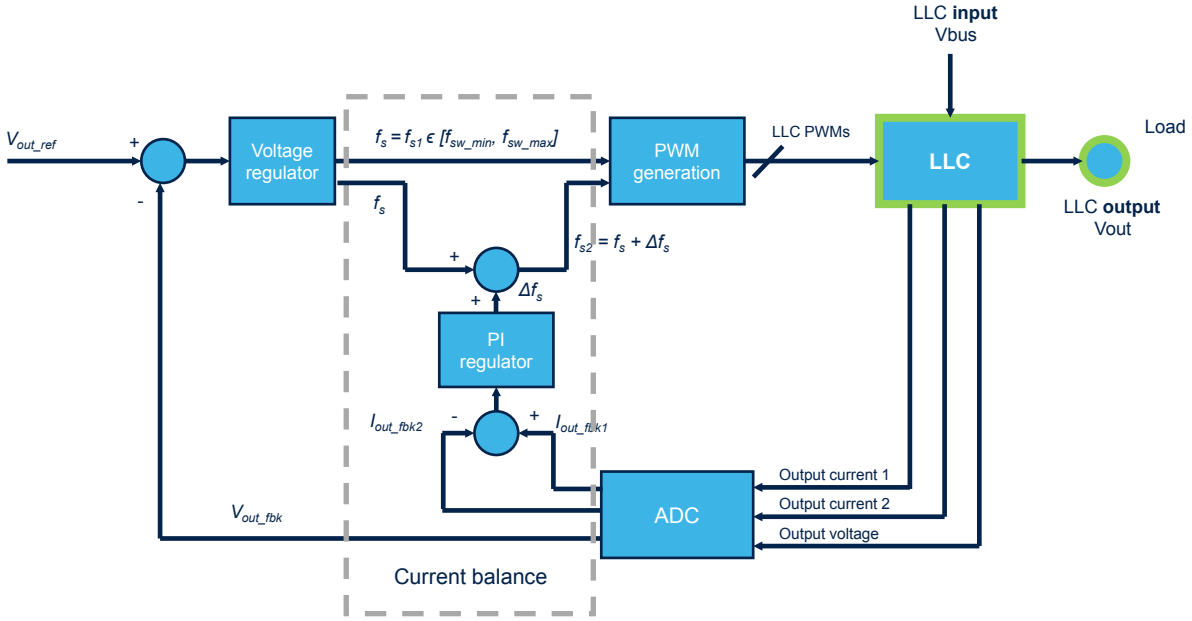
***PWM9**: HS1B (Q11) and LS2B (Q14)*
***PWM10**: HS2B (Q13) and LS1B (Q12)*
} *Complementary Mode, 50% duty cycle, independent from PWM7 – PWM8*

The command signals for each LLC resonant full bridge converter are square waves with 50% duty and dead time. Each PWM group mentioned as PWM7 and PWM8 in the figure above is used at the same time for Q7-Q10 and Q9-Q8, respectively. The same is for PWM9 and PW10 for Q11-Q14 and Q13-Q12, respectively.

In the constant voltage mode, the two full bridge LLC converters can be driven in the interleaved mode. In this case, the PWM signals have the same frequency and are 90 degrees shifted. However, due to the tolerance of the electric parameters of the two resonant tanks, the output current balance is not ensured.

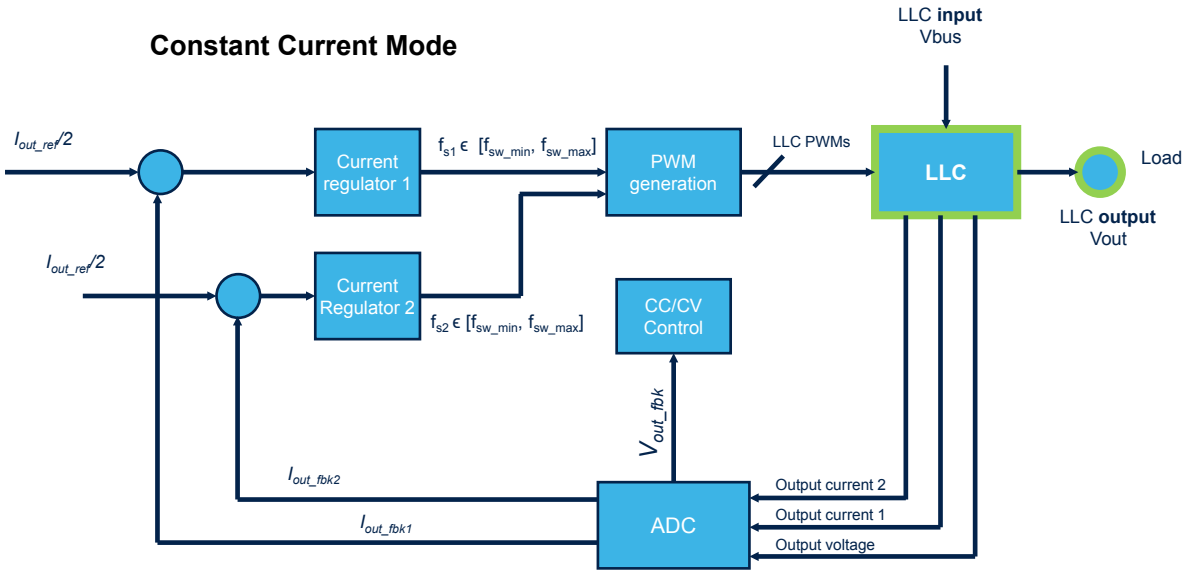
A dedicated control has been implemented to solve the unbalanced current issue. If a certain unbalance on the output current is present, the control provides a change on the PWM9 frequency with respect to the PWM7. A Δfs is introduced thanks to a PI regulator, executed at a lower frequency, to obtain the switching frequency of the second converter (fs2) in order to balance the output currents of the two stages (see the Figure 29. Constant voltage with current control block).

Figure 29. Constant voltage with current control block



The figure below shows the block diagram of the constant current control.

Figure 30. Constant current control block



In this case, the current loops are independent. The two switching frequencies, fs1 and fs2, are generated by two different current regulators.

The charger is able to switch from the constant current to the constant voltage mode via firmware, depending on the battery voltage value and following the desired charging profile.

6.12 MCU LLC tasks

Table 3. LLC tasks

Task name	Priority	Frequency	Description
Main control loop	High	50 kHz	Current mode and voltage mode are set according to the status of the battery and its charging profile. Current mode: two PID regulators calculate the switching period to regulate the two output currents. Voltage mode: a PID regulator calculates the switching period to regulate the output voltage. An additional PID regulator assures current balance at 5 kHz.
Frequency decrease	Medium	50 kHz or lower	Start up procedure to linearly decrease the switching frequency up to the reference value to avoid overcurrent. It occurs at startup phase instead of the main control loop.
Slow protection checks	Low	-	Compares the measured values with high and low thresholds, and manages the state machine: • Input under/over voltage; • Input under/over frequency; • Output under/over voltage; • Overtemperature • Current sensor calibration error; • Startup failed protection.
Fast protection checks	Very high (hardware)	Immediately after computation delay	Fast hardware protection and related Irq handler: • Resonant current 1 overcurrent; • Resonant current 2 overcurrent.
Serial communication	Very low	5 Hz or immediately after a fault on the primary side	Manages primary to secondary side opto-coupled communication in a two-MCU solution.
CAN communication	Very low	-	Manages communication with the user interface and/or among the three modules.

7 Test setup

7.1 Test conditions and equipment

- 2 x SR5E1 control board in lock-step mode or 1 x SR5E1 control board in decoupled mode with cable adapter
- 1 x STDES-7KWOBC power board
- 1 x 7 kW DC-DC 600 V 24 A power source by Magna-Power electronics (for DC-DC test only)
- 1 x 7.5 kW programmable AC power source by adaptive power system
- 1 x 800 V, 90 A max. electronic DC load by ZS electronic load H&H (CC and CV mode)
- 1 x HD08108A multichannel digital oscilloscope by Teledyne Lecroy
- 4 x HVD3206A differential voltage probes (galvanically insulated) by Teledyne Lecroy
- 2 x 30 A current probe by Teledyne Lecroy (four probes for tests in 4.3.2)
- 2 x 34401A digital multimeters by Agilent (optionally)
- 1 x 20 mV/A CWT18 Rogowski current transducer (optionally for resonant current sensing)
- 1 x Lauterbach + JTAG ARM® cable (to reprogram the SR5E1 MCU)
- 1 x cooling free air base plate (20 x 42 x 6 mm)
- Ambient temperature = 25°C

7.2 Procedure

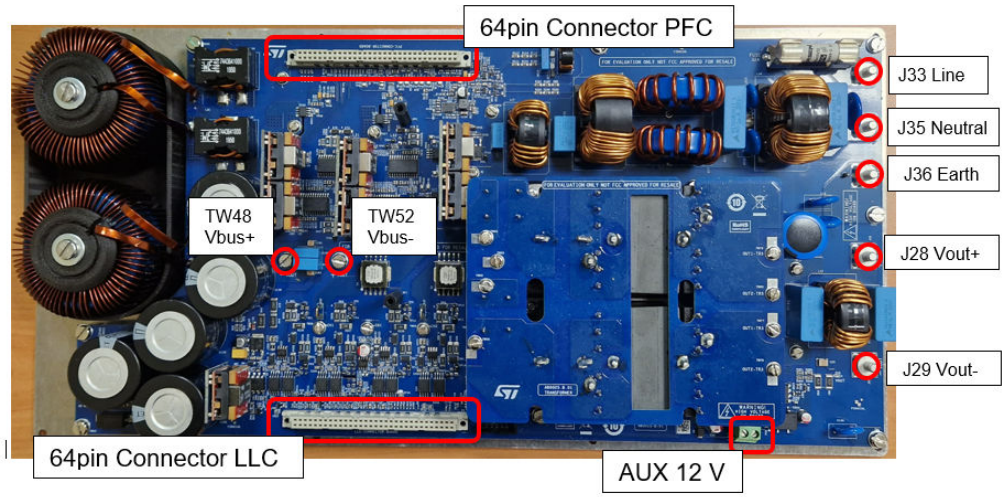
Step 1. Connect the programmed control board to the proper 64-pin connector. Different firmware packages are used for the PFC section and the LLC section.

To program a new control board (based on SR5E1 MCU), power it through an external 5 V through the supply connector, or connect it to the power board and just provide the auxiliary 12 V supply voltage only. The green LED indicates that control board is correctly powered and can be reprogrammed, then remove auxiliary supply voltage.

Step 2. Connect the programmable AC voltage source to the control board AC input voltage J33-J35 through cable, taking into account the proper cross-section gauge able to sustain 32 A.

To test the complete system, connect the output load to J28-J29 connectors with a cable with an appropriate cross-section to carry the desired load current (20 A max.) and considering the correct polarity.
To test the PFC section only, the output load (600V, 20 A min) could be connected to TW48 and TW52 (bulk capacitors).
To test the DC-DC section only, do not connect the AC power source, connect the DC power supply (600 V 20A min) to TW48 and TW52 and connect the output load to J28-J29, as previously described.

Figure 31. STDES-OBC7KW top view



Note: Always connect the earth to the input connector.

Step 3. Verify that STDES-7KWOBC is not powered yet and connect all oscilloscope probes according to the section that is going to be tested (PFC, DC-DC or both) and the waveforms of interest: for example, inductor currents, mains voltage, bus voltage for PFC stage and resonant currents, tank voltages, output voltage for DC-DC converter, as described in the following sections.

Step 4. Supply the auxiliary 12 V supply voltage by JP1 connector and check that control boards are correctly powered (green LEDs ON) and FAULT red LEDs blink signaling an undervoltage error, according to the following tables.

Step 5. Turn-on AC power source supplying 120 Vac, 60 Hz or 230 Vac, 50 Hz to test the complete solution or the PFC stage only.

Step 6. Check the correct startup procedure and apply electronic load (in CC mode for PFC or DC-DC when it works in CV mode, in CV mode for DC-DC when it works in CC mode), in normal operation FAULT red LEDs of the two control boards should be OFF and STATUS blue LEDs should be ON.

Step 7. After tests, disconnect the input power supply keeping the load to discharge output capacitors, then remove the auxiliary 12 V supply voltage also.

Table 4. PFC error codes

Error	Condition	Blinks N°	Speed
PFC_BUS_OVER_VOLTAGE	V_{bus} > 450 V_{DC}	2	Low
PFC_BUS_UNDER_VOLTAGE	V_{bus} < 290 V_{DC}	3	Low
PFC_MAINS_OVER_VOLTAGE	V_{mains_rms} > 270 V_{AC}	4	Low
PFC_MAINS_UNDER_VOLTAGE	V_{mains_rms} < 90 V_{AC}	5	Low
PFC_MAINS_OVER_FREQUENCY	f_{mains} > 70 Hz	6	Low
PFC_MAINS_UNDER_FREQUENCY	f_{mains} < 40 Hz	7	Low
PFC_ OVER_CURRENT	I_L1 or I_L2 > 26 A (peak)	2	High
PFC_ OVER_TEMPERATURE	NTC temperature > 50 °C	3	High
PFC_INIT_ERROR	Current sensor offset outside boundaries [1600, 2400] during calibration	4	High
PFC_ICL_ERROR	V_{bus} < 0.9*□2* V after ICL	5	High

Table 5. DC-DC error codes

Error	Condition	Blinks N°	Speed
DCDC_OUT_OVER_VOLTAGE	V_{out} > 470 V_{DC}	3	Low
DCDC_OUT_UNDER_VOLTAGE	V_{out} < 250 V_{DC}	2	Low
DCDC_IN_OVER_VOLTAGE	V_{in} > 435 V_{DC}	4	Low
DCDC_IN_UNDER_VOLTAGE	V_{in} < 90 V_{DC}	5	Low
DCDC_STARTUP_FAILED_ERROR	V_{bus} < 250 V_{DC} after frequency ramp-up	6	Low
DCDC_OUT_ OVER_CURRENT	$I_{out}1$ or $I_{out}2$ > 11 A	3	High
DCDC_ OVER_CURRENT	$I_{res}1$ or $I_{res}2$ > 22.8 A (peak)	2	High
DCDC_ OVER_TEMPERATURE	NTC Temperature > 55 °C	4	High

8 Measurements/waveforms/test data

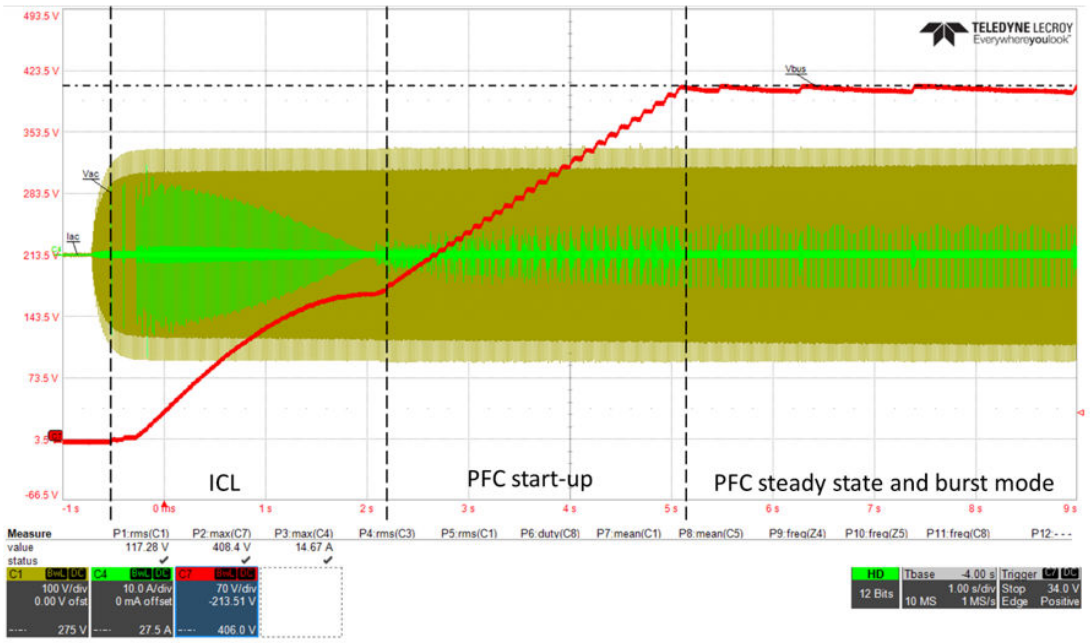
8.1 PFC section

8.1.1 Inrush current limiter (ICL) and PFC start-up waveforms

Once the platform is supplied, at start-up, you can check the limitation of the input current and the evolution of the bulk capacitor voltage thanks to the presence of the inrush current limiter circuit.

Figure 32. Input current and bus voltage evolution during start-up

1. Mains voltage (yellow)
2. Input current, limited at a peak of 12 A (green)
3. Smooth bulk capacitor charging (red)



After the input voltage connection (Vac), the SCRs in low frequency leg are driven for a short time to limit the input current peaks (whose envelop remains below 12 A) and to charge smoothly the bulk capacitors (Vbus). Once the bus voltage reaches the rectified input voltage (Vac*√2), the PFC begins the start-up phase, closing the control loop and increasing the bus voltage up to the reference value of 400 V and in case of no load or light load, going in burst mode around 420-430 V.

In the figure below, the SCRs driving signals are shown during the ICL phase: initially each SCR, according to Vac polarity, is turned on only for a small interval just before the zero crossing of input voltage, to limit the voltage difference between the input and the output, hence also the current that flows to the bulk capacitors. The conduction time is then increased step-by-step until reaching 1/4th of the input period (peak of input voltage), then it is set at 1/2nd of input period (with safety delays), as shown in Figure 34. Start-up waveforms – zoom 2 and Figure 35. Start-up waveforms – zoom 3 .

Figure 33. Start-up waveforms – zoom 1

1. Mains voltage (yellow)
2. Input current (green)
3. Smooth bulk capacitor charging (red)
4. SCR1 driving waveform (gray)
5. SCR2 driving waveform (violet)

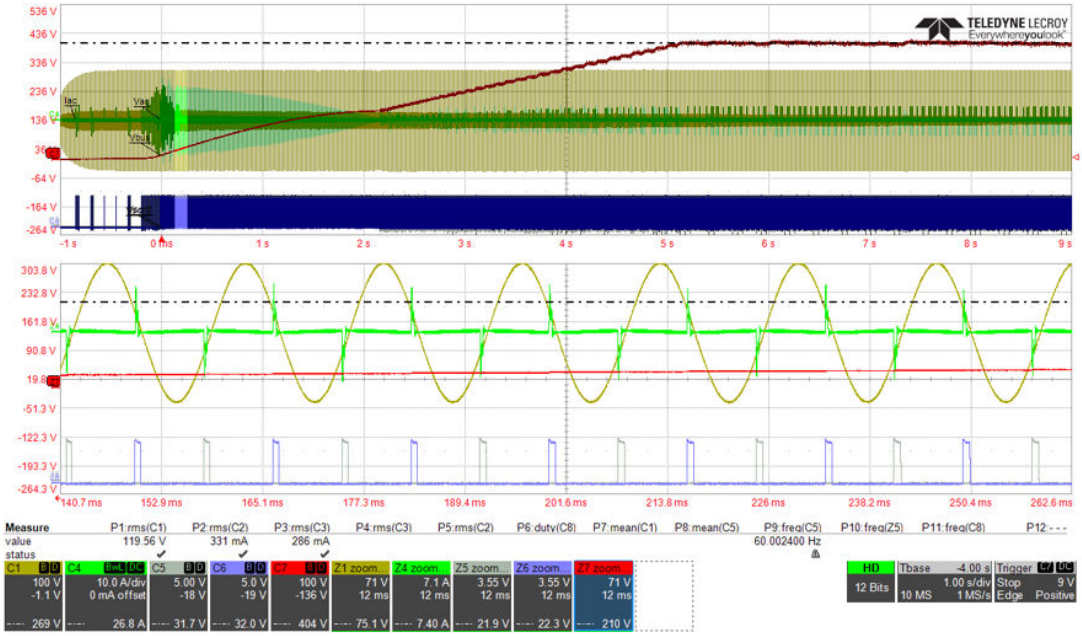


Figure 34. Start-up waveforms – zoom 2

1. Mains voltage (yellow)
2. Input current (green)
3. Smooth bulk capacitor charging (red)
4. SCR1 driving waveform (gray)
5. SCR2 driving waveform (violet)

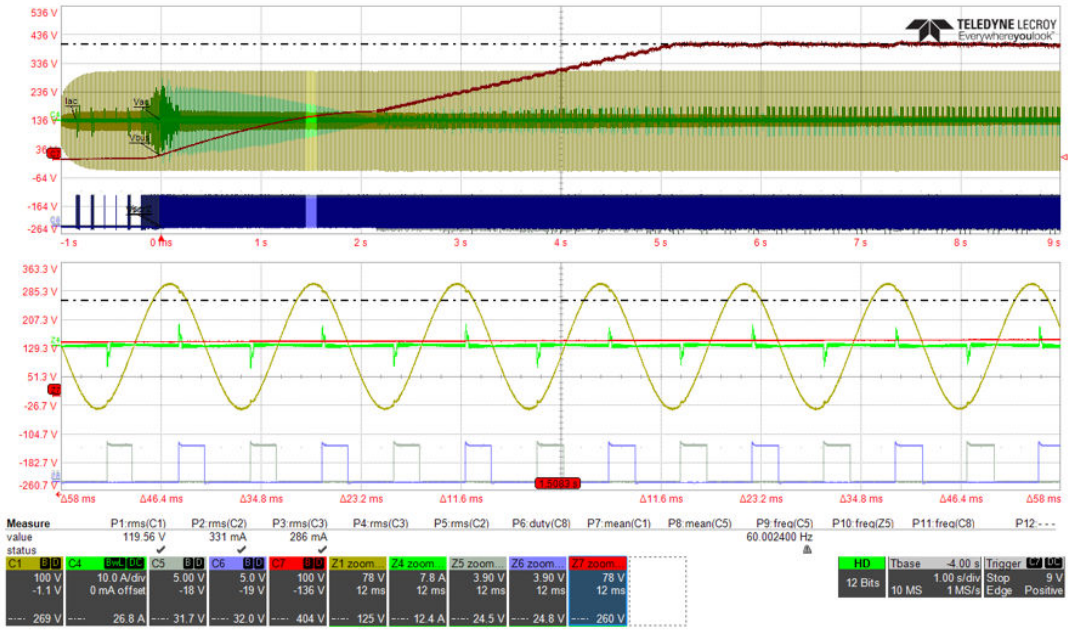
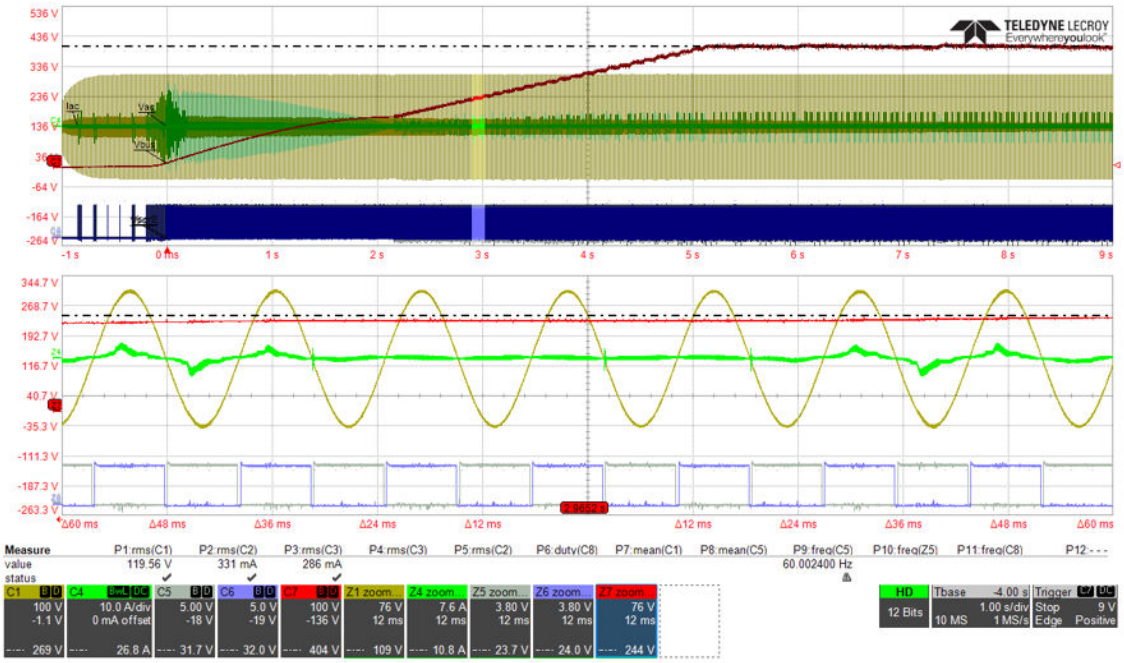


Figure 35. Start-up waveforms – zoom 3

1. Mains voltage (yellow)
2. Input current (green)
3. Smooth bulk capacitor charging (red)
4. SCR1 driving waveform (gray)
5. SCR2 driving waveform (violet)



PFC start-up test: PASSED.

In the following figure the input voltage, inductor currents, together with Vgs driving signals of the first high-frequency leg (Vgs_HS1 and Vgs_LS1), are shown when 750 W load is applied with Vin = 120Vac, 60 Hz.

Figure 36. PFC waveforms – Vac = 120 V 60 Hz, Iac = 6 A

1. Mains voltage (yellow)
2. Inductor Current 1 (magenta)
3. Inductor Current 2 (blue)
4. Vgs_HS1 (red)
5. Vgs_LS1 (violet)

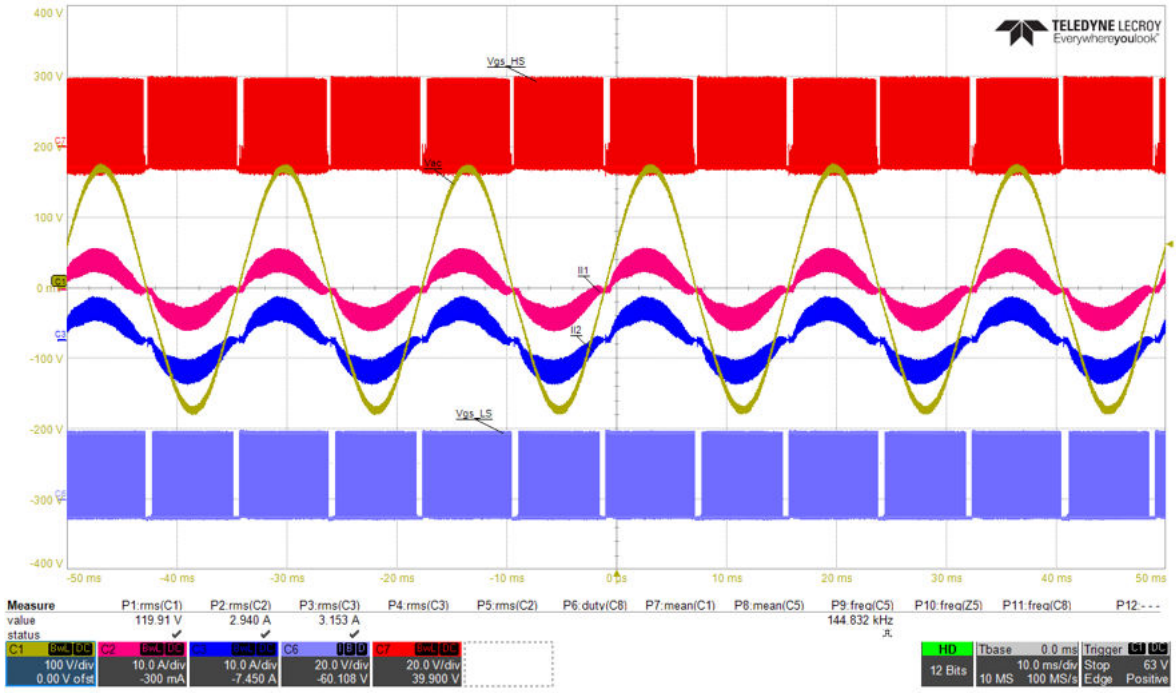
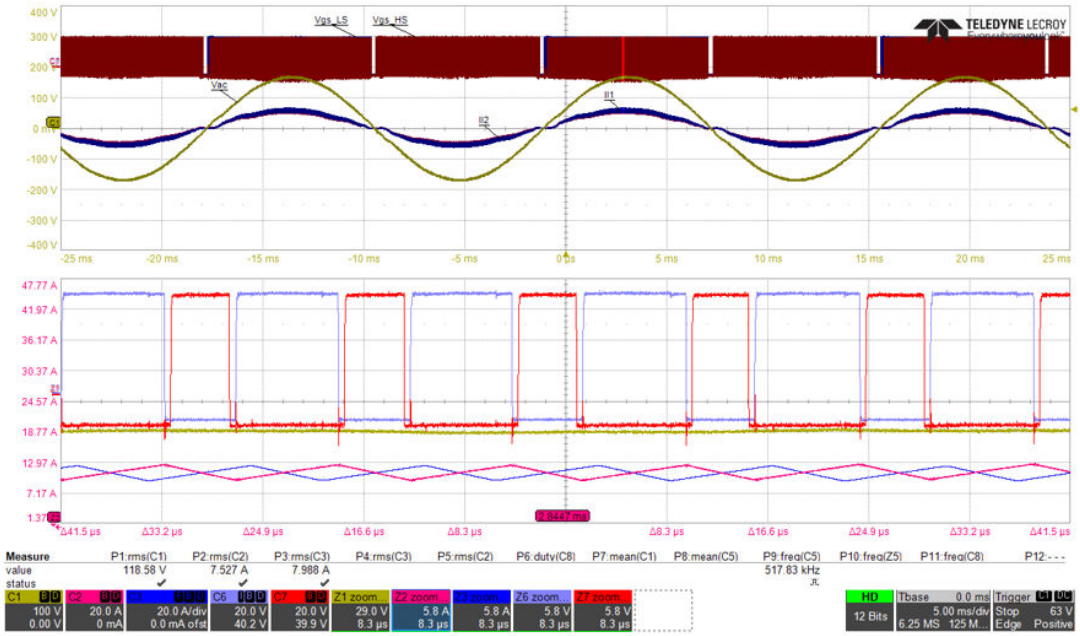


Figure 37. PFC waveforms – Vac = 120 V 60 Hz, Iac = 16 A

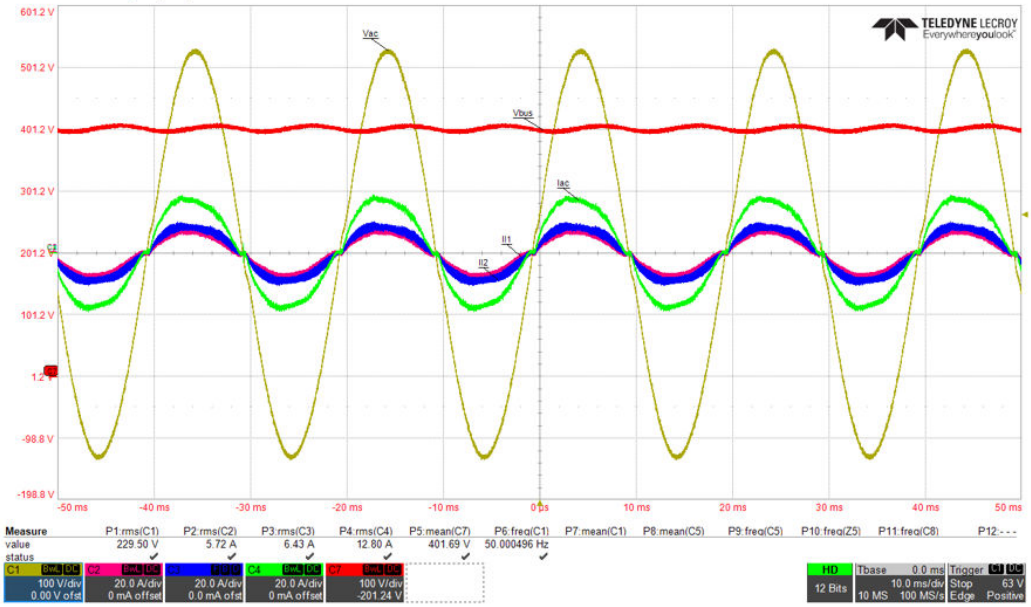
1. Mains voltage (yellow)
2. Inductor Current 1 (magenta)
3. Inductor current 2 (blue)
4. Vgs_HS1 (red)
5. Vgs_LS1 (violet)



Similar results can be obtained supplying the converter with Vin = 230 Vac, 50 Hz, as shown in the following figure.

Figure 38. PFC waveforms – Vac = 230 V 50 Hz, Iac = 16 A

1. Mains voltage (yellow)
2. Inductor Current 1 (magenta)
3. Inductor current 2 (blue)
4. Input current (green)
5. Bus voltage (red)



PFC steady-state test: PASSED.

8.1.2 Duty cycle soft-start waveforms

An important feature that could be verified is the duty cycle soft-start near the zero-crossing of input voltage, at both positive and negative slopes, as shown in Figure 39. PFC waveforms – duty cycle soft start in positive slope and Figure 40. PFC waveforms – duty cycle soft start in negative slope.

This technique consists in increasing slowly the duty cycle of the active switch before closing again the control loop, which would require a high duty cycle and before activating the complementary switch; this will reduce the inductor current spike due to the charged parasitic capacitances of low frequency leg devices.

Figure 39. PFC waveforms – duty cycle soft start in positive slope

1. Mains voltage (yellow)
2. Inductor Current 1 (magenta)
3. Inductor current 2 (blue)
4. Vgs_HS1 (red)
5. Vgs_LS1 (violet)

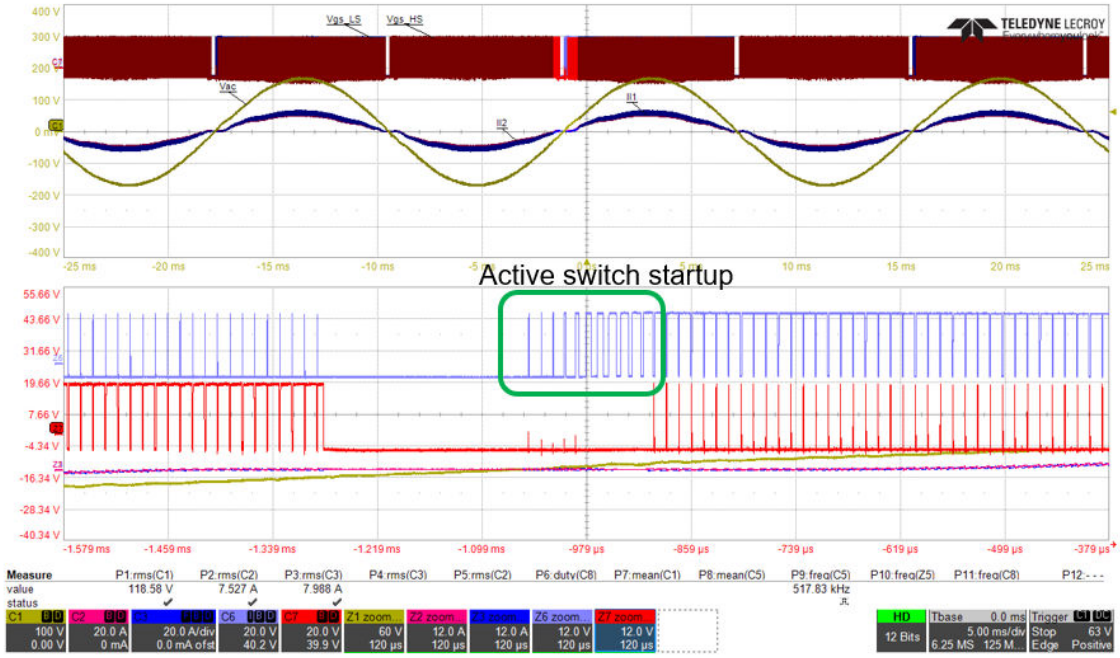
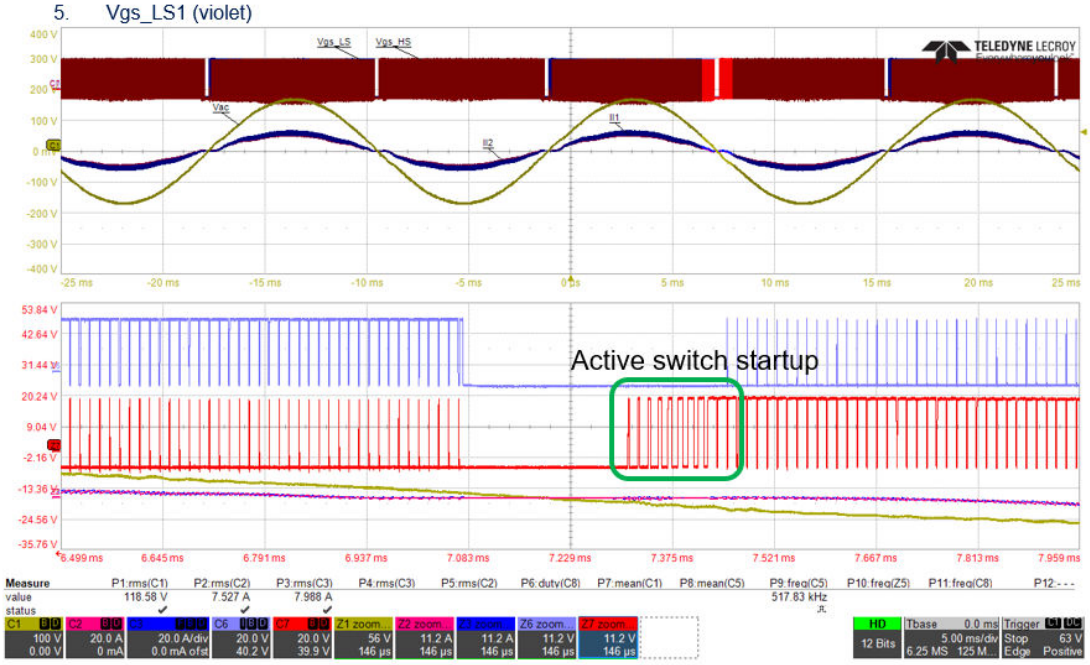


Figure 40. **PFC waveforms – duty cycle soft start in negative slope**

1. Mains voltage (yellow)
2. Inductor Current 1 (magenta)
3. Inductor current 2 (blue)
4. Vgs_HS1 (red)
5. Vgs_LS1 (violet)



8.1.3 Efficiency

The table below lists the PFC efficiency measurement preliminary results with the following working conditions:

- VIN = 230 V, 50 Hz
- VOUT = 400 VDC, 7.5 A

Table 6. **PFC efficiency measurements**

Time lapse (minutes)	PIN [kW]	POUT [kW]	%	PF	Low side temperature [°C] No Data available	High side temperature [°C]
0-30	1.531	1.5	98	0.982	42	42
30-60	3.058	3	98.5	0.995	55	61
60-90	3.058	3	98.5	0.995	59	62

The table below lists the PFC efficiency measurement preliminary results with the following working conditions:

- VIN = 230 V, 50 Hz
- VOUT = 400 VDC, 7.5 A

No Data available

Table 7. **PFC efficiency measurements**

Time lapse (minutes)	PIN [kW]	POUT [kW]	%	PF	Low side temperature [°C]	High side temperature [°C]
0-30	1.531	1.5	98	0.982	42	42
30-60	3.058	3	98.5	0.995	55	61

Time lapse (minutes)	PIN [kW]	POUT [kW]	%	PF	Low side temperature [°C]	High side temperature [°C]
60-90	3.058	3	98.5	0.995	59	62

8.1.4 PFC CPU Load

In the following table are reported the execution duration, and the related CPU load of all interrupts and tasks.

For some minor tasks it was impossible to measure the CPU load (such as the CC of the TIM3) because as soon as we insert a pin toggle the code no longer works correctly, but that should have a negligible impact.

Other tasks, such as TIM2 Irq and Analog Watchdog interrupt of ADC1 and ADC4 are not considered for CPU load computation as they have an impact only in case of fault.

At last, inside the while(1) loop of the main, the state machine task, low-priority faults check and LEDs blinking are executed; these tasks are performed only when other tasks are not running and therefore their impact is not considered for CPU load computation.

Table 8. PFC CPU Load

Task Name	Description	Frequency [Hz]	Duration [µs]	Load %
ADC1 Irq	**Current loop 1** 2 x SW start regular conversion sequences 1 x read injected measure (inductor current1) Control algorithm: • Get state machine and HF switch status variables • Calc Vmains abs • Calculation of sinusoidal current reference • Manage HF SR enable/disable • 2p2z regulator execution Modulator/PWM actuation	70000	2.84	19.88
ADC4 Irq	**Current loop 2** 1 x read injected measure (inductor current2) Control algorithm: • Get state machine and HF switch status variables • Get Vmains abs • Manage HF SR enable/disable • 2p2z regulator execution Modulator/PWM actuation	70000	2.11	14.77
TIM7 Irq	**Voltage loop** Vbus Low pass filter	6000	2.22	0.978

Task Name	Description	Frequency [Hz]	Duration [µs]	Load %
	2p2z regulator execution Manage LF SR enable/ disable (only for MOSFETs) Calc Vrms Calc current reference amplitude			
TIM6 Irq	**Low frequency task** Temperature filtering Conversion of Vbus, Vmains and temperature in [V] and [°C]	100	1.53	0.0153
TIM2 Irq	**Input frequency timeout** Manage frequency error if no input voltage is detected	Asynchronous	No impact in normal operation	-
ADC1/ADC4 Irq (AWD)	**Overcurrent protection** Manage inductor current 1 and inductor current 2 overcurrent protection in case of fault	Asynchronous	No impact in normal operation	-
TIM3 Irq	**Mains frequency detection** Rising edge • Read period from register • Calc frequency and check correct range • LF driving actuation Falling edge • Read positive duration CCR3 • Manage blanking window CCR4 • Manage blanking window	fmains [45:65]Hz	3.14 0.397 No impact No impact	0.0354 (@fmains = 50 Hz)
TIM8 Irq	**Set active and SR switch** 4xFmains (one instruction)	fmains [45:65]Hz	No impact	-
Main while(1) loop	**State machine, low-priority fault check, LEDs blinking** (performed only when other tasks are not in execution)	-	Not considered	-
			Total	35.679

8.2 LLC section

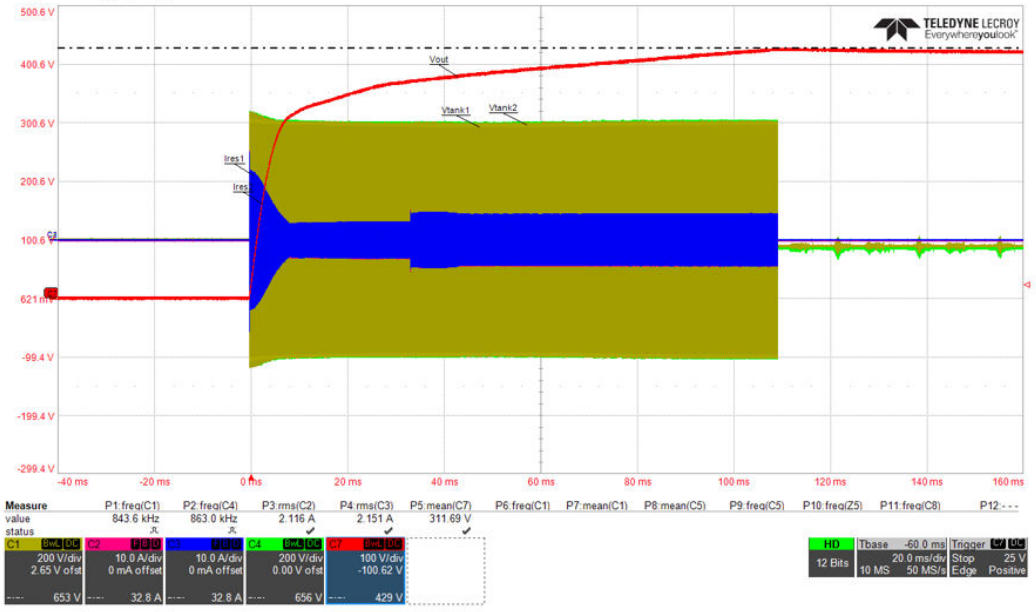
8.2.1 LLC start-up waveforms

When the bus voltage is in the correct range (350 V; 435 V), either regulated by PFC converter at 400V, or supplied externally, the LLC converter begins the start-up procedure; the latter consists in driving the two resonant stages with the maximum switching frequency (350 kHz), this one is then linearly decreased to the minimum value (92 kHz) unless the output voltage reaches the preset value to close the control loop (300V); in this way it is possible to reduce the amplitude of the two resonant tank currents.

In the following figure the output voltage (in red), together with the voltages applied to the two resonant tanks (yellow and green) and their respective currents (in magenta and blue) are shown during the start-up phase; it is possible to notice that both LLC converters go in burst mode when output voltage reaches 430 V because no load is applied.

Figure 41. LLC waveforms – start-up at no load

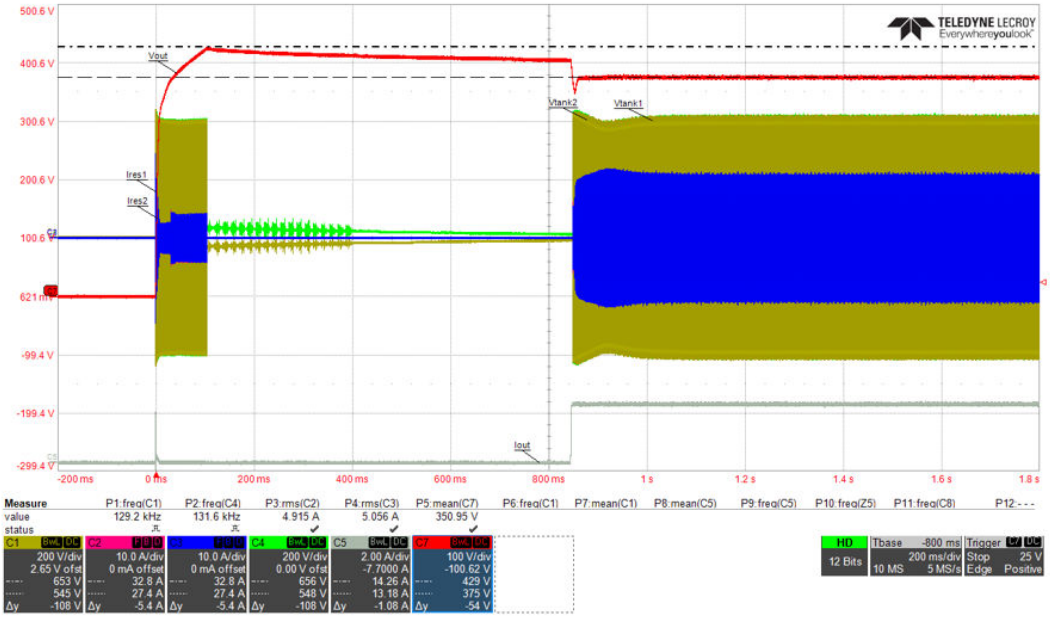
1. Voltage applied to resonant tank 1 (yellow)
2. Voltage applied to resonant tank 2 (green)
3. Resonant tank current 1 (blue)
4. Resonant tank current 2 (magenta)
5. Output voltage (red)



In the following figure the LLC start-up waveforms are shown when a current is applied in output (gray) during the burst mode, it is possible to notice that, after a settling time, the output voltage is regulated at 375 V in constant voltage (CV).

Figure 42. **LLC waveforms – start-up with load applied**

1. Voltage applied to resonant tank 1 (yellow)
2. Voltage applied to resonant tank 2 (green)
3. Resonant tank current 1 (blue)
4. Resonant tank current 2 (magenta)
5. Output voltage (red)
6. Output current (gray)



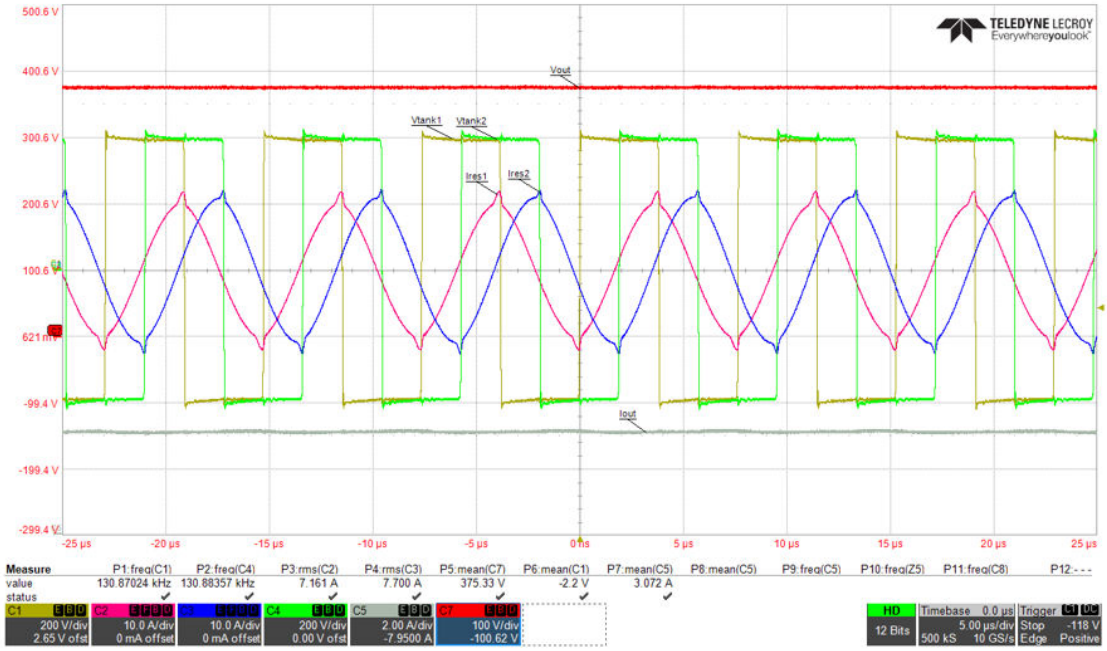
8.2.2 LLC steady-state waveforms

The dual full bridge LLC can be configured to work either in Constant Voltage (CV) mode or in Constant Current (CC) mode; in the first case the output voltage is regulated at 375 V, whereas in the second case the current reference is set by FW.

When working in CV mode, the interleaved modulation can be enabled, it consists in driving the two full bridge LLC converters with the same switching frequency (given by a PID control loop), but PWMs are phase-shifted by 90° to reduce output current ripple, as shown in the following figure, in this case the output current balance of the two stages is not possible.

Figure 43. LLC waveforms – steady state in CV mode with interleaved actuation

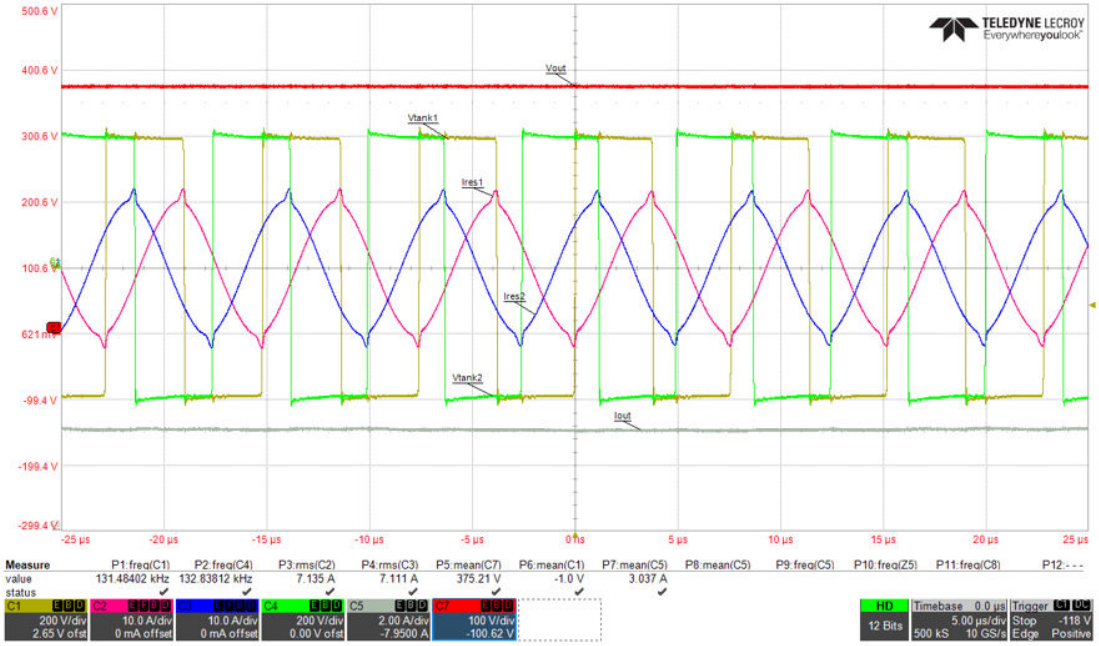
1. Voltage applied to resonant tank 1 (yellow)
2. Voltage applied to resonant tank 2 (green)
3. Resonant tank current 1 (blue)
4. Resonant tank current 2 (magenta)
5. Output voltage (red)
6. Output current (gray)



If interleaved actuation is disabled in FW configuration, the second LLC converter is driven with a different switching frequency in order to balance the output currents of the two stages, thanks to a slow inner current control loop; in this case also the two resonant currents have a similar amplitude, but the 90° phase-shift in driving waveforms is lost (see the following figure).

Figure 44. **LLC waveforms – steady state in CC mode**

1. Voltage applied to resonant tank 1 (yellow)
2. Voltage applied to resonant tank 2 (green)
3. Resonant tank current 1 (blue)
4. Resonant tank current 2 (magenta)
5. Output voltage (red)
6. Output current (gray)



8.2.3 LLC CPU Load

Similarly to PFC code, the following table reports the execution duration, and related CPU load, of all interrupts and tasks.

The main control loop, executed in TIM6 Irq, can be set either in Constant Voltage (CV) or in Constant Current (CC), then two different values are considered. In CV mode the output current balance loop can be enabled and executed at 1/10th of main control frequency.

At last, inside the while(1) loop of the main, the state machine task, low-priority faults check and LEDs blinking tasks are executed; these tasks are performed only when other tasks are not running and therefore their impact is not considered for CPU load computation.

Table 9. **LLC CPU Load (data not available)**

TASK name	Description	Freq [Hz]	Duration [µs]	Load %
TIM6 Irq	**Main control loop (CV or CC)** Current mode and voltage mode are set depending on the status of the battery according to battery charging profile **Current mode**: two PID regulators to calculate the switching period to regulate the two output currents **Voltage mode**: PID regulator calculates the switching period to regulate output voltage.	50000	3.20 or 2.49	16.01% Or 12.45%
TIM6 Irq	**Output current balance**	10000	0.712	0.712%

TASK name	Description	Freq [Hz]	Duration [µs]	Load %
	An additional regulator assures output current balance, (executed, if enabled, in CV mode only at 1/5th of main control frequency)			
TIM16 Irq	**Low frequency task** Temperature measure filtering Input voltage measure filtering Update configuration (only if changed on-thefly) Conversion of Vbus, Vout, Iout1, Iout2 and temperature in [V], [A] and [°C], respectively	100	2.80	0.028%
HRTIM1 Flt_Irq	**Overcurrent protection** Manage resonant current 1 and resonant current 2 fast overcurrent protection when a fault occurs	asynchronous	No impact in normal operation	-
Main while(1) loop	**State machine, low-priority fault check, LEDs blinking** (performed only when other tasks are not in execution)	-	Not considered	-
			Total	16.04% (for CC mode) 12.48% (for CV interleaved mode) 13.19% (for CV + current balance mode)

8.3 Entire solution test

8.3.1 Complete start-up

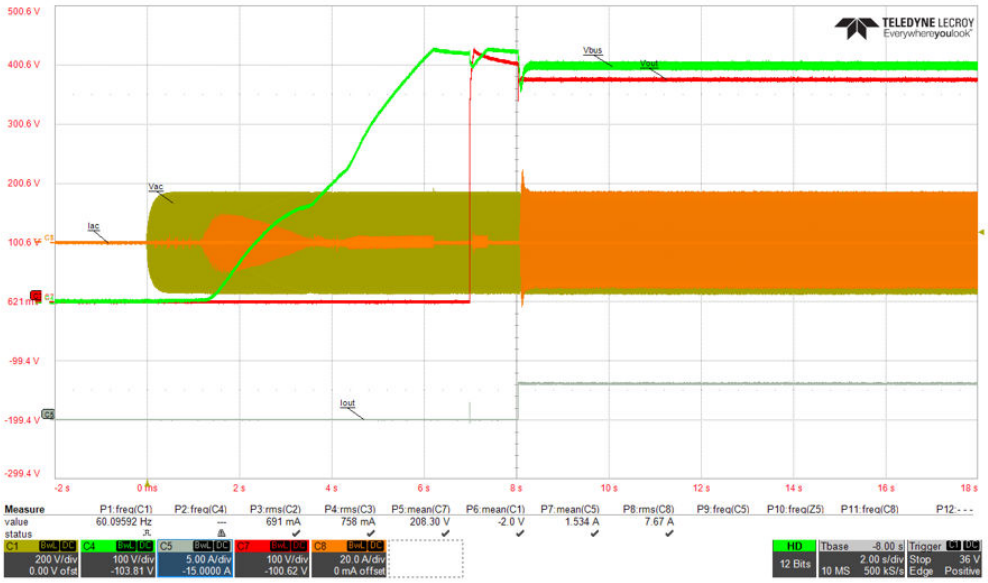
The complete start-up procedure (PFC and DC-DC) is shown in the following figure.

In this picture the output voltage of the PFC (V_{bus} in green) is increased performing the inrush current limitation (Iac in orange), as explained in Section 8.1 PFC section.

After reaching the reference value, the DC-DC output voltage (V_{out} in red) is increased as well, as explained in Section 8.2 LLC section, after that a load step is applied (I_{out} in gray), control loops keep V_{bus} and V_{out} voltages regulated at their reference values, 400 V and 375 V respectively.

Figure 45. Complete start-up waveforms

1. Mains voltage (yellow)
2. Input current (orange)
3. Bus voltage (green)
4. Output voltage (red)
5. Output current (gray)

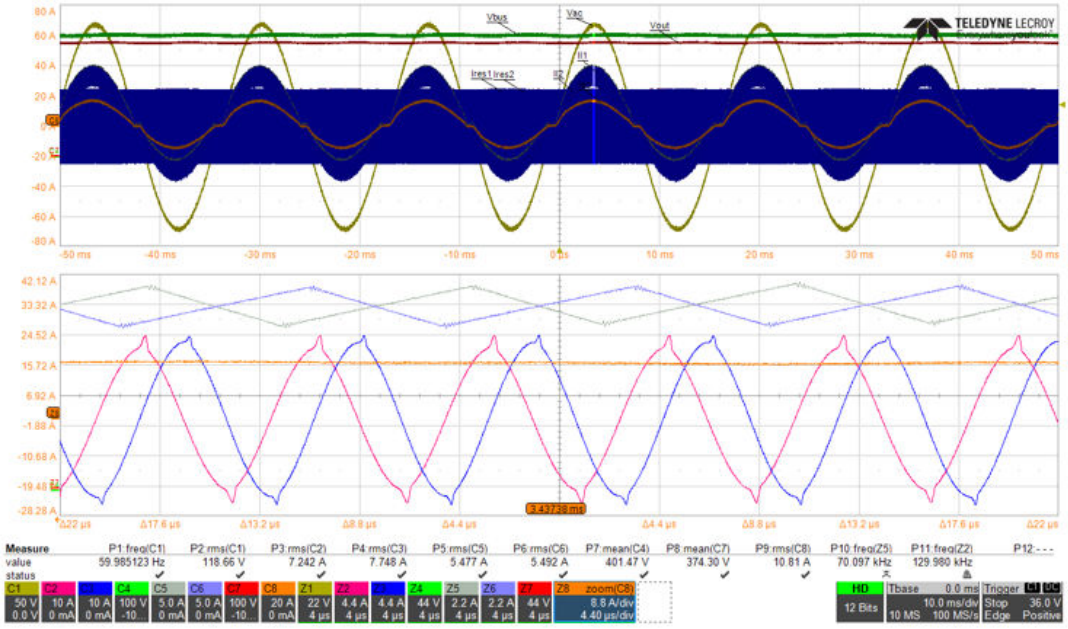


8.3.2 PFC + LLC steady state

The following figure shows the main waveforms (with corresponding zoom-in) when applied Vin = 120 Vac, 60 Hz, Pout ≈ 1300W and both PFC and DC-DC are in steady state.

Figure 46. PFC + LLC steady-state waveforms

1. Mains voltage (yellow)
2. Input current (orange)
3. Bus voltage (green)
4. Output voltage (red)
5. Inductor current 1 (gray)
6. Inductor current 2 (violet)
7. Resonant current 1 (magenta)
8. Resonant current 2 (blue)



Entire solution test: PASSED.

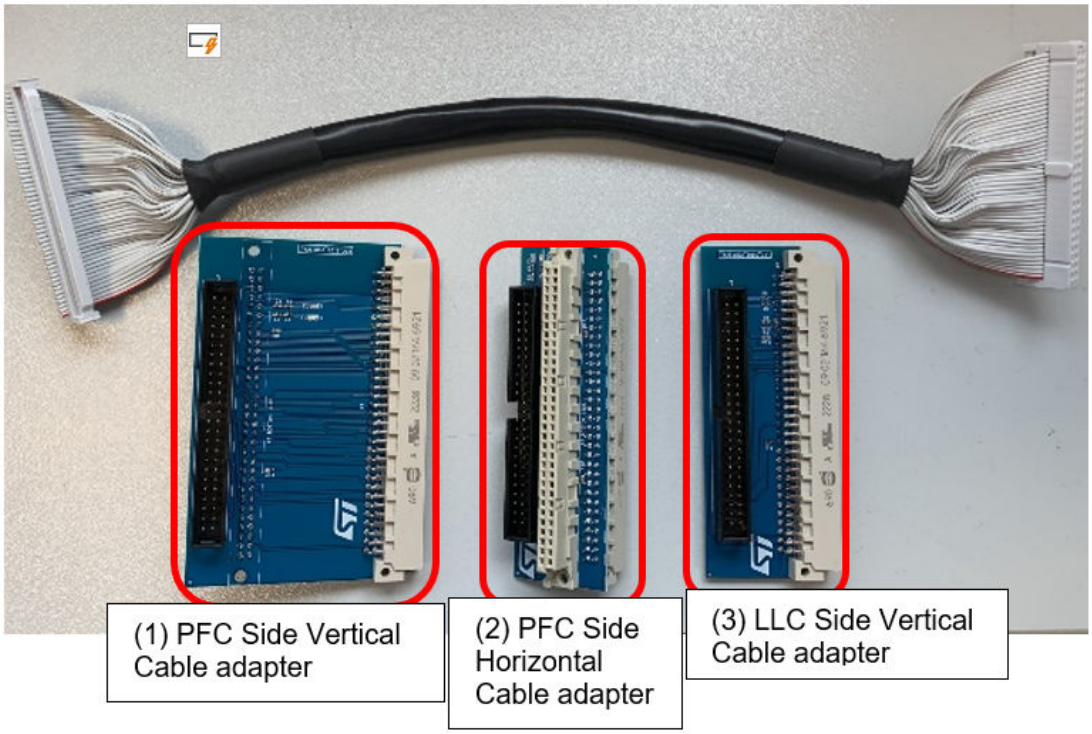
9 Dual core operations

9.1 Dual core adapter

The dual core adapter has been designed to be connected to both PFC and LLC DSMPS female connectors, housing one SR5E1 control board to drive the two power stages.

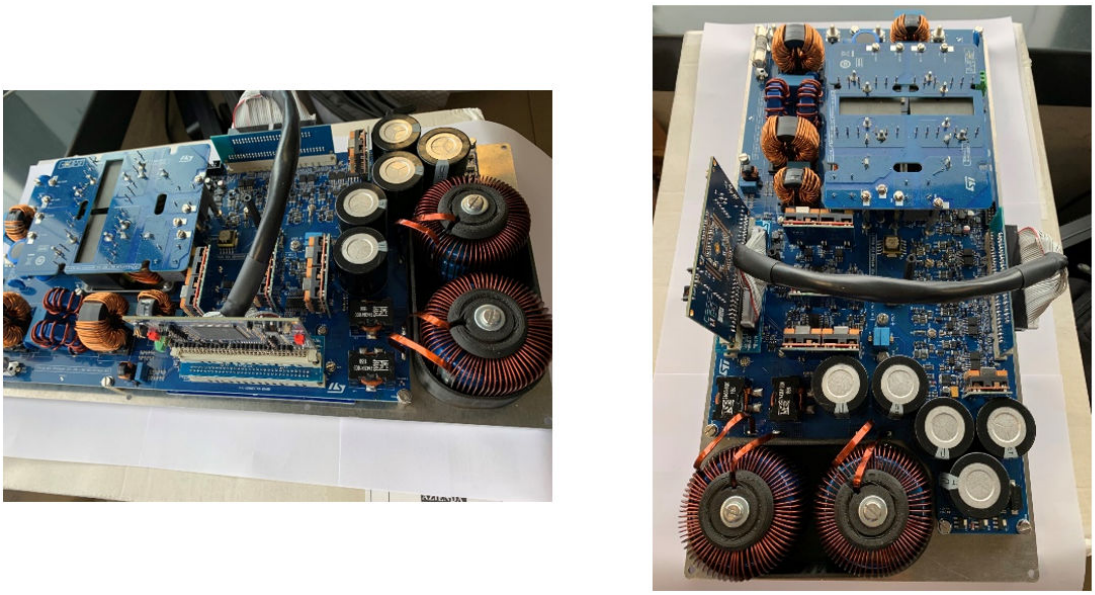
Dual core adapter is a connection of three sub-modules, the PFC control board dual-core connector (vertical or horizontal layout), PFC to LLC connector cable and the LLC Cable adapter, all components are visible in the following figure.

Figure 47. Dual core adapter components



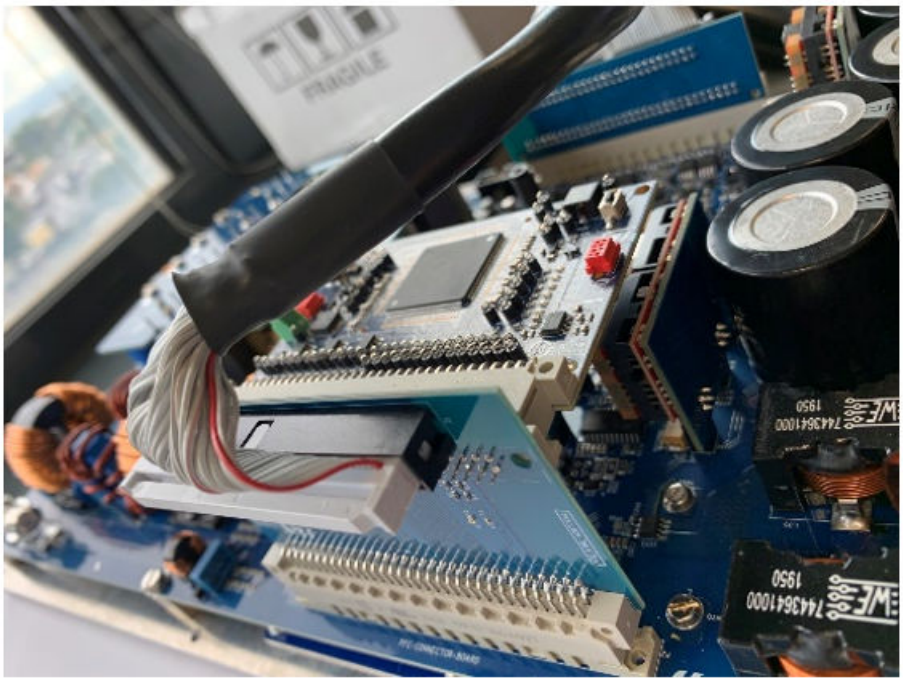
The fully assembled system using PFC Horizontal Adapter (2) and LLC vertical adapter (3) is shown in the following figure.

Figure 48. **Assembled dual core adapter using (2) and (3)**



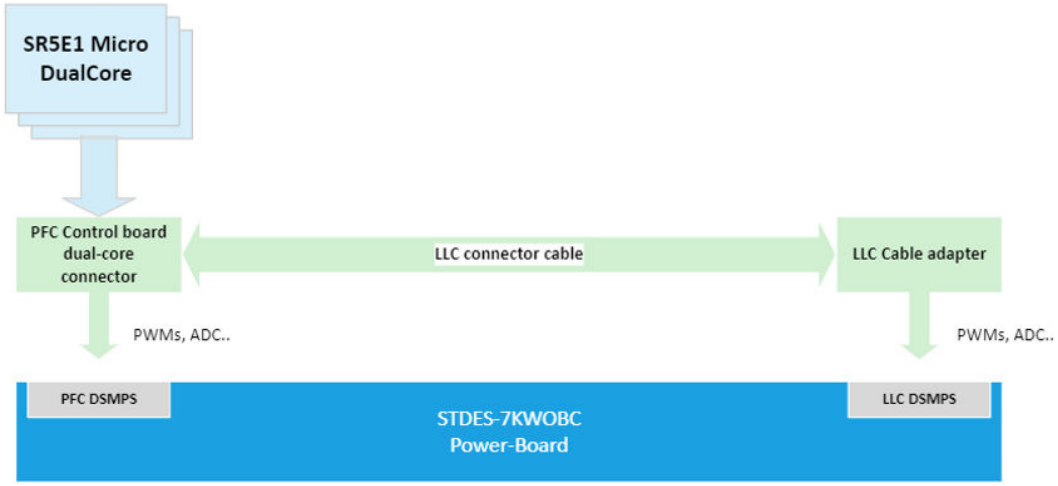
The fully assembled system using PFC Vertical Adapter (1) and LLC vertical adapter (3) is shown in the following figure.

Figure 49. **Dual Core adapter for micro in horizontal position using (1) and (3)**



The adapter provides all needed resources to PFC and LLC, guaranteeing independence by selecting different peripheral modules and avoiding any shared hardware peripheral between the two applications.

Figure 50. **Dual core adapter block schematic**



Two additional LEDs, a blue LED for STATUS and yellow LED for FAULT, are mounted on a PFC control board dual-core connector, in order to be driven by the LLC application, whereas the LEDs already present in SR5E1 control board, are dedicated to STATUS and FAULT signaling.

9.2 Lauterbach script file

A dedicated Lauterbach script (SR5E1_multicoreAMP.cmm file) has been released to debug in Asymmetrical MultiProcessing (AMP) mode the main cores of SR5E1: Core_1 and Core_2.

In this debugging mode, running the script, an individual TRACE32 instance is started for each core and an image is programmed for core.

The prerequisites to rightly use the script are:

1. implement in the main_core2.c file the following **weak** function

```
void __early_init(void)
{

    RCC->C2_VTOR_INIT_REG  = 0x080F0000UL;
    RCC->C2_BOOT_CTRL_REG |= (RCC_C2_BOOT_CTRL_REG_C2_RES_RELEASE);
    RCC->C2_BOOT_CTRL_REG |= (RCC_C2_BOOT_CTRL_REG_C2_CPU_WAIT_RELEASE);   //set break h
ere using lauterbach script
}
```

2. add in main_core2.c file the wait for the Core_2 clock initialized by Core_1, that means a “while loop” instead of the clock_init() function

```
/* Sync Core 2: Wait until clock has been configured by core 1 */
while ((RCC->CFGR & RCC_CFGR_SWS) != (CLOCK_CFG_SW << 3U))
{};
```

After the reset, Core_1 is woken-up, Core_2 may be woken-up.

The process of waking-up the other CPU (Core_2) is handled by means of __early init() function.

With the first two instructions, the function configures the address of the vector table of the M7 CORE_2 after reset release and releases the core reset.

The SR5E1_multicoreAMP.cmm sets a break point at third line to wait for the CORE_2 wake_up.

In this way it is possible to attach the Core_2 at the programmed reset-vector address.

Once executed the “go main” command in the script, both Core_1 and Core_2 are stopped at beginning of the main() routine.

9.3 LLC Firmware modification

To avoid peripheral resource assignment conflicts between PFC and LLC projects, the LLC one has been modified as follows:

The selected ADC modules are ADC3 and ADC5 instead of ADC1 and ADC4 plus ADC2 with regular conversions

Table 10. ADC resources change

Resources name	Micro in lock step	Core 2 used for LLC	Value
LLC Output Current sensing 1	SAR4_IN4 / COMP8_INM / SAR1_IN11	SAR5_IN1	Injected
LLC Output Current sensing 2	SAR1_IN4 / COMP2_INM / SAR4_IN11	SAR5_IN2	Regular
LLC VOUT Monitor sensing	SAR1_IN3 / COMP2_INP2 / SAR4_IN15	SAR3_IN3	Injected
LLC Temperature sensing	SAR2_IN7 / HRTIM1_EEV2 / COMP8_OUT	SAR3_IN2	Regular
LLC Resonant Current sensing 2	SAR1_IN2 / COMP1_INP2 / SAR4_IN17 / HRTIM1_FLT4	SAR3_IN1	Regular
LLC VBUS Monitor sensing	SAR2_IN2 / COMP3_INP2 / COMP3_INM / SAR5_IN17	SAR3_IN15	Regular
LLC Resonant Current sensing 1	SAR1_IN1 / COMP1_INP1 / COMP2_INP1 / SAR4_IN16 / HRTIM1_FLT1	SAR5_IN16	Regular

Regarding HRTimer, as SR5E1 have 2 modules we can reserve the HRTIM2 for LLC:

Table 11. HRTIM resources change

Resources name	Micro in lock step	Core 2 used for LLC
LLC_PWM_HS1_A	HRTIM1_CHA1	HRTIM2_CHE1
LLC_PWM_LS1_A	HRTIM1_CHA2	HRTIM2_CHE2
LLC_PWM_HS1_B	HRTIM1_CHC1	HRTIM2_CHA1
LLC_PWM_LS1_B	HRTIM1_CHC2	HRTIM2_CHA2

Regarding COMP and DAC for Over current we have the following resources modifications:

Table 12. COMP/DAC resources change

Resources name	Micro in lock step	Core 2 used for LLC
COMP_OC1	COMP2/DAC2_CH2	COMP3/DAC2_CH1
COMP_OC2	COMP1/DAC1_CH1	COMP5/DAC3_CH1

Finally, the LLC application in Lock step mode uses TIM6 with Vector100 to have a periodic task@50KHz while the code for dual core application uses TIM5 with VectorFC.

9.4 LLC HW modification

1. R7 and R8 resistors mounted on SR5E1 control board, to have SAR5_IN1 and SAR5_IN2 connected to the DSMPS male connector.
2. R128 removed on STDES-7KWOBC power board to disconnect AUX_ENABLE signal:
   There was a HW conflict and no more pin available so if it is reset at the beginning it can be left floating.
3. 3.3V_A signal connected in PFC cable adaptor using an external wire.
4. R8, R11 mounted on LLC cable adapter to provide +3.3V_LLC and A_VDD_LLC.
5. Filter capacitance on VDDA line (analogic supply) mounted in LLC cable adapter.
6. 2.2 k resistors mounted in series to PWM signals in the LLC cable adapter to lower the impedance and reduce any cable reflections.

9.5 Waveforms

Figure 51. Dual core waveforms

1. Mains voltage Vac (yellow)
2. Inductor Current 1 (magenta)
3. Inductor Current 2 (blue)
4. Resonant current for converter A (grey)

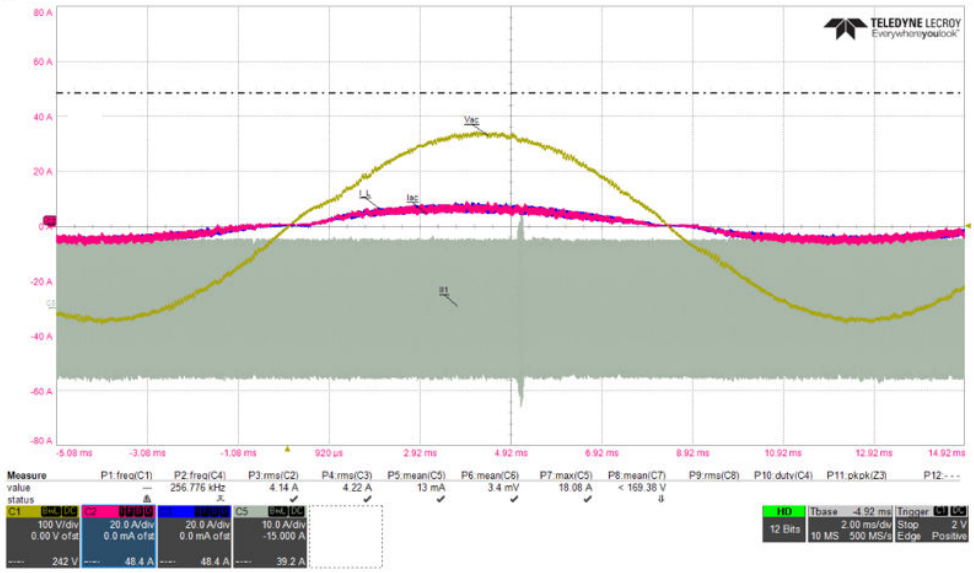
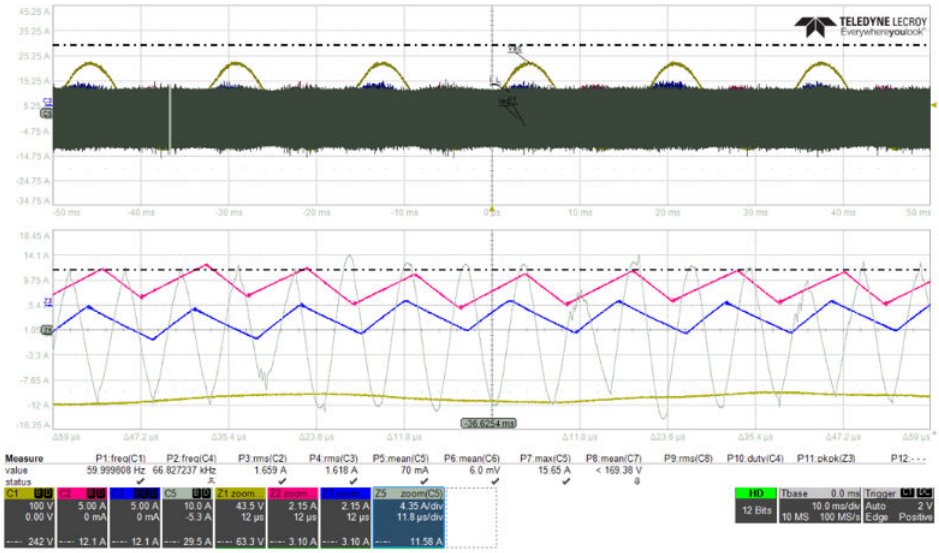


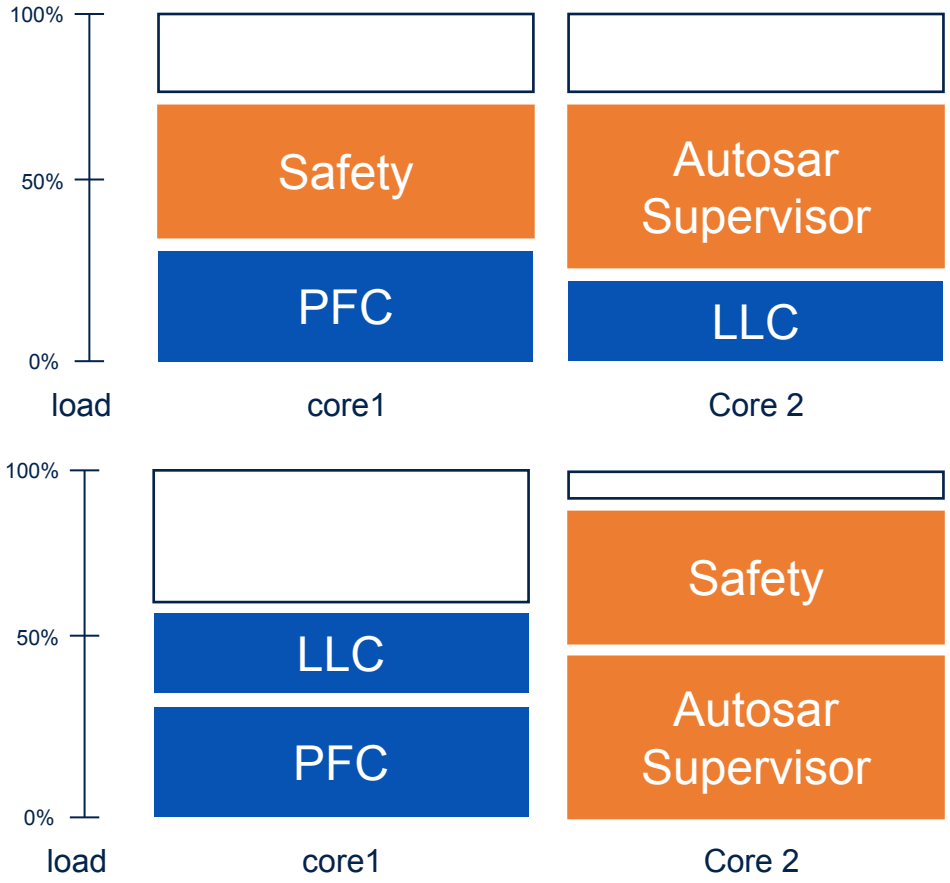
Figure 52. Zoom of dual core waveforms



9.6 Dual core vs lock step application

Test using one single SR5E1 MCU even if not performed at maximum power for some noise limitation on the adapter demonstrates that single SR5E1 is able to execute the PFC and LLC algorithm with high level of performance allowing a good level of room on the two micros that can be used for running a full Autosar stack and possible addition of safety and diagnostic libraries to match customer use cases. Possible microcontroller allocations options are represented into the following figure.

Figure 53. **Dual core vs lock step application**



10 Conclusions

The STDES-7KWOBC reference design consists of two separate sections: an interleaved totem pole PFC with inrush current limiter and a dual full bridge LLC resonant DC-DC converter, both power stages have been tested in each condition, showing the good performances of power devices and the capabilities of SR5E1 microcontroller to control an OBC system.

The SR5E1 microcontroller, with ARM architecture and 2 x high-resolution timers (HRTIM), has revealed to be the best choice as MCU for its analog peripherals and for control algorithm implementation in both PFC and DC-DC stages.

The 55 mΩ SCTH35N65G2V SiC MOSFETs in H2PAK proved to be suitable in Totem Pole PFC application achieving high efficiency and optimal thermal capability.

The galvanically isolated gate driver STGAP1AS, with 5 A capability, advanced protection, configuration and diagnostic features, showed a high noise immunity level.

The TN3050H-12GY-TR Thyristors (SCRs), placed in low frequency leg, allowed to reduce the number of components, performing the in-rush current limitation without using relay and NTC, and with a configurable timing set by MCU.

The high-voltage MDMesh DM6 STH47N60DM6-7AG power MOSFET with fast recovery diode shows effective switching behavior in resonant converter applications. On the other side, the ultra-high-performance power Schottky diode STPSC20065GY in SiC guarantees a high efficiency in rectification stage.

Appendix A Reference design warnings, restrictions and disclaimer

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Appendix B Reference documents

Table 13. **Reference documents**

Document name	Title
UM2940	Getting started with the STDES-7KWOBC 7 kW on-board charger reference design
RM0483	SR5E1x 32-bit Arm® Cortex®-M7 architecture microcontroller for electrical vehicle applications

Revision history

Table 14. **Document revision history**

Date	Version	Changes
08-Nov-2023	1	First release.

Contents

List of tables

List of figures