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Application note

SR5 E1 line–Resolver sensor in electric motor control demo

Introduction

The SR5 E1 line 32-bit Arm® Cortex® -M7 microcontrollers specifically developed for embedded applications integrate technologies that are particularly suited for driving electrical vehicles. SR5 E1 line typical applications include advanced electric motor control applications where sensing and/or controlling speed and rotor position are a fundamental requirement.

This technical note focuses on an electric motor speed and angle calculation technique with SR5 E1 microcontrollers. After an overview of the electric motor field oriented control, it is described in detail the configuration and usage of the SR5 E1 peripherals for speed and rotor position calculation, using a resolver sensor, implemented in the SR5 E1 motor control tool kit (MCTK) demo application (refer to STMicroelectronics local representative for reference hardware and software).

Stellar

1 FOC

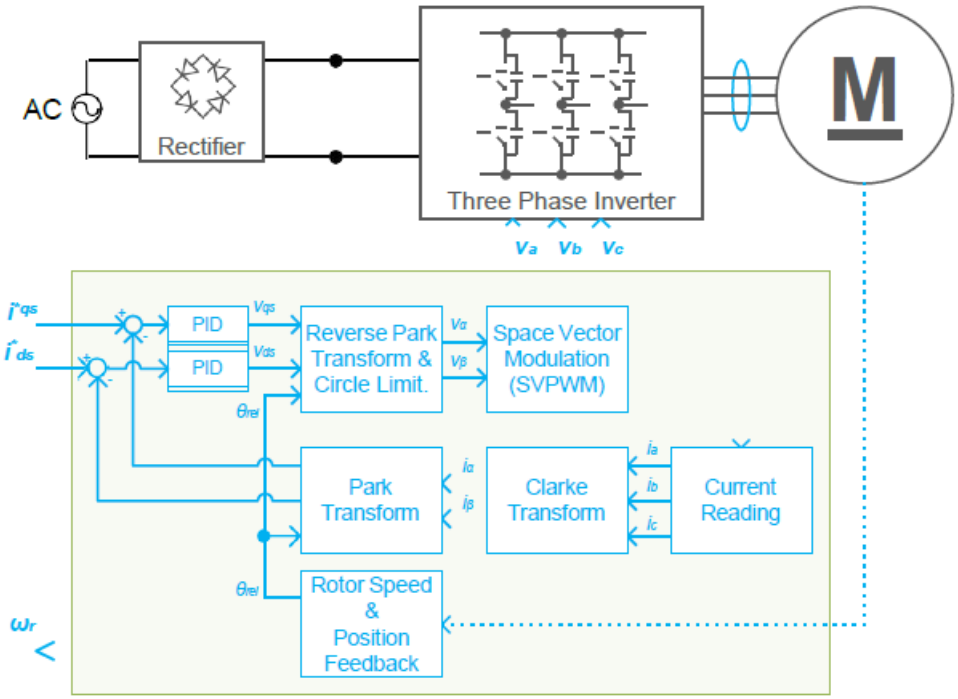
1.1 Introduction to PMSM FOC drive

The field oriented control (FOC) is a vectorial control strategy for driving permanent-magnet synchronous motors (PMSM). It consists of controlling the stator currents represented by a space vector, phase angle and magnitude, by which the terminology “vector control”.

With this approach, it is possible to offer electromagnetic torque (Te) regulation and, to some extent, flux weakening capability by controlling the two currents iqs and ids, which are mathematical transformations of the stator currents. Therefore, FOC consists in controlling and orienting stator currents in phase and quadrature with the rotor flux. So, it is clear that the fundamental is the measuring of stator currents and the rotor angle and rotor speed.

The structure of the FOC algorithm is represented in the following figure.

Figure 1. Basic FOC algorithm structure, torque control



- The *iq*s* and *id*s* current references can be selected to perform electromagnetic torque and flux control.
- The Space vector PWM block (SVPWM) implements an advanced modulation method that reduces current harmonics, thus optimizing DC bus exploitation.
- The current reading block allows the system to measure stator currents correctly, using either cheap shunt resistors or market-available Hall sensors or isolated current sensors (ICS).
- The rotor speed/position feedback block allows the system to handle Hall sensor, incremental encoder, or resolver signals to correctly acquire the rotor angular velocity and position.
- The PID controller implements proportional, integral, and derivative feedback controllers (current regulation).
- The Clarke, park, reverse park, and Circle limitation blocks implement the mathematical transformations required by FOC.

2 Rotor angle and rotor speed calculation in SR5 E1 electric motor control demo

As described in Section 1.1: Introduction to PMSM FOC drive, field-oriented electric motor control depends on the motor phase current, the accurate acquisition of rotor angle position and rotor speed.

There are different possible rotor position acquisition techniques based on the type of sensors used. The most common are hall sensors, encoders and resolvers. Each type of sensor has its pros and cons in terms of hardware costs, simplicity of software implementation and the accuracy of speed and rotor position.

The resolver, among the three, is an analog sensor and it is the best method to precisely know the rotor position and speed. It offers the best information that can be used in feedback motor control to optimize the motor performance.

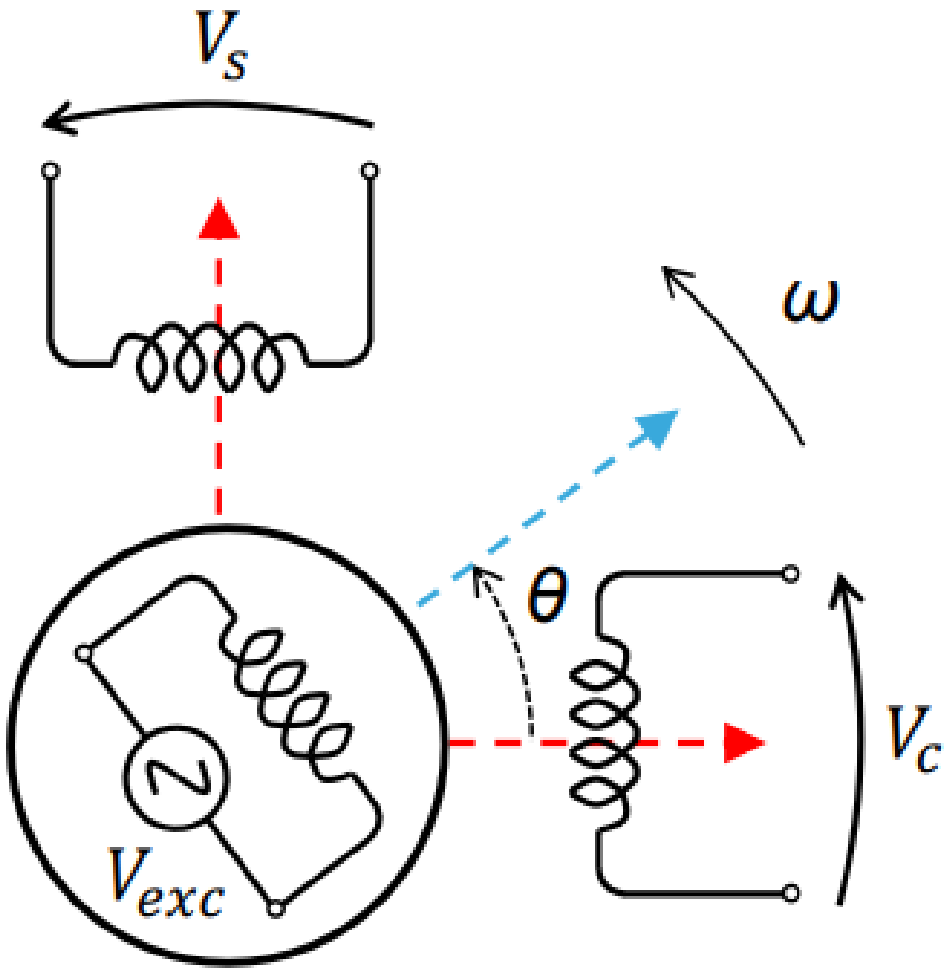
In the following paragraphs the focus is rotor position and speed measurement implementation with resolver and details are given about SR5 E1 peripherals and techniques used to excite the resolver with an SR5 E1 B-DAC peripheral and acquisition of resolver signals with the SR5 E1 ADC.

2.1 Resolver model and equations

The Figure 2. Resolver sensor modelshows the electrical model of the resolver. Resolver hardware can be viewed as two inductive position sensors, which, upon a supplied sinusoidal shaped signal on the input, generate two sinusoidal signals on the output. When the primary winding is excited with a sinusoidal signal V_{exc}, two voltages V_C and V_S are induced in the secondary windings.

The output signal amplitudes depend on the position of the motor rotor. In particular the amplitude of one signal is proportional to the sine, the amplitude of the other is proportional to the cosine of the motor rotor angle position as described in the following equations.

Figure 2. Resolver sensor model



Resolver input:

$$V_{exc} = V_0 \sin\ (2\pi f_{exc})$$

Resolver outputs

$$V_C = t_r V_0 \sin\ \left(2\pi f_{exc} t\right) \cos\left(\omega t\right)$$

$$V_s = t_r V_0 \sin\ (2\pi f_{exc} t) \cos\ (\omega t)$$

Where:

V_0= is the excitation amplitude

f_{exc}= is the excitation frequency

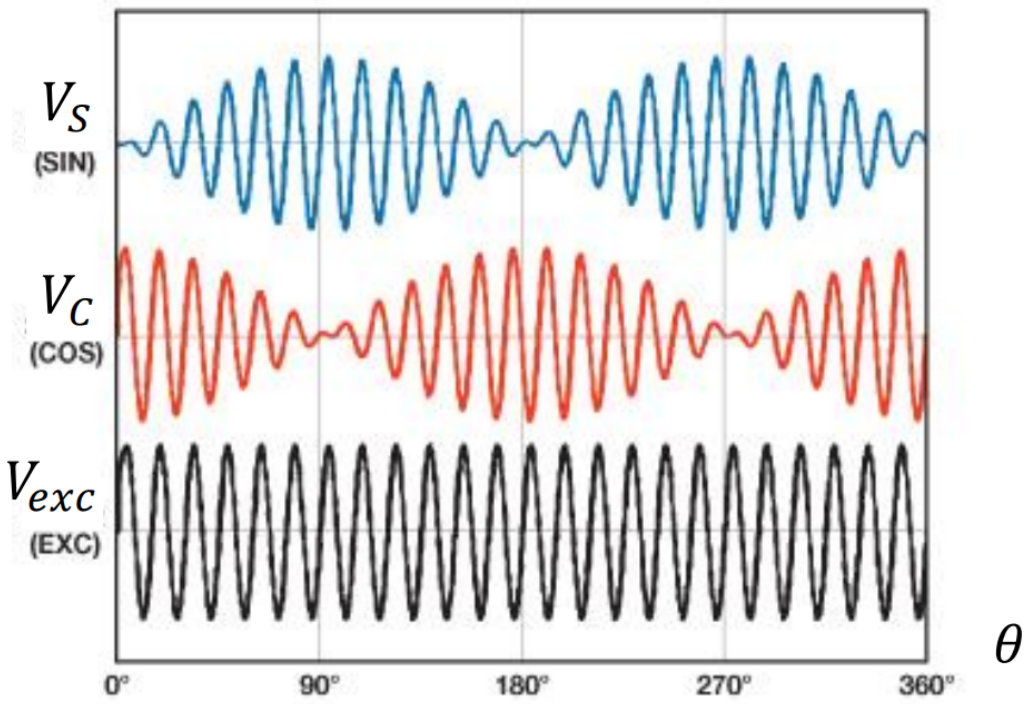
ω is the motor shaft angular speed

ωt=Ø is the shaft angle

t_r=transfer ratio

The V_C and V_S resolver outputs are modulated by the sin (Ø) and cos (Ø) with Ø = *ωt*. When the angular speed ω of the motor is constant a graphical representation of excitation signal and resolver outputs are shown in the following figure.

Figure 3. Resolver sensor input output signal



An hardware/software system interfacing a resolver has to implement at least the following four main tasks to get rotor position and speed:

- Generate the exciting signal V_{exc} for the resolver.
- The acquisition of the V_S and V_C resolver output signals that are proportional respectively to the sin (ωt) and cos (ωt), with ωt = Ø.
- Demodulation of resolver outputs: that is getting the sin (Ø) and cos (Ø) with Ø motor rotor position.
- Calculate Ø and ω from sin (Ø) and cos (Ø).

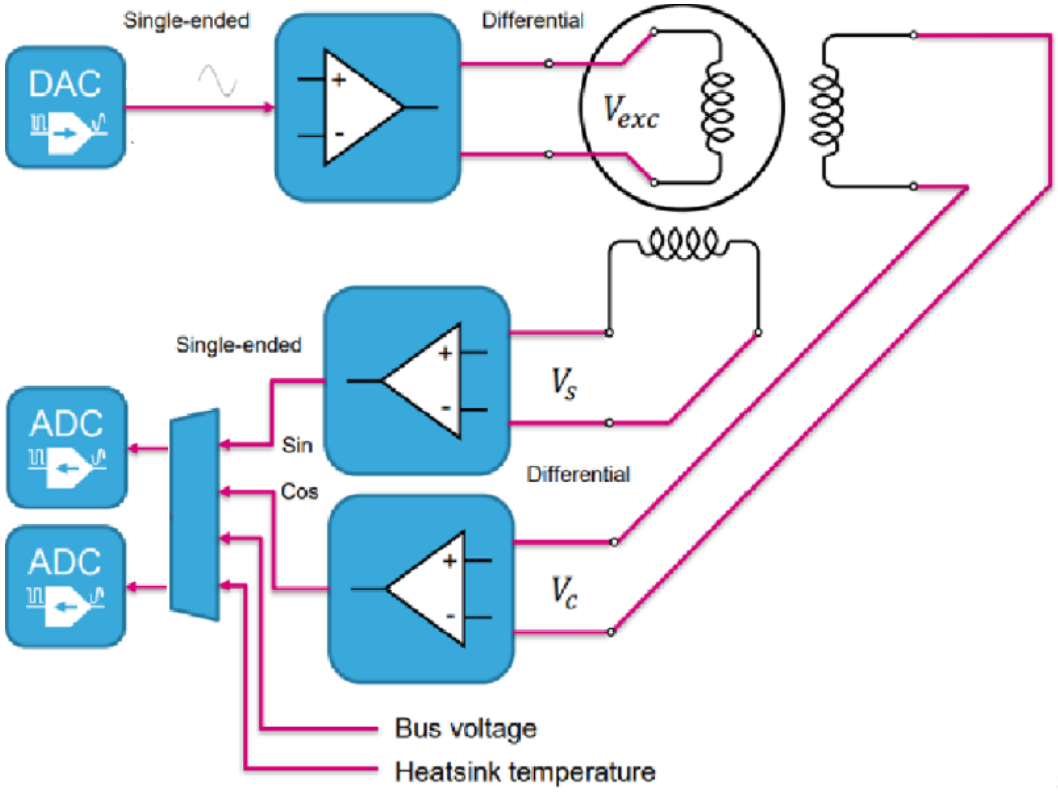
In the following paragraphs are shown details about the HW/SW interface in SR 5E1 MCTK that implements the previous four tasks. Here after there are references to SR5 E1 peripherals and registers and reference to MCTK software parameter driver, so the user could refer to SR5 E1 MCTK SW and documentation for further details.

2.2 MCTK hardware interfacing the resolver

In the MCTK the signals exchanged between the resolver and microcontroller IPs need an interface circuit. The resolver output signals are differential and have to be converted to single-ended so to be managed by the SR5 E1 ADC. In the same way the SR5 E1 B-DAC signal implementing the exciting sinusoid is single-ended and must be converted to a differential signal to be used as the exciting V_{exc} signal to the resolver

The following figure shows the block diagram of SR5E1 peripherals connected to the resolver sensor through an amplifier-based circuitry needed for single ended to differential and vice versa signal conversion.

Figure 4. HW interfacing the resolver in MCTK



In particular the following figure details the MCTK circuitry for single ended to differential conversion of the V_{exc} output signal (RES_EXC_FROM_MCU) of SR5E1 DAC. The Figure 6. SR5E1–resolver output conversion circuitry details the circuitry for differential to single ended conversion of the resolver output (E_RES_SIN+/- FROM SENSOR, E_RES_COS+/- FROM SENSOR) to be managed by SR5E1 ADCs.

Figure 5. SR5E1–DAC output conversion circuitry

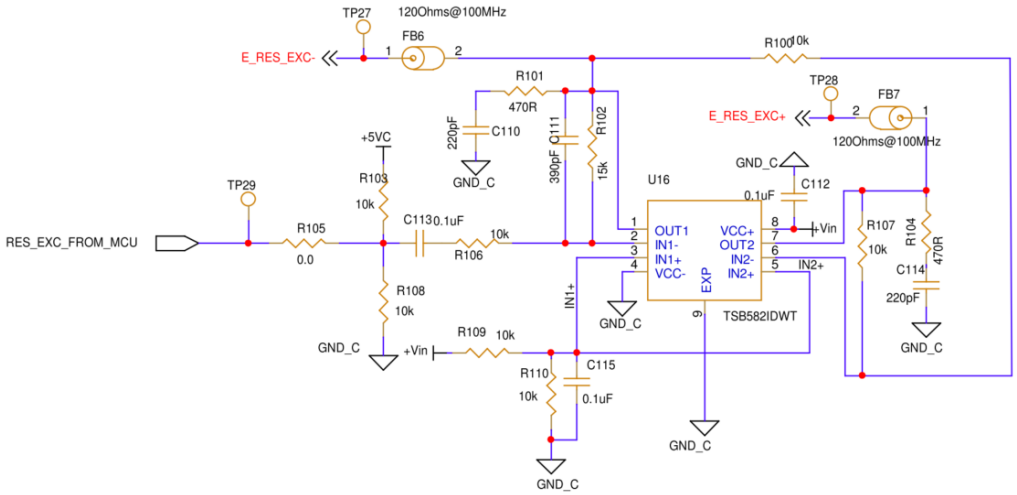
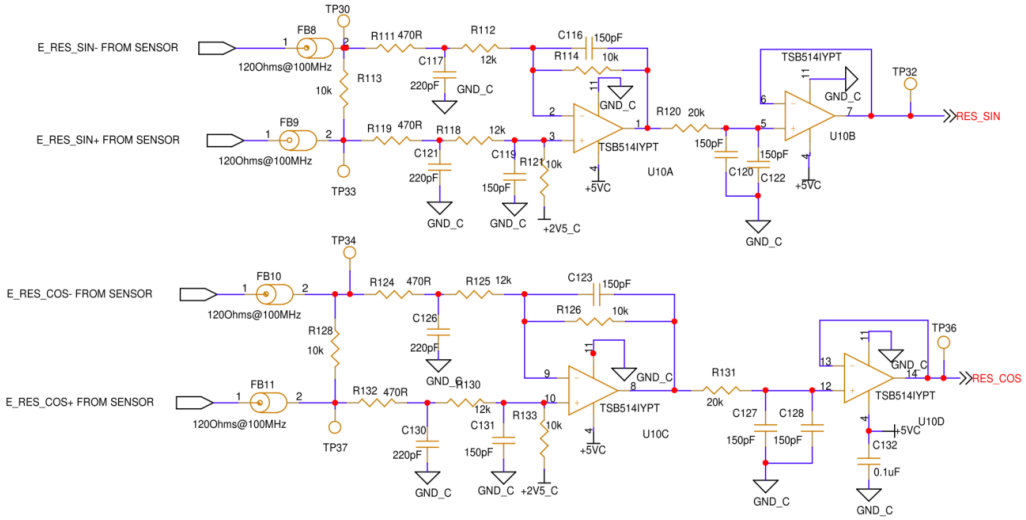


Figure 6. **SR5E1–resolver output conversion circuitry**



2.3 Exciting signal generation

In the MCTK the SR5E1 B-DAC1 peripheral is used to generate an excitation V_{exc} signal.

B-DAC1 is triggered by timer TIM6 and in particular the TIM6_TRGO signal is used to trigger the updating of the B-DAC1 output voltage whose values are taken from the hSin lookup table composed of N_{elem} elements. (Update event of TIM6 is selected as a trigger output setting MMS[3:0]=b0010 bits in the TIM6_CR2 register). hSin table is a software variable (array table) that contains the sinusoidal data to be converted in voltage.

The f_{exc} frequency of resolver exciting signal, that is $V_{exc} = V_0 \sin(2\pi f s_{exc})$, is set configuring appropriately timer TIM6. In particular, to have the desired resolver exciting f_{exc} frequency, the auto reload TIM6 ARR field register value is given by the following equation:

$$TIM6ARR = \frac{\text{TIMfreq}}{Nelem * fexc}$$

With

TIMfreq= 150 MHz

N_{elem} = 64

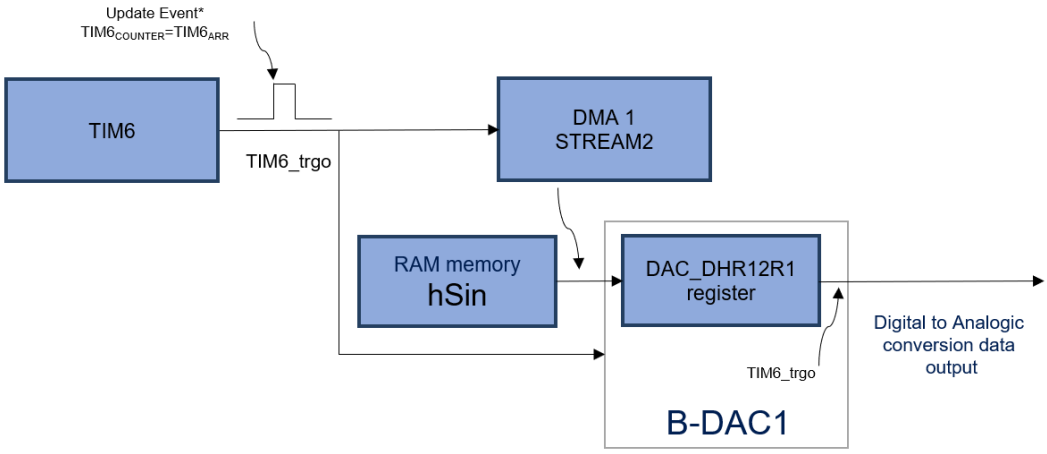
f_{exct} = it is the excitation frequency

In the MCTK the DMA is used to update, with no CPU load, the B-DAC1 output register. In particular the DMA1 stream 2, triggered by TIM6_trgo (TIM6 overflow), moves the data hSin available in memory to B-DAC1 output register DAC_DHR12R1. The DMA is programmed in circular mode with memory increments enabled and peripheral increments not enabled.

The TIM6_trgo signal is also used to trigger the B-DAC1 digital to analogical conversion of the transferred data in DAC_DHR12R1 register available in output. TIM6_trgo is linked to the B-DAC1 setting in the DAC_CR register the bitfield TSEL1[3:0]=0x7 and then enabling it setting DAC_CR.TEN1=b1.

In the following figure it is shown TIM6 trgo signal connection for triggering DMA transfer of hsin table and for digital to analogical conversion.

Figure 7. TIM6 trgo signal connection



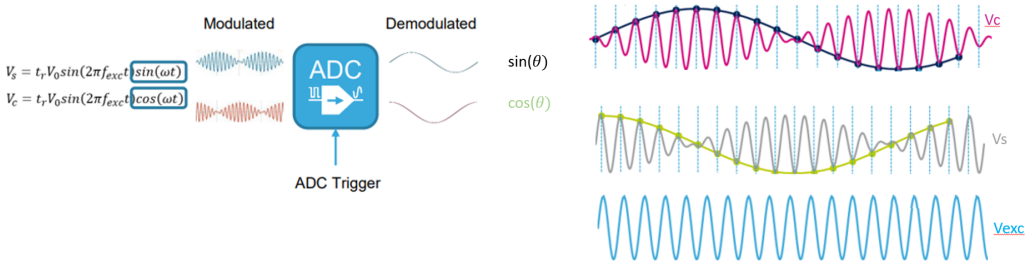
Note: An update event is generated at each TIM6 counter overflow.

2.4 Resolver output demodulation

As seen in Section 2.1: Resolver model and equations, the two resolver output V_s and V_c are signals modulated with sin (Ø) and cos (Ø) with Ø motor rotor position . To get the values of the sin (Ø) and cos (Ø) a demodulation is needed.

The demodulation, as shown in the following figure, is performed sampling with ADC V_S and V_C signals in their peak values (these are also peaks of exciting signal). In the following figure the yellow and black lines connecting all the peaks values are the sin (Ø) and cos (Ø).

Figure 8. Demodulation of resolver output



In the MCTK two SAR-ADC units are used to sample the resolver V_S and V_C signals:

- SAR ADC 3 (or SAR ADC 1) for V_S demodulation
- SAR ADC 4 (or SAR ADC 2) for V_C demodulation.

ADC injected conversions are preferred to have maximum priority (prevent ADC conversions from being interrupted by others).

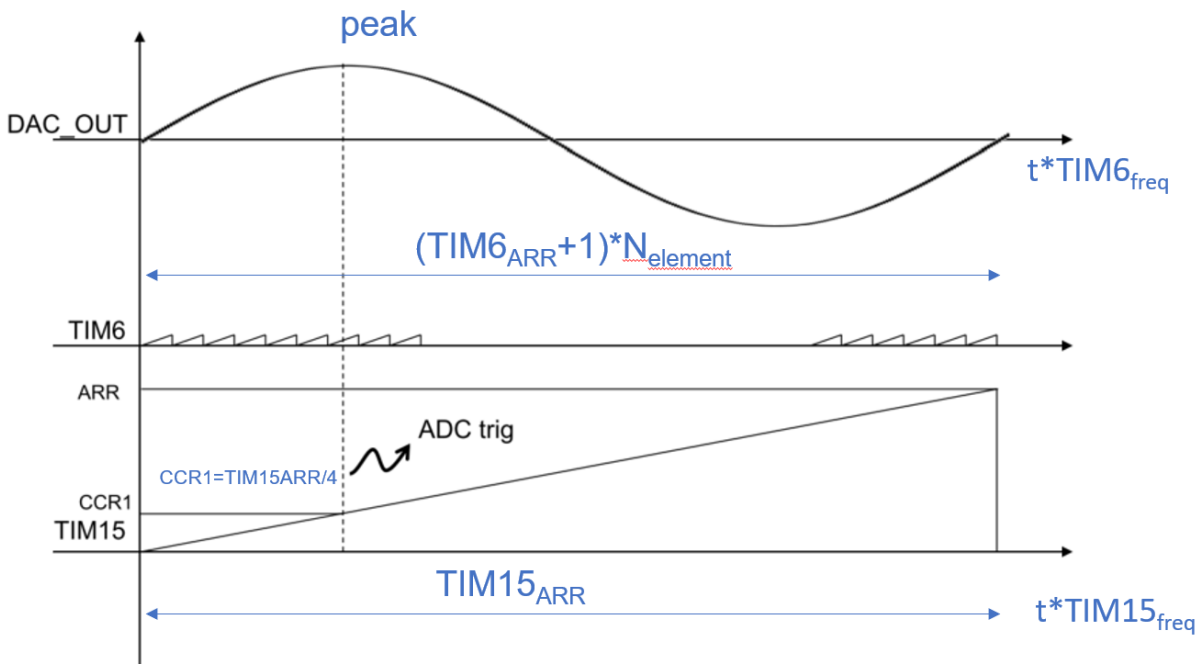
Let us see in detail how the sampling of the V_S and V_C peak signals, using timer TIM15, is implemented in the MCTK demo. The hsin table (containing sinusoidal values to be implemented in output) is composed of $N_{element}$ and each element is sent to the B-DAC1 output register every period of time given by the value of the TIM6 ARR register field. This means that a full sinusoid into B-DAC output is obtained in a period of time proportional to (TIM6ARR+1)*$N_{element}$.

As shown in the following figure, starting timer TIM6 and timer TIM15 in the same instant and having the two timers ARR field registers set according to the following equation:

$$TIM15ARR = (TIM6ARR + 1) * N_{element} - 1$$

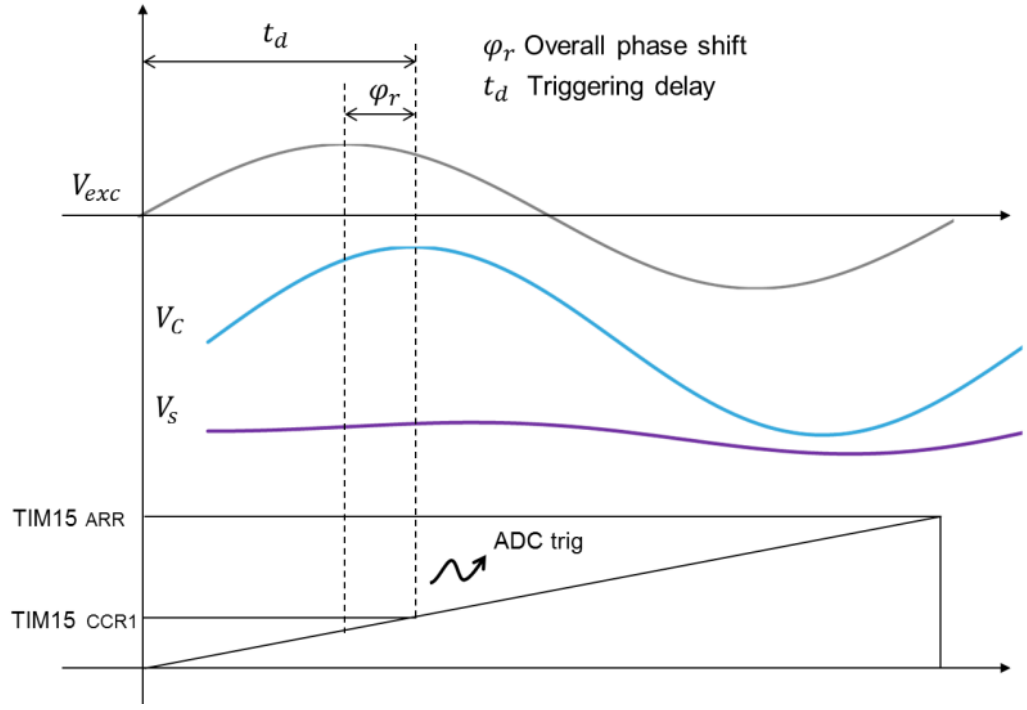
and setting TIM15 field register CCR1=TIM15ARR/4, the TIM15_TRGO triggering signal to the ADC is set exactly on the peak of the B-DAC1 output sinusoid.

Figure 9. SR5E1 TIM6 TIM15 synchronization to sample V_S V_C in their peaks



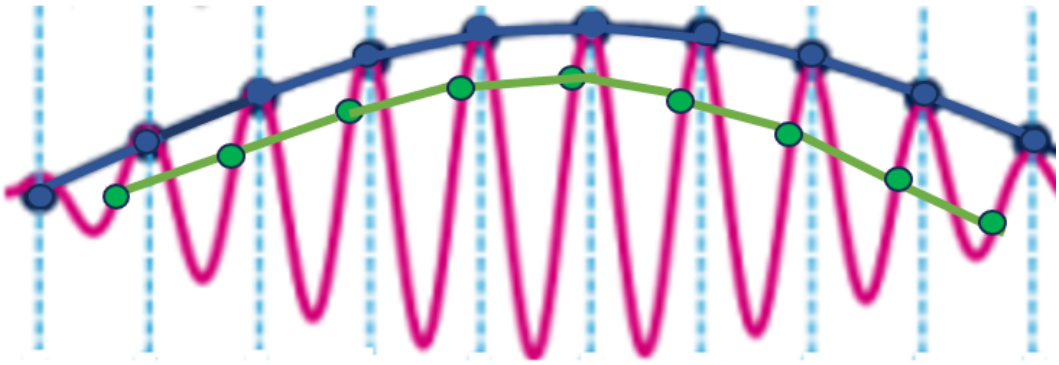
The user should consider that due to hardware delay the maximum value of the V_C and V_S resolver output signal is shifted of φ_r respect to the maximum of the V_{exc} as shown in the following figure. This delay implies that the CCR1 value has to be empirically tuned respect to its ideal value of CCR1=TIM15ARR/4 to have ADC trigger exactly or very close to the peak of V_C and V_S.

Figure 10. Resolver phase delay



In the following figure it is compared the demodulated signal obtained sampling the resolver output in its peak (blue line), with the green demodulated signal obtained sampling the resolver output far from the peaks.

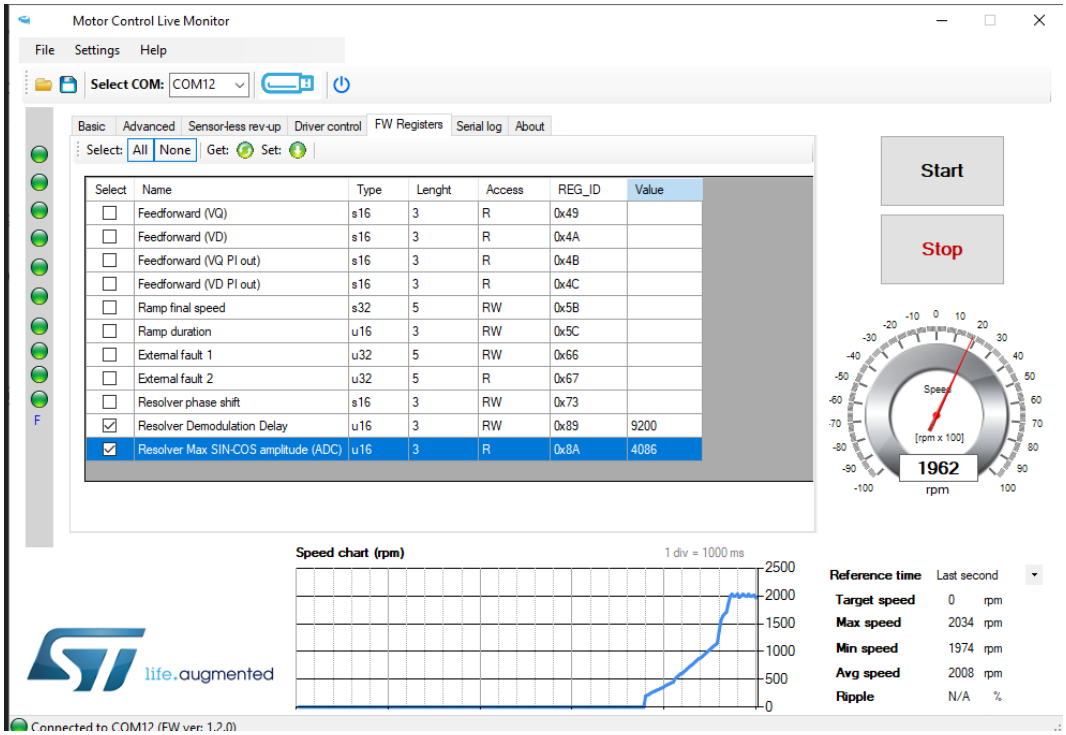
Figure 11. **Resolver output sampling**



Sampling the resolver output on its peaks maximizes the amplitude of the demodulated sine/cosine signals having a better sine cosine signal (bigger signal to noise ratio) to be used for PLL management for rotor and speed calculation.

In the MCTK live monitor GUI, shown in the following figure, there is the possibility to change the value of the parameter **resolver demodulation delay** to implement the tuning of the correct value of the field register CCR1 and compensate the hardware delay. The user, while changing the parameter **resolver demodulation delay,** has to monitor the value of the feedback variable **resolver MAX ADC sin cos.** When this feedback variable is around 4095 (SR5 E1 12-bit ADC resolution) means that the resolver output signals V_C and V_S are sampled close to their maximum values and the demodulated sin/cos signals have the maximum amplitude.

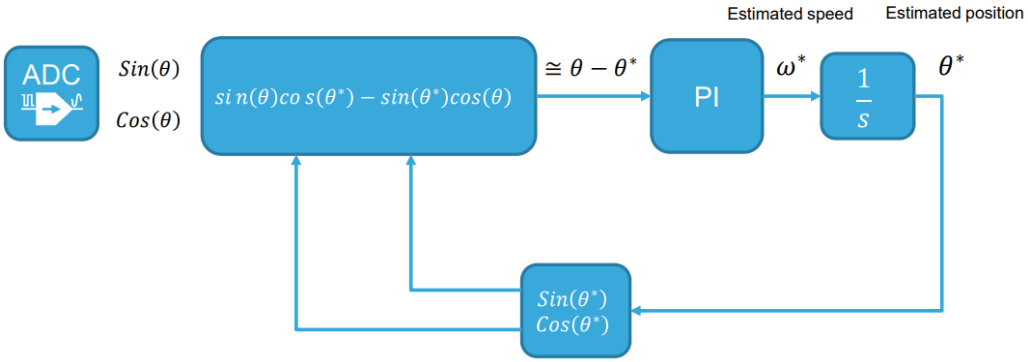
Figure 12. **MCTK live monitor GUI**



2.5 Rotor Angle and speed calculation

The two acquired demodulated resolver signals sampled by the SAR ADC 3 and SAR ADC 4 are subsequentially managed by a phased locked Loop (PLL) to calculate the Ø and ω that are then used in the FOC electric motor control algorithm. The PLL is a well-known algorithm in the technical literature and its description and mode of operation are beyond the scope of this document and here it is only important to know that the MCTK SW driver uses a PLL for calculating Ø and ω from sin (Ø) and cos (Ø) obtained, as seen in the previous paragraphs, by appropriately sampling V_S and V_C in the peaks of the excitation signal.

Figure 13. Phase locked loop block diagram



sin (Ø) cos (Ø) * - sin (Ø) * cos (Ø) = sin (Ø) - (Ø) * ≅ (Ø) - (Ø)

Appendix A Reference documents

The following table shows the list of acronyms used in this document.

Table 1. Terms and abbreviations

Acronym	Definition
A/D	Analog to digital
ADC	Analog-to-digital converter
DAC	Digital analog conversion
FOC	Field oriented control
MC	Motor control
MCTK	Motor control tool kit
MCU	Microcontroller unit
PID	Proportional-integral-derivative (controller)
PLL	Phase locked Loop
PMSM	Permanent magnet synchronous motor
PWM	Pulse width modulation
SVPWM	Space vector pulse width modulation

Revision history

Table 2. **Document revision history**

Date	Version	Changes
20-Feb-2024	1	Initial release.

Contents

List of tables

List of figures