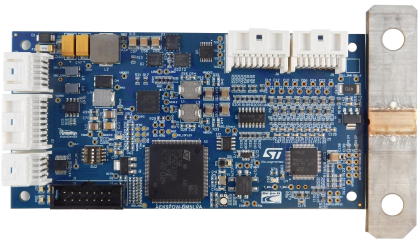
AEK-POW-BMSLV

Data brief

Battery management system evaluation board for low-voltage applications



Product summary	
Battery management system evaluation board for low-voltage applications	AEK-POW-BMSLV
Automotive general purpose SPI to isolated SPI transceiver	L9963T
Automotive chip for battery management applications with daisy chain up to 31 devices	L9963E
32-bit Power Architecture MCU for Automotive General Purpose Applications - Chorus family	SPC58EC80E5QMC1X
Power management IC for highly integrated processors	SPSB100 (customized version)
Quad-channel HSD with analog current sense	VNQ7050AJ
Application	Automotive Battery Management System (BMS)

Features

- Low-voltage (<60V) single board for a complete battery management system (BMS)
- Hosts:
  - L9963E AEC-Q100 qualified automotive multicell battery monitoring and balancing IC
  - L9963T AEC-Q100 qualified automotive general-purpose SPI to isolated SPI bidirectional transceiver
- SPC58EC80E5 microcontroller automotive grade to perform charge balancing and to compute the state of charge (SOC) and the state of health (SOH)
- VNQ7050AJ quad channel high-side driver for battery pack contactor driving
- SPSB100 (custom version with CAN port) fully integrated power management system IC of which the following features have been implemented on the board:
  - CAN FD transceiver for external communication
- Additional external CAN transceiver
- SPI for external communication
- Configurable window watchdog
- System wake-up feature and ignition wake-up
- Fault collection control unit (FCCU) used to collect eventual issues raised by the micro and according to an implemented logic perform some actions like system shutdown
- Fail-safe diagnosis from SPSB100 to microcontroller
- Voltage and current monitoring of every single cell and of the entire battery node
- 8 GPIOs to connect temperature sensors as NTCs, of which four GPIOs wired to the microcontroller while the other four to the L9963E
- Passive balancing is executed through 100kΩ external resistors
- Dimensions: 145x65mm
- Included in the AutoDevKit ecosystem

Description

The AEK-POW-BMSLV is built with automotive-grade components, and it is able to connect to a battery pack and to monitor both state of charge (SOC) and state of health (SOH) of each battery.

It also manages battery balancing by passive discharge, thanks to the software already preloaded on the on-board SPC58EC80E5 microcontroller.

The AEK-POW-BMSLV has been specifically designed to manage the battery management system for low-voltage applications: applications whose voltage range is below 60 V, for example, motorcycles auxiliary power and electric bikes.

The versatile CAN2.0A/B protocol facilitates integration into several systems and efficient component communication.

The AEK-POW-BMSLV is equipped with two CAN ports for flexible networked connections, while four high-side channel outputs optimized power distribution.

The BMS adjusts to various battery configurations, supporting from 4 up to 14 series-connected cells.

It hosts the following devices: SPC58EC80E5, L9963E, L9963T, SPSB100 (customized version with CAN port), and VNQ7050AJ.

The SPC58EC80E5 automotive-grade microcontroller is responsible for calculating the SOC and the SOH of the battery pack connected, based on the measurement provided by the L9963E through the L9963T ISOSPI<>SPI transceiver.

The SPSB100 power mananagement integrated circuit (PMIC) has been integrated in this board as a customized version. This version features an embedded CAN-FD transceiver able to address and transmit the relevant information from the AEK-POW-BMSLV to an external domain control zone.

The VNQ7050AJ is used to drive contactors to disconnect the battery pack in case of maintenance or failure.

Thanks to the L9963T transceiver, the MCU and the L9963E communicate through the ISOSPI protocol, implementing differential communication for higher noise immunity. This is not strictly required considering it is a low voltage application but it opens the possibility for easy extension to the high voltage case.

The main activity of the L9963E is monitoring cells through stack voltage measurement, cell voltage measurement, temperature measurement, and coulomb counting. Measurement and diagnostic tasks can be executed either on demand or periodically, with a programmable cycle interval.

The main functions of a standard BMS are monitoring and protecting the battery pack. The protection function brings the system to a safe state in case of under/overvoltage and overheating.

Our board safety features include overload and overvoltage protection, against potential issues that could compromise battery integrity, alongside over-discharge protection to prevent excessive discharge and extend battery life.

AEK-POW-BMSLV core features ensure battery health and longevity. Continuous voltage monitoring provides real-time information about the battery status, enabling quick detection of deviations from ideal voltage levels, ensuring reliability, and preventing potential issues.

The AEK-POW-BMSLV provides an elaborate monitoring network to sense the voltage, current, and temperature of each cell. This sensing allows elaborating the SOC of each battery cell and, consequently, the state of charge of all battery packs.

The SOC allows assessing the remaining battery capacity. For maintenance reasons, it is important to monitor the SOC estimation over time.

According to our algorithm based on an extended Kalman filter for the SOC calculation, the more the SOC differs from its nominal value (that is, its value when the batteries are new), the more a cell of the battery pack risks overdischarge.

Thus, the SOC evolution over time allows asserting the state of health (SOH) of a cell or a battery pack to spot early indications that a cell is at risk of overdischarge or overcharging.

The SOC of a battery cell is required to maintain its safe operation during charge, discharge, and storage.

However, SOC cannot be measured directly and is estimated from other measurements and known parameters (such as characterization curves or look-up tables). This information on the battery cells is necessary to determine how the voltage varies according to the current, the temperature, etc., based on the battery chemical composition and production lot used.

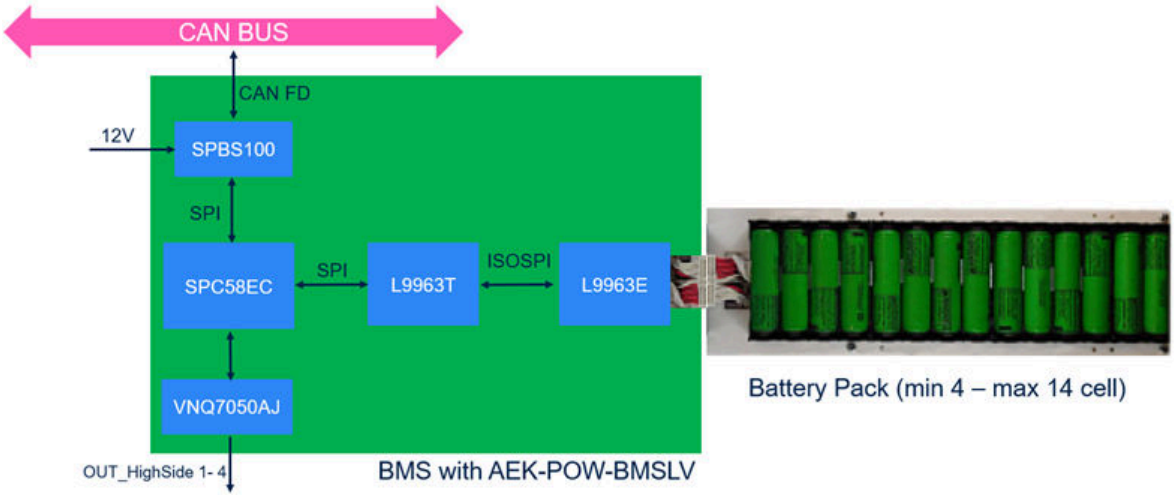
In the AutoDevKit ecosystem, we developed a demo application based on the SPC58EC80E5 microcontroller, to estimate the SOC of 14 cells in a BMS node connected with an AEK-POW-BMSLV evaluation board.

The results of SOC estimation, cell voltage, battery pack temperatures and current can be printed via the serial port to a terminal on the PC with a speed rate of 115200 bps.

For further information about the preloaded algorithm on the board, please refer to UM3185.

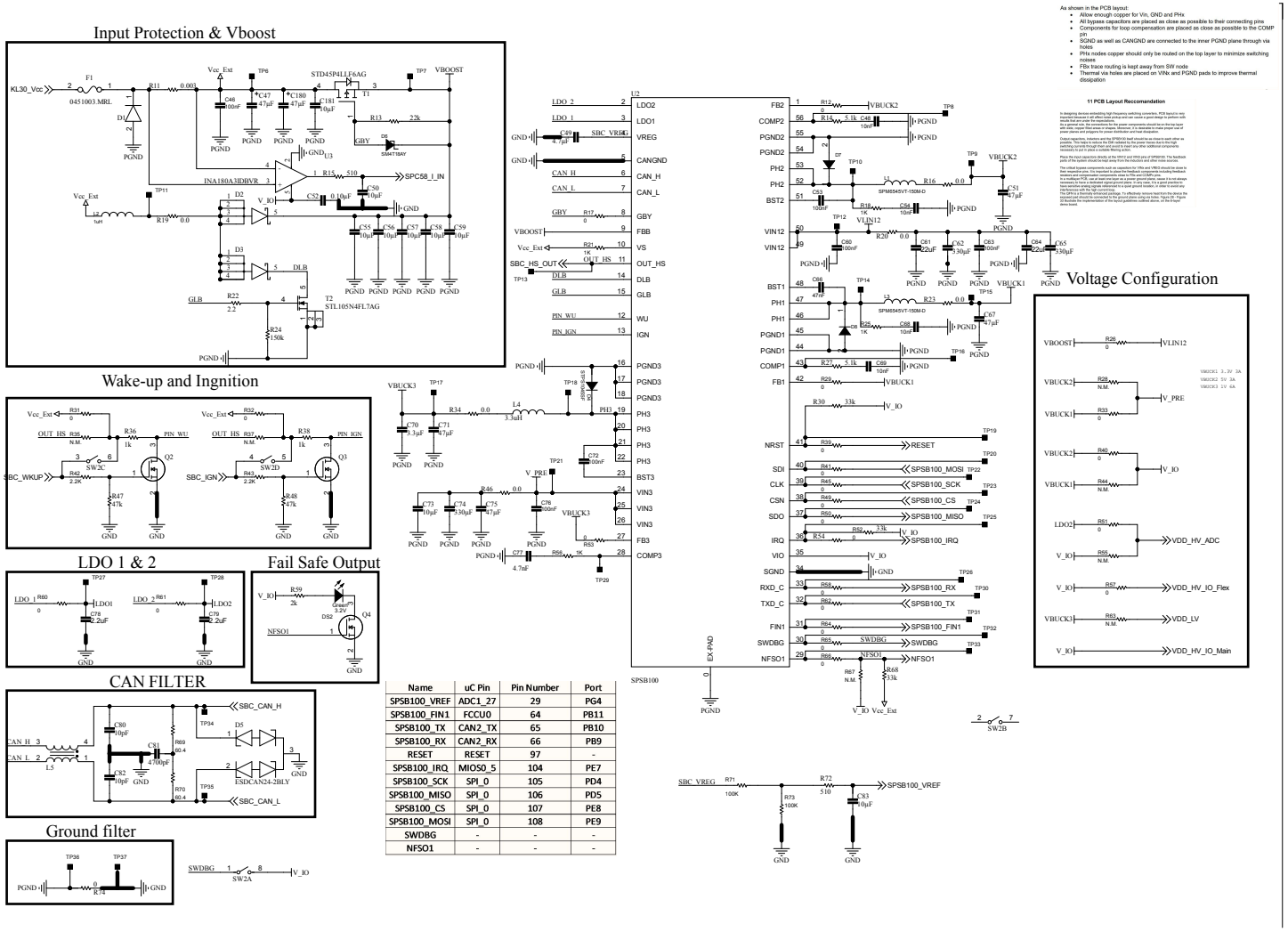
1 Block diagram

Figure 1. **Functional block diagram**



2 Schematic diagrams

Figure 2. **AEK-POW-BMSLV circuit schematic (1 of 11)**



Name	uC Pin	Pin Number	Port
SPSB100_VREF	ADC1_27	29	PG4
SPSB100_FIN1	FCCU0	64	PB11
SPSB100_TX	CAN2_TX	65	PB10
SPSB100_RX	CAN2_RX	66	PB9
RESET	RESET	97	-
SPSB100_IRQ	MIOS0_5	104	PE7
SPSB100_SCK	SPI_0	105	PD4
SPSB100_MISO	SPI_0	106	PD5
SPSB100_CS	SPI_0	107	PE8
SPSB100_MOSI	SPI_0	108	PE9
SWDBG	-	-	-
NFSO1	-	-	-

Figure 3. AEK-POW-BMSLV circuit schematic (2 of 11)

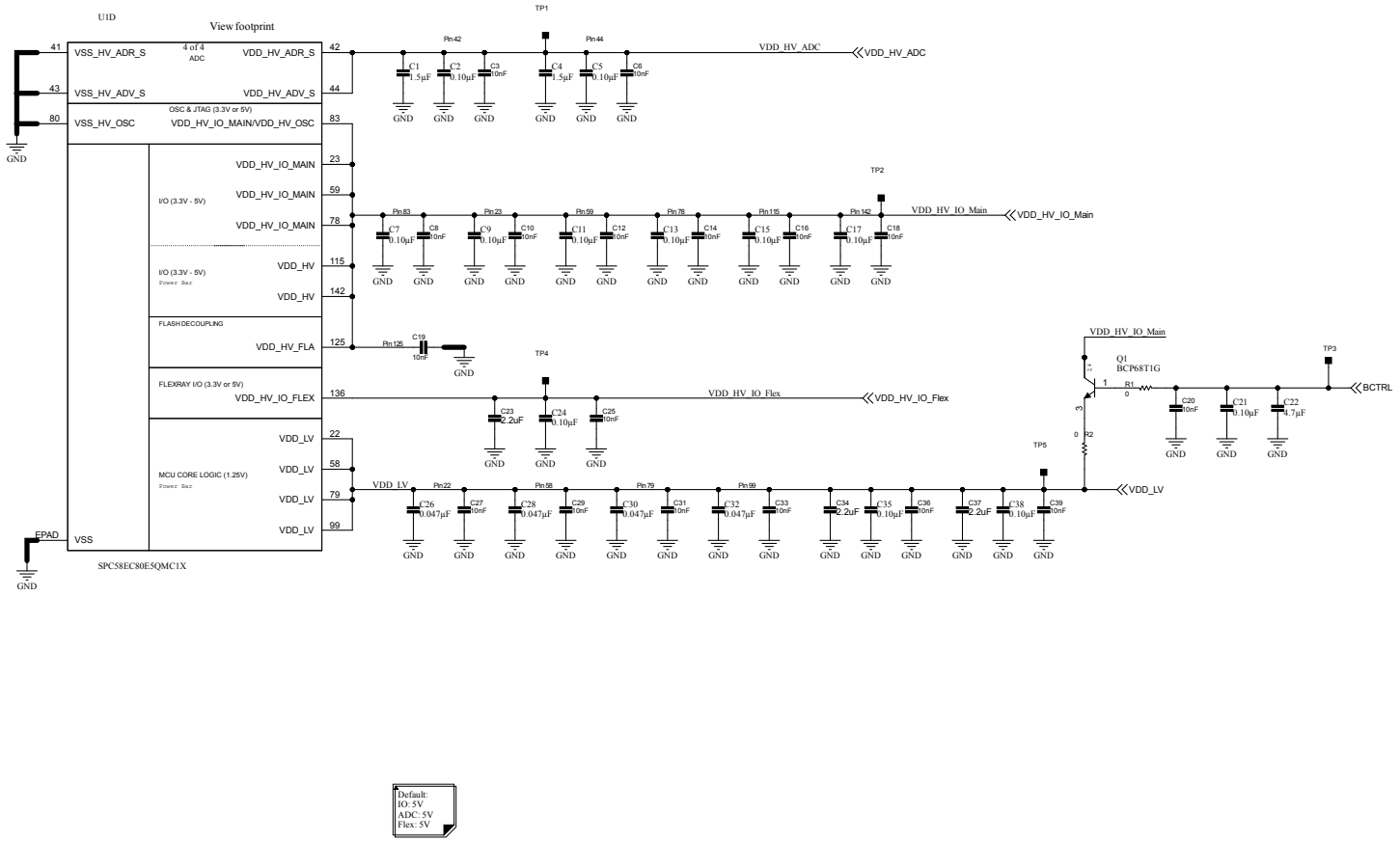
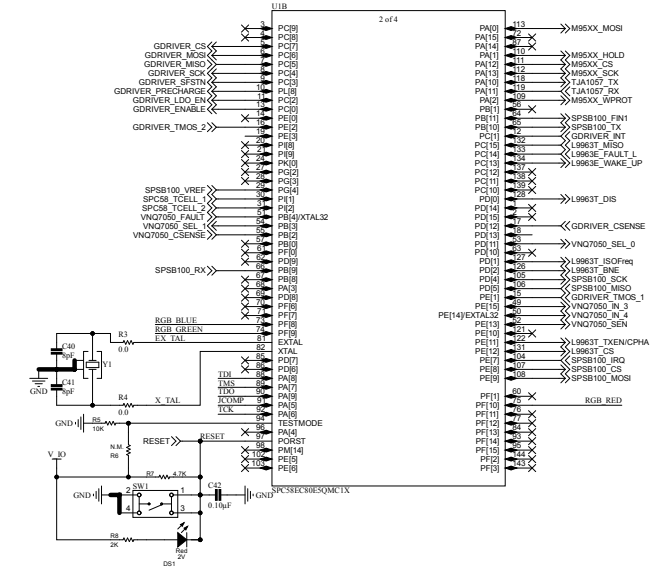
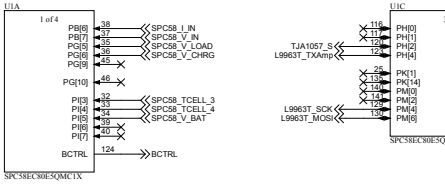
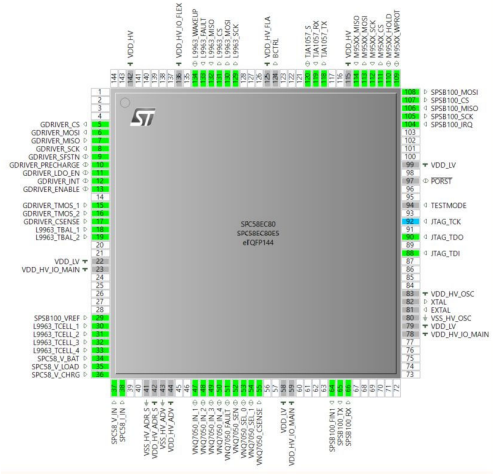


Figure 4. AEK-POW-BMSLV circuit schematic (3 of 11)

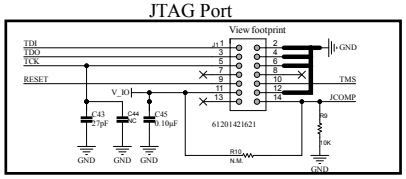




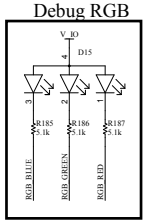


Name	uC Pin	Pin Number	Port
JTAG_TDI	TDI	88	PA8
JTAG_TMS	TMS	89	PA7
JTAG_TDO	TDO	90	PA9
JTAG_TCOMP	TCOMP	91	PA5
JTAG_TCK	TCK	92	PA6

JTAG Port



Debug RGB



Name	uC Pin	Pin Number	Port
GDRIVER_CS	SPI_3	5	PC7
GDRIVER_MOSI	SPI_3	6	PC6
GDRIVER_MISO	SPI_3	7	PC5
GDRIVER_SCK	SPI_3	8	PC4
GDRIVER_SFSTN	GPIO_035	9	PC3
GDRIVER_PRECHARGE	GPIO_184	10	PL8
GDRIVER_LDO_EN	GPIO_034	11	PC2
GDRIVER_INT	MIOSO_09	12	PC1
GDRIVER_ENABLE	GPIO_032	13	PC0
GDRIVER_TMOS_1	ADC1_12	15	PE1
GDRIVER_TMOS_2	ADC1_13	16	PE2
GDRIVER_CSENSE	ADC1_15	17	PD12
SPC58_TBAL_1	ADC1_16	18	PD13
SPC58_TBAL_2	ADC1_17	19	PE3
SPSB100_VREF	ADC1_27	29	PG4
SPC58_TCELL_1	ADC0_35	30	PI1
SPC58_TCELL_2	ADC0_38	31	PI2
SPC58_TCELL_3	ADC0_39	32	PI3
SPC58_TCELL_4	ADC0_40	33	PI4
SPC58_V_BAT	ADC0_41	34	PI5
SPC58_V_LOAD	ADC0_42	35	PG5
SPC58_V_CHRG	ADC0_44	36	PG6
SPC58_V_IN	ADC0_47	37	PB7
SPC58_I_IN	ADC0_48	38	PB6
VNQ7050_IN_1	GPIO_107	47	PG11
VNQ7050_IN_2	GPIO_108	48	PG12
VNQ7050_IN_3	GPIO_079	49	PE15
VNQ7050_IN_4	GPIO_078	50	PE14
VNQ7050_FAULT	GPIO_020	51	PB4
VNQ7050_SEN	GPIO_077	52	PE13
VNQ7050_SEL_0	GPIO_059	53	PD11
VNQ7050_SEL_1	GPIO_019	54	PB3
VNQ7050_CSENSE	ADC3_65	55	PB2
SPSB100_FIN1	FCCU0	64	PB11
SPSB100_TX	CAN2_TX	65	PB10
SPSB100_RX	CAN2_RX	66	PB9
RBG_BLUE	GPIO_088	73	PF8
RGB_GREEN	GPIO_089	74	PF9
RGB_RED	GPIO_090	75	PF10
JTAG_TDI	TDI	88	PA8
JTAG_TMS	TMS	89	PA7
JTAG_TDO	TDO	90	PA9
JTAG_TCOMP	TCOMP	91	PA5
JTAG_TCK	TCK	92	PA6
RESET	RESET	97	-
SPSB100_IRQ	MIOSO_5	104	PE7
SPSB100_SCK	SPI_0	105	PD4
SPSB100_MISO	SPI_0	106	PD5
SPSB100_CS	SPI_0	107	PE8
SPSB100_MOSI	SPI_0	108	PE9
M95XX_WPROT	GPIO_002	109	PA2
M95XX_HOLD	GPIO_001	110	PA1
M95XX_CS	SPI_2	111	PA12
M95XX_SCK	SPI_2	112	PA13
M95XX_MOSI	SPI_2	113	PA0
M95XX_MISO	SPI_2	114	PG15
L9963_SCK	SPI_1	129	PM4
L9963_MOSI	SPI_1	130	PM6
L9963_CS	SPI_1	131	PE12
L9963_MISO	SPI_1	132	PC15
L9963_FAULT	MIOSO_27	133	PC14
L9963_WAKEUP	GPIO_045	134	PC13

Figure 5. AEK-POW-BMSLV circuit schematic (4 of 11)

Pin Name	uC Pin	Pin Number	Port
SPC58_TBAL_1	ADC1_16	18	PD13
SPC58_TBAL_2	ADC1_17	19	PE3
SPC58_TCELL_1	ADC0_35	30	PI1
SPC58_TCELL_2	ADC0_38	31	PI2
SPC58_TCELL_3	ADC0_39	32	PI3
SPC58_TCELL_4	ADC0_40	33	PI4
L9963_SCK	SPI_1	129	PM4
L9963_MOSI	SPI_1	130	PM6
L9963_CS	SPI_1	131	PE12
L9963_MISO	SPI_1	132	PC15
L9963_FAULT	MIOS0_27	133	PC14
L9963_WAKEUP	GPIO_045	134	PC13

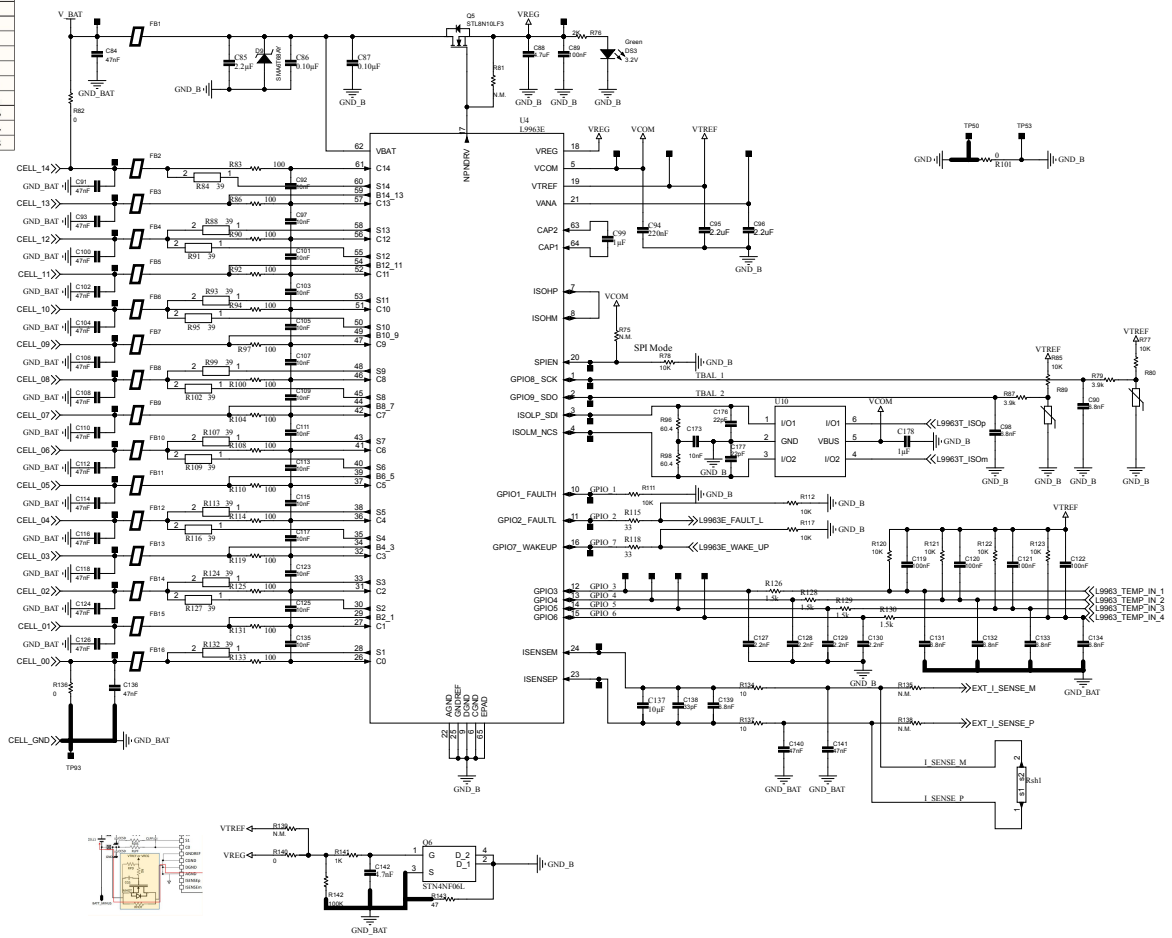


Figure 6. AEK-POW-BMSLV circuit schematic (5 of 11)

DISABLE				
DIS	Digital Input/Output (Open Drain)	Local	High	Transceiver Disable Input. Pull it up with external resistor connected to VIO. When DIS is high, L9963 enters in low power mode. When DIS is low, L9963T is enabled and working in Normal mode. It can be either pulled-down by the MCU to enable the unit, or pulled down internally when a wakeup condition occurs, in order to interrupt the MCU. Pin is internally pulled up with 100 kΩ resistor. Input filtered with RC filter having $f_{CUT\_pull\_is}$ cut frequency.

ISOLATED SPI				
ISOP	Analog Input/Output	Global	-	Isolated SPI Positive terminal
ISOM	Analog Input/Output	Global	-	Isolated SPI Negative terminal
TXAMP	Digital Input	Local		Isolated SPI TX amplitude selection. Set low to select low amplitude/low threshold. Set high to select high amplitude/high threshold. Internally pulled up with a 100 kΩ resistor.
ISOFREQ	Digital Input	Local		Isolated SPI operating frequency selection. Pull high to set high frequency. Pull down to set low frequency. Internally pulled down (active).

SPI				
SDO	Digital Output (Push-Pull)	Local	-	SPI Serial Data Output. Needs external pull up/pull down resistor to define inactive level.

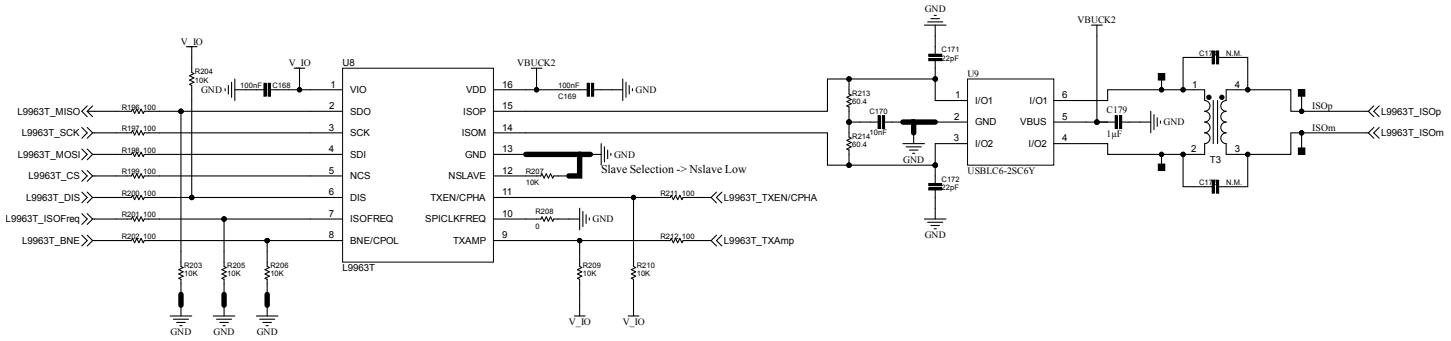


Figure 7. **AEK-POW-BMSLV circuit schematic (6 of 11)**

Pin Name	uC Pin	Pin Number	Port
M95XX_WPROT	GPIO_002	109	PA2
M95XX_HOLD	GPIO_001	110	PA1
M95XX_CS	SPI_2	111	PA12
M95XX_SCK	SPI_2	112	PA13
M95XX_MOSI	SPI_2	113	PA0
M95XX_MISO	SPI_2	114	PG15

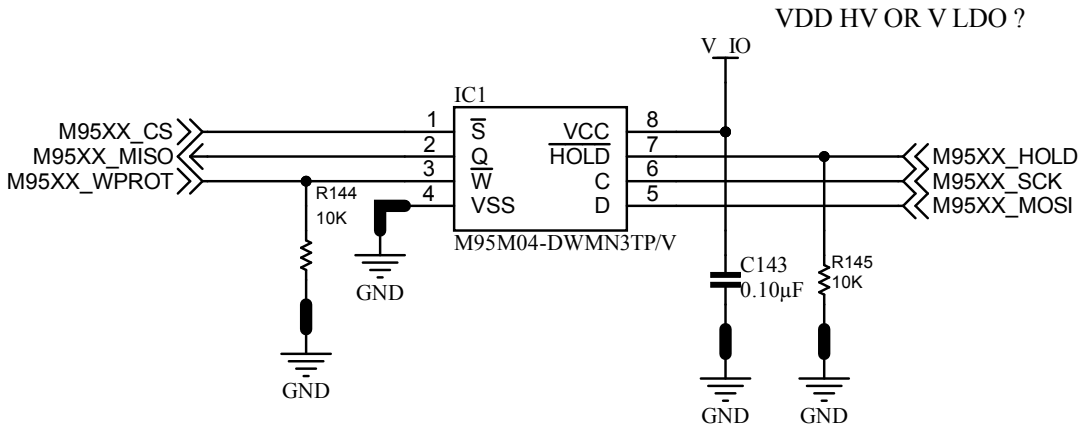
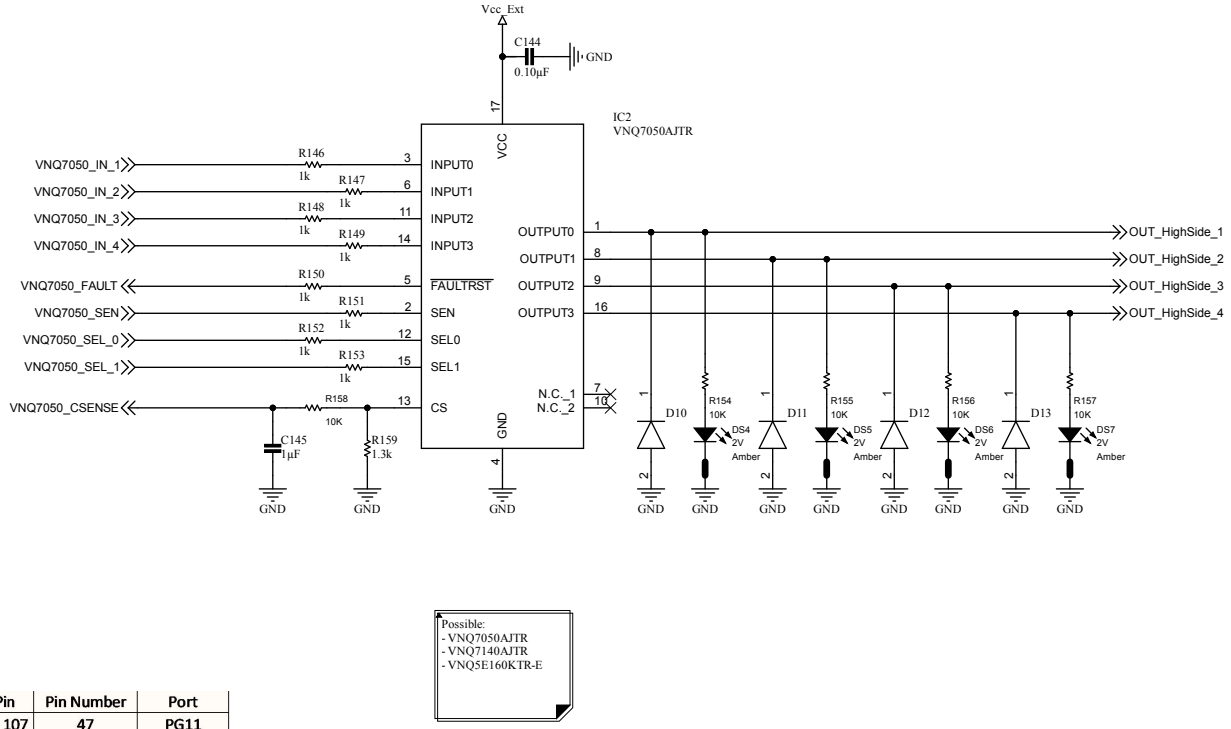


Figure 8. AEK-POW-BMSLV circuit schematic (7 of 11)



Pin Name	uC Pin	Pin Number	Port
VNQ7050_IN_1	GPIO_107	47	PG11
VNQ7050_IN_2	GPIO_108	48	PG12
VNQ7050_IN_3	GPIO_079	49	PE15
VNQ7050_IN_4	GPIO_078	50	PE14
VNQ7050_FAULT	GPIO_020	51	PB4
VNQ7050_SEN	GPIO_077	52	PE13
VNQ7050_SEL_0	GPIO_059	53	PD11
VNQ7050_SEL_1	GPIO_019	54	PB3
VNQ7050_CSENSE	ADC3_65	55	PB2

Figure 9. AEK-POW-BMSLV circuit schematic (8 of 11)

Opamp Temp 1 - 4

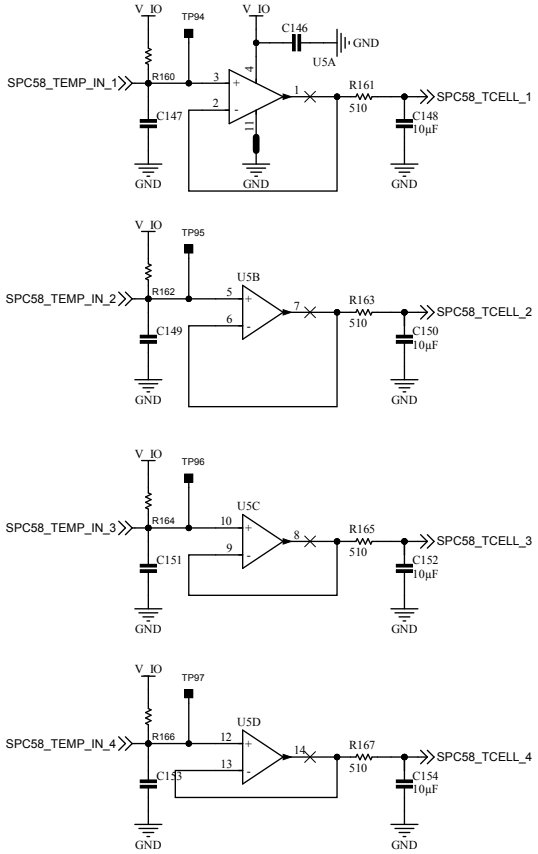


Figure 10. **AEK-POW-BMSLV circuit schematic (9 of 11)**

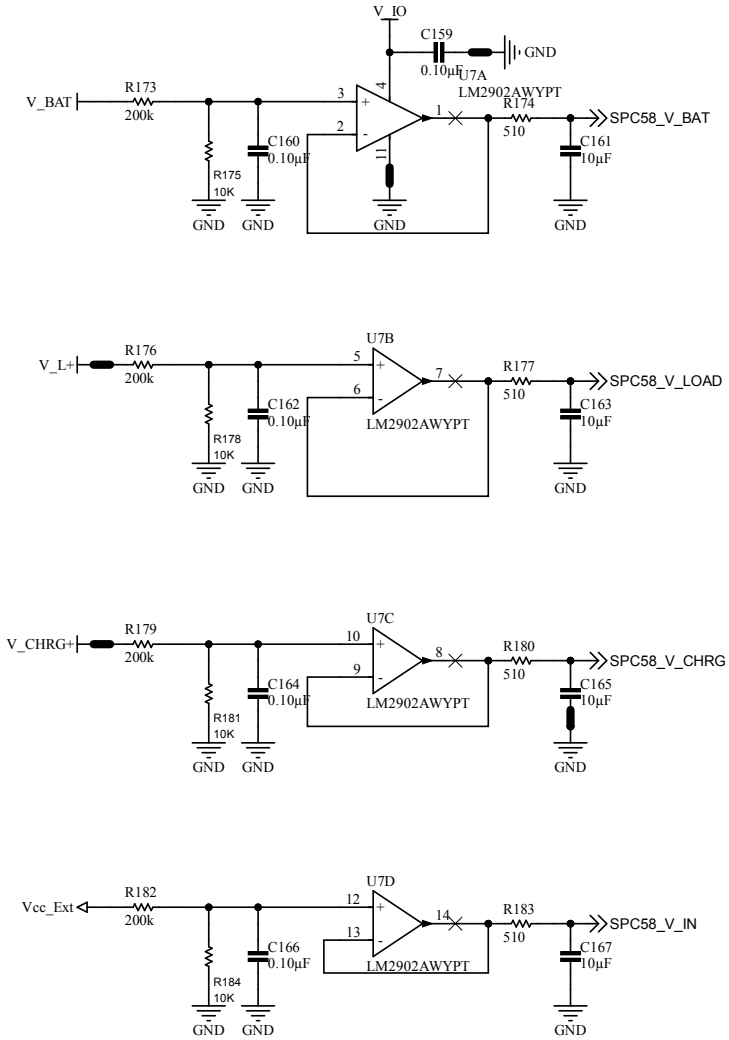
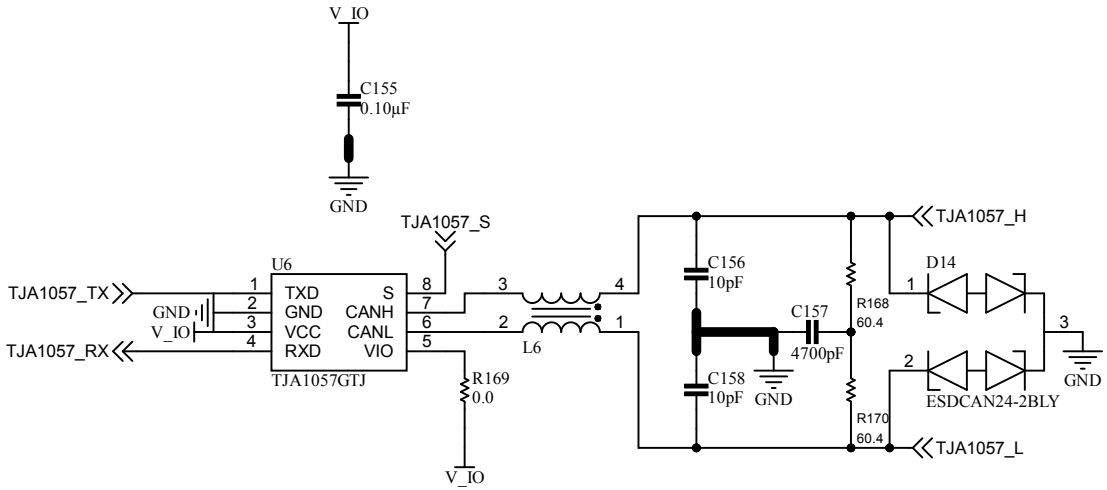
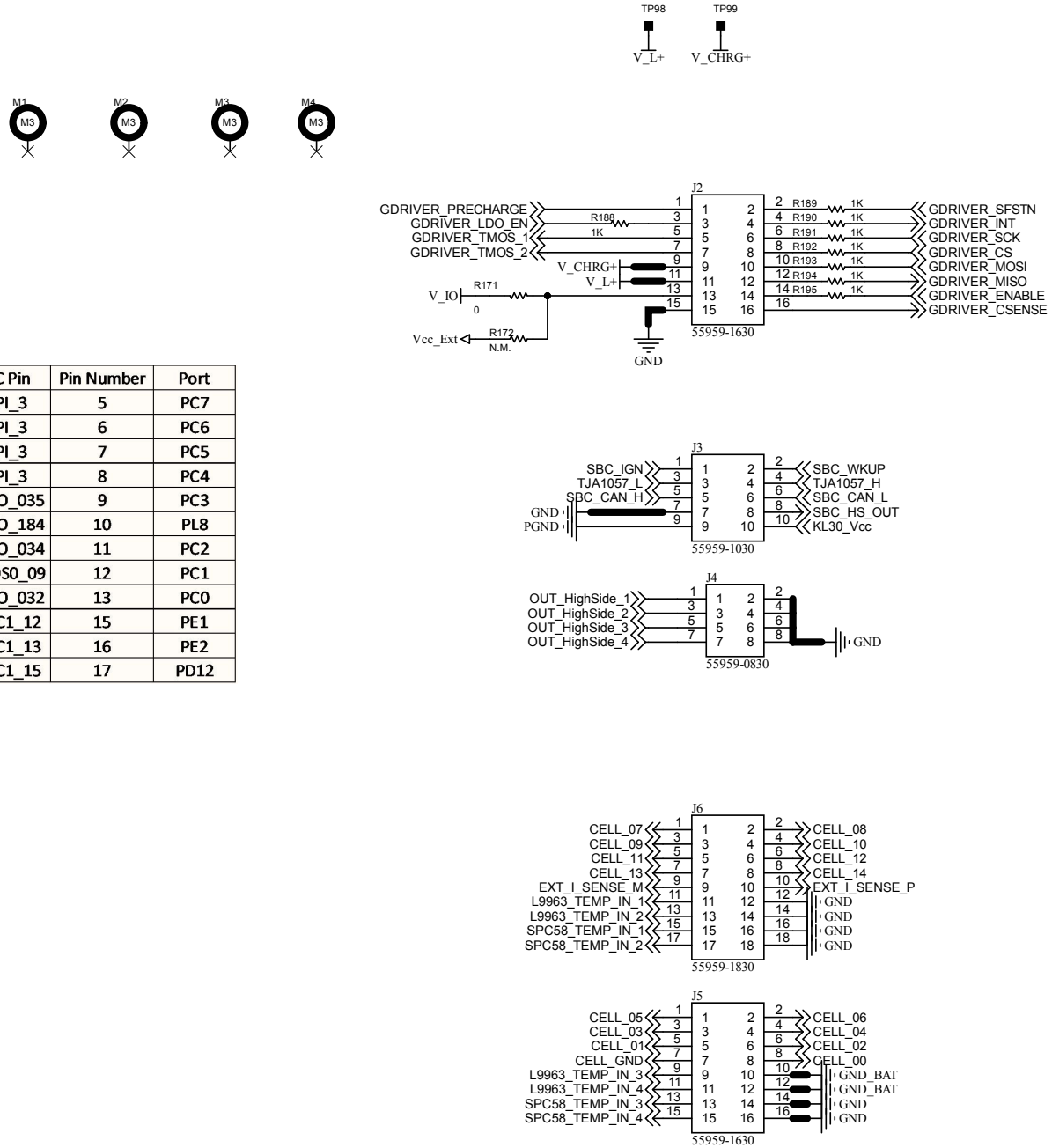


Figure 11. **AEK-POW-BMSLV circuit schematic (10 of 11)**



Name	uC Pin	Pin Number	Port
TJA1057_TX	CAN2_TX	118	PA10
TJA1057_RX	CAN2_RX	119	PA11
TJA1057_S	GPIO_114	120	PH2

Figure 12. AEK-POW-BMSLV circuit schematic (11 of 11)



Pin Name	uC Pin	Pin Number	Port
GDRIVER_CS	SPI_3	5	PC7
GDRIVER_MOSI	SPI_3	6	PC6
GDRIVER_MISO	SPI_3	7	PC5
GDRIVER_SCK	SPI_3	8	PC4
GDRIVER_SFSTN	GPIO_035	9	PC3
GDRIVER_PRECHARGE	GPIO_184	10	PL8
GDRIVER_LDO_EN	GPIO_034	11	PC2
GDRIVER_INT	MIOS0_09	12	PC1
GDRIVER_ENABLE	GPIO_032	13	PC0
GDRIVER_TMOS_1	ADC1_12	15	PE1
GDRIVER_TMOS_2	ADC1_13	16	PE2
GDRIVER_CSENSE	ADC1_15	17	PD12

3 Board versions

Table 1. AEK-POW-BMSLV versions

PCB version	Schematic diagrams	Bill of materials
AEK$POW-BMSLVA (1)	AEK$POW-BMSLVA schematic diagrams	AEK$POW-BMSLVA bill of materials

1. *This code identifies the AEK-POW-BMSLV evaluation board first version. It is printed on the board PCB.*

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
20-Jun-2024	1	Initial release.
09-Jul-2024	2	Updated Section Features, product summary table and Section 2: Schematic diagrams.
16-Oct-2024	3	Updated Figure 2. AEK-POW-BMSLV circuit schematic (1 of 11) and Figure 11. AEK-POW-BMSLV circuit schematic (10 of 11).