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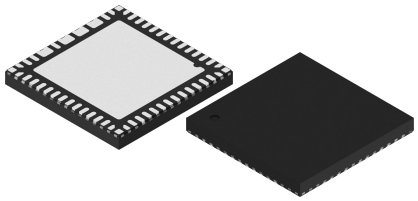
SPSB100

Datasheet

Automotive power management IC for highly integrated processors



VFQFN56 + 4L
8x8x0.9 mm

Product status link
SPSB100

Product summary		
Order code	**Packing**	**Description**
SPSB100BTR	Tape and reel	System supply configuration 1
SPSB100PTR		System supply configuration 2

Features

- AEC-Q100 qualified
- 2 configurable (6.5 V, 5 V, 3.3 V) BUCK converters and typ peak switching current limit of 3.0 A at 2.4 MHz or 400 kHz
- 1 configurable (3.3 V, 1.25 V, 1.2 V, 1.1 V, 0.98 V) BUCK converter and typ peak switching current limit up to 6.0 A at 2.4 MHz, with fine-tuning configurability around 0.98 V (0.95 V to 1.01 V)
- Overcurrent detection and limitation for all BUCKs
- Integrated soft start on BUCK stages
- Boost controller 8-9.5 V and typ peak switching current limit of 4.2 A at 400 kHz, for sustaining low battery condition occurring for a transitory time and deep cranking pulse (external power components can be optionally populated)
- One 5 V voltage regulator (120 mA, 2% acc.)
- One configurable (5 V or 3.3 V) low drop voltage tracker of all regulators (10 mA, ±10 mV)
- One high side driver for contact monitoring (R_{ON} = 55 Ω) with open-load and overcurrent diagnosis
- Dedicated interrupt pin for failure communication
- Device operates in low power mode
- Very low quiescent current in DEEP-SLEEP state
- MCU reset generator
- Configurable window watchdog with extended long open window up to 9 s and enable/disable function through NVM bit
- Device contains temperature warning and protection
- Thermal clusters
- A/D conversion of supply voltages and internal temperature sensors
- STMicroelectronics standard serial peripheral interface (32 Bit/ST_SPI) including 4-bit CRC
- 1 fail-safe output
- 1 input pin supporting static and dynamic error signal reporting
- Programmable periodic system wake-up feature
- Documentation available for customers that need support when dealing with ASIL requirements as per ISO26262
- VFQFN56+4L 8x8x0.9 with wettable flank, 0.8 mm package

Description

The SPSB100 is a fully integrated automotive power management system IC, especially designed for highly integrated application processors (for example, Stellar G and P MCU families), offering low power mode and high current capability: the device comes with enhanced system power supply functionality.

It combines a 3-switch mode power supply together with two integrated linear voltage regulators. The device integrates a further 2 wake-up inputs and advanced fail-safe functionalities.

The boost controller is intended only to sustain cold cranking pulses, start stop and weak battery conditions for a transitory time.

Different combinations enable to supply the system microcontroller, external peripheral loads and sensors in several and adjustable voltage and current ranges. SPSB100 is delivered out of ST factory with default values (rails, power-up and down sequences) stored in USER-NVM space as reported in system supply configuration 1 for SPSB100B and in system supply configuration 2 for SPSB100P, but can be also reprogrammed by customers based on different application needs.

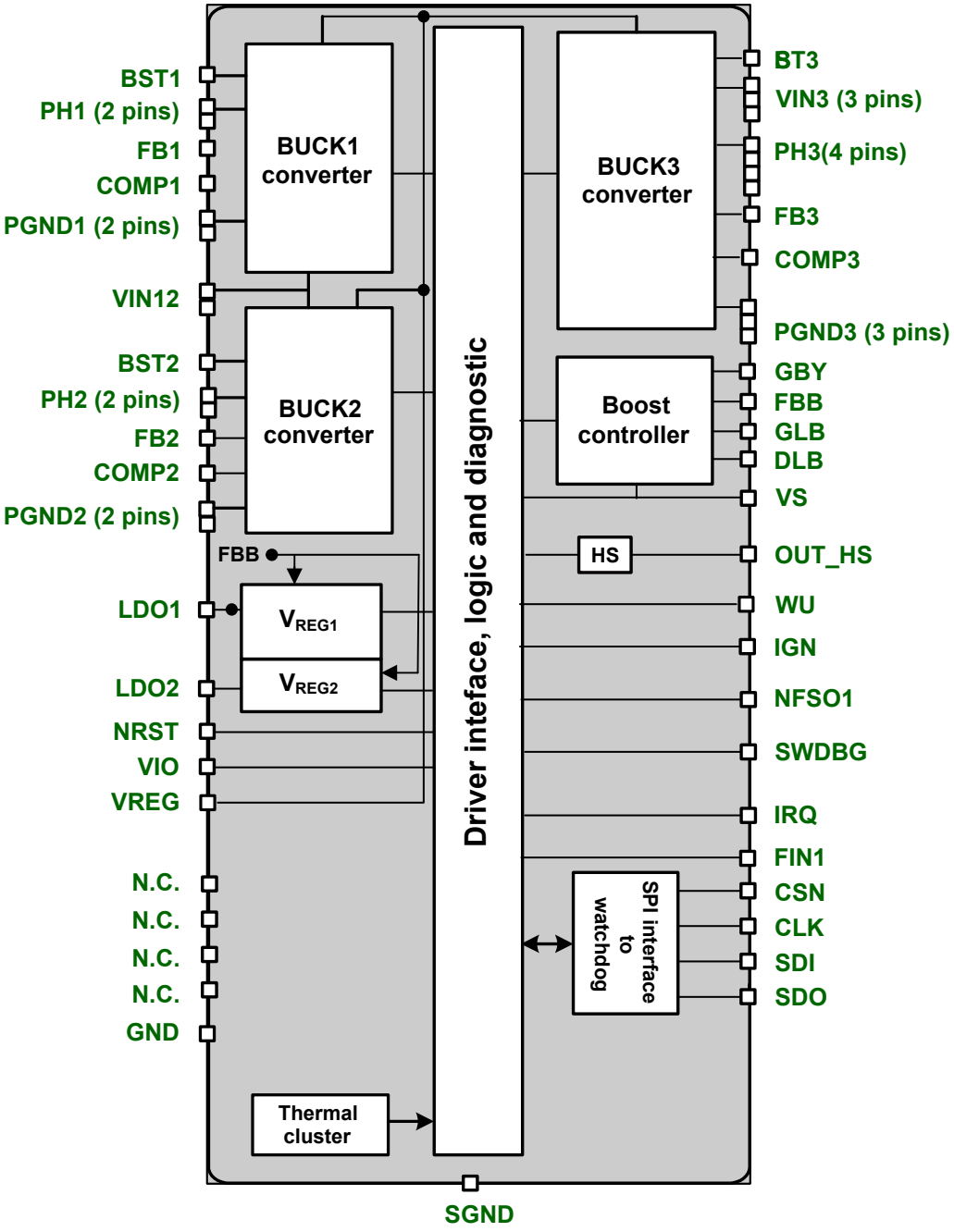
The ST standard SPI interface allows control and diagnosis of the device and enables generic software development.

The device offers a set of features to support applications that need to fulfill functional safety requirements as defined by Automotive Safety Integrity Level (ASIL).

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. **Pin connection (top view)**

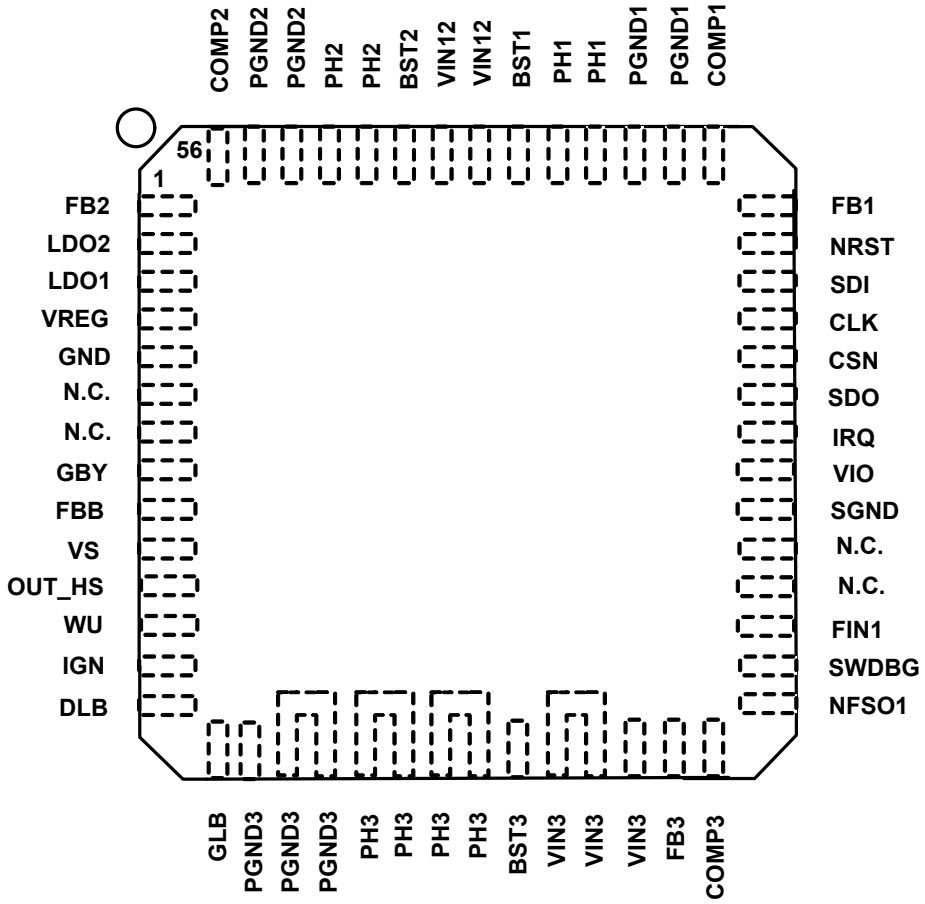


Table 1. **Pin function**

#	Name	Description	I/O type
1	FB2	BUCK2 feedback voltage (to internal voltage monitors)	I
2	LDO2	Voltage regulator 5 V/3.3 V - tracker of BUCKs output (supply for microcontroller)	O
3	LDO1	5 V voltage regulator 1 output	O
4	VREG	3.3 V regulator output for BUCK bootstrap	O
5	GND	DS monitoring ground	-
6	N.C.(1)	Not connected	-
7	N.C.(1)	Not connected	-
8	GBY	Gate driver of external MOS bypass BOOST	O
9	FBB	BOOST feedback pin and supply for LDO1 and LDO2, OUT_HS, VREG, WU and IGN blocks	I
10	VS	Boost input	I
11	OUT_HS	High-side-driver output to supply contacts	O
12	WU	Wake-up input for static or cyclic monitoring of external contact	I
13	IGN	Wake-up input for static or cyclic monitoring of external contact with KL15 feature	I
14	DLB	Drain monitoring of external low-side MOS of BOOST	I

#	Name	Description	I/O type
15	GLB	Gate driver of external low-side MOS of BOOST	O
16	PGND3	BUCK3 power ground	-
17	PGND3, 2nd pin	Current capability (pin description see above)	-
18	PGND3, 3rd pin	Current capability (pin description see above)	-
19	PH3	Switching node BUCK3	I/O
20	PH3, 2nd pin	Current capability (pin description see above)	O
21	PH3, 3rd pin	Current capability (pin description see above)	O
22	PH3, 4th pin	Current capability (pin description see above)	O
23	BST3	Boot-strap capacitor to supply BUCK3 high-side MOS gate-driver circuitry	-
24	VIN3	Input voltage BUCK3	I
25	VIN3, 2nd pin	Current capability (pin description see above)	I
26	VIN3, 3rd pin	Current capability (pin description see above)	I
27	FB3	BUCK3 feedback voltage (to internal voltage monitors)	I
28	COMP3	BUCK3 error amplifier compensation network	-
29	NFSO1	Fail-safe output (active low, open drain)	O
30	SWDBG	Debug input to deactivate the window watchdog (active high) and entering pin for NVM emulation mode	I
31	FIN1	FCCU sequence input	I
32	N.C.(1)	Not connected	-
33	N.C.(1)	Not connected	-
34	SGND	Signal ground (analog and digital reference)	-
35	VIO	I/O power supply (3.3 V or 5 V)	I
36	IRQ	Interrupt (open drain)	O
37	SDO	SPI serial data output	O
38	CSN	SPI chip select not input	I
39	CLK	SPI serial clock input	I
40	SDI	SPI serial data input	I
41	NRST	Reset output to microcontroller, internal pull-up (open drain)	O
42	FB1	BUCK1 feedback voltage (to internal voltage monitors)	I
43	COMP1	BUCK1 error amplifier compensation network	-
44	PGND1	BUCK1 power ground	-
45	PGND1, 2nd pin	Current capability (pin description see above)	-
46	PH1	Switching node BUCK1	I/O
47	PH1, 2nd pin	Current capability (pin description see above)	O
48	BST1	Boot-strap capacitor to supply BUCK1 high-side MOS gate-driver circuitry	-
49	VIN12	Input voltage BUCK1 and BUCK2	I
50	VIN12	Current capability (pin description see above)	I
51	BST2	Boot-strap capacitor to supply BUCK2 high-side MOS gate-driver circuitry	-
52	PH2	Switching node BUCK2	I/O
53	PH2, 2nd pin	Current capability (pin description see above)	O
54	PGND2	BUCK2 power ground	-

#	Name	Description	I/O type
55	PGND2, 2nd pin	Current capability (pin description see above)	-
56	COMP2	BUCK2 error amplifier compensation network	-

1. *It is suggested to connect the N.C. pins to ground.*

2 Maximum ratings

2.1 Operating range

Within the operating range the part operates as specified and without parameter deviations. The device may not operate properly if maximum operating conditions are exceeded.

Once taken beyond the operative ratings and returned back within, the part recovers with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

All voltages are related to the potential at substrate ground pin.

Table 2. Operating conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_S	Global	Supply voltage	3(1)	-	29	V
F_{BB}	Boost output		7.7	-	29	V
VIN_{12}	BUCK1 and BUCK2 supply pin		7.7	-	29	V
VIN_3	BUCK3 supply pin		3	-	7	V
VIO	Digital interface supply pin		3	-	5.5	V

1. *V_S operating range from 3 V up to V_{fbb_regx} is intended as a transitory time during cranking conditions.*

2.1.1 Supply voltage ranges

All SPI communication, logic and oscillator parameters work down to $V_S = V_{PORVS\_F}$ and are specified accordingly:

- SPI thresholds
- Oscillator frequency (delay times correctly elapsed)
- Internal register status correctly kept (reset at default values for $V_S < V_{PORVS\_F}$)
- Reset threshold correctly detected

2.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

All voltages are related to the potential at substrate ground pin.

Table 3. Absolute maximum ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{S_JS}	DC supply voltage	Jump start	-0.3	-	29	V
V_{S_LD}	DC supply voltage	Load dump 400 ms max	-0.3	-	40	V
V_{S_rev}	DC supply voltage for reverse battery	Reverse battery with limited current at max 30 mA	-1.0	-	-	V
V_{FBB_JS}	Boost output voltage range Supply for LDO1 and 2, OUT_HS, IGN and WU blocks	Jump start	-0.3	-	29	V
V_{FBB_LD}	Boost output voltage range Supply for LDO1 and 2, OUT_HS, IGN and WU blocks	Load dump 400 ms max	-0.3	-	40	V
V_{GLB}	Boost gate driver voltage range	$V_{GLB} < V_{FBB}$ + 0.3 V	-0.3	-	13.4	V
V_{DLB}	Boost external drain voltage range		-0.3	-	40	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{GBY}	Bypass gate driver voltage range	$V_{GBY} < V_{FBB} + 0.3$ V	-0.3	-	40	V
V_{REG}	3.3 V regulator output for bucks bootstrap		-0.3	-	4.6	V
V_{IN12_JS}	BUCK1 and 2 input voltage range	Jump start $V_{IN12} < V_{FBB} + 0.3$ V	-0.3	-	29	V
V_{IN12_LD}	BUCK1 and 2 input voltage range	$V_{IN12} < V_{FBB} + 0.3$ V Load dump 400 ms max	-0.3	-	40	V
V_{FB1}	BUCK1 input voltage range	$V_{FB1} < V_{FBB} + 0.3$ V	-0.3	-	20	V
V_{FB2}	BUCK2 input voltage range	$V_{FB2} < V_{FBB} + 0.3$ V	-0.3	-	20	V
V_{PH1}(1)	BUCK1 input voltage range		-0.3	-	40	V
V_{PH2}(1)	BUCK2 input voltage range		-0.3	-	40	V
V_{BST1}	BUCK1 input voltage range		-0.3	-	40	V
V_{BST2}	BUCK2 input voltage range		-0.3	-	40	V
V_{COMP1}	BUCK1 input voltage range		-0.3	-	4.6	V
V_{COMP2}	BUCK2 input voltage range		-0.3	-	4.6	V
V_{IN3}	BUCK3 input voltage range		-0.3	-	20	V
V_{FB3}	Buck3 feedback voltage range		-0.3	-	20	V
V_{PH3}(1)	Buck3 feedback voltage range		-0.3	-	20	V
V_{BST3}	Buck3 feedback voltage range		-0.3	-	20	V
V_{COMP3}	Buck3 feedback voltage range		-0.3	-	4.6	V
V_{LDO1}	Stabilized supply voltage 1	$V_{LDO1} < V_{FBB}$	-0.3	-	6.5	V
V_{LDO2}	Stabilized supply voltage 2	$V_{LDO2} < V_{FBB}$	-0.3	-	20	V
V_{IO}	I/O supply voltage		-0.3	-	20	V
VS_{DI}	Logic input		-0.3	-	20	V
V_{CLK}	Logic input		-0.3	-	20	V
V_{CSN}	Logic input		-0.3	-	20	V
VS_{DO}	Logic output		-0.3	-	20	V
V_{NRST}	Open drain output (with internal pull up)		-0.3	-	20	V
V_{IRQ}	Open drain output (with internal pull up)		-0.3	-	20	V
V_{SWDBG}	Debug input pin voltage range		-0.3	-	20	V
V_{FIN1}	FIN1 input voltage range		-0.3	-	20	V
V_{NFSO1}	Open drain output (without internal pull up)		-0.3	-	40	V
V_{WU_JS}	DC wake-up input voltage	Jump start	-0.3	-	29	V
V_{IGN_JS}	DC wake-up input voltage	Jump start	-0.3	-	29	V
V_{WU_LD}	DC wake-up input voltage	Load dump 400 ms max	-0.3	-	40	V
V_{IGN_LD}	DC wake-up input voltage	Load dump 400 ms max	-0.3	-	40	V
I_{Input}(2)	Current injection into FBB related input pins WU, IGN		-20	-	20	mA
I_{out_inj}(2)	Current injection into FBB related outputs OUT_HS		-20	-	20	mA
V_{OUT_HS}	Output voltage		-0.3	-	40	V
I_{OUT_HS}	Current injection OUT_HS(2)		-20	-	20	mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{SGND}	Maximum current at SGND(3)		-1.25	-	1.25	A
I_{VIN12}	Maximum current at V_{IN12}(3) (x 2)		-5	-	5	A
I_{PGND1}, I_{PGND2}	Maximum current at PGND1 and 2(3) (x 2)		-5	-	5	A
I_{PH1}, I_{PH2}	Maximum current at PH1 and 2(3) (x 2)		-5	-	5	A
I_{VIN3}	Maximum current at V_{IN3}(3) (x 3)		-5	-	5	A
I_{PGND3}	Maximum current at PGND3(3) (x 3)		-5	-	5	A
I_{PH3}	Maximum current at PH3(3) (x 4)		-5	-	5	A
V_{PGND}	PGND versus GND		-0.3	-	0.3	V
V_{GND}	SGND versus GND		-0.3	-	0.3	V

1. *Transients on this pin can be tolerated for a duration < 100 ns, not exceeding -3 V.*
2. *Guaranteed by design.*
3. *Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits. Guaranteed by design.*

2.3 ESD robustness

Table 4. ESD protection

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Pins	All pins	HBM(1)	-2	-	2	kV
Power output pin	OUT_HS	HBM(2)	-4	-	4	kV
Pins(3)	All pins	CDM (values for corner pins in brackets)	-500/(-750)	-	500/(750)	V

1. *HBM (human body model, 100 pF, 1.5 kΩ) according to the AEC-Q100-0022.*
2. *HBM with all none zapped pins grounded.*
3. *CDM (charged device model) according to the AEC-Q100-011.*

2.4 Temperature ranges and thermal data

Table 5. Temperature ranges and thermal data

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{amb}	Operating temperature (ECU environment)		-40	-	125	°C
T_j	Operating junction temperature		-40	-	175	°C
T_{stg}	Storage temperature		-55	-	150	°C
T_W (1)	Thermal over temperature warning threshold		140	-	160	°C
T_{SD} (1)	Thermal shut-down junction temperature		165	-	185	°C
T_{SDC}	Central thermal shut-down junction temperature		175	-	195	°C
T_{SDhys}	Thermal shut-down temperature hysteresis		0	5	10	°C
T_{F_TJ}	Thermal warning/shutdown filter time	Covered by scan	60	75	90	µs
T_{F_TSDC}	Central thermal shutdown filter time	Covered by scan	25.6	32	38.4	µs
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient	4 layers board		19		°C/W

1. *Non-overlapping.*

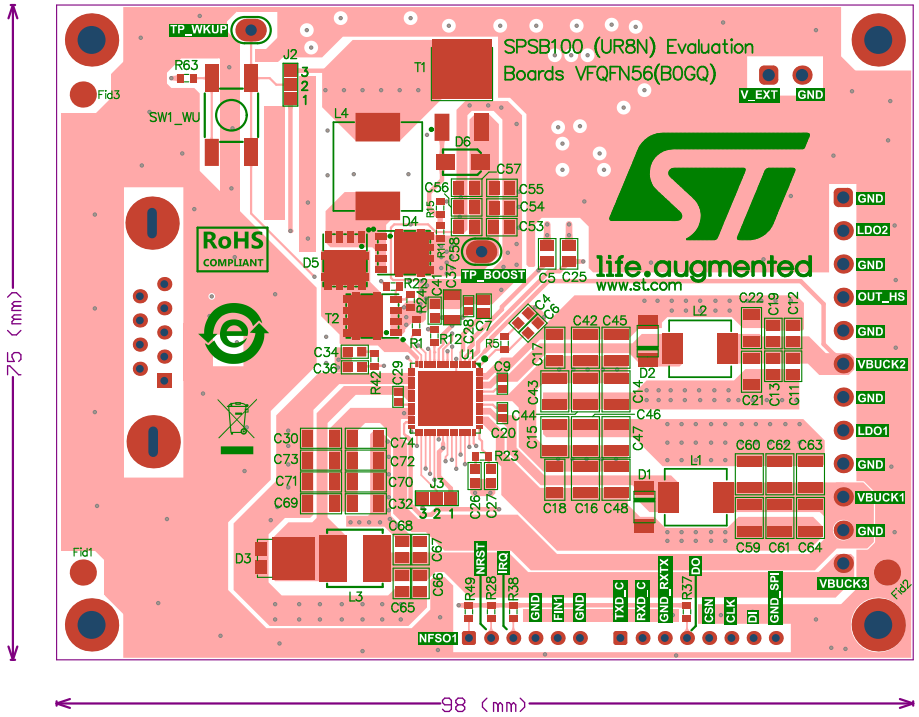
All the parameters are guaranteed in the temperature range -40 to 150 °C (unless otherwise specified); the device is still operative and functional up to 185 °C.

The parameters limits at higher temperatures than 150 °C may change with respect to what is specified as per the standard temperature range.

The device functionality over 150 °C is guaranteed by characterization.

The SPSB100 embeds a multitude of junctions housed in a relatively small piece of silicon. The devices contain, among all the described features, two voltage regulators (one of which can work as a voltage tracker) and three BUCK converters with internal power stages and one high side driver. For this reason, using the thermal impedance of a single junction (that is, voltage regulator or major power dissipation contributor) does not allow to predict thermal behavior of the whole device and therefore it is not possible to assess if a device is thermally suitable for a given activation profile and loads characteristics. Thermal information is provided as temperature reading by different clusters placed close to the most dissipative junctions. Some representative and realistic case thermal profiles are described below in a 4 layers board.

Figure 3. VFQFN56+4L printed circuit board 4 layers - Top layer



The following describes 2 typical application scenarios related to system configuration 1 and differentiated based on the BUCK1, 2 selected frequencies:

V_{bat} = 16 V, R_{thja} = 19 °C/W, T_{jmax} = 170 °C

Case A

- LDO1 (5 V): charged with 100 mA (DC activation)
- LDO2 (5 V): charged with 5 mA (DC activation)
- OUT_HS: Iload = 20 mA (DC activation)
- BUCK1 (3.3 V): charged with 1 A (DC activation) at 400 kHz
- BUCK2 (5.0 V): charged with 1 A (DC activation) at 400 kHz
- BUCK3 (0.98 V): charged with 2 A (DC activation) at 2.4 MHz

Case B

- LDO1 (5 V): charged with 100 mA (DC activation)
- LDO2 (5 V): charged with 5 mA (DC activation)
- OUT_HS: Iload = 20 mA (DC activation)
- BUCK1 (3.3 V): charged with 1 A (DC activation) at 2.4 MHz

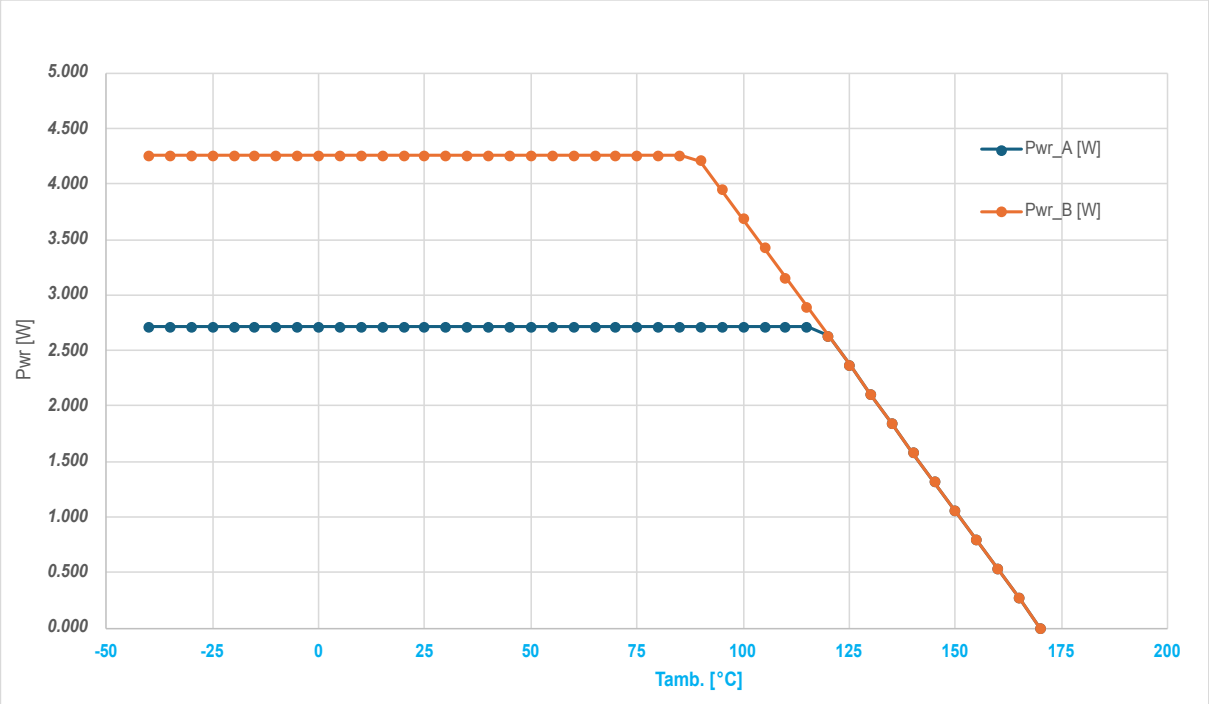
- BUCK2 (5.0 V): charged with 1 A (DC activation) at 2.4 MHz
- BUCK3 (0.98 V): charged with 2 A (DC activation) at 2.4 MHz

Note:

1. *BUCK3 load current is already considered in the power dissipation calculation, so 1 A is referred to BUCK1 external loads current.*
2. *Selecting the switching frequency at 2.4 MHz for BUCK1 and BUCK2 will lower the regulators efficiency and this extra power to be dissipated can generate a faster thermal shut-down. In case the application requires a high DC current load, it is strongly suggested using the switching frequency at 400 kHz for BUCK1 and BUCK2.*

The following curves show the relationship between max power dissipation vs ambient temperature:

Figure 4. Max power dissipation vs ambient temperature for case "A" and case "B"



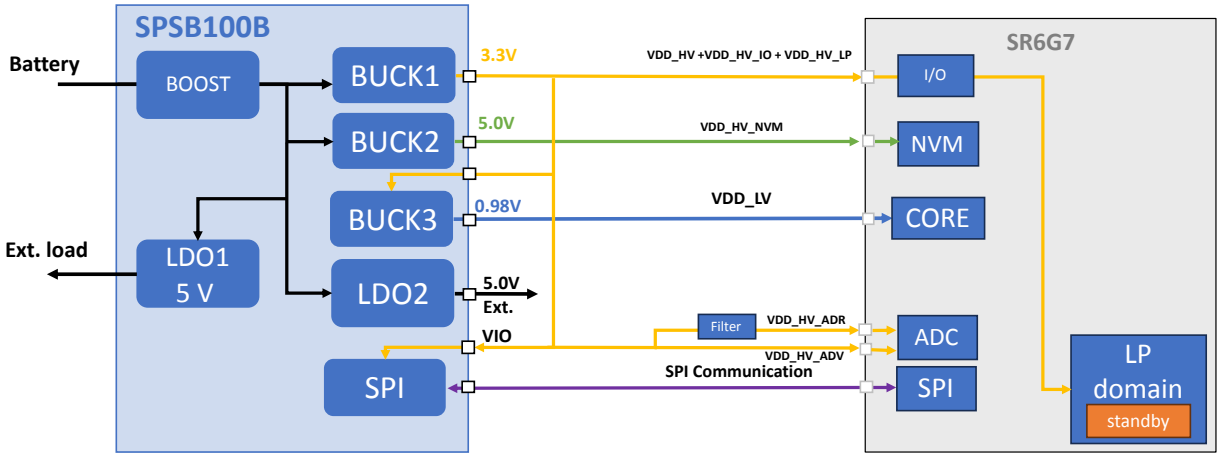
3 Functional description

3.1 Supply configurations

The battery supplies the boost controller. FBB, the boost output, supplies internal regulated voltages of analog and digital blocks, the wake-up blocks, OUT_HS output and fail-safe block. BUCK1, BUCK2 and BUCK3 have independent supply pins to allow different supply configurations according to the applications. Here we describe the two main configurations where it is required to provide direct or indirect supply to the microcontroller core.

3.1.1 System supply configuration 1

Figure 5. Configuration 1: direct supply of the microcontroller core



In this configuration BUCK3 is supplied by BUCK1 and is configured to provide a 0.98 V high current supply to the micro core. BUCK1 and BUCK2 are supplied by the boost and supply respectively the 3.3 V and the 5 V rails with a switching frequency of 400 kHz. Boost supplies always LDO1 and LDO2, both providing 5 V for external loads.

The power-up and power-down sequence associated to such supply configuration are the following:

Power-up sequence

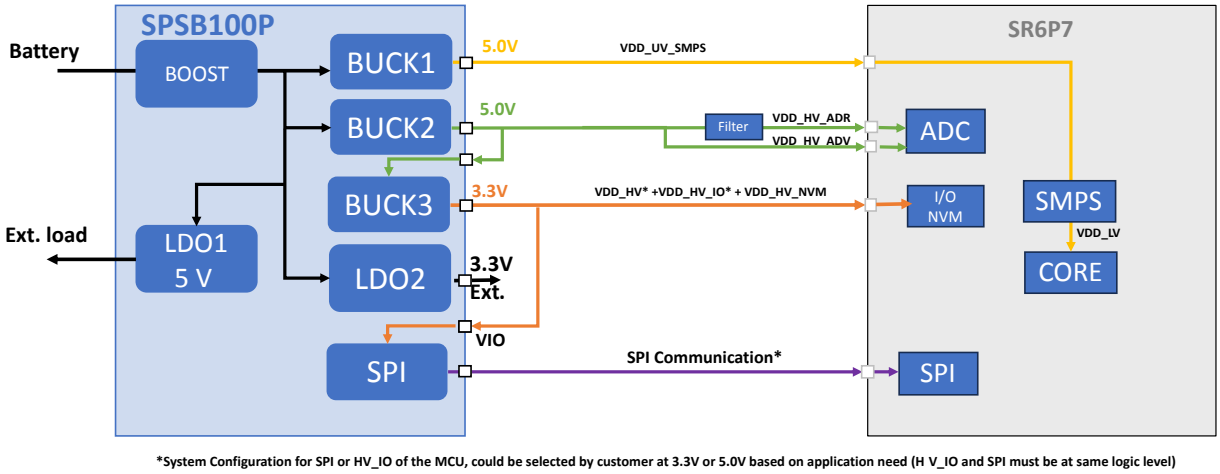
1. Turn ON BUCK1 at 3.3 V, wait PG (BUCK1_PG_OK flag);
2. Turn ON BUCK3 at 0.98 V, wait PG (BUCK3_PG_OK flag);
3. Turn ON BUCK2 at 5 V, wait PG (BUCK2_PG_OK flag);
4. Turn ON LDO2 in tracker of buck 2, wait PG (LDO2_PG_OK flag);
5. Turn ON LDO1, wait PG (LDO1_PG_OK flag).
6. Deassert NRST, wait 0 ms

Power-down sequence

1. Assert NRST, wait 2 ms;
2. Turn OFF LDO2 and LDO1, wait 2 ms;
3. Turn OFF BUCK3, wait 2 ms;
4. Turn OFF BUCK1 and BUCK2, wait 2 ms;
5. Turn OFF V_{REG} after 10 ms.

3.1.2 System supply configuration 2

Figure 6. Configuration 2: direct supply of the microcontroller core by internal SMPS



*System Configuration for SPI or HV_IO of the MCU, could be selected by customer at 3.3V or 5.0V based on application need (H V_IO and SPI must be at same logic level)

In configuration 2, BUCK1 is configured to provide a 5 V to supply the SMPS of microcontroller that will manage internally the supply of the core with a switching frequency of 400 kHz. BUCK2 and BUCK3 supply respectively the 5 V and the 3.3 V rails with a switching frequency of 400 kHz and 2.4 MHz respectively. BUCK3 is supplied by BUCK2, while the boost supplies BUCK1 and 2 and LDO1 and LDO2, providing 5 V and 3.3 V respectively for external loads.

The power-up and power-down sequences associated to such supply configuration are the following:

Power-up sequence

1. Turn ON BUCK1 at 5 V, wait PG (BUCK1_PG_OK flag);
2. Turn ON BUCK2 at 5 V, wait PG (BUCK2_PG_OK flag);
3. Turn ON BUCK3 at 3.3 V, wait PG;
4. Deassert NRST, wait 0 ms;
5. Turn ON LDO2 in tracker of BUCK3, wait 0 ms;
6. Turn ON LDO1, wait PG (LDO1_PG_OK flag).

Power-down sequence

1. Turn OFF LDO1, wait 0 ms;
2. Turn OFF LDO2, wait 0 ms;
3. Assert NRST, wait 2 ms;
4. Turn OFF BUCK3, wait 2 ms;
5. Turn OFF BUCK2, wait 2 ms;
6. Turn OFF BUCK1, wait 0 ms;
7. Turn OFF V_{REG} after 10 ms.

Note: The SR6P7 does not embed LP domain, anyway when the SPI is supplied by BUCK3 at 3.3 V it is not possible to use SPSB100P in low power mode otherwise SPI will be not supplied and it cannot be possible to communicate with MCU. The only way to use SPSB100P in low power mode is when both SPI and VDD_HV_IO are supplied by 5 V through BUCK1 set at 5 V and only in this case, it could be possible to use SPSB100P in low power mode allowing SPI communication.

3.1.3 Digital interface supply: VIO

VIO pin supplies the SPI interface, and pins IRQ, FIN1, NRST, RxD_C, TxD_C.

VIO can be supplied from one of SPSB100's BUCK, or from an external regulator.

Digital pins functionalities are guaranteed when VIO > $V_{VIO\_UV\_R}$ (VIO_UV flag not raised).

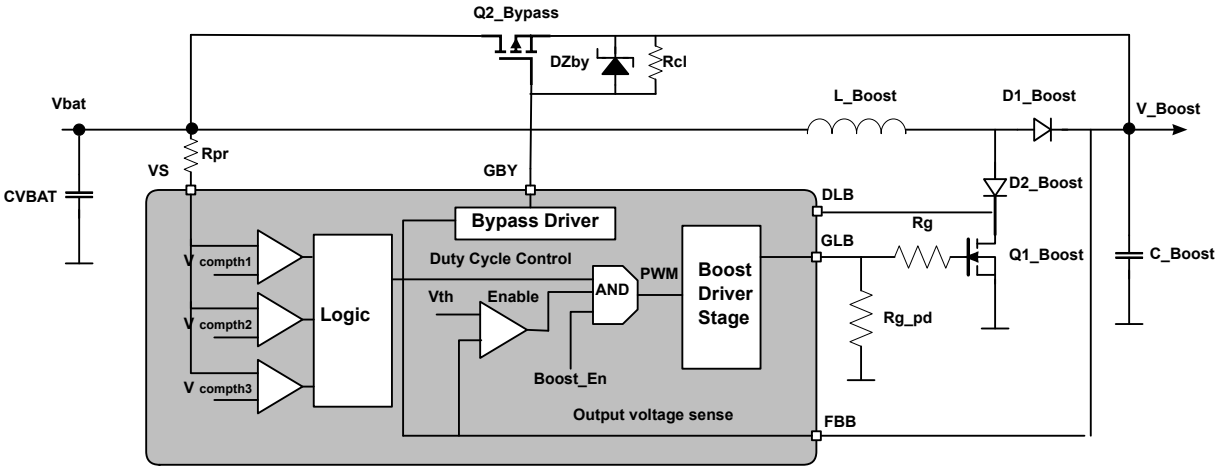
3.2 Boost controller

The boost, or step up controller, generates an output voltage that supplies the SPSB100 device and the BUCK converters, only during a transitory time at power up to reach a normal operating range (12 V battery range), or only during low battery conditions for a transitory time, or for sustaining deep cranking.

In case the V_S voltage exceeds the V_{TH_BYPASS} threshold, the converter is deactivated and battery supplies, via separate bypass MOSFET, the BUCK converters. The live bit BOOST_ENA_STATUS reflects the state of the boost.

The block diagram of the boost is shown in the figure below.

Figure 7. Boost controller block diagram



According to the sensed battery voltage on VS pin (V_{S_LOW}, V_{S_MID} and V_{S_HIGH} thresholds), the boost duty cycle is suitably adjusted (BOOST_DC_Max when V_S voltage is between V_{S_POR} and V_{S_LOW}, BOOST_DC_High when V_S is between V_{S_LOW} and V_{S_MID}, BOOST_DC_Mid when V_S is between V_{S_MID} and V_{S_HIGH} and BOOST_DC_Low when V_S is higher than V_{S_HIGH}) to keep the output voltage quite over the selected thresholds (V_{FBB_REG1} or V_{FBB_REG2}, automatically set by state machine and readable by status register bit BOOST_LEVEL_SET).

The system is compliant to the new defined “cold cranking pulse” required by start-stop systems. Moreover, a suitable bypass MOSFET is driven when the BOOST is not switching to bypass the inductor, minimizing the overall losses during normal operation.

The boost and the bypass drivers can be switched permanently OFF by setting respectively BOOST_DIS = 1 and BYPASS_DIS = 1 in the USER-NVM space.

If the BOOST function is used (BOOST_DIS = 0):

- At power-up, the bypass control is enabled when the state machine enters in INIT state (after successful safety checks). If $V_S > V_{TH\_BYPASS\_R}$, the external bypass switch is turned on (BYPASS_STATUS = 1) while the boost pwm is forced low. When $V_S < V_{TH\_BYPASS\_F}$, the external switch is turned off (BYPASS_STATUS = 0) and the boost switching is activated.
- In ACTIVE–FULL-POWER mode and in RECOVERY-1 state, when $V_S > V_{TH\_BYPASS\_R}$, the external bypass switch is turned on after $t_{F\_BYPASS\_EN}$ timing (BYPASS_STATUS = 1) and the boost pwm is forced low if FBB > FBB_REG1 (or FBB_REG2) threshold. When $V_S < V_{TH\_BYPASS\_F}$, the bypass switch is turned off after $t_{F\_BYPASS\_DIS}$ timing (BYPASS_STATUS = 0) and the boost switching is activated if FBB < FBB_REG1 (or FBB_REG2) threshold.
- In ACTIVE–LOW-POWER mode, the BYPASS controller is disabled, turning off the external switch (BYPASS_STATUS = 0): the consumption on the battery is limited to a few mAmps so no dissipation issue is expected in the external diode.
- In ACTIVE–LOW-POWER mode, the BOOST IP is disabled to reduce the overall SPSB100 consumption. It is woken up when the monitored VFBB becomes close to the minimum operating supply (FBB_OK_LP_F1 or FBB_OK_LP_F2) for the remaining active BUCK with duty cycle BOOST_DC_LP.
- In RECOVERY-2 or DEEP-SLEEP state, the boost is always OFF and the BYPASS controller is always disabled (BYPASS_STATUS = 0).

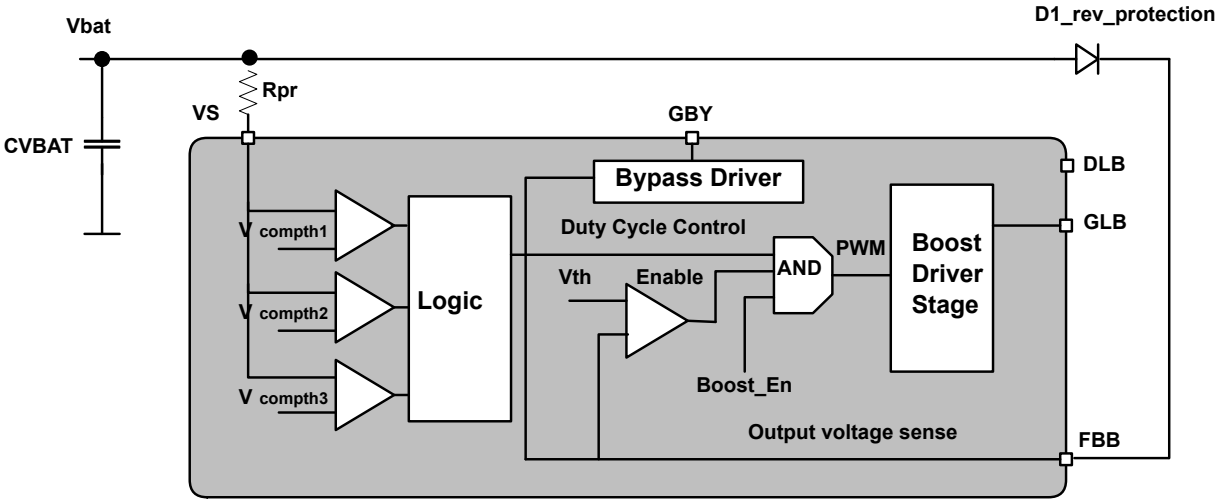
If the BOOST function is not used (USER-NVM BOOST_DIS = '1' or SPI bit BOOST_OFF = 1):

- At power-up, the bypass control is enabled, turning on the external switch (BYPASS_STATUS = 1), as soon as the state machine reaches the INIT state and following successful safety checks.
- In ACTIVE–FULL-POWER mode and in RECOVERY-1 state, the BYPASS switch is turned on whatever the V_S voltage (BYPASS_STATUS = 1).
- In ACTIVE–LOW-POWER mode, DEEP-SLEEP or RECOVERY-2 state, the BYPASS controller is disabled, turning off the external switch (BYPASS_STATUS = 0).

The block diagram of the device when boost is not used is shown in the figure Figure 8.

Note: The D1_rev_protection diode is needed only if there is not a reverse battery protection solution already implemented in the application.

Figure 8. Boost controller disabled block diagram



3.2.1 Power-up/down and voltage drop behavior

The boost role is crucial for SPSB100 operation, so its behavior related to normal or accidental variation of voltage supply should be clearly defined. General behavior is described in the following figures.

Figure 9. Battery plug/unplug behavior

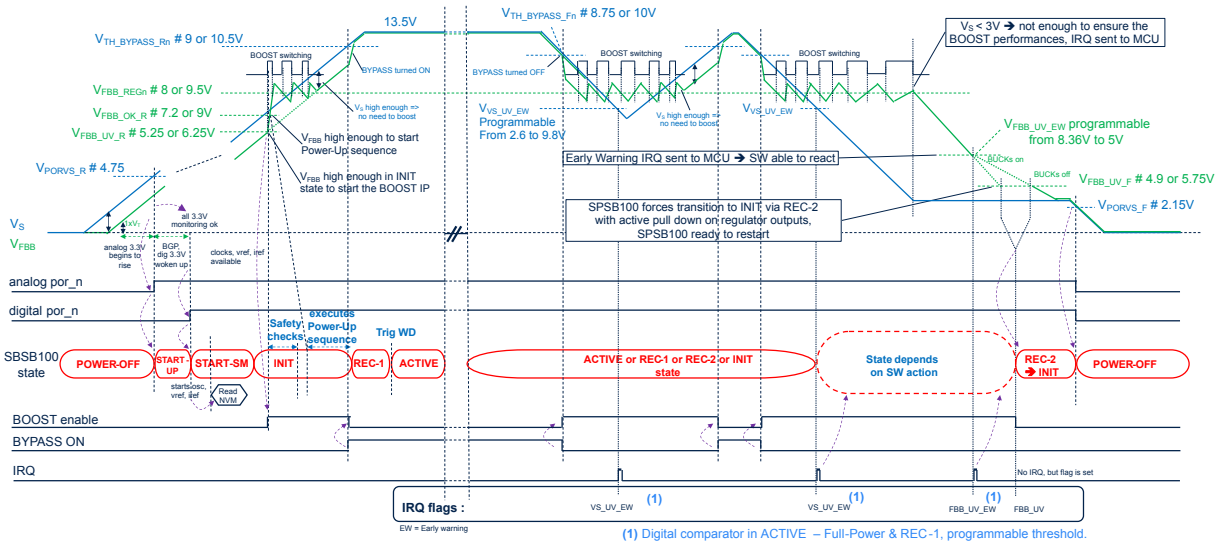
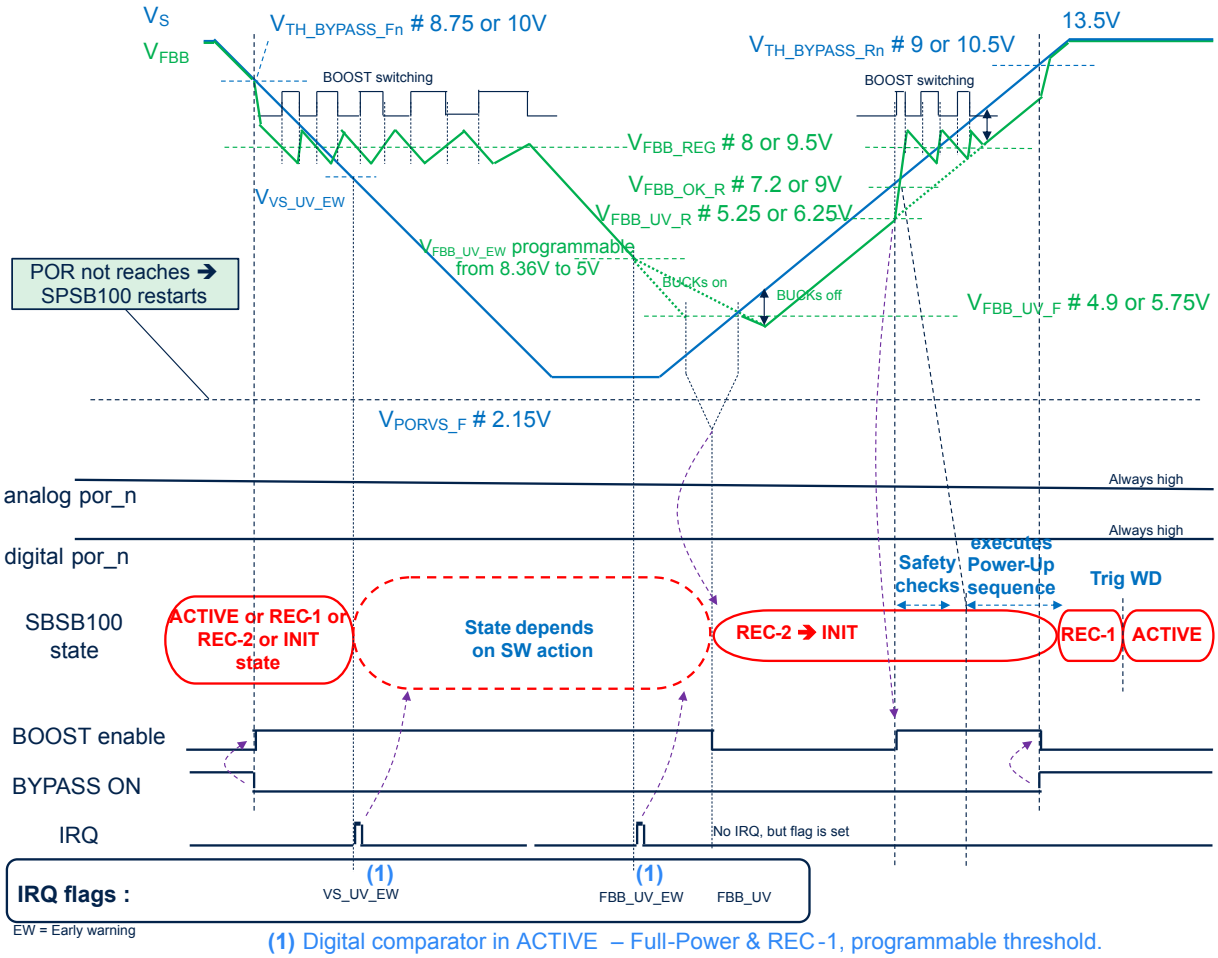


Figure 10. Battery drop behavior

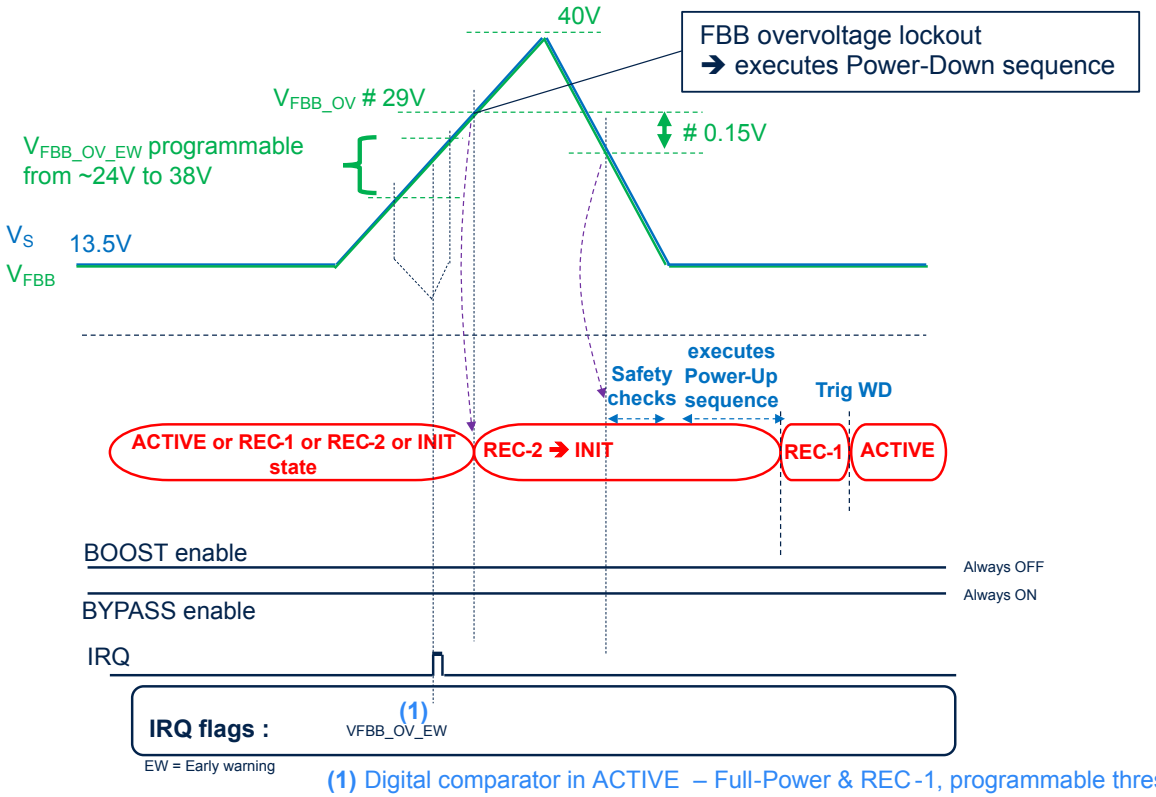


(1) Digital comparator in ACTIVE – Full-Power & REC-1, programmable threshold.

Overvoltage cases are not critical for the boost itself (the bypass is ON) but for the regulators (BUCKs, LDOs…) that are directly supplied. These are managed according to configured thresholds (through V_{FBB_OV} threshold) which trigger in any case a power down sequence. Power up is initiated as long as the voltage decreases below the overvoltage FBB_OV_F.

Undervoltage cases are critical for the regulators (BUCKs, LDOs…) that are directly supplied. These are managed according to configured thresholds (through $V_{FBB\_UV\_F}$ threshold) which trigger in any case a power down sequence. Power-up is initiated as long as the voltage increase above the undervoltage related threshold $V_{FBB\_UV\_R}$.

Figure 11. **Behavior on battery over voltage**



(1) Digital comparator in ACTIVE – Full-Power & REC-1, programmable threshold.

3.3 BUCK converters

3.3.1 BUCK1 converter

The BUCK1 regulator is a synchronous converter compatible to battery level, with integrated power mos. Stability compensation network is external.

Output voltages are programmable via USER-NVM through the bit BUCK1_PU_VALUE.

The switching frequency can be selected either at 400 kHz or 2.4 MHz, by USER-NVM BUCK1_FREQ. To limit emission in audio bandwidth, refresh frequency can be forced at 25 kHz by USER-NVM bit BUCK1_REFRESH_FREQ set low (1 kHz when high). The draw back will be an extra consumption in low power mode.

The spread spectrum feature is configurable by SPI bit BUCK1_SPREAD_ENA (disabled by default).

BUCK1 integrates a low power mode (automatically set by LOW_POWER_SET by SPI) that optimizes its efficiency in active low power mode. (BUCK1 is a mandatory regulator in active low power mode).

BUCK1 can be disabled by the SPI bit VBUCK1_ENA (only after SPI_PROTECT_ACCESS has been set). In active low power mode, the action of enable BUCK1 is not allowed.

The live bit VBUCK1_ENA_STATUS reflects the state of BUCK1 output.

Note: After first power up is needed to align the live bit associated in DSR18 (VBUCK1_ENA_STATUS) with the current value associated in DCR1.

In active full power, the BUCK1 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK1_UV). BUCK1 is therefore switched off after timing tbuck1_UV_TO except if SPI bit MASK_BUCK1_UV_POWER_OFF is set.
- Undervoltage detection generates an IRQ except if MASK_BUCK1_IRQ is set.
- OV detection to monitor the output voltage (flag is BUCK1_OV bit) BUCK1 is therefore switched off after timing tbuck1_OV_TO. Status register bit BUCK1_OV must be read and cleared before switching ON the regulator by SPI bit VBUCK1_ENA to allow a proper start-up (only when BUCK1 is not critical for MCU).
- Overvoltage detection generates an IRQ except if MASK_BUCK1_IRQ is set.

- Power-good used to signal BUCK power on success (flag is BUCK1_PG_OK bit and IRQ is generated except if MASK_BUCK1_PG_IRQ is set):
  - If not, after $T_{BUCK1\_PG\_TO}$ timing, BUCK1 is switched off and flag BUCK1_PG_TIMEOUT is set.
- Not successful power-good detection generates an IRQ except if MASK_BUCK1_PG_TIMEOUT_IRQ is set.
- Configurable over current protection through U-NVM BUCK1_IPEAK (flag is BUCK1_OC bit). BUCK1 is therefore switched off after timing tbuck1_OC_TO except if MASK_BUCK1_OC_POWER_OFF is set.
- Overcurrent detection generates an IRQ except if MASK_BUCK1_OC_IRQ is set.
- Warning temperature detection by a local thermal sensor (flag is TW_CL1).
- Warning temperature detection generates an IRQ except if MASK_CL1_TW_IRQ is set.
- Overtemperature detection by a local thermal sensor (flag is TSD_CL1, see also the Section 4.7: Temperature monitoring) and buck1 is switched off.
- BUCK1 internal regulators detection flag is BUCK1_INT_FAIL and the BUCK1 is switched off.
- Internal fail generates an IRQ except if MASK_BUCK1_IRQ is set
- After a fault detection (UV, OV,OC, FBLOSS, TSD_CL1 or PG timeout), BUCK1 can be re enabled by setting BUCK1_ENA = 0 followed by BUCK1_ENA = 1.
- BUCK1 feedback (FB1) pin disconnection, flag is BUCK1_FBLOSS and the BUCK1 is switched off.
- FB1 pin disconnection generates an IRQ except if MASK_BUCK1_IRQ is set.
- Overtemperature detection by a central thermal sensor (flag is TSD_CL0, see also the Section 4.7: Temperature monitoring) and device is executed power down sequence.

In active low power, BUCK1 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK1_UV). BUCK1 is therefore switched off except if SPI bit MASK_BUCK1_UV_POWER_OFF is set.
- Undervoltage detection generates an IRQ except if MASK_BUCK1_IRQ is set.
- OV detection to monitor the output voltage (flag is BUCK1_OV bit) BUCK1 is therefore switched off.
- Overvoltage detection generates an IRQ except if MASK_BUCK1_IRQ is set.
- Overcurrent protection (flag is BUCK1_OC bit). BUCK1 is therefore switched off except if MASK_BUCK1_OC_POWER_OFF is set.
- Overcurrent detection generates an IRQ except if MASK_BUCK1_OC_IRQ is set.
- BUCK1 feedback (FB1) pin disconnection, flag is BUCK1_UV and the BUCK1 is switched off.
- FB1 pin disconnection generates an IRQ except if MASK_BUCK1_IRQ is set.
- Overtemperature detection by central thermal sensor (flag is TSD_CL0, see also the Section 4.7: Temperature monitoring) and device is executed power down sequence.

In active and REC-1 states, when BUCK1_REGFAIL_GO_REC is set at 1 in USER-NVM, in case of PG timeout, OV, UV, INT_FAIL, OC, FBLOSS, or TSD events the device executes a power down sequence, enters in REC-2 state and makes an automatic retry. PG_TIMEOUT, OV, UV, OC, INT_FAIL, FBLOSS or TSD flags are not blocking to re-enable the BUCK1 after a fail event.

According to a suitably configured output voltage, it can be also used to supply other BUCKs. It is not recommended to use MASK_BUCK1_OC_POWER_OFF and MASK_BUCK1_UV_POWER_OFF in the same time.

3.3.2 BUCK2 converter

The BUCK2 converter is the same as the BUCK1.

The BUCK2 regulator is a synchronous converter compatible to battery level, with integrated power mos. Stability compensation network is external.

Output voltages are programmable via USER-NVM through the bit BUCK2_PU_VALUE.

The switching frequency can be selected either at 400 kHz or 2.4 MHz, by USER-NVM BUCK2_FREQ. To limit emission in audio bandwidth, refresh frequency can be forced at 25 kHz by USER-NVM bit BUCK2_REFRESH_FREQ set low (1 kHz when high). The draw back will be an extra consumption in low power mode.

The spread spectrum feature is configurable by SPI bit BUCK2_SPREAD_ENA (disabled by default).

BUCK2 integrates a low power mode (automatically set by LOW_POWER_SET by SPI) that optimizes its efficiency in active low power mode. (BUCK2 can be optionally enabled in active low power mode).

BUCK2 can be disabled by the SPI bit VBUCK2_ENA. (only after SPI_PROTECT_ACCESS has been set). In active low power mode, the action of enable BUCK2 is not allowed.

The live bit VBUCK2_ENA_STATUS reflects the state of BUCK2 output.

Note: After the first power up is needed to align the live bit associated in DSR18 (VBUCK2_ENA_STATUS) with the current value associated in DCR1.

In active full power BUCK2 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK2_UV). BUCK2 is therefore switched off after $t_{buck2\_UV\_TO}$ except if SPI bit MASK_BUCK2_UV_POWER_OFF is set.
- Undervoltage detection generates an IRQ except if MASK_BUCK2_IRQ is set.
- OV detection to monitor the output voltage (flag is BUCK2_OV bit) BUCK2 is therefore switched off after $t_{buck2\_OV\_TO}$. Status register bit BUCK2_OV must be read and cleared before switching ON the regulator by SPI bit VBUCK2_ENA to allow a proper start-up (only when BUCK2 is not critical for MCU).
- Overvoltage detection generates an IRQ except if MASK_BUCK2_IRQ is set.
- Power-good used to signal BUCK power on success (flag is BUCK2_PG_OK bit and IRQ is generated except if MASK_BUCK2_PG_IRQ is set):
  - If not, after $T_{BUCK2\_PG\_TO}$ timing, BUCK2 is switched off and flag BUCK2_PG_TIMEOUT is set.
- Not successful power-good detection generates an IRQ except if MASK_BUCK2_PG_TIMEOUT_IRQ is set.
- Configurable overcurrent protection through U-NVM BUCK2_IPEAK(flag is BUCK2_OC bit). BUCK2 is therefore switched off after $t_{buck2\_OC\_TO}$ except if MASK_BUCK2_OC_POWER_OFF is set.
- Overcurrent detection generates an IRQ except if MASK_BUCK2_OC_IRQ is set.
- Warning temperature detection by a local thermal sensor (flag is TW_CL2).
- Warning temperature detection generates an IRQ except if MASK_CL2_TW_IRQ is set.
- Overtemperature detection by a local thermal sensor (flag is TSD_CL2, see also the Section 4.7: Temperature monitoring) and BUCK2 is switched off.
- BUCK2 internal regulators detection, flag is BUCK2_INT_FAIL and the BUCK2 is switched off.
- Internal fail generates an IRQ except if MASK_BUCK2_IRQ is set.
- BUCK2 Feedback (FB2) pin disconnection, flag is BUCK2_UV and the BUCK2 is switched off.
- FB2 pin disconnection generates an IRQ except if MASK_BUCK2_IRQ is set.
- After a fault detection (UV, OV,OC, FBLOSS, TSD_CL2 or PG timeout), BUCK2 can be re-enabled by setting BUCK2_ENA = 0 followed by BUCK2_ENA = 1.

In active low power, BUCK2 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK2_UV). BUCK2 is therefore switched off except if SPI bit MASK_BUCK2_UV_POWER_OFF is set.
- Undervoltage detection generates an IRQ except if MASK_BUCK2_IRQ is set.
- OV detection to monitor the output voltage (flag is BUCK2_OV bit) BUCK2 is therefore switched off.
- Overvoltage detection generates an IRQ except if MASK_BUCK2_IRQ is set.
- Overcurrent protection (flag is BUCK2_OC bit). BUCK2 is therefore switched off except if MASK_BUCK2_OC_POWER_OFF is set.
- Overcurrent detection generates an IRQ except if MASK_BUCK2_OC_IRQ is set.
- BUCK2 feedback (FB2) pin disconnection, flag is BUCK2_FBLOSS and the BUCK2 is switched off.
- FB2 pin disconnection generates an IRQ except if MASK_BUCK2_IRQ is set.
- Overtemperature detection by a central thermal sensor (flag is TSD_CL0, see also the Section 4.7: Temperature monitoring) and device is executed power down sequence.

In active and REC-1 states, when BUCK2_REGFAIL_GO_REC is set at 1 in USER-NVM, in case of PG timeout, OV, UV, INT_FAIL, OC, FBLOSS or TSD events the device executes a power down sequence, enters in REC-2 state and makes an automatic retry. PG_TIMEOUT, OV, UV, OC, INT_FAIL, FBLOSS or TSD flags are not blocking to re-enable the BUCK2 after a fail event.

It is not recommended to use MASK_BUCK2_OC_POWER_OFF and MASK_BUCK2_UV_POWER_OFF in the same time.

3.3.3 BUCK3 converter

BUCK3 is a postregulator and needs to be supplied by BUCK1 or BUCK2 through the VIN3 pin.

The BUCK3 converter is similar to BUCK1 but with double current capability. Moreover, if the output voltage is configured at 0.98 V, a further SPI fine-tuning in steps of 10 mV is available (BUCK3_FTUNE[2..0] control bits), covering the range between 0.95 V and 1.01 V.

Output voltages are programmable via USER-NVM through the bit BUCK3_PU_VALUE.

The spread spectrum feature is configurable by SPI bit BUCK3_SPREAD_ENA (disabled by default).

To limit emission in audio bandwidth, refresh frequency can be forced at 25 kHz by USER-NVM bit BUCK3_REFRESH_FREQ set low (1 kHz when high).

BUCK3 can be disabled by the SPI bit VBUCK3_ENA. (only after SPI_PROTECT_ACCESS has been set. BUCK3 must be disabled before entering in active low power mode and must not be enabled in this mode).

The live bit VBUCK3_ENA_STATUS reflects the state of BUCK3 output.

Note: After the first power up is needed to align the live bit associated in DSR18 (VBUCK3_ENA_STATUS) with the current value associated in DCR1.

The BUCK3 converter provides the following diagnostics:

- UV detection to monitor the output voltage (flag is BUCK3_UV). BUCK3 is therefore switched off after $t_{buck3\_UV\_TO}$ except if SPI bit MASK_BUCK3_UV_POWER_OFF is set.
- Undervoltage detection generates an IRQ except if MASK_BUCK3_IRQ is set.
- OV detection to monitor the output voltage (flag is BUCK3_OV bit) BUCK3 is therefore switched off after $t_{buck3\_OV\_TO}$. It must be read and cleared before switching ON the regulator by SPI bit VBUCK3_ENA to allow a proper start-up (only when BUCK3 is not critical for MCU).
- Overvoltage detection generates an IRQ except if MASK_BUCK3_IRQ is set.
- Power-good used to signal BUCK power on success (flag is BUCK3_PG_OK bit and IRQ is generated except if MASK_BUCK3_PG_IRQ is set):
  - If not, after $T_{BUCK3\_PG\_TO}$ timing, BUCK3 is switched off and flag BUCK3_PG_TIMEOUT is set.
- Not successful power-good detection generates an IRQ except if MASK_BUCK3_PG_TIMEOUT_IRQ is set.
- Configurable overcurrent protection voltage (flag is BUCK3_OC bit). BUCK3 is therefore switched off after $t_{buck3\_OC\_TO}$ except if MASK_BUCK3_OC_POWER_OFF is set.
- Overcurrent detection generates an IRQ except if MASK_BUCK3_OC_IRQ is set.
- Warning temperature detection by a local thermal sensor (flag is TW_CL3).
- Warning temperature detection generates an IRQ except if MASK_CL3_TW_IRQ is set.
- Overtemperature detection by local thermal sensor (flag is TSD_CL3, see also the Section 4.7: Temperature monitoring) and BUCK3 is switched off.
- BUCK3 internal regulators detection, flag is BUCK3_INT_FAIL and the BUCK3 is switched off.
- Internal fail generates an IRQ except if MASK_BUCK3_IRQ is set.
- After a fault detection (UV, OV,OC, INT_FAIL, TSD_CL3 or PG timeout), BUCK3 can be re-enabled by setting BUCK3_ENA = 0 followed by BUCK3_ENA = 1.

In active and REC-1 states, when BUCK3_REGFAIL_GO_REC is set at 1 in USER-NVM, in case of PG timeout, OV, UV, OC, INT_FAIL or TSD events the device executes a power down sequence, enters in REC-2 state and makes an automatic retry. PG_TIMEOUT, OV, UV, OC, INT_FAIL or TSD flags are not blocking to re-enable the BUCK3 after a fail event.

It is not recommended to use MASK_BUCK3_OC_POWER_OFF and MASK_BUCK3_UV_POWER_OFF in the same time.

3.4 Linear voltage regulators

3.4.1 LDO1

The LDO1 is dedicated to supply external loads. It is supplied by FBB pin. LDO1 has a 5 V output and 120 mA current capability.

It can be enabled/disabled through the LDO1_ENA control bit (only after SPI_PROTECT_ACCESS has been set).

The voltage regulator is protected against undervoltage (flag is LDO1_UV) and LDO1 is switched off.

The undervoltage detection generates an IRQ except if it is masked with MASK_LDO1_IRQ the live bit LDO1_ENA_STATUS reflects the state of LDO1 output.

Note: After the first power up is needed to align the live bit associated in DSR18 (LDO1_ENA_STATUS) with the current value associated in DCR1.

- Power-good used to signal LDO1 power on success (flag is LDO1_PG_OK bit):
  - If not, after $T_{LDO1\_PG\_TO}$ timing, LDO1 is switched off and flag LDO1_PG_TIMEOUT is set.
- The power on success generates an IRQ except if it is masked with MASK_LDO1_PG_IRQ.
- Not successful power-good detection generates an IRQ except if MASK_LDO1_PG_TIMEOUT_IRQ is set.
- After a fault detection (UV or PG timeout), LDO1 can be re-enabled by setting LDO1_ENA = 0 followed by LDO1_ENA = 1, even if fail flags are not cleared.

Current limitation I_{LDO1_Cmax} of the regulator ensures fast charge of external decoupling capacitors.

The output voltage is stable for ceramic load capacitors $C_{LDO1\_load} \geq 1$ µF.

Warning temperature detection by a local thermal sensor (flag is TW_CL0).

Warning temperature detection generates an IRQ except if MASK_CL0_TW_IRQ is set.

In case the device temperature exceeds the TSD_CL0 threshold, the device executes a power down sequence before entering in REC-2 state.

3.4.2 LDO2

The SPSB100 embeds one low dropout tracking regulator designed to provide an output voltage that closely tracks bucks reference at ±10 mV while delivering on the LDO2 output pin up to 10 mA. The LDO2 voltage tracker is supplied by pin FBB.

LDO2_ENA SPI bit is used to enable/disable this LDO (only after SPI_PROTECT_ACCESS has been set. LDO2 must be disabled before entering in active low power mode and must not be enabled in this mode).

LDO2 can be configured by means of the USER-NVM LDO2_TRK bits to track one of BUCK1, BUCK2 or BUCK3 if related output voltages are 5 V or 3.3 V (see the Table 6).

Table 6. Voltage regulators configuration

Tracking configuration	LDO2_TRK[0,1] USER-NVM configuration bits	Selected voltage source	Source output voltage	LDO2 behavior
1	00	BUCK1	3.3 V or 5 V	Tracks buck1
			6.5 V	OFF what ever LDO2_ENA
2	01	BUCK2	3.3 V or 5 V	Tracks buck2
			6.5 V	OFF what ever LDO2_ENA
3	1x	BUCK3	0.98 V ÷ 1.25 V	OFF what ever LDO2_ENA
			3.3 V	Tracks buck3

LDO2 is supplied by FBB.

The tracking regulator is protected against:

- The live bit LDO2_ENA_STATUS reflects the state of LDO2 output.

Note: After the first power-up is needed to align the live bit associated in DSR18 (LDO2_ENA_STATUS) with the current value associated in DCR1.

- Overvoltage detection to monitor the output voltage (flag is LDO2_OV bit) and LDO2 is therefore switched off.
- Overvoltage detection generates an IRQ except if MASK_LDO2_IRQ is set.
- Undervoltage detection (the flag is LDO2_UV bit) and LDO2 are therefore switched off.
- Undervoltage detection generates an IRQ except if MASK_LDO2_IRQ is set.
- Power-good used to signal LDO2 power on success (flag is LDO2_PG_OK bit).
- If not, after $T_{LDO2\_PG\_TO}$ timing, LDO2 is switched off and flag LDO2_PG_TIMEOUT is set.
- The power-on success generates an IRQ except if it is masked with MASK_LDO2_PG_IRQ.
- Not successful power-good detection generates an IRQ except if MASK_LDO2_PG_TIMEOUT_IRQ is set.
- Warning temperature detection by a local thermal sensor(flag is TW_CL4).
- Warning temperature detection generates an IRQ except if MASK_CL4_TW_IRQ is set.

- Overtemperature detection by local thermal sensor (flag is TSD_CL4, see also the Section 4.7: Temperature monitoring) and LDO2 is switched off.
- After a fault detection (UV, OV, TSD_CL4 or PG timeout), LDO2 can be re-enabled by setting LDO2_ENA = 0 followed by LDO2_ENA = 1, even if fail flags are not cleared.
- LDO2 is switched off if a fault on the track regulator is detected.
- In active and REC-1 states, when LDO2_REGFAIL_GO_REC is set at 1 in USER-NVM, in case of PG timeout, OV, UV or TSD events the device executes a power down sequence, enters in REC-2 state and makes an automatic retry.

3.5 Operating modes

The device can work in a normal operation mode (ACTIVE state - FULL-POWER mode) or in a reduced operation mode (ACTIVE state - LOW-POWER mode).

The transition between FULL-POWER and LOW-POWER mode is managed by SPI command (LOW_POWER_SET control bit, only after SPI_PROTECT_ACCESS has been set).

In ACTIVE state the device is fully controllable and configurable through SPI.

Moreover, a DEEP-SLEEP state is available to minimize current consumption during not-operating time frames by SPI command DO_POWER_DOWN (only after SPI_PROTECT_ACCESS has been set). Status bits DEEP-SLEEP_FROM_DO_POWER_DOWN will be set at “01” if transition from active state or “1x” if transition from REC-1 state.

DEEP-SLEEP_FROM_DO_POWER_DOWN can be cleared by CLR_DEEP_SLEEP_FROM_DO_POWER_DOWN bit.

3.5.1 Wake-up from DEEP-SLEEP to ACTIVE state

A wake-up from DEEP-SLEEP state will transit the device to INIT state as described in the Section 3.6.3: States and transitions description.

To avoid disabling all wake-up capability, a hard protection is implemented: the SPI writing to disable the last wake-up possibility define in the Table 7 is not taken into account and a status register bit SPI_ALL_WAKEUP_DISABLE is set and generates an IRQ except if MASK_SPI_ERROR_IRQ is set.

Current consumption in DEEP-SLEEP mode is calculated as I_{VS_DP} + wake-up current consumption contributions.

This can be initiated by one or more of the following events:

Table 7. Wake-up events description

Wake up source	Description	Flag
Level change of wake-up (WU)	Can be configured by SPI (WU_ENA(1) bit)	WU_WAKE
Level change of wake-up (IGN)	Can be configured by SPI (IGN_ENA(1) bit)	IGN_WAKE
Cyclic monitoring (WU)	Can be configured by SPI (WU_FILT bit with TIMER_ENA = 1)	WU_WAKE
Cyclic monitoring (IGN)	Can be configured by SPI (IGN_FILT bit with TIMER_ENA = 1)	IGN_WAKE
Timer	Can be configured by SPI (TIMER_WAKE_ENA bit with TIMER_ENA = 1)	TIMER_WAKE

1. *Wake-up event can be missed during SPI writing to DO_POWER_DOWN = 1.*

3.5.2 Wake-up events in ACTIVE mode

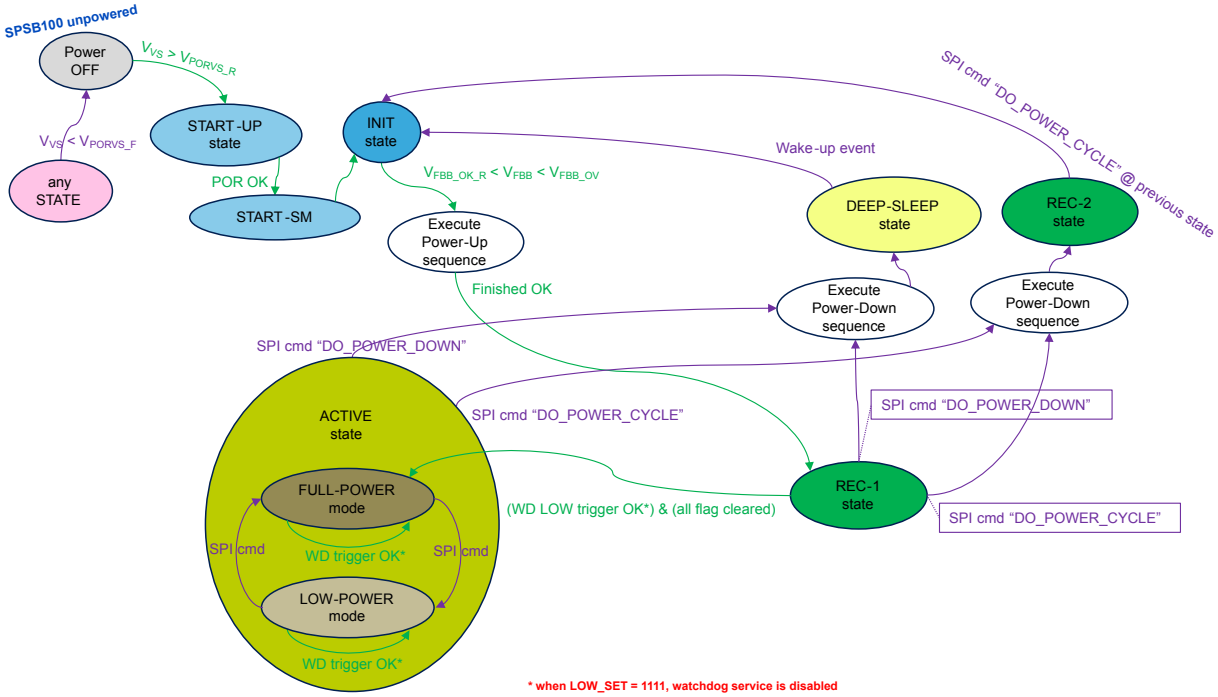
All enabled wake-up events described in the Table 7 in ACTIVE mode are signaled to the microcontroller by an interrupt request on IRQ pin.

3.6 Functional overview - State machine

To make the reading easier the State machine description has been split in three parts: first the state diagram is presented with the normal transitions (see the Section 3.6.1: State machine without fault transitions), then transitions resulting to a fault event detection are exposed (see the Section 3.6.2: State machine focusing on fault transitions), finally the full state machine is described and states and transitions detailed (see the Section 3.6.3: States and transitions description).

3.6.1 State machine without fault transitions

Figure 12. State machine without fault transitions



Until the voltage on VS pin reaches V_{PORVS_R} for the first time the device is in POWER-OFF state, after that the device transits to START-UP state where internal power supplies are established. Then core logic reset is released and START-SM state is reached where oscillators start and NVM is read and checked.

Refer to the Section 3.8: User's NVM modification procedure for details of USER-NVM space programming.

After startup completion the device reaches INIT state where digital BIST is run, and when the FBB voltage reaches $V_{FBB\_OK\_R}$ the device executes a power-up sequence which turns ON all regulators as per application requirements stored in USER-NVM space. The sequence includes the NRST pin deassertion to high level and at the same time the start of watchdog long open window. See the power-up sequence description in the Section 3.7.1: Power-up sequence for details. After the power-up sequence the device enters in RECOVERY-1 state: SPSB100 is waiting that MCU boots up and trigs the watchdog, except if LOW_SET[3:0] = 1111, before expiration of watchdog long open window timeout. After the valid trig of the watchdog during its long open window timeout the device reaches ACTIVE state in FULL-POWER mode. In an active state the device is fully controllable by SPI: the MCU can configure SPSB100 features as per application needs to optimize ECU performances and global power consumption. In particular some regulators can be switched OFF by SPI and SPSB100 can be set in LOW-POWER mode to reduce ECU power consumption while delivering the strict minimum power supply and supervision to the MCU. Later the MCU can reconfigure the SPSB100 in FULL-POWER mode by SPI.

In active state, the MCU can also request a power cycle to SPSB100: a power-down sequence is then executed, followed by digital BIST in INIT state before executing a power-up sequence. In an ACTIVE state, the MCU can also request a power down to SPSB100: a power-down sequence is then executed and DEEP-SLEEP state is reached. It is left upon a wake-up event. Wake-up events sensitivity shall be programmable by SPI in ACTIVE state and includes cyclic sensing of WU pin with cyclic powering of OUT_HS, edge and level detection on IGN wake-up frame detection.

3.6.2 State machine focusing on fault transitions

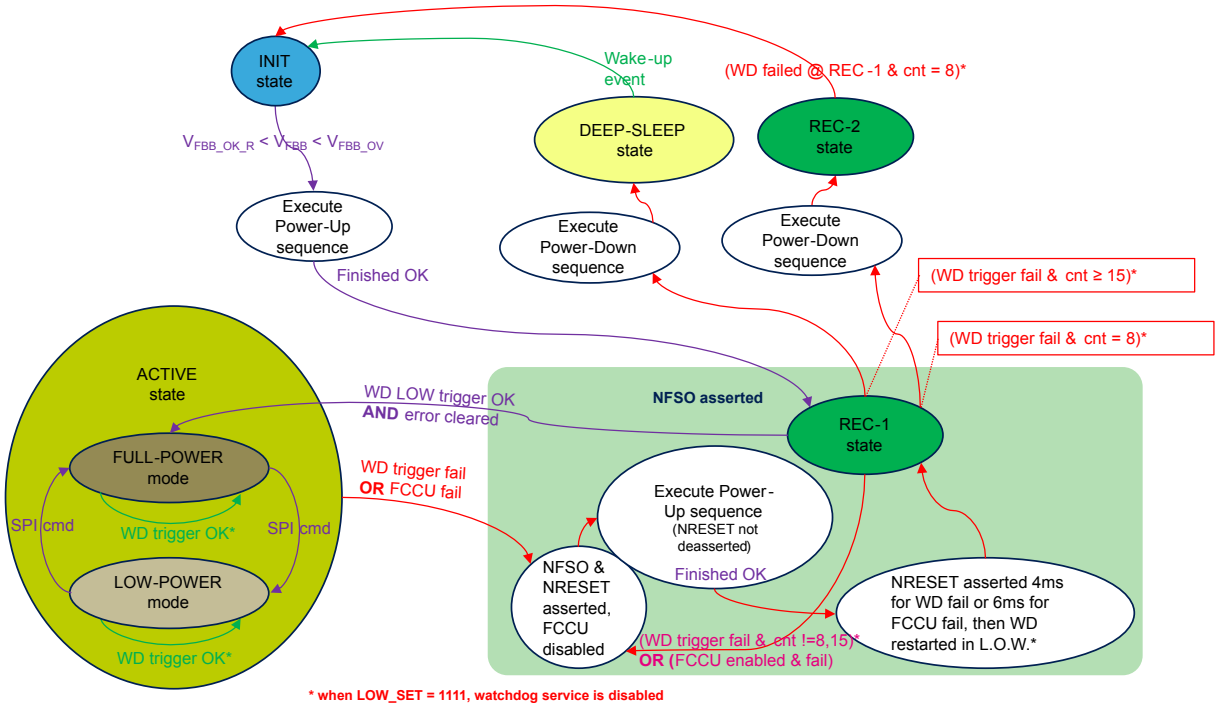
3.6.2.1 NVM faults management

The NVM faults management are explained in the Section 3.8.1: Starts-up with valid NVM data and NVM faults management.

3.6.2.2 *Watchdog trig and FCCU monitor faults management*

The watchdog is launched during the power-up sequence when the NRST pin is deasserted high, it starts with a long open window timeout. After the power-Up sequence, the SPSB100 reaches RECOVERY-1 state which is dedicated to watchdog and FCCU monitor faults management.

Figure 13. State machine details with WD trig and FCCU monitor faults management



While in RECOVERY-1 state, a read and clear of error flags and a proper trig of the watchdog in long open window timeout will initiate a transition to ACTIVE state.

If the watchdog is triggered without clearing all flags, then the device remains in RECOVERY-1 state and the watchdog runs with normal window timings.

In an ACTIVE state the watchdog runs with normal window timings. Proper trig of the watchdog maintains SPSB100 in an ACTIVE state, while a failure in watchdog service or a fault detected on FCCU monitor will:

- Increment the watchdog trig fault counter (only on watchdog trig fault);
- Assert NRST pin low;
- Disable and reset the FCCU monitor;
- Initiate a power-up sequence: this is mandatory to power backup regulators that could have been switched off by SPI.

Then the NRST pin remains asserted for 4 ms, at least, in case of watchdog trig fault, 6 ms at least, in case of FCCU monitor fault, before being released, watchdog starts a long open window timeout and SPSB100 reaches RECOVERY-1 state.

In case of successive faults in servicing the watchdog in a long open window the watchdog trig fault counter is incremented, a power-up sequence is run, a 4 ms NRST pulse is generated and a long open window timeout is restarted.

If the watchdog is properly served during the long open window, then the watchdog trig fault counter is reset and SPSB100 enters in ACTIVE state.

The 8 successive watchdog trig faults force SPSB100 to initiate a power cycle through RECOVERY-2 and INIT states. And in case of 15 successive watchdog trig faults SPSB100 will enter in a DEEP-SLEEP state.

Note: In this specific case, the I_{VDS} current consumption is higher (worst case 4.8 mA max) than expected (40 µA max).

The FCCU monitor is disabled and its configuration reset after the first watchdog trig fault. FCCU monitor can be reconfigured and enabled through SPI in RECOVERY-1 or ACTIVE state.

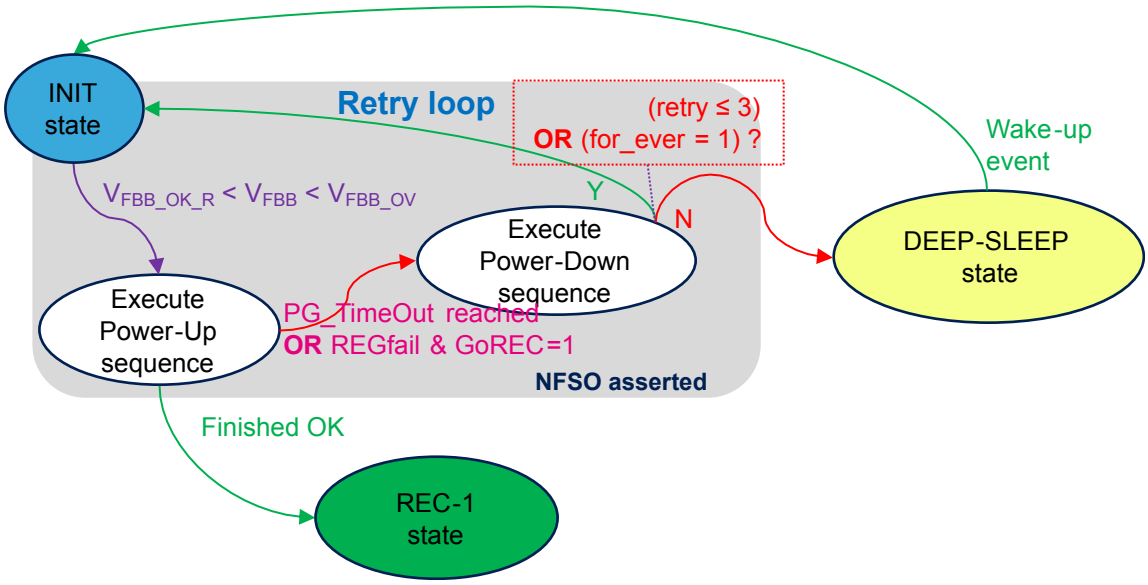
3.6.2.3 *Power-up fault management*

The power-up sequence can be programmed to wait the power-good signal of any of the turned-on regulator (see the power-up sequence description in the Section 3.7.1: Power-up sequence for details). In such case a timeout counter runs, it is longer than the maximum rising time of SPSB100 regulators.

If the timeout elapses, the SPSB100 executes a power-down sequence, the power-up retry counter POWUP_RETRY_CNT is incremented and SPSB100 retries 4 times to power-up the regulators (POWUP_RETRY_CNT counter can be cleared by CLR_POWUP_RETRY_COUNT bit). If 4 successive faults occur and the PU_LOOP_FOR_EVER bit is not set, then SPSB100 enters in DEEP-SLEEP state, clears the POWUP_RETRY_CNT and generates a status register flag FORCED_SLEEP_POWUP. If the PU_LOOP_FOR_EVER bit is set SPSB100 retries to power-up forever.

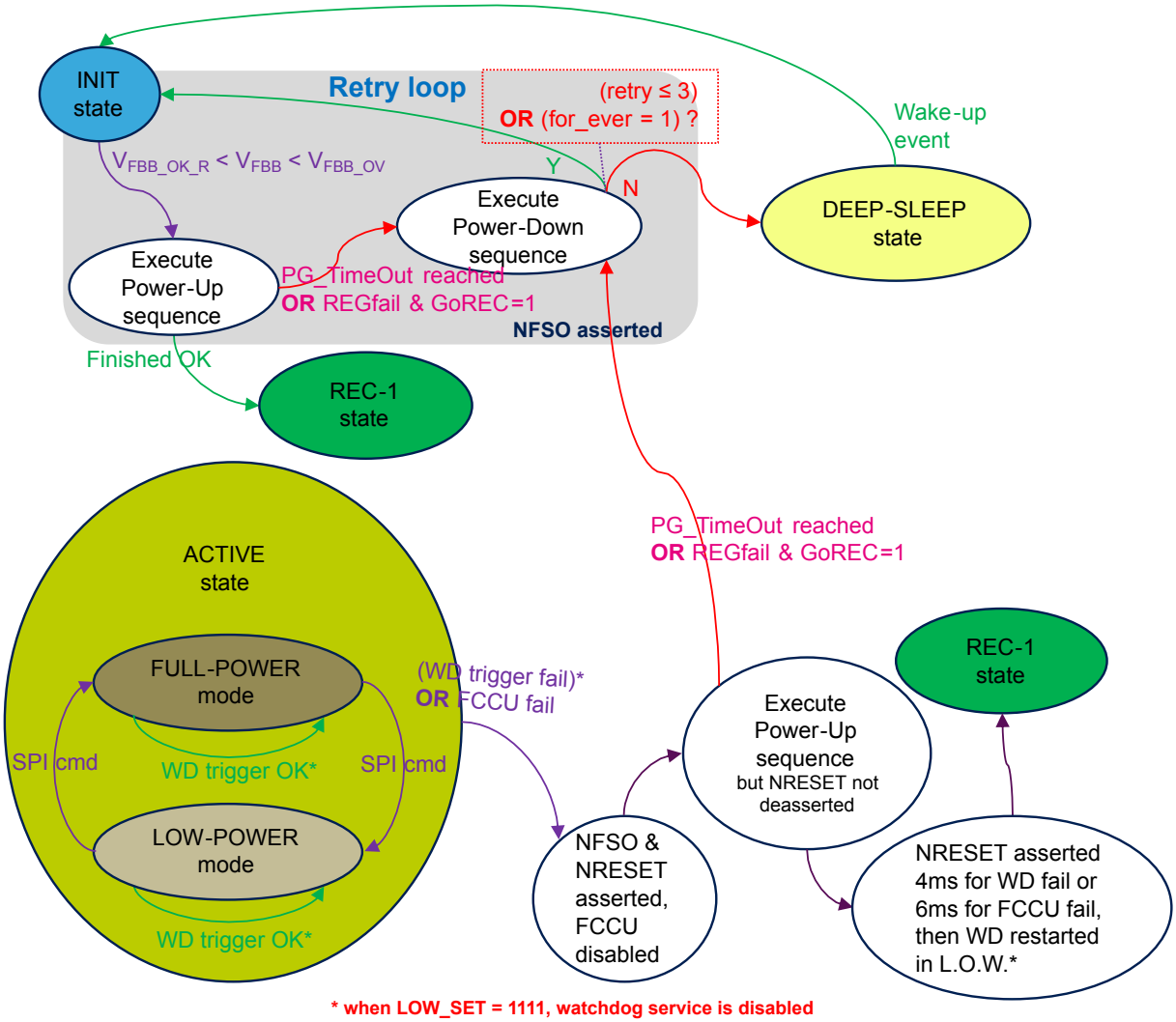
The same retry loop applies if a fault on a regulator is detected during the power-up sequence and the regulator has its REGFAIL_GO_REC configuration bit set to 1. See the Section 3.7.1: Power-up sequence for details.

Figure 14. State machine details on power-up fault (1)



The behavior is similar if the power-up sequence timeout is reached when the sequence is executed after a watchdog trig fault or a FCCU monitor fault detection as shown in the following figure.

Figure 15. **State machine details on power-up fault (2)**



*** when LOW_SET = 1111, watchdog service is disabled**

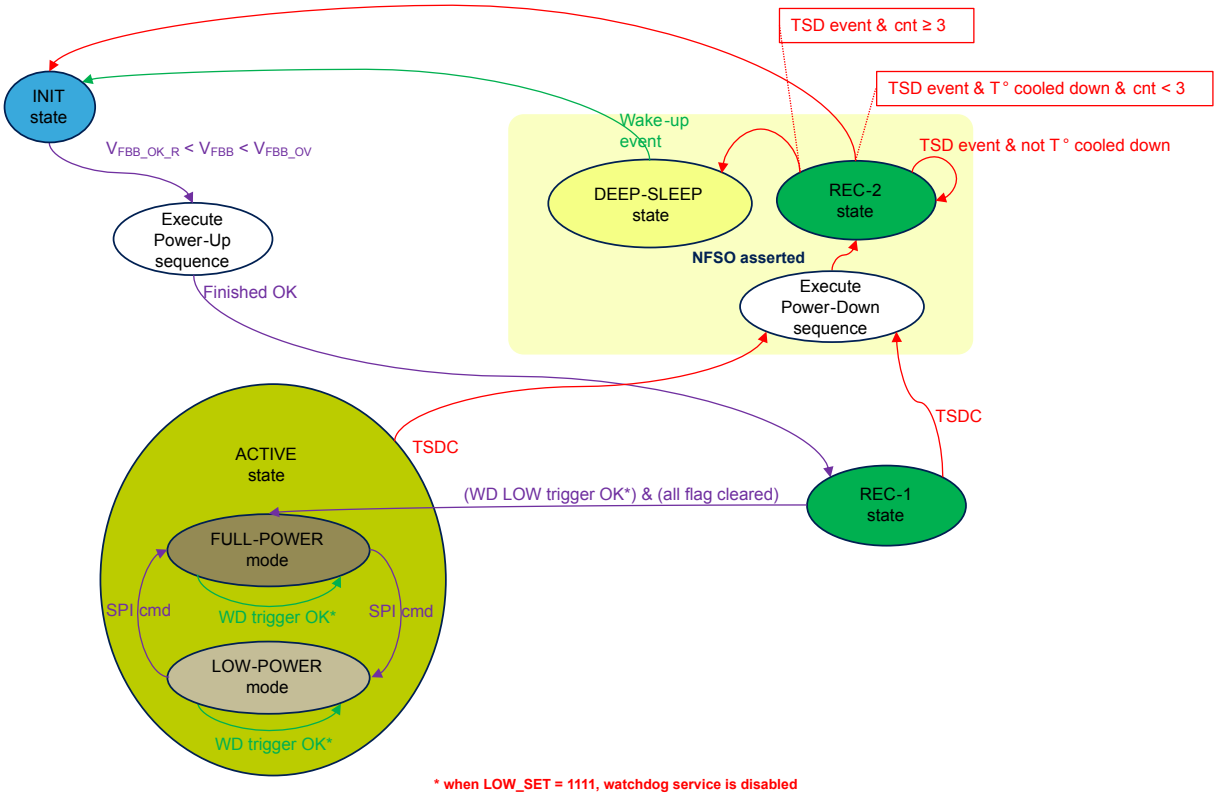
3.6.2.4 *Central thermal sensor fault management*

The central thermal sensor plays a major role in protecting the whole device. This sensor is monitoring the temperature of the SPSB100 core. If SPSB100 core temperature exceeds the TSDC threshold a power-down is run and SPSB100 reaches RECOVERY-2 state.

In RECOVERY-2 state all regulators are OFF, the TSD event counter TSD_CNT_FAIL is incremented. After the temperature cooled down, if TSD_CNT_FAIL is less than 3 then SPSB100 transits to INIT state and initiates a power-up sequence, if not then SPSB100 transits to DEEP-SLEEP state until a wake-up event and generates a status register flag FORCED_SLEEP_TSD.

The TSD event counter, TSD_CNT_FAIL, is readable through SPI and can be cleared by CLR_TSD_CNT_FAIL bit. This counter is incremented after a TSD event on any of the clusters.

Figure 16. **State machine details onTSDC fault**



3.6.2.5 *Regulator faults management*

Each SPSB100 regulator has the following monitors:

- Temperature sensor with a warning threshold (TW) and a shut-down threshold (TSD)
- Undervoltage comparator (UV) except for LDO1
- Overvoltage comparator (OV)
- Power-good comparator (PG_TIMEOUT)
- Overcurrent comparator (OC) on BUCKs
- Internal regulator comparator (INT_FAIL) on BUCKs
- FB pin disconnection (FBLOSS for BUCK1 and BUCK2)

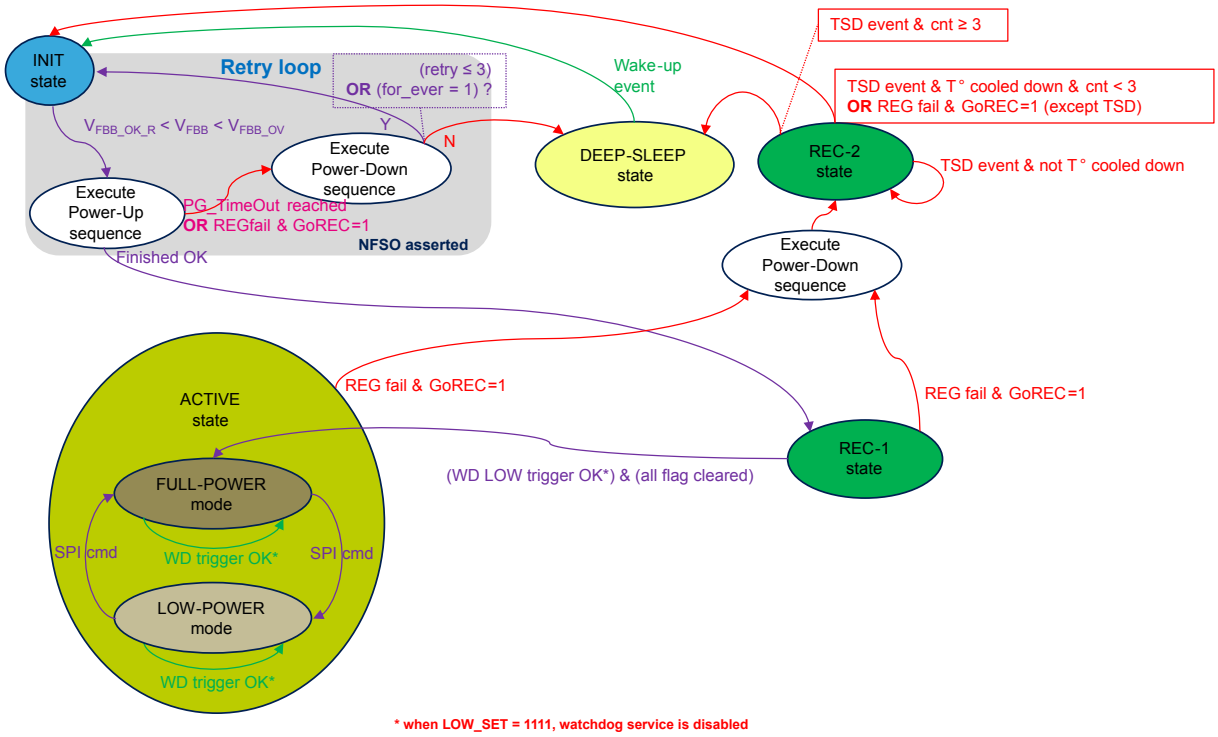
The user can decide how SPSB100 shall react on an event of those monitors, this is done through the USER-NVM bit REGFAIL_GO_REC of each of them.

A TW event sets the associated flag and generates an interruption, while the reaction to a TSD, UV, PG_TIMEOUT, OC, INT_FAIL, FBLOSS and OV event depends on the regulator REGFAIL_GO_REC bit.

When REGFAIL_GO_REC is set to ‘1’, a fault detected on regulator TSD, UV, PG_TIMEOUT, OC, INT_FAIL, FBLOSS and OV monitors will initiate a power-down sequence, then the state machine transits to INIT state and runs a power-up sequence: if a fault is detected then the retry sequence described in the Section 3.6.2.3: Power-up fault management is executed. In the case of TSD the SPSB100 reaction is the same as for the TSDC event described in the Section 3.6.2.4: Central thermal sensor fault management.

A fault event counter REG_FAIL_CNT is incremented when a power-down sequence is initiated by a regulator fault event. When the counter reaches 3, SPSB100 transits to DEEP-SLEEP state where the counter is reset and the SPI flag FORCED_SLEEP_REGFAIL is set. REG_FAIL_CNT is cleared by SPI bit CLR_REG_FAIL_CNT.

Figure 17. Regulator faults reaction with REGFAIL_GO_REC = 1

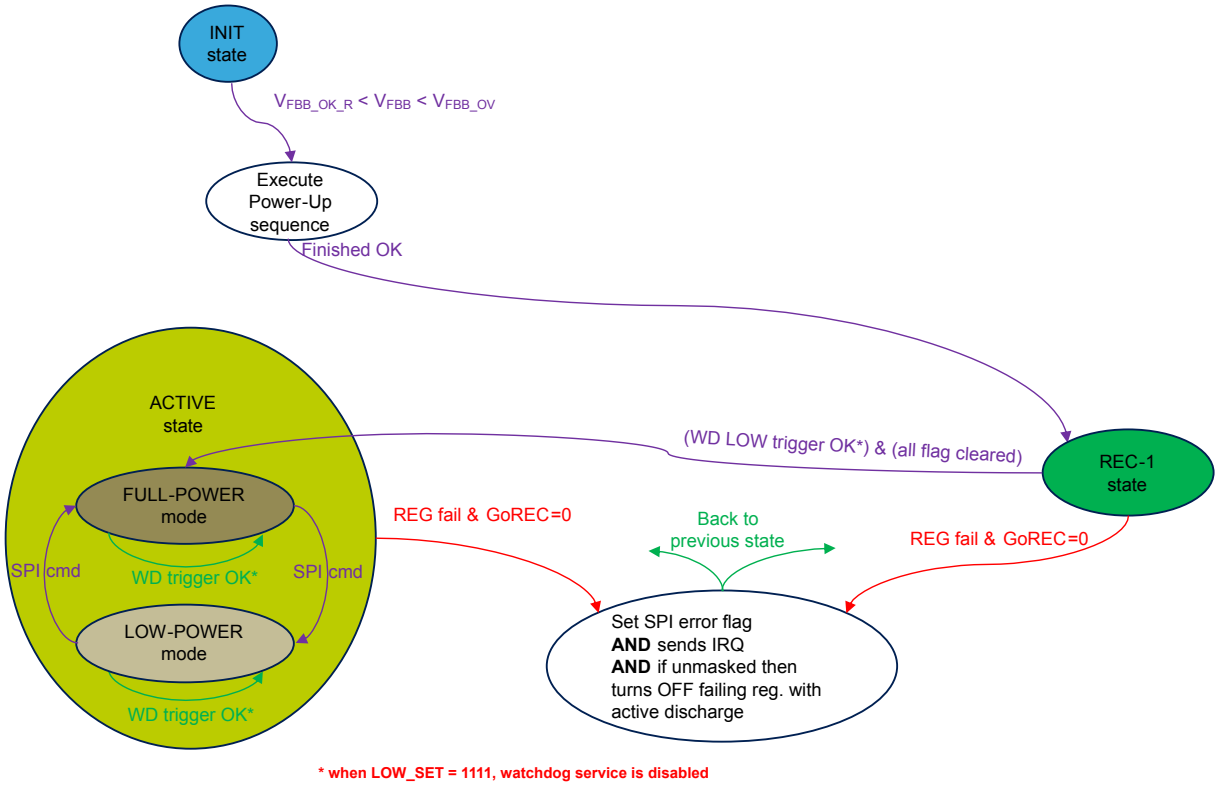


When REGFAIL_GO_REC is reset to ‘0’, a fault detected on regulator, TSD, UV, OC, INT_FAIL, FBLOSS and OV monitors will:

- Set the associated flag.
- Send an interruption. The interruption can be masked for UV, OC, INT_FAIL, FBLOSS and OV and TW, not for TSD.
- Switch OFF the regulator if the action is not masked. Action of UV and OC is maskable, while an INT_FAIL, FBLOSS, OV and TSD event always switch OFF the regulator. TW event never switches OFF the regulator.

The state machine does not change its state if REGFAIL_GO_REC is reset to ‘0’.

Figure 18. **Regulator faults reaction with REGFAIL_GO_REC = 0**

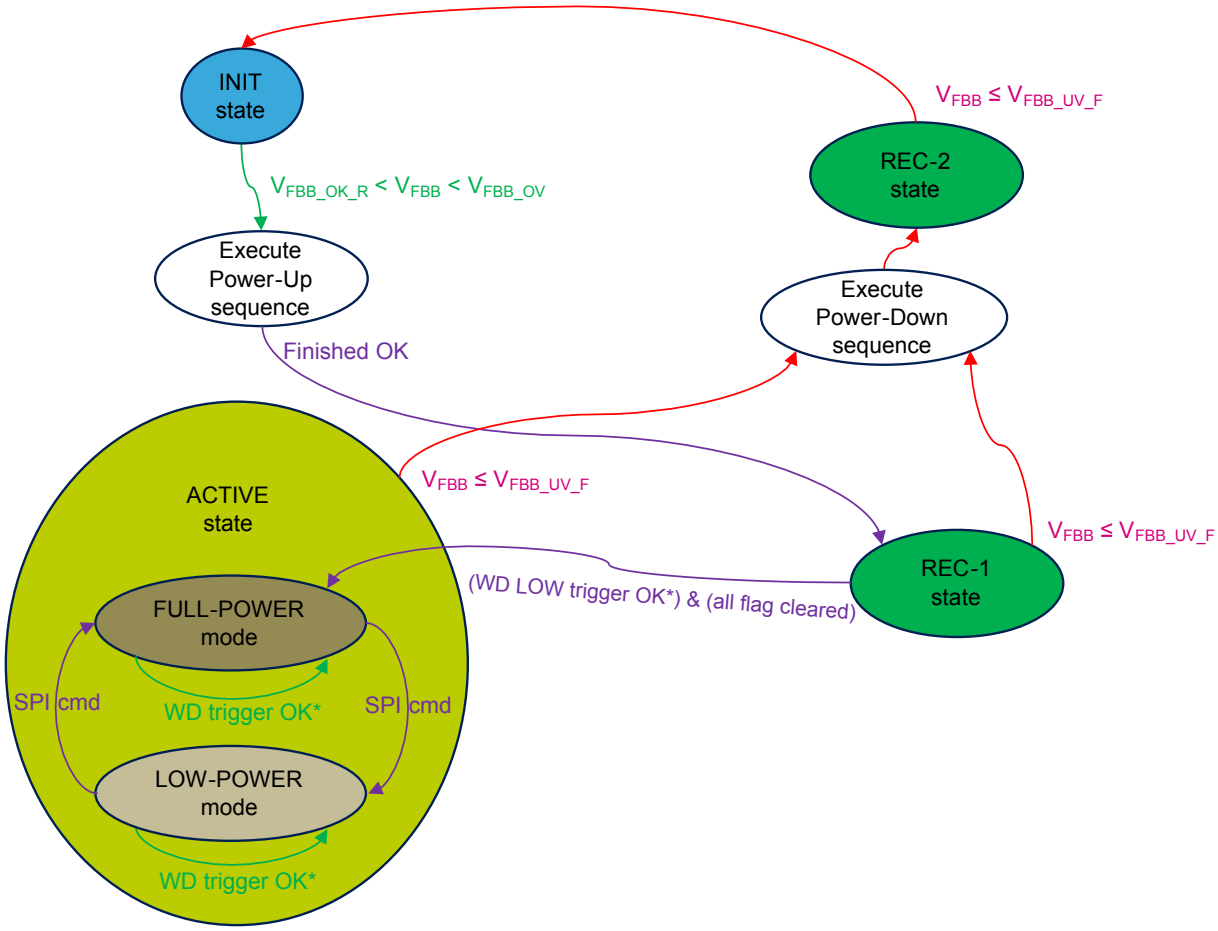


*** when LOW_SET = 1111, watchdog service is disabled**

3.6.2.6 *FBB voltage drop management*

SPSB100 monitors the voltage on FBB pin. The state machine reacts in case of FBB pin voltage drops below $V_{FBB\_UV\_F}$ threshold by executing a power-down sequence and transitioning to RECOVERY-2 then INIT state. In INIT state SPSB100 restarts when the FBB pin voltage rises above $V_{FBB\_OK\_R}$.

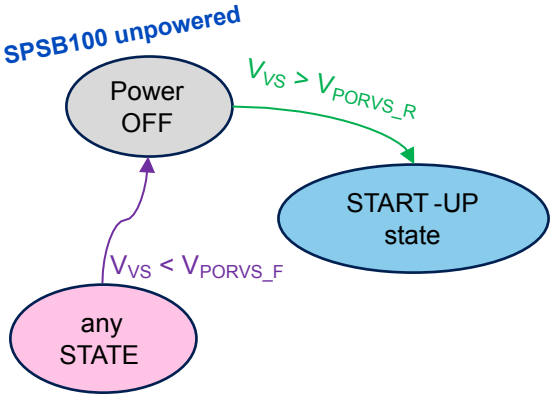
Figure 19. FBB pin voltage fault reaction



*** when LOW_SET = 1111, watchdog service is disabled**

In case VS pin voltage drops below V_{PORVS_F} a hard reset of SPSB100 is generated independently of SPSB100 current state, the POWER-OFF state is forced. SPSB100 starts up again after VS pin voltage rises above V_{PORVS_R}.

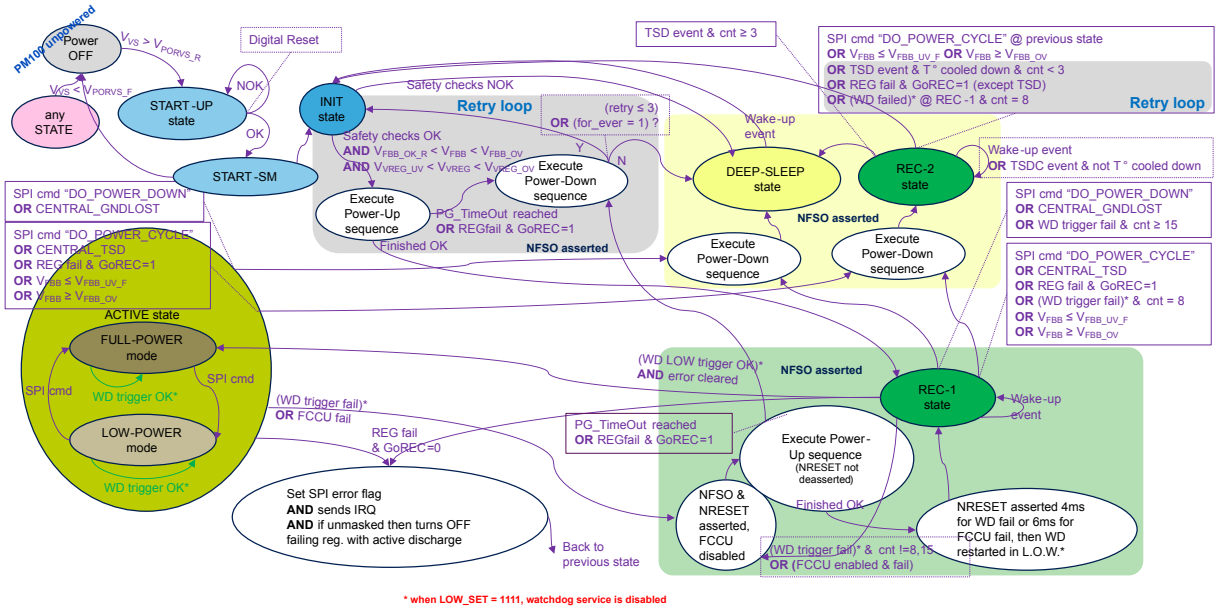
Figure 20. VS pin voltage fault reaction



3.6.3 States and transitions description

The following figure shows the entire state machine.

Figure 21. State machine



SPSB100 states can be read by status register bits DEV_STATE.

3.6.3.1 *Power-OFF state*

Power-OFF state is the default state when SPSB100 is not powered.

This state is entered unconditionally when VS pin voltage drops below V_{PORVS_F}.

3.6.3.2 *START-UP state*

START-UP state is entered from Power-OFF state when VS pin voltage reaches V_{PORVS_R}.

In this state internal power supplies are established, and the digital core reset is released.

SPSB100 transits to START-SM state.

3.6.3.3 *START-SM state*

START-SM state is entered after the START-UP completion when the digital core reset is released.

In this state oscillators start and the main state machine is executed. It is possible to enter in USER-NVM programming mode, refers to the Section 3.8: User's NVM modification procedure for details.

When USER-NVM programming mode is not entered, SPSB100 transits automatically from START-SM to INIT state.

3.6.3.4 *INIT state*

The INIT state is entered:

- After completion of START-SM state and NVM is loaded without error.
- From a DEEP-SLEEP state upon a wake-up event.

- From RECOVERY-2 state when:
  - MCU sent a SPI command DO_POWER_CYCLE (only after SPI_PROTECT_ACCESS has been set) in ACTIVE or RECOVERY-1 state.
  - FBB pin voltage is below $V_{FBB\_UV\_F}$ and VS pin voltage above V_{PORVS_F}.
  - One thermal sensor detected a TSD event, the chip temperature cooled down and the TSD counter does not reached 3.
  - A fault has been detected on a critical regulator output voltage (REGFAIL_GO_REC = 1).
  - 8 successive watchdog trigger faults have been detected
- In case a fault has been detected during the power-up sequence and the power-up retry counter does not reach 3, or LOOP_FOR_EVER bit is set to 1.

In INIT state, when FBB pin voltage rises above $V_{FBB\_OK\_R}$ (the minimum voltage allowing SPSB100 to power-up), SPSB100 executes the digital BIST before initiating a power-up sequence.

3.6.3.5 *ACTIVE state*

ACTIVE state is the state reached after a successful power-up sequence, after the MCU did a read and clear of SPI error flags in RECOVERY-1 state and trig the watchdog in long open window timeout.

In ACTIVE state the SPSB100 can be configured in FULL- or LOW- POWER modes.

In both modes the MCU can configure the watchdog timings and control NFSO1 pin through SPI.

Reactions to fault detection are independent of the POWER modes.

3.6.3.5.1 FULL-POWER mode

FULL-POWER mode is the default mode when entering ACTIVE state from RECOVERY-1 state.

In FULL-POWER mode, all features of SPSB100 are accessible and configurable by SPI registers, in particular MCU can switch OFF some regulators to optimize ECU power consumption.

In FULL-POWER mode, regulator monitors are active and analog and digital BIST can be run on demand by the MCU. Watchdog is running and must be served, except if LOW_SET = 1111. NFSO1 pin is controllable by SPI register.

3.6.3.5.2 LOW-POWER mode

LOW-POWER mode is accessible by SPI in ACTIVE state from FULL-POWER mode. In this mode the SPSB100 power consumption is reduced by:

- Turning OFF low-level hardware monitors.
- Turning OFF the redundant voltage and current bias blocks.
- Turning OFF NVM runtime checks.
- Turning OFF the ADC.
- Analog and digital BIST shall not be executed on demand.

In LOW-POWER mode:

- The watchdog is running and must be served (except if WD_LP_ENA is set at 0), its timing is configurable to further reduce power consumption.
- Central thermal monitoring is active,
- If BUCK 1 and/or BUCK 2 and/or LDO 1 is/are kept ON in its/their low power setting then OV and UV monitoring are active (see the Section 3.8: User's NVM modification procedure for functional safety details).
- Other regulators must be turned OFF before entering in LOW-POWER mode,

MCU can decide to leave this mode by SPI command and return to FULL-POWER mode.

In LOW-POWER mode the VIO must be supplied and SPSB100 offers three possibilities:

- All regulators are turned OFF: in this case VIO must be supplied by an external regulator.
- Only BUCK1 is kept ON in its low-power configuration. BUCK1, or an external regulator, is used to supply VIO.
- BUCK1 and 2 are kept ON in their low-power configuration. BUCK1 or 2, or an external regulator, are used to supply VIO.

3.6.3.5.3 Transitions between FULL-POWER and LOW-POWER modes

Transitions between the two modes are under the responsibility of the MCU.

To transit to LOW-POWER mode the following sequence must be played by the MCU:

- Assert low NFSO1 output (optional).
- Reconfigure watchdog timing (optional).
- Disable the watchdog by setting WD_LP_ENA = 0 (optional).
- Turn off the FCCU monitoring feature.
- Turn OFF regulators BUCK3 and LDO2.
- BUCK1 and/or BUCK2 can be kept ON if one of it is used to supply VIO.
- Configure wake-up sources and IRQ generation (optional).
  Until this step, the SPSB100 is still in FULL-POWER mode, but with tuned settings.
- Set to 1 SPI bit LOW_POWER_SET (only after SPI_PROTECT_ACCESS has been set).

This last action sets SPSB100 in LOW-POWER mode, SPSB100 generates an interruption to confirm the proper entrance in LOW-POWER mode (except if MASK_LP_READY_IRQ is set) and sets status bit LP_READY.

To transit from LOW-POWER to FULL-POWER mode the following sequence must be played by the MCU:

- Clear to 0 SPI bit LOW_POWER_SET (only after SPI_PROTECT_ACCESS has been set).

This first action sets SPSB100 in FULL-POWER mode, SPSB100 generates an interruption to confirm the proper entrance in FULL-POWER mode and sets status bit FP_READY. MCU must wait for this confirmation before continuing, then:

- Clear low power setting of regulator(s) 1 and/or 2 kept ON before its/their load current increases.
- Turn ON other regulator(s) as per application needs.
- Reconfigure watchdog timing to satisfy functional safety requirements (optional).
- Turn ON the FCCU monitoring feature.
- Trigger watchdog during LOW if WD_LP_ENA = 0 (optional).
- Configure wake-up sources and IRQ generation (optional).
- Deassert NFSO1 output.

The low-level hardware monitoring is turned back ON when SPI bit LOW_POWER_SET is cleared. If a hardware fault is detected, SPSB100 transits asynchronously to DEEP-SLEEP state.

LOW_POWER_SET, FP_READY and LP_READY are not automatically cleared in case of transition due to hard fail.

3.6.3.6 *RECOVERY-1 state*

SPSB100 enters in RECOVERY-1 state in two cases:

- From INIT state after the power-up sequence ended successfully.
- From ACTIVE state after a WD trigger issue or a FCCU fault is detected.

When entering the RECOVERY-1 state:

- NFSO1 output is asserted low.
- FCCU monitoring is turned OFF.
- WD starts a LOW, except if LOW_SET = 1111.

In this state all voltage regulators are set according to the power-up sequence settings stored in USER-NVM. If some of the voltage regulators configured in the power-up sequence were switched off in ACTIVE state through the SPI, they are enabled upon entering in RECOVERY-1 state.

The transition from RECOVERY-1 to ACTIVE state is started after the MCU has read and cleared error flags (if any, see the Section 9.8: Status register that must be cleared to enter into active FP mode) and trigged the WD in LOW.

In RECOVERY-1 state, the MCU cannot deassert NFSO1 output. A further WD trigger fault generates a NRST low pulse of at least 4 ms long. See the Section 3.10: Configurable time-out window watchdog for further details. If FCCU is enabled by MCU and a FCCU fault is detected then SPSB100 remains in RECOVERY-1 state and generates a NRST low pulse of at least 6 ms long. See the Section 3.11: FIN1 input for details.

3.6.3.7 *RECOVERY-2 state*

SPSB100 enters in RECOVERY-2 state from ACTIVE state and generates status register bit FSM_TO_REC2 = 0 in case of:

- DO_POWER_CYCLE SPI command (only after SPI_PROTECT_ACCESS has been set).
- The temperature of the central sensor overpassed the TSDC threshold.

- A fault on one of the regulators occurred and its REGFAIL_GO_REC configuration bit is set to 1.
- FBB pin voltage falls below its power down threshold.

SPSB100 enters in RECOVERY-2 state from ACTIVE state and generates status register bit REC2_FROM_DO_POWER_CYCLE = 01 in case of DO_POWER_CYCLE SPI command (only after SPI_PROTECT_ACCESS has been set) REC2_FROM_DO_POWER_CYCLE can be cleared by CLR_REC2_FROM_DO_POWER_CYCLE bit.

SPSB100 enters in RECOVERY-2 state from RECOVERY-1 state and generates status register bit FSM_TO_REC2 = 1 in case of:

- DO_POWER_CYCLE SPI command (only after SPI_PROTECT_ACCESS has been set).
- The temperature of the central sensor overpassed the TSDC threshold.
- A fault on one of the regulators occurred and its REGFAIL_GO_REC configuration bit is set to 1.
- 8 consecutive WD trigger faults.
- FBB pin voltage falls below its power down threshold.

SPSB100 enters in RECOVERY-2 state from RECOVERY-1 state and generates status register bit REC2_FROM_DO_POWER_CYCLE = 1X in case of DO_POWER_CYCLE SPI command (only after SPI_PROTECT_ACCESS has been set) REC2_FROM_DO_POWER_CYCLE can be cleared by CLR_REC2_FROM_DO_POWER_CYCLE bit.

When entering RECOVERY-2 state:

- The NFSO1 output is asserted low.
- FCCU monitoring is turned OFF.
- NRST is asserted low and regulators are turned off according to the programmed power-down sequence.
- In case of a TSD event the TSD counter is incremented and SPSB100 waits that the temperature cools down.

From RECOVERY-2 state SPSB100 transits to DEEP-SLEEP state for unrecoverable fault, or to INIT state to power-up again.

3.6.3.8 *DEEP-SLEEP state - Unrecoverable faults*

SPSB100 enters in DEEP-SLEEP state from ACTIVE-FULL-POWER mode or REC-1 states in case of:

- DO_POWER_DOWN SPI command (only after SPI_PROTECT_ACCESS has been set).
- Power ground lost.

SPSB100 enters in DEEP-SLEEP state from RECOVERY-1 state in case of:

- DO_POWER_DOWN SPI command (only after SPI_PROTECT_ACCESS has been set).
- Power ground lost.
- 15 consecutive WD trigger faults.

SPSB100 enters in DEEP-SLEEP state from RECOVERY-2 state in case of:

- The temperature of one sensor overpassed the TSD threshold and the TSD counter (TSD_CNT_FAIL) reached 3.
- The counter of regulator (REG_FAIL_CNT) fail events reached 3.

When entering the DEEP-SLEEP state from ACTIVE or RECOVERY-1 states:

- The NFSO1 output is asserted low.
- FCCU monitoring is turned OFF.
- NRST is asserted low and regulators are turned off according to the programmed power-down sequence.

SPSB100 remains in a DEEP-SLEEP state until a wake-up event occurs. The design of SPSB100 has been optimized to offer a very-low power consumption while being wake-able by external events.

DEEP-SLEEP state is also entered:

- In case of hardware low-level error, refer to the Section 4.8: HW low-level monitors for details.
- From INIT state in case of safety check error, refer to the Section 4.17: Safety checks for details.
- In case of repetitive power-up fault, refer to the Section 3.6.2.3: Power-up fault management.

3.7 Power-up and power-down sequence

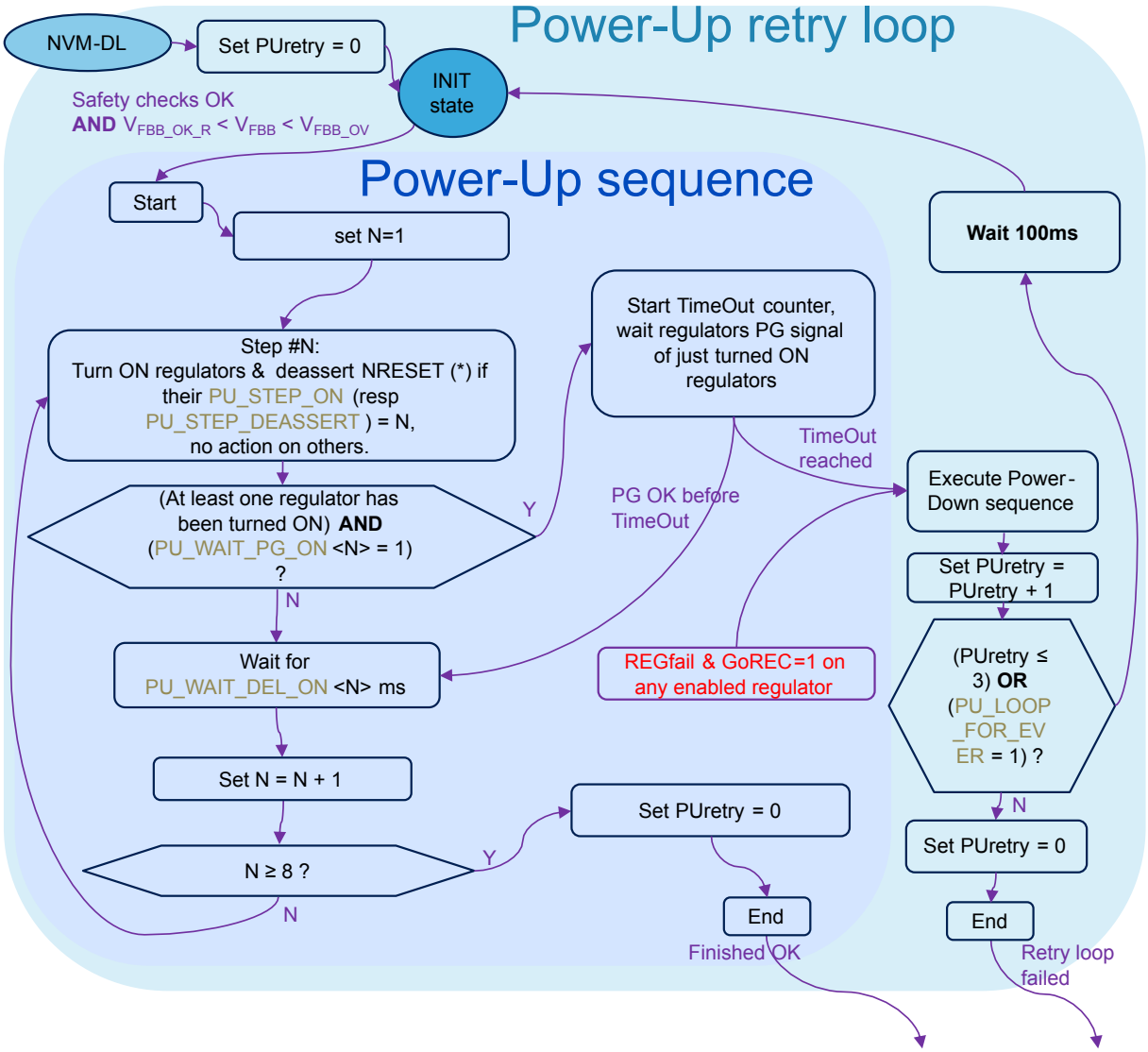
Power-up and power-down sequences turn ON and OFF all the regulators automatically. The sequences are executed by the device state machine as described in the Section 3.6: Functional overview - State machine and are fully programmable through the USER-NVM space to cover a broad range of applications.

The sequences control BUCK1, 2, 3 and LDO1, 2 regulators, together with NRST pin.

3.7.1 Power-up sequence

Power-up sequence is made of 7 steps as described below.

Figure 22. Power-up sequence



Each of BUCK-1, -2, -3, and LDO-1, -2 can be turned ON with USER-NVM bits BUCK1_PU_STEP_ENA, BUCK2_PU_STEP_ENA, BUCK3_PU_STEP_ENA, LDO1_PU_STEP_ENA, LDO2_PU_STEP_ENA at any step from 1 to 7. None, or more than one regulator can be turned ON at a step.

The NRST pin can be deasserted at any step from 1 to 7, with USER-NVM bits NRESET_PU_STEP_DEASSERT independently of regulators setting. Note that the watchdog time-out starts at the step where NRST is deasserted.

After a regulator has been turned ON at step N the sequence offers the possibility to wait for power-good signal with USER-NVM bits PU_WAIT_PG_ENA_X (X equal to steps from 1 to 7):

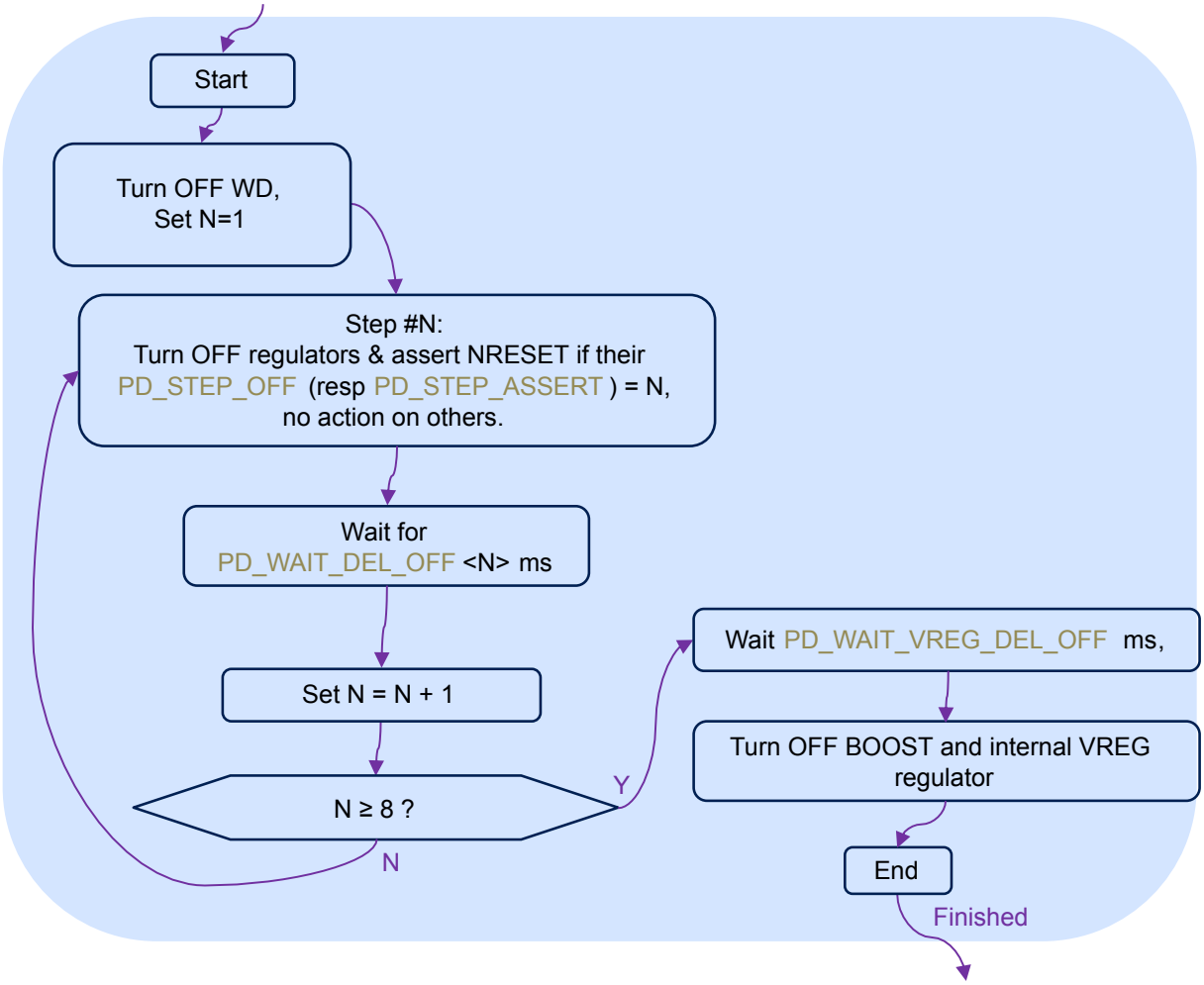
- If this option is selected, then the device waits for the PG signal of all turned ON regulators at step N. A time-out is used to detect a fault: if the time-out expires a power-down sequence is executed and a retry procedure is started as described in the Section 3.6.2.3: Power-up fault management.
- If not, or when PG level is reached, the sequence is paused for a programmable delay with USER-NVM bits PU_WAIT_DEL_ENA_X (X equal to steps from 1 to 7) before proceeding to the next step.

While the sequence executes, any regulator fault is managed as per its REGFAIL_GO_REC setting as described in the Section 3.6.2.5: Regulator faults management.

3.7.2 Power-down sequence

Power-down sequence is made of 7 steps as described below.

Figure 23. Power-down sequence



Each of BUCK-1, -2, -3, and LDO-1, -2 can be turned OFF with USER-NVM bits BUCK1_PD_STEP_OFF, BUCK2_PD_STEP_OFF, BUCK3_PD_STEP_OFF, LDO1_PD_STEP_OFF, LDO2_PD_STEP_OFF at any step from 1 to 7. None, or more than one regulator can be turned OFF at a step.

The NRST pin can be asserted at any step from 1 to 7 with USER-NVM bits NRESET_PD_STEP_ASSERT, independently of regulators setting. Note that the watchdog is stopped before step 1.

After a regulator has been turned OFF at step N the sequence offers the possibility to wait for programmable delay with USER-NVM bits PD_WAIT_DEL_OFF_X (X equal to steps from 1 to 7).

When the sequence ends, an extra delay can be programmed before turning OFF the BOOST and internal VREG with USER-NVM bits PD_WAIT_VREG_DEL_OFF.

3.8 User's NVM modification procedure

SPSB100 integrates nonvolatile memory (NVM) to store ST factory trim data and customer's personalization data. Trim data are stored in ST-NVM space while customer's data are stored in USER-NVM space.

SPSB100 is delivered out of ST factory with default values stored in USER-NVM space. Default value ensures a proper behavior of application with SR6x microcontroller as in configuration 1 shown in the Figure 5, details of default power-up and power-down settings can be found in the Section 3.1.1: System supply configuration 1.

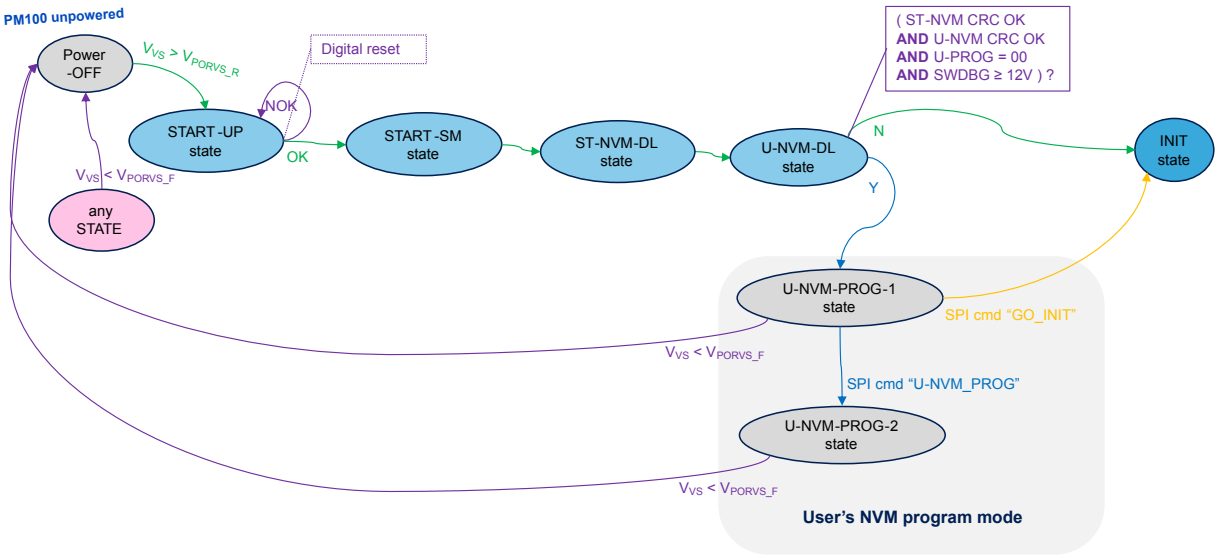
The customer has the possibility to reprogram USER-NVM space only once; or use default values stored by ST.

The U_NVM_RELEASE<15:0> bits in USER-NVM space can be used to store a USER-NVM configuration release. The default value is 0d.

The Figure 24 describes the way to program the NVM. The following color code is used to indicate the offered possibilities:

- Green: SPSB100 starts up with valid data stored in ST-NVM and USER-NVM (USER-NVM previously programmed by ST or by the customer).
- Blue: SPSB100 enters in the USER-NVM programming procedure.
- Orange: USER-NVM emulation feature is used.

Figure 24. Procedure to program the NVM



3.8.1 Starts-up with valid NVM data and NVM faults management

The ST-NVM data are read in ST-NVM-DL state, then USER-NVM data are read in U-NVM_DL state.

If the conditions to enter in USER-NVM modification procedure are not meet the state machine proceeds to INIT state where further safety check will be performed.

3.8.2 USER-NVM emulation

It is possible to emulate the USER-NVM content using the data stored in RAM image.

This can only be done when the USER-NVM has not been programmed by user.

To do it, force the voltage on SWDBG higher than VNVM_EMU_H (20 V max), before plugging the power supply, to enter in USER-NVM modification mode. The modification mode is entered after current ST- and U- NVM data have been read and their CRC checked.

First the state machine enters the USER-NVM-PROG-1 state. In this state the user must supply VIO externally (3.3 or 5.0 V).

At this stage, the SWDBG pin can be released and do not have to be maintained higher than VNVM_EMU_H. Then user can modify USER-NVM RAM through SPI access and the U_NVM SPI registers from DCR10 up to DCR28 can be written.

When completed, the user can set through SPI access the GO_INIT. Doing this, the state machine transits on INIT state.

It is forbidden to enable regulators in the USER-NVM-PROG-1 state.

The USER-NVM emulated values are lost if power supply at VS pin is below V_{PORVS_R}.

During emulation mode the value of U_NVM_CRC0 and U_NVM_CRC1 bits in DCR17 and DCR25 is not considered by the device.

In USER-NVM emulation mode the runtime check of USER-NVM is disabled. For this reason, the USER-NVM emulation mode shall be used for debug purpose only.

3.8.3 USER-NVM programming procedure

The user can emulate the USER-NVM as many times as he wants as far as the USER-NVM is not programmed by the user. Once programmed by user, the USER-NVM cannot be emulated and the device proceeds with valid data stored in USER-NVM.

To program USER-NVM, it is necessary to first emulate the USER-NVM with desired configuration. During this emulation for programming, the user must perform at least write to DCR17 and DCR25 with any value corresponding to its need. This is needed to initiate some bits that will be used to allow proper programming. USER-NVM uses NVM CRC to check that NVM content is correct but during programming, the user does not have to care of this because the correct CRC will be calculated by SPSB100 from emulated data and will be programmed with emulated data.

Then, instead of GO_INIT bit set through SPI access, the user must set the U-NVM_PROG bit (only after SPI_PROTECT_ACCESS has been set). This starts the USER-NVM programming and sets the device in USER-NVM-PROG-2 state.

When the USER-NVM programming is completed, the status bit NVM_PROG_DONE is set. The user can read this status bit through SPI access. When this bit is set, the user can read the NVM_PROG_OK status bit to verify that the USER-NVM programming has completed correctly because the USER-NVM programming is followed by the USER-NVM verification.

If the USER-NVM programming has failed and the NVM_PROG_OK status bit is low when the NVM_PROG_DONE status bit is set, the user may request a new programming by resetting the U-NVM_PROG control bit (only after SPI_PROTECT_ACCESS has been set) then setting again this bit. This operation can be done 2 times, so there is a maximum programming of 3 times. If at the end of 3 USER_NVM programming request, NVM_PROG_OK is still low when NVM_PROG_DONE is high, the chip cannot anymore be programmed and cannot start correctly. In this case, any new programming request is ignored.

After valid USER-NVM programming procedure the U_NVM SPI registers from DCR10 to DRC28 can be only readable.

3.8.4 Loading USER-NVM data in RAM image

To program the USER-NVM it is necessary to load the data (CRC included) in a dedicated portion of the RAM. It is automatically done by state machine.

3.9 Wake-up inputs: IGN and WU

Both inputs can be configured as wake-up sources (through IGN_ENA and WU_ENA control bits). In particular, the input IGN can be used as a wake-up source connected to ignition (KL15) via a resistor.

The voltage can be also read back via SPI through a 10-bit ADC monitoring (IGN[9..0] bits, in addition to WU[9..0] ones). This can be achieved only if WU_CONFIG bit and IGN_CONFIG bit are set to ”1”.

Each wake-up input is sensitive to any level transition (positive and negative edge) and can be configured for static or cyclic monitoring of the input voltage level by suitable setting of bits WU_FILT and IGN_FILT which allows to choose the monitoring among static or cyclic with timer. When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.

For static contact monitoring, a filter time of t_{WU_stat}, t_{IGN_stat} is implemented. The filter is started when the input voltage crosses the specified threshold V_{wuthp}, V_{IGNthp} (both thresholds are linked to V_{FBB} level). Wake-up status bit (WU_WAKE and IGN_WAKE bits) is set only if this threshold is passed for more than t_{WU_stat}, t_{IGN_stat}.

Cyclic contact monitoring allows instead periodical (not threshold dependent) activation of the wake-up input to read the status of the external contact. The periodical activation is driven by timer whose settings (on-time and period) can be configured through T1_PER[2..0] and T1_ENA[2..0] bits.

The input signal is filtered with a filter time of t_{WU_cyc} (t_{IGN_cyc}) after a delay (80% of the configured timer on-time). A wake-up will be processed if the status has changed versus the previous cycle, therefore wake-up status WU_WAKE and IGN_WAKE bits are set only if the status during consecutive on-time is different, after configured delay and $t_{WU\_cyc.}$ (t_{IGN_cyc}). This can be done only if WU_CONFIG and IGN_CONFIG are configured as wake-up inputs.

In active low power or DEEP-SLEEP modes the inputs WU and IGN are configurable with an internal pull-up or pull-down current source according to the setup WU_PU and IGN_PU SPI bits.

In active full power mode the inputs have an internal pull-down resistor (R_{WU_act}) and the inputs status can be read by WU_STATE and IGN_STATE. This can be done only if WU_CONFIG and IGN_CONFIG are configured as wake-up inputs and if WU_ENA and IGN_ENA are set high.

The output OUT_HS can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the wake-up input.

If WU_ENA = 1 and WU_CONFIG = 1, the wake up capability and the voltage measurement through ADC are both activated on WU pin.

If IGN_ENA = 1 and IGN_CONFIG = 1, the wake up capability and the voltage measurement through ADC are both activated on IGN pin.

3.10 Configurable time-out window watchdog

During normal operation, the watchdog monitors the microcontroller within a programmable trigger cycle.

After the power-up sequence, the watchdog starts with a long open window t_{LW}. The watchdog allows the microcontroller to run its own setup and then to start the window watchdog by setting WD_TRIG=1.

Long open window t_{LW} is configurable by USER-NVM through the bits LOW_SET [3..0].

Subsequently, the microcontroller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area $T_{swx.}$. The trigger time is configurable by SPI.

A correct watchdog trigger signal will immediately start the next cycle.

A watchdog trig will not take into account if NRST pin is low.

If LOW_SET [3..0] is set at “1111”, the long open window is set in infinite duration. In this case, if the application does not require a watchdog, the microcontroller must not trig the watchdog. So, the device will transit from REC-1 to active full power after a read and clear of error flags. If the watchdog is triggered even with LOW_SET [3..0] set to “1111”, the watchdog starts with the default window and then has to be served. Note that in the case of LOW_SET = 1111, so in the case of the watchdog service is disabled, it must be considered in the safety analysis based on FIT calculation, as described in the safety manual.

The watchdog trigger time can be configured by setting the WD_TIME [3..0] bits (only after SPI_PROTECT_ACCESS has been set) and the default value is 0001 (window 2). The change of watchdog window timing through WD_TIME in SPI registers cannot be done when the watchdog is in long open window counting.

The microcontroller can read the LOW_STATUS bit to know if the watchdog is in long open window phase (when LOW_STATUS is high) or in normal window (when LOW_STATUS is low). When in long open window phase, the LOW_STATUS bit is high even if the watchdog is in infinite long open window. When not in infinite long open window, if FSM is in ACTIVE_HP or ACTIVE_LP state, the LOW_STATUS is low and watchdog counts in normal window. When LOW_STATUS is high, the current watchdog LOW is given by LOW_SET[3:0]. When LOW_STATUS is low, the current watchdog window is given by WD_TIME_STATUS[3:0]. During REC-1 FSM state, WD_TIME[3:0] cannot be written because the watchdog is counting in long open window.

In the case of WD_FAIL or FCCU_FAIL occurs the watchdog starts in long open window when NRST rises. In this case, the watchdog trig bit is automatically cleared. So, the microcontroller can trig the watchdog with a WD_TRIG bit high.

The new value of WD_TIME is loaded in the watchdog module on the next trig event after the SPI configuration. The following watchdog cycle uses the new programmed value.

This means that when a watchdog is running on a current window, to change the window, the microcontroller must:

- Write in WD_TIME(3-0) the new watchdog window.
- Trig the watchdog in the current window.

Doing this, the watchdog restarts using the new window.

It is possible to disable the watchdog in ACTIVE - LOW-POWER mode only through the WD_LP_ENA bit set at “0” (only after SPI_PROTECT_ACCESS has been set). If WD_LP_ENA is set high during ACTIVE - LOW-POWER mode, the watchdog will stay disabled and will restart with a long open window after the transition Active-LP to Active-FP.

Fault conditions can be detected through the following bits:

- The status bit WD_ENA_ECHO indicates that the watchdog is running when high.

- The status bit WD_ENA_ECHO_ERROR indicates a watchdog echo error and generates an IRQ. This error can be masked by MASK_WD_ENA_ECHO_ERROR_IRQ.
- In case of watchdog fail a flag WDFAIL is set and the watchdog fail counter WDFAIL_CNT is incremented up to 15 consecutive watchdog trig faults. After 15 consecutive watchdog trig faults, the bit FORCED_SLEEP_WDFAIL is set and the device will reach the DEEP-SLEEP state.
- WDFAIL_CNT can be reset by CLR_WDFAIL_CNT bit.
- The microcontroller can know the current state of watchdog by reading WD_TIMER_STATE(1-0) WD_TIMER_STATE = 00, WD trig is too early widow trig, WD_TIMER_STATE = 01, WD trig is in valid window trig.

3.11 FIN1 input

SPSB100 integrates an MCU fault monitoring called FCCU. FCCU block can be configured to detect error reported by the MCU through FIN1 input. Two error reporting protocols are available: static and dynamic protocols.

3.11.1 Static protocol

In this protocol MCU signals its own errors to SPSB100 by driving FIN1 input pin at low or high level.

MCU shall configure the SPSB100 FCCU block as the following:

- FCCU_PROTOCOL shall be reset to 0.
- FCCU_STATIC_ERROR shall be reset to 0 if MCU signals error driving FIN1 low, or set to 1 if MCU signals error driving FIN1 high.
- MCU shall drive FIN1.
- FCCU_ENA shall be set at 1 to enable the monitoring feature (only after SPI_PROTECT_ACCESS has been set).

3.11.2 Dynamic protocol

In this protocol MCU signals its own error to SPSB100 by increasing the period, or half period, of the toggling signal sent to FIN1 input.

The FCCU block shall be programmed to monitor half period of the toggling signal received on FIN1. The FCCU block is made of a counter clocked by a 400 kHz clock derived from the main oscillator. The counter is reset at each transition on FIN1 input, if the counter overflows then an error is signaled.

The counter overflow threshold is programmed on FCCU_COUNTER<12:0> (only after SPI_PROTECT_ACCESS has been set). The oscillator accuracy shall be considered to calculate the value of this threshold, the following formula can be used:

FCCU_COUNTER > FIN1_half_period * (400 kHz + main oscillator accuracy)

Example: with an MCU toggling signal at 4 882.8 Hz (min) with 50% of duty cycle, and 20% accuracy of SPSB100 oscillator.

FCCU_COUNTER > (204.8/2) µs * (400 kHz * 1.2) = 49.15

Gives FCCU_COUNTER = 50 at minimum.

MCU shall configure the SPSB100 FCCU block as the following:

- FCCU_PROTOCOL shall be set to 1.
- FCCU_STATIC_ERROR can be used to configure an internal pull-up (set to 1) or an internal pull-down (reset to 0) on FIN1 input.
- FCCU_COUNTER shall be loaded to the overflow threshold (only after SPI_PROTECT_ACCESS has been set).
- MCU shall drive FIN1 with the proper toggling signal.
- FCCU_ENA shall be set at 1 to enable the monitoring feature (only after SPI_PROTECT_ACCESS has been set).

Each time a transition is detected on FIN1 input the register FCCU_LAST_STABLE<12:0> is loaded with the last value of the FCCU counter. MCU can read back this value through SPI.

3.11.3 Reaction on error

When an error is detected by the MCU fault monitoring, the NRST pin is asserted low, the status bit FCCUFAIL is set, the state machine reacts as described in the Section 3.6.2.2: Watchdog trig and FCCU monitor faults management. The live status bit FIN1_STATE shows the current state of FIN1 input.

To properly restart FCCU block after a FCCUFAIL detection, MCU has to write FCCU_ENA = 0, clear the FCCUFAIL flag and re-enable the monitoring by setting FCCU_ENA = 1.

The live bit FCCU_ENA_STATUS reflects the state of the FCCU block.

3.12 High-side output OUT_HS

In active, FULL-POWER or LOW-POWER modes, and in DEEP_SLEEP states the high side driver output OUT_HS can be configured for supplying external loads or contacts.

The high side output can be either controlled:

- Permanently ON (OUTHS_[1..0] = 01)
- Permanently OFF (OUTHS_[1..0] = 00)
- Through an internal timer (OUTHS_[1..0] = 1x)

In timer mode configuration (when TIMER_ENA = 1) the activation period can be configured through the bits T1_PER [2..0] in the following range {10, 20, 50,100, 200, 500, 1000, 2000 ms}.

On-time is configurable through bits T1_ENA[1..0] in the following range {0.1, 0.3, 1, 10, 20 ms}.

In case the wake-up inputs WU and IGN are configured in cyclic sense mode(WU_FILT = 1, IGN_FILT = 1)), the capture of their input state is synchronized with the high-side timer mode:

- A switched ON delay time $t_{DON\_OUT\_HS}$ is applied after the high-side is turned ON.
- A switched OFF delay time $t_{DOFF\_OUT\_HS}$ is applied after the high-side is turned OFF.
- A fixed filter time of t_{WU_cyc} is applied after blanking time has elapsed before refreshing the WU_WAKE or IGN_WAKE.
- In case of status change detection between the previous and the new captured state, the status bits WU_WAKE and IGN_WAKE will be set in the status register. Depending on the dedicated settings applied on each wake-up input, wake-up detection could wake-up the SPSB100 and/or generate an interrupt signal on the IRQ pin.

In case of overcurrent, detection is done by OUTHS_OC bit, OUTHS driver is switched off after filter time toc_out_hs and an IRQ is generated except if MASK_OUTHS_IRQ is set.

After an OC detection, OUTHS can be re-enabled by clearing the status bit OUTHS_OC.

In case of open load, detection is done by OUTHS_OL bit, an IRQ is generated except if MASK_OUTHS_IRQ is set.

The live bit OUTHS_ENA_STATUS reflects the state of OUTHS output.

Note: The high-side driver OUT_HS is intended to drive resistive loads only. Therefore, only a limited energy (E < 1 mJ) can be dissipated by the internal ESD-diodes in freewheeling condition. For inductive loads (L > 100 µH) an external freewheeling diode connected between GND and the OUT_HS pin is required.

3.13 Fail-safe output - NFSO1

NFSO1 is asserted low when a fault event is detected. The objective of this pin is to drive an electrical safe circuitry independent from the MCU to deactivate the whole system and set the ECU in a protected and known state.

The NFSO1 pin is an open drain output. An external pull-up circuitry must be connected to VIO or VBAT.

The NFSO1 pin is controlled by an asynchronous OR of:

- Asynchronous supervisor of internal voltage reference. When a difference between the main and monitoring voltage reference is detected the NFSO1 pin is asserted low.
- Synchronous monitor of main oscillator. When an oscillator frequency drift or a stuck at is detected the NFSO1 pin is asserted low.
- When a watchdog or FCCU fail occurs the NFSO1 pin is asserted low.
- The SPI control bit NFSO_ASSERT_LOW (only after SPI_PROTECT_ACCESS has been set):
  - NFSO_ASSERT_LOW = 1: pin is asserted low.
  - NFSO_ASSERT_LOW = 0: pin is in high impedance. Its level is defined by external pull-up.

To avoid extra current drain consumption in deep sleep due to the external pull up on NFSO1 pin, the default state can be selected by user-NVM bit NFSO_STATE_IN_DEEP_SLEEP. When, NFSO_STATE_IN_DEEP_SLEEP = 0, the NFSO1 pin is asserted (level low), instead when NFSO_STATE_IN_DEEP_SLEEP = 1, the NFSO1 in de-asserted (level high) in DEEP-SLEEP.

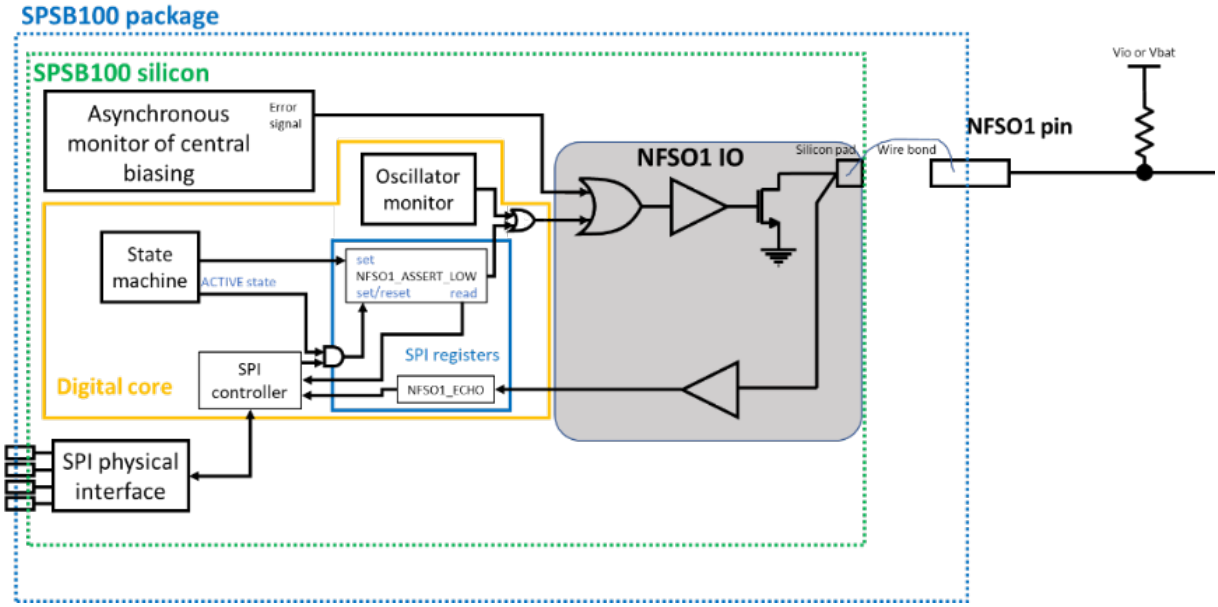
Note: NFSO1 state is HIGH, instead of LOW after a wake-up from DEEP-SLEEP when NFSO_STATE_IN_DEEP_SLEEP = 1. So, it is suggested, to set after a wake-up from DEEP SLEEP the NFSO_ASSERT_LOW = "1" then to set NFSO_ASSERT_LOW = "0". NFSO1 pin level is defined by external pull-up.

The state machine can only set NFSO_ASSERT_LOW to 1, while the MCU can set, reset and read it, making NFSO1 pin fully controllable by the MCU in ACTIVE state.

The SPI bit NFSO1_ECHO is sensing the NFSO1 state on its silicon pad:

- NFSO1_ECHO = 0: NFSO1 output pad is asserted low.
- NFSO1_ECHO = 1: the NFSO1 output pad is pulled-up by external circuitry.

Figure 25. NFSO1 implementation details



After a battery plug, or after each power-up sequence, or during a power-down sequence, or in INIT, REC-1, REC-2, DEEP-SLEEP states the NFSO1 pin is asserted low. This is insured by the state machine that sets the SPI bit NFSO_ASSERT_LOW to 1. In ACTIVE state the MCU can decide to release the NFSO1 pin through the SPI when the application is ready to start.

Figure 26. **NFSO1 output pin behavior at battery plug**

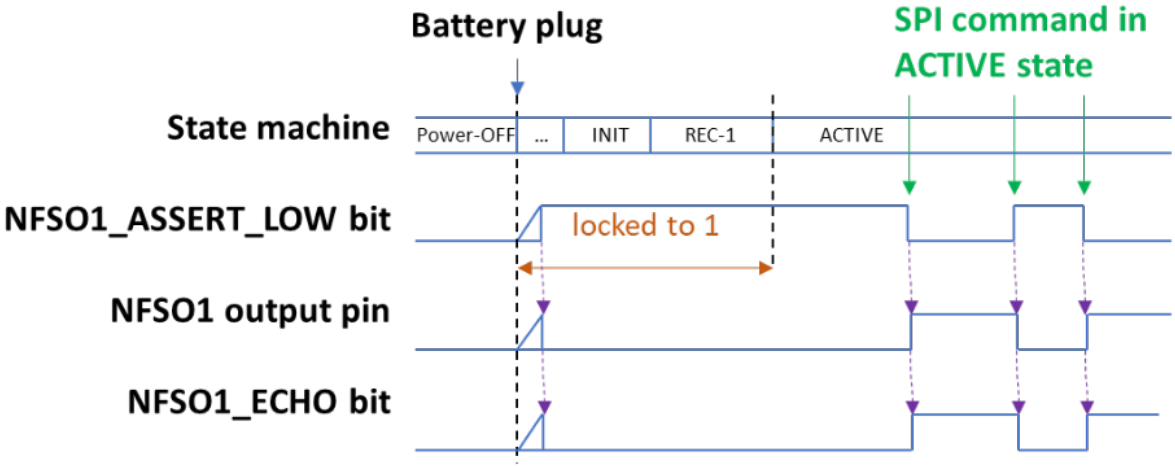
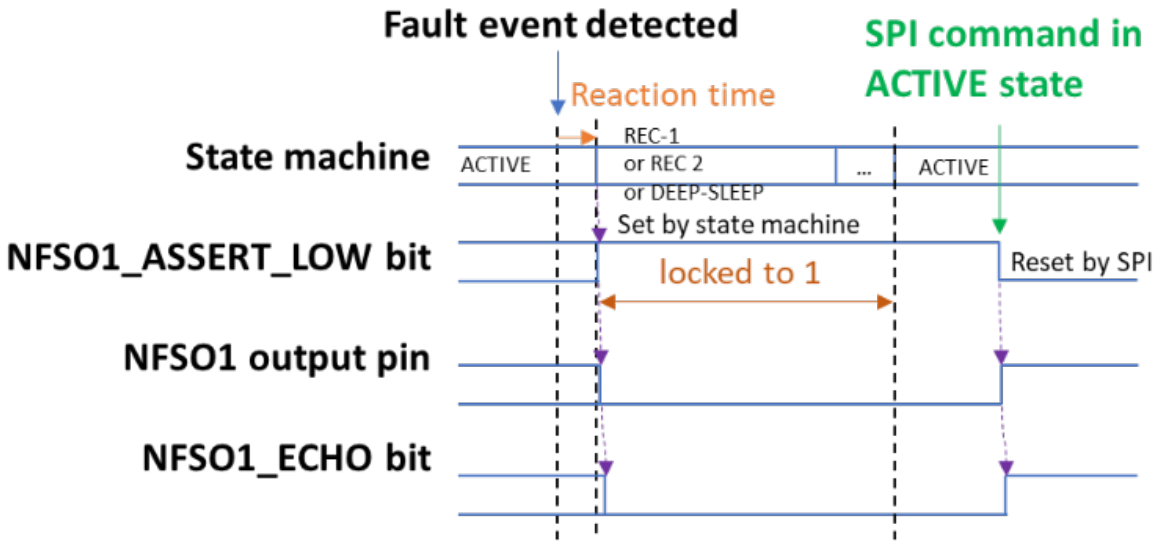


Figure 27. **NFSO1 output pin behavior after a failure is detected**



3.14 Interrupt - IRQ

IRQ pin is an open-drain with an internal pull-up for the echo-generation. An external pull-up to VIO level close to MCU is strongly recommended. IRQ pin is set low if any of the following events is happening, as showed in the table below.

Table 8. **IRQ events**

SPI status bit name	IRQ generated	IRQ SPI mask name
ABIST_COMPLETE	Y	Not maskable
LBIST_COMPLETE	Y	Not maskable
BOOST_IN_LP	Y	MASK_BOOST_IN_LP_IRQ
BOOST_VDSMON_ERROR	Y	MASK_BOOST_VDSMON_IRQ
BUCK1_OC	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_OC_IRQ
BUCK1_OV	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_IRQ
BUCK1_FB	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_IRQ

SPI status bit name	IRQ generated	IRQ SPI mask name
BUCK1_PG_OK	Y	MASK_BUCK1_PG_IRQ
BUCK1_PG_TIMEOUT	Y	MASK_BUCK1_PG_TIMEOUT_IRQ
BUCK1_UV	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_IRQ
BUCK2_OC	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_OC_IRQ
BUCK2_OV	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_IRQ
BUCK2_FB	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_IRQ
BUCK2_PG_OK	Y	MASK_BUCK2_PG_IRQ
BUCK2_PG_TIMEOUT	Y	MASK_BUCK2_PG_TIMEOUT_IRQ
BUCK2_UV	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_IRQ
BUCK3_OC	Y if BUCK3_REGFAIL_GO_REC = 0	MASK_BUCK3_OC_IRQ
BUCK3_OV	Y if BUCK3_REGFAIL_GO_REC = 0	MASK_BUCK3_IRQ
BUCK3_PG_OK	Y	MASK_BUCK3_PG_IRQ
BUCK3_PG_TIMEOUT	Y	MASK_BUCK3_PG_TIMEOUT_IRQ
BUCK3_UV	Y if BUCK3_REGFAIL_GO_REC = 0	MASK_BUCK3_IRQ
BUCK1_INT_FAIL	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_IRQ
BUCK2_INT_FAIL	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_IRQ
BUCK3_INT_FAIL	Y if BUCK3_REGFAIL_GO_REC = 0	MASK_BUCK3_IRQ
BYPASS_VDSMON_ERROR	Y	MASK_BYPASS_VDSMON_IRQ
NFSO1_ECHO_ERROR	Y	MASK_NFSO1_ECHO_ERROR_IRQ
FBB_OV	Y	MASK_FBB_OV_IRQ
FBB_OV_EW	Y	MASK_FBB_OV_EW_IRQ
FBB_UV	Y	MASK_FBB_UV_IRQ
FBB_UV_EW	Y	MASK_FBB_UV_EW_IRQ
FCCU_ENA_ECHO_ERROR	Y	MASK_FCCU_ENA_ECHO_ERROR_IRQ
IRQ_REQUEST	Y	Not maskable
LDO1_PG_OK	Y	MASK_LDO1_PG_IRQ
LDO1_PG_TIMEOUT	Y	MASK_LDO1_PG_TIMEOUT_IRQ
LDO1_UV	Y	MASK_LDO1_IRQ
LDO2_OV	Y if LDO2_REGFAIL_GO_REC = 0	MASK_LDO2_IRQ
LDO2_PG_OK	Y	MASK_LDO2_PG_IRQ
LDO2_PG_TIMEOUT	Y	MASK_LDO2_PG_TIMEOUT_IRQ
LDO2_UV	Y if LDO2_REGFAIL_GO_REC = 0	MASK_LDO2_IRQ
NVM_PROG_DONE	Y	Not maskable
OUTHS_OC	Y	MASK_OUTHS_IRQ
OUTHS_OL	Y	MASK_OUTHS_IRQ
SPI_ALL_WAKEUP_DISABLE	Y	MASK_SPI_ERROR_IRQ
SPI_REG_COMP_ERROR	Y	MASK_SPI_ERROR_IRQ
SPI_CLK_CNT	Y	MASK_SPI_ERROR_IRQ
SPI_CRC_ERR	Y	MASK_SPI_ERROR_IRQ
SPI_CSN_TIMEOUT	Y	MASK_SPI_ERROR_IRQ
SPI_LBISTED	Y	MASK_SPI_ERROR_IRQ

SPI status bit name	IRQ generated	IRQ SPI mask name
SPI_SDI_STUCK_HIGH	Y	MASK_SPI_ERROR_IRQ
SPI_SDI_STUCK_LOW	Y	MASK_SPI_ERROR_IRQ
SPI_STATUS_WRT	Y	MASK_SPI_ERROR_IRQ
SPI_UNDEF_ADD	Y	MASK_SPI_ERROR_IRQ
VS_UV_EW	Y	MASK_VS_EW_IRQ
TSD_CL1	Y if BUCK1_REGFAIL_GO_REC = 0	Not maskable
TSD_CL2	Y if BUCK2_REGFAIL_GO_REC = 0	Not maskable
TSD_CL3	Y if BUCK3_REGFAIL_GO_REC = 0	Not maskable
TSD_CL4	Y if LDO2_REGFAIL_GO_REC = 0	Not maskable
TW_CL0	Y	MASK_CL0_TW_IRQ
TW_CL1	Y	MASK_CL1_TW_IRQ
TW_CL2	Y	MASK_CL2_TW_IRQ
TW_CL3	Y	MASK_CL3_TW_IRQ
TW_CL4	Y	MASK_CL4_TW_IRQ
IGN_WAKE	Y	Not IGN_WAKEUP_ENA
TIMER_WAKE	Y	Not TIMER_WAKE_ENA
WU_WAKE	Y	Not WU_WAKEUP_ENA
SWDBG_VIO	Y	MASK_SWDBG_VIO_IRQ
ABIST_COMPLETE	Y	Not maskable
BOOST_IN_LP	Y	MASK_BOOST_IN_LP_IRQ
BOOST_VDSMON_ERROR	Y	MASK_BOOST_VDSMON_IRQ
BUCK1_FB	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_IRQ
BUCK1_INT_FAIL	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_IRQ
BUCK1_OC	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_OC_IRQ
BUCK1_OV	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_IRQ
BUCK1_PG_OK	Y	MASK_BUCK1_PG_IRQ
BUCK1_PG_TIMEOUT	Y	MASK_BUCK1_PG_TIMEOUT_IRQ
BUCK1_UV	Y if BUCK1_REGFAIL_GO_REC = 0	MASK_BUCK1_IRQ
BUCK2_FB	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_IRQ
BUCK2_INT_FAIL	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_IRQ
BUCK2_OC	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_OC_IRQ
BUCK2_OV	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_IRQ
BUCK2_PG_OK	Y	MASK_BUCK2_PG_IRQ
BUCK2_PG_TIMEOUT	Y	MASK_BUCK2_PG_TIMEOUT_IRQ
BUCK2_UV	Y if BUCK2_REGFAIL_GO_REC = 0	MASK_BUCK2_IRQ
BUCK3_INT_FAIL	Y if BUCK3_REGFAIL_GO_REC = 0	MASK_BUCK3_IRQ
BUCK3_OC	Y if BUCK3_REGFAIL_GO_REC = 0	MASK_BUCK3_OC_IRQ
BUCK3_OV	Y if BUCK3_REGFAIL_GO_REC = 0	MASK_BUCK3_IRQ
BUCK3_PG_OK	Y	MASK_BUCK3_PG_IRQ
BUCK3_PG_TIMEOUT	Y	MASK_BUCK3_PG_TIMEOUT_IRQ
BUCK3_UV	Y if BUCK3_REGFAIL_GO_REC = 0	MASK_BUCK3_IRQ

SPI status bit name	IRQ generated	IRQ SPI mask name
BYPASS_VDSMON_ERROR	Y	MASK_BYPASS_VDSMON_IRQ
FBB_OV	Y	MASK_FBB_OV_IRQ
FBB_OV_EW	Y	MASK_FBB_OV_EW_IRQ
FBB_UV	Y	MASK_FBB_UV_IRQ
FBB_UV_EW	Y	MASK_FBB_UV_EW_IRQ
FCCU_ENA_ECHO_ERROR	Y	MASK_FCCU_ENA_ECHO_ERROR_IRQ
IGN_WAKE	Y	Not IGN_ENA
IRQ_REQUEST	Y	Not maskable
LBIST_COMPLETE	Y	Not maskable
LDO1_PG_OK	Y	MASK_LDO1_PG_IRQ
LDO1_PG_TIMEOUT	Y	MASK_LDO1_PG_TIMEOUT_IRQ
LDO1_UV	Y	MASK_LDO1_IRQ
LDO2_OV	Y	MASK_LDO2_IRQ
LDO2_PG_OK	Y	MASK_LDO2_PG_IRQ
LDO2_PG_TIMEOUT	Y	MASK_LDO2_PG_TIMEOUT_IRQ
LDO2_UV	Y	MASK_LDO2_IRQ
NFSO1_ECHO_ERROR	Y	MASK_NFSO1_ECHO_ERROR_IRQ
NVM_PROG_DONE	Y	Not maskable
OUTHS_OC	Y	MASK_OUTHS_IRQ
OUTHS_OL	Y	MASK_OUTHS_IRQ
SPI_ALL_WAKEUP_DISABLE	Y	MASK_SPI_ERROR_IRQ
SPI_CLK_CNT	Y	MASK_SPI_ERROR_IRQ
SPI_CRC_ERR	Y	MASK_SPI_ERROR_IRQ
SPI_CSN_TIMEOUT	Y	MASK_SPI_ERROR_IRQ
SPI_LBISTED	Y	MASK_SPI_ERROR_IRQ
SPI_REG_COMP_ERROR	Y	MASK_SPI_ERROR_IRQ
SPI_SDI_STUCK_HIGH	Y	MASK_SPI_ERROR_IRQ
SPI_SDI_STUCK_LOW	Y	MASK_SPI_ERROR_IRQ
SPI_STATUS_WRT	Y	MASK_SPI_ERROR_IRQ
SPI_UNDEF_ADD	Y	MASK_SPI_ERROR_IRQ
SWDBG_VIO	Y	MASK_SWDBG_VIO_IRQ
TIMER_WAKE	Y	Not TIMER_WAKE_ENA
TSD_CL1	Y if BUCK1_REGFAIL_GO_REC = 0	Not maskable
TSD_CL2	Y if BUCK2_REGFAIL_GO_REC = 0	Not maskable
TSD_CL3	Y if BUCK3_REGFAIL_GO_REC = 0	Not maskable
TSD_CL4	Y if LDO2_REGFAIL_GO_REC = 0	Not maskable
TW_CL0	Y	MASK_CL0_TW_IRQ
TW_CL1	Y	MASK_CL1_TW_IRQ
TW_CL2	Y	MASK_CL2_TW_IRQ
TW_CL3	Y	MASK_CL3_TW_IRQ
TW_CL4	Y	MASK_CL4_TW_IRQ

SPI status bit name	IRQ generated	IRQ SPI mask name
VS_UV_EW	Y	MASK_VS_EW_IRQ
WD_ENA_ECHO_ERROR	Y	MASK_WD_ENA_ECHO_ERROR_IRQ
WU_WAKE	Y	Not WU_ENA
FP_READY	Y	Not maskable
LBIST_STOPPED	-	Not maskable
LP_READY	Y	MASK_LP_READY_IRQ

Interrupt is a NOR of all information except if some masks are set. A read and clear of all setted flags is needed to allow the IRQ pin to be set high.

Interrupt output pin indicates:

- Warnings and errors which must be reported to the MCU.
- Confirmation of a requested action from the MCU.

3.15 Reset output - NRST

The NRST pin is an open-drain with an internal pull-up for the echo-generation. An external pull-up to VIO level close to MCU is strongly recommended.

The aim of NRST output is to drive the MCU NRST input pin.

The NRST is released after a proper power-up sequence before reaching the RECOVERY-1 state, and is asserted low after t_{NRST_rt}, in case of error as described in the Section 3.6.3: States and transitions description.

3.16 10-bit ADC

In ACTIVE – FULL-POWER mode and RECOVERY-1 state the voltage signals VS, FBB, WU, IGN, TH_CL0, TH_CL1, TH_CL2, TH_CL3, and TH_CL4 are read out sequentially. Related bit names in the status register are VS[0..9], FBB[0..9], WU[0..9], IGN[0..9], TEMP_CL0[0..9], TEMP_CL1[0..9], TEMP_CL2[0..9], TEMP_CL3[0..9] and TEMP_CL4[0..9].

The voltage signals are multiplexed to an ADC. The ADC is realized as a 10-Bit SAR. Each channel is converted with a conversion time tcon, therefore an update of the ADC value is available every tcon * 13.

The voltage measurement on V_S, FBB, WU and IGN can be calculated from the binary coded register value using the following formula:

Decimal code = (V_{IN}/LSB_V) – 1

The temperature measurement on TEMP_CL0-4 can be calculated from the binary coded register value using the following formula:

Decimal code = ((355 – T_j)/LSB_T) – 1

In case of WU, or IGN, is directly connected to battery line, the input must be protected by a series resistance of typical 1 kΩ to sustain reverse battery condition.

3.17 SW-Debug mode

The SW-Debug mode is intended for software development. In SW-Debug mode SPSB100 is fully operational except that the watchdog is not started and consequently does not monitor proper watchdog trig.

To set the device in SW-DEBUG mode, the SWDBG pin must be shorted to VIO before a power-up sequence (cold start or wake up from DEEP-SLEEP). With such setting the device executes the power-up sequence and, instead of reaching RECOVERY-1 state, the device transits to SWDBG state.

In SWDBG state the timeout t_{SWDBG_TO} is launched.

The timeout is used to prevent the system from being stuck in SWDBG state:

If the timeout expires, then SW-Debug mode entry is canceled. The device transits to RECOVERY-1 state and starts the watchdog with a long open window. Status register bit SWDBG_VIO is set, an IRQ (maskable by MASK_SWDBG_VIO_IRQ) is generated to indicate that SWDBG pin is shorted to VIO.

If the short to VIO is removed before timeout expiration then the device transits to RECOVERY-1 state, the watchdog is disabled. To transit to ACTIVE-FULL-POWER mode the software must clear error flags and set WD_TRIG, this is the unique access to WD_TRIG that the software must handle in SW-Debug mode.

Any further voltage attachment to SWDBG pin at VIO is ignored, until the next SPSB100 power-up sequence. This helps to protect unwanted SW-Debug mode entry and well enables possible share of this pin with other functions.

Once the SW-Debug mode is established, it persists until terminated via SPI command SWDBG_EXIT or until the next power on reset (battery unplug and replug). If terminated by SPI command the watchdog starts immediately with a long open window.

The SW-Debug mode status can be monitored by the SPI status register WD_ENA_ECHO = 0.

The state of the SWDBG pin can be monitored by the live bit SWDBG_STATE.

In final application, it is possible to detect the hardware fault “SWDBG shorted to VIO” using the following procedure.

After the MCU boot-up, the software shall read the SPSB100 state. The expected state is REC-1. If the SWDBG pin is faulty shorted to VIO then the device reaches SWDBG state.

In such a case it is possible to kill the timeout by setting the KILL_SWDBG_TIMEOUT control bit: the device transits to REC-1 state and the watchdog is enabled disregarding the SWDBG pin voltage.

This feature is useful to prevent an increase of start-up time when the hardware fault “SWDBG shorted to VIO” is present.

3.18 VREG

The VREG is dedicated to generate the bootstrap voltage for the BUCKs in active and REC-1 states. It is supplied by FBB pin in active-full power and by FB1 in active-low power.

VREG has a 3.3 V output and 150 mA current capability.

VREG cannot be used to supply external blocks.

The voltage regulator is protected against undervoltage: if the VREG output voltage is going below V_{VREG_UV} for a delay higher than t_{VREG_UV}, flag INT_REG_UV is set and the device will execute a power down sequence to enter in DEEP-SLEEP state.

The voltage regulator is protected against overvoltage: if the VREG output voltage is going above V_{VREG_OV} for a delay higher than t_{VREG_OV}, flag INT_REG_OV is set and the device will execute a power down sequence to enter in DEEP-SLEEP state.

The voltage regulator is protected against a short to ground during INIT state. If the VREG output voltage is not able to reach V_{VREG_UV} after t_{VREG_stup}, flag INT_REG_UV is set and the device will make a transition to DEEP-SLEEP state.

Current limitation I_{VREG_CCmax} of the regulator ensures fast charge of external decoupling capacitor.

The output voltage is stable for ceramic load capacitors, see C_{VREG} in the Section 7.22: VREG voltage regulator.

Warning temperature detection is managed by a local thermal sensor (flag is TW_CL0).

Warning temperature detection generates an IRQ except if MASK_CL0_TW_IRQ is set.

In case the device temperature exceeds the TSD_CL0 threshold, the device executes a power down sequence before entering in REC-2 state.

4 Protection, diagnosis and monitoring signals

4.1 Supply monitoring

4.1.1 VS pin

The battery line is monitored through a VS pin.

The VS input voltage is monitored through analog comparators and the ADC:

- VS input voltage can be read back by SPI access, by VS[9..0].
- The ADC is used to detect under voltage early warnings (flagged by VS_UV_EW bit).

The thresholds are programmable by SPI (VS_UV_EW_TH[4..0]) and an interrupt is issued when thresholds are crossed except if MASK_VS_EW_IRQ is set.

4.1.2 FBB pin

The FBB input voltage is monitored through analog comparators and the ADC:

- Analog comparator is used to detect over and undervoltages. The reaction to a FBB voltage fault is described in the Section 3.6.2.6: FBB voltage drop management.
- An analog comparator is used to detect over voltage. The flag is FBB_OV and generates an IRQ except if MASK_FBB_OV_IRQ is set. The state machine executes a power down sequence to enter in DEEP-SLEEP.
- An analog comparator is used to detect undervoltage. The flag is FBB_UV and generates an IRQ except if MASK_FBB_UV_IRQ is set. The state machine executes a power down sequence to enter in DEEP-SLEEP.
- The ADC is used to detect overvoltage early warnings (flagged by FBB_OV_EW bit).
- The ADC is used to detect undervoltage early warnings (flagged by FBB_UV_EW bit).
- The thresholds are programmable by SPI (FBB_OV_EW_TH[3..0]) and an interrupt is issued when thresholds are crossed except if MASK_FBB_OV_EW_IRQ is set.
- The thresholds are programmable by SPI (FBB_UV_EW_TH[3..0]) and an interrupt is issued when thresholds are crossed, except if MASK_FBB_UV_EW_IRQ is set.
- The result of ADC conversion is also readable back via SPI, by FBB[9..0].

4.1.3 VIO pin

VIO voltage is monitored through an analog comparator and digital communication is blocked if VIO voltage is below V_{VIO_UV} threshold for a delay higher than $T_{F\_VIO\_UV}$ (flag is VIO_UV bit).

4.2 Regulators output voltage protection

The 3 BUCKs and LDO2 outputs are monitored through analog comparators to detect over and undervoltages. (through BUCKx_UV, BUCKx_OV, LDO2_UV and LDO2_OV bits). The reaction to a fault is described in the Section 3.6.2.5: Regulator faults management. In addition, LDO2 is also turned OFF when the tracked regulator is turned OFF in reaction to a fault.

When a regulator is turned ON, by SPI or power-up sequence, a short to ground is detected if the output voltage does not reach the power-good threshold in the time-out period (BUCKx_PG_TIMEOUT bit), in such case the regulator is switched OFF.

In addition, when turned ON through the SPI, an interrupt is generated as soon as their output voltage reaches the power-good threshold(BUCKx_PG and LDO2_PG bits).

Latent fault detection of OV, UV, PG analog comparators is insured by Analog-BIST.

Latent fault of regulator monitor handler is insured by Digital-BIST.

4.3 Boost and bypass V_{ds} monitoring

The BOOST driver includes a comparator to monitor the voltage drop across the boost external transistor. The voltage is monitored between DLB and GND pins.

The monitor issues a fault (whose threshold is set by BOOST_DSMON_TH[2..0] bits) if the monitored voltage is above the programmed threshold for 5 consecutive periods of the BOOST PWM signal.

When a fault is detected (the flag is BOOST_VDSMON_ERROR), an interruption is sent on the IRQ pin (except if it is masked by MASK_BOOST_VDSMON_IRQ) and the BOOST external transistor is permanently turned OFF. MCU shall read and clear the status flag to turn back ON the BOOST driver.

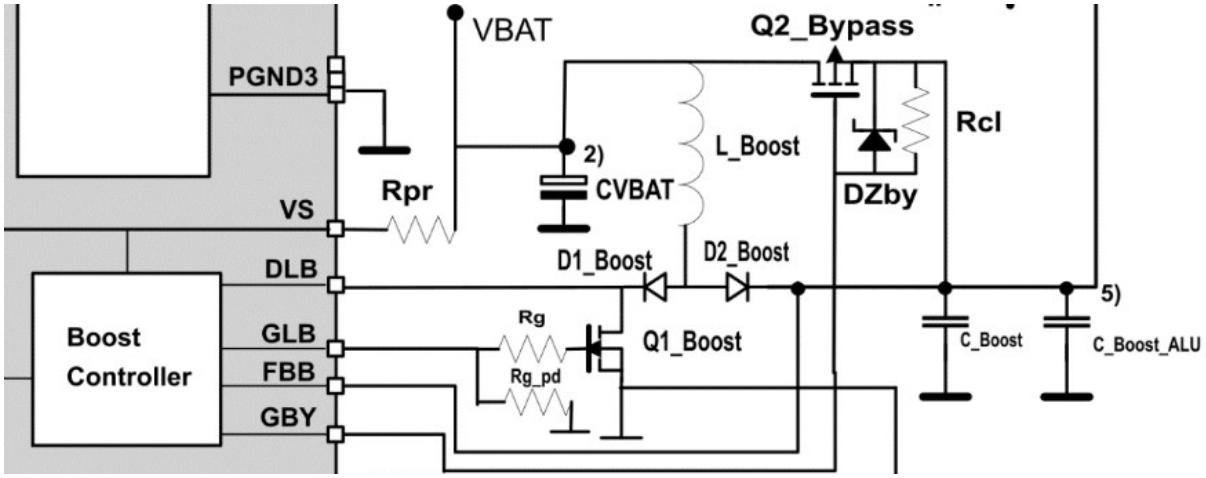
The BYPASS driver includes a comparator to monitor the voltage across the bypass external transistor this comparator is enabled as soon BYPASS is switched ON with a digital blanking time, $t_{B\_BYPASS\_VDSM}$. The voltage is monitored between VS and FBB pins.

The monitor issues a fault if the monitored voltage is above the programmed threshold (BYPASS_DSMON_TH[2..0] bits) for a delay higher than $t_{F\_BYPASS\_VDSM}$ time.

When a fault is detected (flag is BYPASS_VDSMON_ERROR), an interruption is sent on the IRQ pin (except if it is masked by MASK_BYPASS_VDSMON_IRQ), the BYPASS external transistor is switched off.

Latent fault detection of comparators is insured by Analog-BIST.

Figure 28. Boost and bypass V_{ds} monitoring (extracted by application scheme)



4.4 Boost activity monitoring

In ACTIVE – FULL-POWER and in RECOVERY-1 states, the BOOST activity can be monitored through the live SPI status bit BOOST_ENA_STATUS.

In ACTIVE – LOW-POWER state a flag is set BOOST_IN_LP and an interrupt is generated through IRQ pin (except if it is masked by MASK_BOOST_IN_LP_IRQ) when the BOOST starts to switch.

In other states the BOOST is disabled.

4.5 WU and IGN monitoring

WU and IGN voltages can be measured through the ADC and values read back via SPI (WU[9..0] and IGN[9..0]).

4.6 Ground pin monitoring

Analog comparators are cross-monitoring the voltage on the three ground pads GND, Analog-GND and Digital-GND (both bonded on SGND pin).

If at least one ground pad is electrically disconnected from the PCB ground plane with a level above $V_{Gnd\_Loss\_th}$ then a Ground loss is detected (GNDLOSS) after $t_{Gnd\_Loss\_FILT}$ and the reaction is described in the Section 4.8: HW low-level monitors.

Latent fault detection of ground comparators is insured by Analog-BIST.

4.7 Temperature monitoring

To provide an advanced on-chip temperature control, the power outputs are grouped in clusters with dedicated thermal sensors. The sensors are suitably located on the device.

If the temperature of a cluster reaches the thermal warning threshold then a dedicated status flag (TW_CLx bit) is set and an interrupt is issued.

If the temperature of a cluster reaches the thermal shutdown threshold then a dedicated status flag is set, the outputs assigned to that cluster are shut down and depending on their configuration bit REGFAIL_GO_REC all outputs are shut down or not as described in the Section 3.6.2.5: Regulator faults management.

Figure 29. Thermal cluster identification

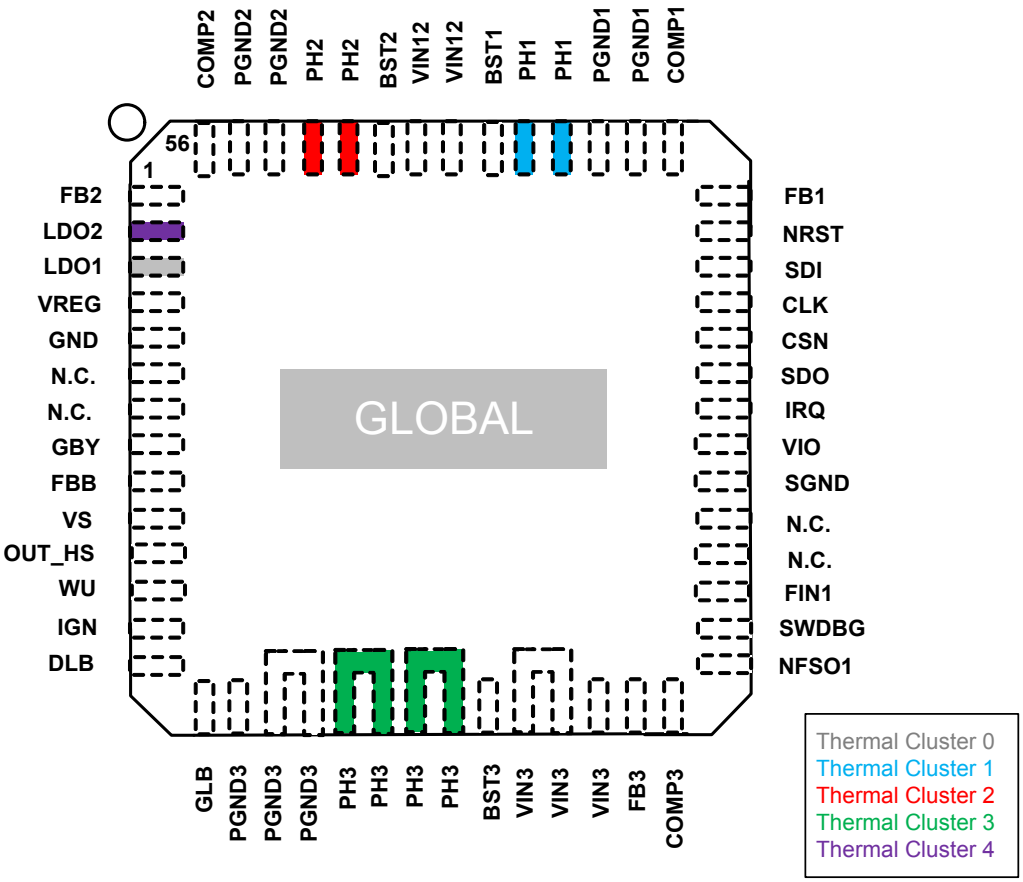


Table 9. Thermal cluster definition

Th_CL0	Th_CL1	Th_CL2	Th_CL3	Th_CL4
LDO1, central	BUCK1	BUCK2	BUCK3	LDO2
TW digitally managed TSDC analog managed	TW and TSD Both digitally managed	TW and TSD Both digitally managed	TW and TSD Both digitally managed	TW and TSD Both digitally managed

Clusters temperature is converted through the ADC and readable by SPI (through TEMP_CLx[9..0] bits), only in active full-power mode

Note:
- *In the DEEP-SLEEP state all clusters are disabled.*
- *In active low power all clusters are disabled except Th_CL0 to detect TSDC.*

Monitoring of central thermal cluster is insured by analog comparator, while other thermal clusters are monitored through the ADC.

Latent fault detection of TSDC thermal comparator is covered by Analog-BIST.

Latent fault detection of digital thermal monitor and ADC handler is covered by a Digital-BIST.

4.8 HW low-level monitors

The SPSB100 integrates asynchronous monitors of low-level blocks in ACTIVE-FULL-POWER mode and REC-1 states:

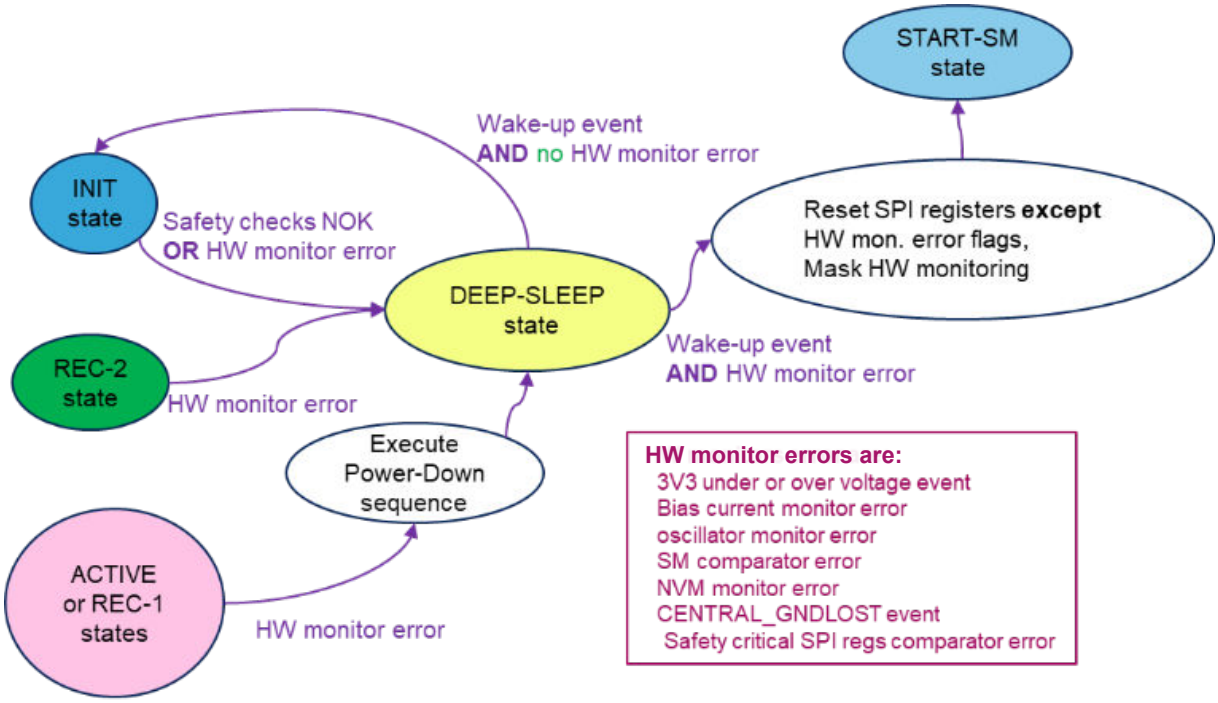
- Voltage difference between main and monitoring digital and analog power supplies (INT_REG_UV, INT_REG_OV bits).
- Current difference between main and monitoring current sources (CURRENT_MISMATCH bit).

and synchronous monitors of:

- Frequency difference between main and redundant oscillators (OSC_ERROR bit).
- State machine's state by comparison of main and redundant State machine(FSM_COMP_ERROR bit).
- NVM data by:
  - Comparison of NVM data and redundant registers (NVM_COMP_ERROR bit).
  - CRC check at NVM download(NVM_CRC_ERROR bit).
- Safety critical SPI registers by comparison of main and redundant registers (SPI_REG_COMP_ERROR bit generates an IRQ except if MASK_SPI_ERROR_IRQ is set).
- Ground loss connection by cross-checking ground domains(GNDLOSS bit).

A fault detected by low-level monitors trigs a power-down sequence and SPSB100 reaches the DEEP-SLEEP state. In such situation, after a wake-up event (except for OSC_ERROR where SPSB100 restarts automatically if oscillators recover their frequencies), all SPI registers are reset except HW low-level monitor flags and SPSB100 transit to START-SM state.

Figure 30. HW low level monitors



4.9 Communication interface

The SPI communication protocol embeds the following safety mechanisms:

- A 4-bit CRC SPI_CRC_ERR is set in case of error detected, and an IRQ is generated except if MASK_SPI_ERROR_IRQ is set.
- Clock monitor: during communication (CSN low phase) a clock monitor counts the valid CLK edges. If the CLK edges do not correlate with the SPI data length then SPI_CLK_CNT is set, an IRQ is generated except if MASK_SPI_ERROR_IRQ is set, the actual communication is rejected.

- CLK phase check: To verify that the CLK phase of the SPI controller is set correctly a special device information register is implemented. By reading this register the data must be 55H. In case AAH is read the CPHA setting of the SPI controller is wrong and a proper communication cannot be guaranteed.
- CSN timeout: if CSN is set low for t > tCSN fail then the frame is rejected and SDO is released to tri-state (SPI_CSN_TIMEOUT is set). An IRQ is generated except if MASK_SPI_ERROR_IRQ is set.
- SDI stuck at high detection: an SPI frame consisting of all bits ‘1’ is detected as failure and will be rejected, SPI_SDI_STUCK_HIGH is set and an IRQ is generated except if MASK_SPI_ERROR_IRQ is set.
- SDI stuck at low detection: an SPI frame consisting of all bits ‘0’ is detected as failure and will be rejected, SPI_SDI_STUCK_LOW is set and an IRQ is generated except if MASK_SPI_ERROR_IRQ is set.
- SDO stuck: the global status byte (GSB) is transmitted within every SPI frame; the definition of the GSB guarantees that a content of all ‘1’ or all ‘0’ is not possible; therefore, the microcontroller can identify if the SDO signal is stuck at high or low level.
- Functional safety relevant configuration registers are locked by a dedicated bit SPI_PROTECT_ACCESS. A first SPI command must be sent to unprotect the functional safety relevant registers, then a successive SPI command is sent to modify those configuration registers.
- SPI undefined address access is detected by a dedicated bit SPI_UNDEF_ADD. An IRQ is generated except if MASK_SPI_ERROR_IRQ is set.
- SPI unwanted write access on a status register is detected by a dedicated bit SPI_STATUS_WRT. An IRQ is generated except if MASK_SPI_ERROR_IRQ is set.
- SPI unwanted access during LBIST test is detected and SPI_LBISTED is set. An IRQ is generated except if MASK_SPI_ERROR_IRQ is set. In this case, the SPI frame is rejected.
- Functional safety relevant configuration registers are duplicated and a runtime comparison mechanism check the coherency of their data. In case of error the reaction is described in the Section 4.8: HW low-level monitors.

Latent fault detection of SPI digital handler, functional safety redundant configuration register and comparison mechanism are covered by a Digital-BIST.

4.10 IRQ pin monitoring

To check that the IRQ line is properly connected to the MCU, an IRQ can be sent to the MCU through SPI request.

When MCU sets the SPI bit IRQ_REQUEST, an interrupt is generated on IRQ pin.

The MCU can verify that the IRQ has well been sent by checking the IRQ_SENT status bit. Pin IRQ shall be set high after read and clear of IRQ_SENT flag.

To detect IRQ stuck high fault, the device embeds:

- An echo signal of the IRQ pin: IRQ_ECHO live bit in the status register.
- An echo error detection mechanism: IRQ_ECHO_ERROR status bit is set if the device detects an IRQ_ECHO high signal when IRQ pin is asserted low after a filter time $T_{IRQ\_ECHO\_FILT}$.

4.11 NRST pin monitoring

To detect NRST stuck high fault, the device embeds:

- An echo signal of the NRST pin: NRST_ECHO live bit in the status register.
- An echo error detection mechanism: NRST_ECHO_ERROR status bit is set if the device detects an NRST_ECHO high signal when NRST pin is asserted low after a filter time $T_{NRST\_ECHO\_FILT}$.

4.12 NFSO1 pin monitoring

To detect NFSO1 stuck high fault, the device embeds:

- An echo signal of the NFSO1 pin: NFSO1_ECHO live bit in status register.
- An echo error detection mechanism: NFSO1_ECHO_ERROR status bit is set if the device detects an NFSO1_ECHO high signal when NFSO1 pin is asserted low, after a filter time $T_{NFSO\_ECHO\_FILT}$ and an interrupt is sent to IRQ pin, except if MASK_NFSO1_ECHO_ERROR_IRQ is set.

4.13 Watchdog block monitoring

To detect an improper turn-OFF of the watchdog feature, the device embeds:

- An echo signal of the watchdog block enable signal: WD_ENA_ECHO live bit in the status register.
- An echo error detection mechanism: WD_ENA_ECHO_ERROR status bit is set if the device detects that the watchdog block is turned OFF while the device is not in SW-DEBUG mode, and an interrupt is sent to IRQ pin, except if MASK_WD_ENA_ECHO_ERROR_IRQ is set.

4.14 FCCU block monitoring

To detect an improper turn-OFF of the FCCU monitor feature, the device embeds:

- An echo signal of the FCCU monitor block enable signal: FCCU_ENA_ECHO live bit in the status register.
- An echo error detection mechanism: FCCU_ENA_ECHO_ERROR status bit is set if the device detects that the FCCU monitor block is turned OFF in ACTIVE state, when FCCU_ENA has been set and an interrupt is sent to IRQ pin, except if MASK_FCCU_ENA_ECHO_ERROR_IRQ is set.

4.15 Analog BIST

ABIST is performed on SPI request.

ABIST is not run on blocks that are turned OFF. The MCU shall ensure the proper turn ON of a block when its ABIST is expected to be run.

ABIST covers latent fault detection of:

- OV, UV, PG analog comparators.
- Internal voltage and current supplies monitor.
- Central thermal monitor.
- BOOST and BYPASS VDS monitors.

ABIST must be run only in Active-Full power mode by MCU through the SPI. MCU shall write ABIST bit to request its execution (only after SPI_PROTECT_ACCESS has been set).

After TABIST, ABIST is finished, the status bit ABIST_COMPLETE is set and an interrupt is sent to IRQ pin.

ABIST_ERROR is set in case an error is detected.

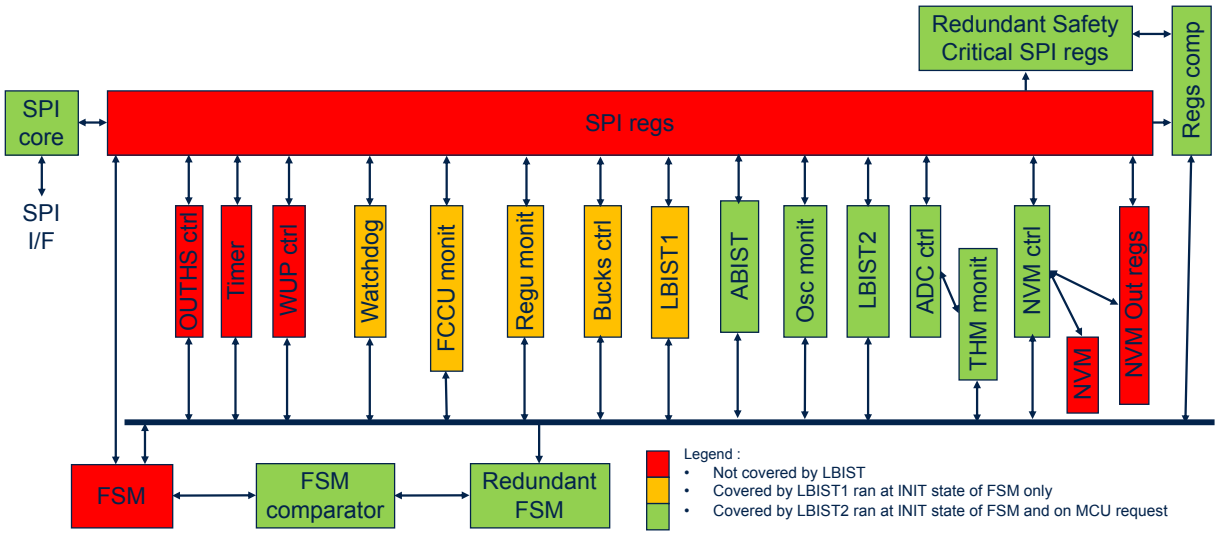
For boost VDSM monitoring, to avoid false ABIST error, a status bit ABIST_BOOST_IGNORED will be set at 1 if ABIST request is done during boost PWM activity.

4.16 Logic BIST

The SPSB100 integrates two logic BIST:

- LBIST1 is performed at INIT state only.
- LBIST2 is performed at INIT state and on SPI request.

Figure 31. Logic BIST



LBIST2 must be run only in Active-Full power mode by MCU through the SPI. MCU shall write LBIST bit to request its execution (only after SPI_PROTECT_ACCESS has been set). The LBIST2 execution is delayed until the NVM controller terminates its self-test

After t_{LBIST}, the LBIST2 is finished, the status bit LBIST_COMPLETE is set and an interrupt is sent to IRQ pin.

LBIST_ERROR_1 is set in case a LBIST2 error is detected.

SPSB100 does not take any action in case of an LBIST2 error is detected. It is the duty of the MCU to proper react on such a signaled error.

LBIST error detected in INIT state is considered as a safety check error (see the Section 4.17: Safety checks).

Fault management while LBIST is executed:

- When LBIST1 and LBIST2 are executed in INIT state the internal faults processed by the blocks under LBIST are masked, their processing by SPSB100 is delayed until the end of LBIST1 & LBIST2.
- When LBIST2 is executed on demand in active-full power mode the faults (UV, OV, TSD…) processed by the blocks under LBIST2 are not masked. If a fault occurs the LBIST2 is stopped, status bit LBIST_STOPPED is set and an IRQ is generated, the fault is processed by SPSB100 with appropriate reaction.
- As a consequence the watchdog window must be properly set before requesting a LBIST2 execution to let the LBIST2 complete before the next watchdog trig through SPI.

4.17 Safety checks

Safety checks are executed in INIT state. They are made of:

- Digital BIST LBIST1 and LBIST2.
- Ground pin monitor.
- NVM checks: CRC and U-PROG value.

In case of error the state machine transits to DEEP-SLEEP where the device can be woken up to INIT state where safety checks are run again.

4.18 NVM integrity monitor

To detect an improper turn-OFF of NVM monitor feature, the device embeds an echo signal of the NVM monitor block enable signal: NVM_COMPARE_ENA_STATUS live bit in the status register. This status bit is set if a fault disables the comparison of NVM data with redundant registers, in such case an interrupt is sent to IRQ pin. The reaction of the NVM monitor features in case of error is described in the Section 4.8: HW low-level monitors.

5 Serial peripheral interface (SPI)

A 32-bit SPI is used for bidirectional communication with the microcontroller.

The microcontroller SPI peripheral shall be configured with CPOL = 0 and CPHA = 0: SDI input data is sampled by the rising CLK edge, and SDO output data is updated on the falling CLK edge.

This device is not limited to microcontroller with a built-in SPI peripheral, instead three CMOS-compatible output pins and one input pin may be used to communicate with the device. A fault condition can be detected by setting CSN to low, in such condition the SDO pin reflects the global error flag GSBN of the device.

- Chip select not (CSN)
  The CSN input pin is used to select the serial interface of this device. When CSN is high, the output pin SDO is in a high impedance state. CSN low activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame. If CSN is low for $t > t_{CSNfail}$ the SDO output will be switched back to high impedance not to block the signal line for other SPI nodes.
- Serial data in (SDI)
  The SDI input pin is used to transfer data into the device. The data applied to SDI are sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register is transferred to the data input register. The writing to the selected data input register is enabled if exactly 32 bits are transmitted within one communication frame (that is, CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored and a SPI error is signaled. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame. Due to this safety functionality, a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.
- Serial data out (SDO)
  The data output driver is activated by a logical low level at the CSN input and will go from high impedance to a low or high level depending on the global error flag GSBN. The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK will shift the next bit out. As SDO is in high impedance when CSN is high, it is possible to link several SPI target devices that respect this rule with a dedicated CSN line for each SPI target.
- Serial Clock (CLK)
  The CLK input is used to synchronize the input and output bit streams. The data input (SDI) is sampled at the rising edge of the CLK and the data output SDO is updated on the falling edge of the CLK signal.

5.1 ST-SPI

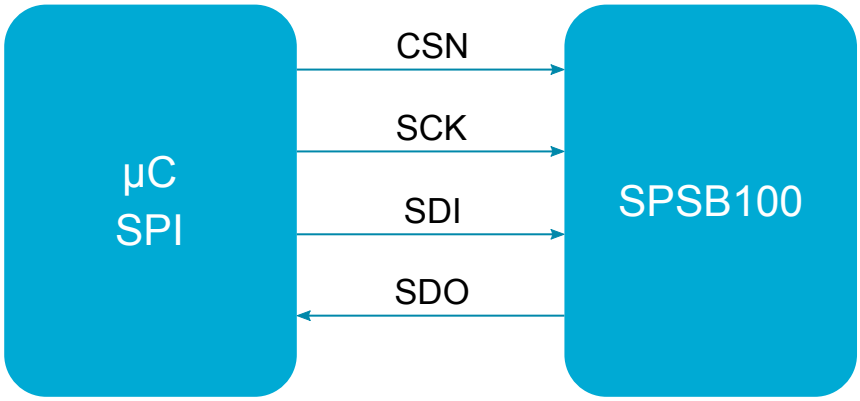
The ST-SPI is a standard used in ST automotive ASSP devices.

This chapter describes the SPI protocol. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST-SPI allows usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, safety mechanisms are implemented to protect the communication from external influences and wrong or unwanted usage.

5.1.1 Physical Layer

Figure 32. **SPI pin description**



5.2 Signal description

Chip select not (CSN)

The communication interface is deselected when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. At CSN falling and rising edges the serial clock (CLK) has to be logically low. The serial data out (SDO) is in high impedance when CSN is high or a communication timeout is detected.

Serial clock (CLK)

CLK provides the clock of the SPI. Data present at serial data input (SDI) is latched on the rising edge of serial clock (CLK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to serial data out (SDO).

Serial data input (SDI)

This input is used to transfer data serially into the device. Data is latched on the rising edge of the serial clock (CLK).

Serial data output (SDO)

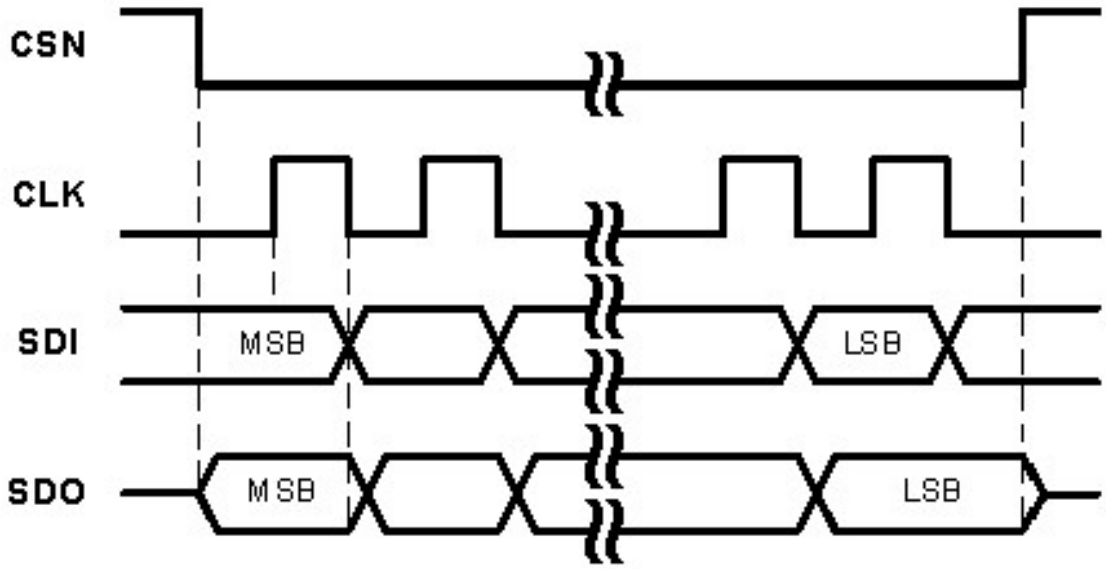
This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock (CLK).

5.2.1 Clock and data characteristics

The ST-SPI can be driven by a microcontroller with its SPI peripheral running in the following modes:

- CPOL = 0
- CPHA = 0

Figure 33. **SPI signal description**



The communication frame starts with the falling edge of the CSN (Communication Start). CLK has to be low.

The SDI data is then latched at all following rising CLK edges into the internal shift registers.

After Communication Start the SDO leaves high impedance state and present the MSB of the data shifted out to the SDO. At all following falling CLK edges data is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication took place, the requested operation according to the operating code is performed.

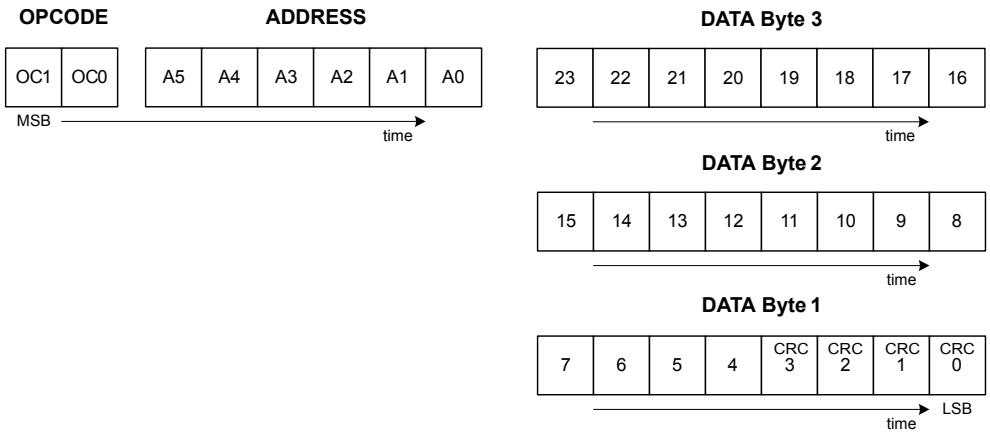
5.2.2 Communication protocol

5.2.2.1 SDI frame

The devices data-in frame consists of 32 bits (OpCode (2 bits) + address (6 bits) + data (20 bits) + CRC (4 bits)). The first two received bits (MSB, MSB-1) contain the operation code which indicates the instruction to be performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation is performed.

The subsequent bytes contain the payload.

Figure 34. **SDI frame**



5.2.2.2 *Operation code*

The operating code is used to distinguish among different access modes to the registers of the target device.

Table 10. Operation codes

OC1	OC0	Description
0	0	Write operation
0	1	Read operation
1	0	Read and clear operation
1	1	Read device information

A ***Write operation*** leads to a modification of the addressed data by the payload if a write access is allowed (for example, control register, valid data). Beside this a shift out of the content (data present at *Communication start*) of the same register is performed.

A ***Read operation*** shifts out the data present in the addressed register at *Communication start*. The SDI payload data is ignored and internal data will not be modified. Burst read cannot be performed. Even if the first 8 bits of SDO are sent during read device information, the chip must receive a full frame with CRC on SDI otherwise a SPI_CLK_CNT and a SPI_CRC_ERR will be set generating a SPIE.

A ***Read and clear operation*** will lead to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload data bits set to '1'. Beside this a shift out of the content (data present at *Communication start*) of the same register is performed.

Note: Status registers which change status during communication could be cleared by the actual Read and clear operation and are neither reported in actual communication nor in the following communications. To avoid a loss of any reported status it is recommended to clear status registers which have been read in the previous communication (Selective bitwise clear).

5.2.2.3 *Advanced operation code*

A *'clear all status registers'* command is performed when an OpCode '10' at address b'111111 is performed.

5.2.2.4 *Data-in payload*

The *payload* (Data bits) is the data transferred to the device within every SPI communication. The *payload* always follows the OpCode and the address bits.

For write access the *payload* represents the new data written to the addressed register. For *read and clear* operations the *payload* defines which bits of the addressed status register will be cleared. In case of a '1' at the corresponding bit position the bit will be cleared.

For a *Read operation* the SDI *payload* is not used. For functional safety reasons it is recommended to set unused *payload* to '0'.

5.2.2.5 *SDO frame*

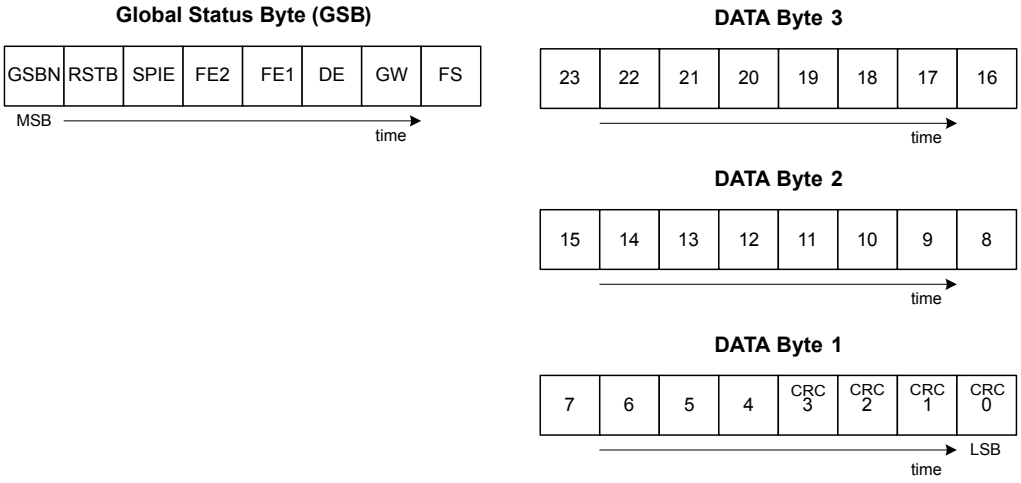
The data-out frame consists of 32 bits (GSB + data bits + CRC).

The first eight transmitted bits contain device related status information (GSB) and are latched into the shift register at the time of the *Communication start*. These 8 bits are transmitted at every SPI transaction.

The subsequent bytes contain the payload data together with the four LSB bits containing CRC and are latched into the shift register with the eighth positive CLK edge.

This could lead to an inconsistency of data between the GSB and *payload* due to different shift register load times. Anyhow, no unwanted status register clear should appear, as status information should just be cleared with a dedicated bit clear after.

Figure 35. **SDO frame**



5.2.2.6 *Global status byte (GSB)*

Bits 0 to 5 represent a logical OR combination of bits located in the status registers. Therefore, no direct read and clear can be performed on these bits inside the GSB.

Table 11. **Global status byte**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GSBN	RSTB	SPIE	RES	FE1	DE	GW	FS

- Global status bit not (GSBN)
  The GSBN is a logically NOR combination of bit 0 to bit 6. This bit can also be used as a *global status flag* without starting a complete communication frame as it is present directly after pulling CSN low.
  OUTHS open load can be masked in GSBN by setting bit MASK_OL_GSB.
  Global warning can be masked in GSBN by setting bit MASK_GW_GSB.
- Reset bit (RSTB)
  The RSTB indicates a SPSB100 reset. In case this bit is set, all internal control and status registers are set to default.
  The RSTB bit is cleared after a *read and clear* of the VPOR bit in the *status registers* which caused the reset event.
- SPI error (SPIE)
- Functional error 1 (FE1)
  The FE1 is a logical OR combination of errors coming from functional blocks.
- Device error (DE)
  The DE is a logical OR combination of errors related to device specific blocks.
- Global warning (GW)
  The GW is a logical OR combination of warning flags (for example, thermal warning).
  Thermal warning can be masked in GW by setting bit MASK_TW_GW.
- Fail-safe (FS)
  The FS bit indicates that the device was forced into a safe state due to mistreatment or critical internal errors (for example, watchdog failure, voltage regulator failure).

5.2.2.7 *Data-out payload*

The data-out *payload* (20 data bits + 4 CRC bits) is the data transferred from the target device within every SPI communication to the controller device.

5.2.3 Address definition

Table 12. RAM and ROM address range

Operation code		
OC1	**OC0**	**Description**
0	0	Write operation, allowed to RAM control registers
0	1	Read operation, allowed to RAM status or control registers
1	0	Read and clear operation, allowed to RAM status registers
1	1	Read device information in ROM registers

Table 13. RAM address

RAM address	Description	Access
3FH	Special OpCode	R/W
…	-	-
32H	Status register 18	R/C
…	…	-
22H	Status register 2	R/C
21H	Status register 1	R/C
…	…	-
1CH	Control register 28	R/W
…	…	-
02H	Control register 2	R/W
01H	Control register 1	R/W
00H	Reserved	-

Table 14. ROM address

RAM address	Description	Access
…	-	-
3EH	<GSB Options>	R
…	-	-
20H	<SPI CPHA test>	R
…	-	-
15H	<WD bit pos. 3>	R
14H	<WD bit pos. 2>	R
13H	<WD bit pos. 1>	R
12H	<WD Type 2>	R
11H	<WD Type 1>	R
10H	<SPI mode>	R
…	-	-
0AH	<Silicon Ver.>	R
…	-	-
05H	<Device No.4>	R

RAM address	Description	Access
04H	<Device No.3>	R
03H	<Device No.2>	R
02H	<Device No.1>	R
01H	<Device Family>	R
00H	<Company Code>	R

5.2.3.1 *Device information registers*

The *device information registers* can be read by using OpCode '11'. After shifting out the GSB the 8bit wide payload will be transmitted. By reading *device information registers* a communication width which is minimum 16 bits can be used. After shifting out the GSB followed by the 8bit wide payload a series of '0' is shifted out at the SDO.

Table 15. Information registers map

ROM address	Description	Access	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
…										
3EH	<GSB Options>	R	0	0	0	0	0	0	0	0
…										
20H	<SPI CPHA test>	R	0	1	0	1	0	1	0	1
…										
15H	<WD bit pos. 3>	R	00H							
14H	<WD bit pos. 2>	R	C0H							
13H	<WD bit pos. 1>	R	44H							
12H	<WD Type 2>	R	91H							
11H	<WD Type 1>	R	Watchdog long open window (refers to watchdog definition)							
10H	<SPI mode>	R	32H							
…										
0AH	<Silicon Ver.>	R	Major revision				Minor revision			
…										
06H	<Device No.5>	R	01H: SPSB100B and SPSB100P							
05H	<Device No.4>	R	4EH							
04H	<Device No.3>	R	38H							
03H	<Device No.2>	R	52H							
02H	<Device No.1>	R	55H							
01H	<Device Family>	R	01H							
00H	<Company Code>	R	00H							

5.2.3.1.1 Device identification registers

These registers represent a unique signature to identify the device and silicon version.

<*Company Code*>: 00H (STMicroelectronics)

<*Device Family*>: 01H (BCD power management)

<*Device No. 1*>: 55H (ASCII code for U)

<*Device No. 2*>: 52H (ASCII code for R)

<*Device No. 3*>: 38H (ASCII code for 8)

<*Device No. 4*>: 4EH (ASCII code for N)
<*Device No. 5*>: 01H: SPSB100B and SPSB100P

5.2.3.1.2 SPI modes

By reading out the <SPI Mode> register general information of SPI usage of the *device application registers* can be read.

Table 16. SPI mode register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BR	FL2	FL1	FL0	SPI8	0	S1	S0
0	0	1	1	0	0	1	0

<*SPI Mode*>: 32H (no burst mode available, 32 bit, CRC used)

5.2.3.1.3 CRC

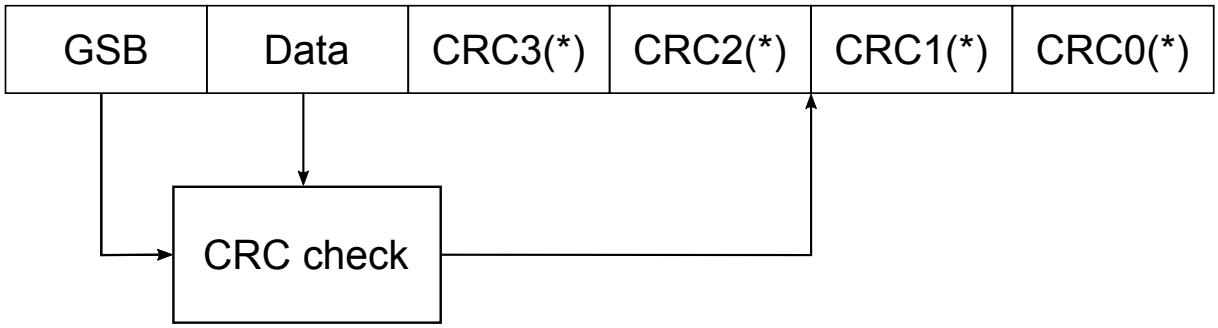
SDI:

The CRC check is performed on the complete communication frame using the polynomial (X4 + X + 1).
The frame is valid only if the result of the CRC check is equal to '0'. If not, the frame is rejected and a SPIE bit is set.

SDO:

CRC is calculated on GSB + data -4 bit and the 4-bits result is saved in data LSB_3 to data LSB_0.

Figure 36. CRC (cyclic redundancy check) calculation



Exceptions:
The CRC field is not inserted when device information is read in ROM registers.

5.2.3.2 *Watchdog definition*

For more details, refer to the Section 3.10: Configurable time-out window watchdog.
The watchdog default settings can be read out via the *device information registers*.

Table 17. WD Type/Timing

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<WD Type 1>	0	1	x	x	x	x	x	x
			Watchdog long open window WT[5:0]					
<WD Type 2>	1	0	0	1	0	0	0	1
			Open window OW[2:0]			Closed window CW[2:0]		

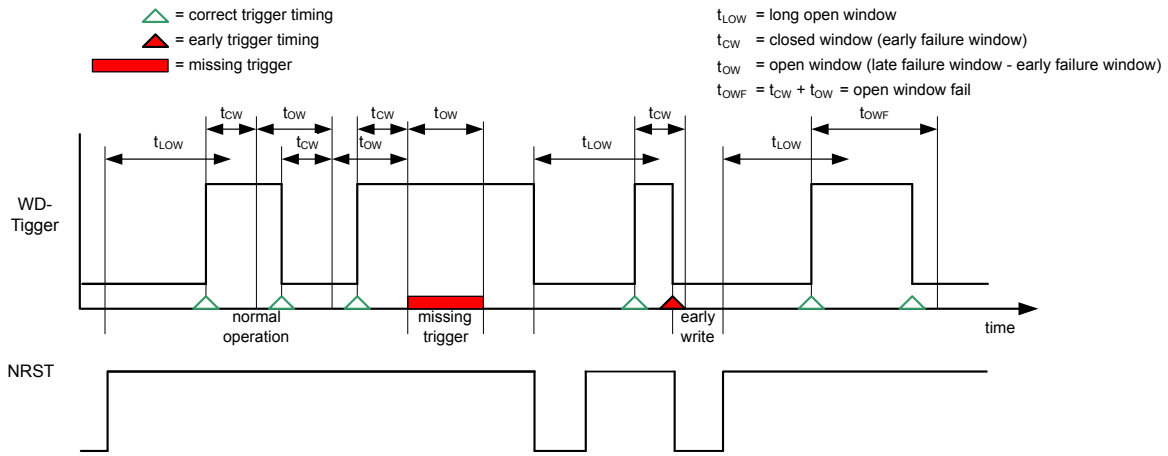
<*WD Type 1*>: long open window: reflects the value of LOW_SET(1:0) bits of USER-NVM
<*WD Type 2*>: 91H (open window. 10 ms, closed window: 5 ms)

<WD Type 1> indicates the Long open window duration. On this byte, bits 5 and 4 are zero and bits 3 to 0 come from LOW_SET(3-0) user NVM bits. Refer to the Table 32 describing the long open window durations according to LOW_SET(3-0) from user NVM.

<WD Type 2> describes the default timing of the window watchdog.

The binary value of CW[2:0] times 5 ms defines the typical closed window time (t_{CW}) and OW[2:0] times 5 ms defines the typical open window time (t_{OW}). See the Figure 37 with $t_{CW} = T_{EFW}$ and $t_{OW} = T_{LFW} - T_{EFW}$.

Figure 37. Window watchdog operation



The watchdog trigger bit location is defined by the <WD bit pos. X> registers.

Table 18. WD bit position

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WD bit pos 1	0	1	0	0	0	1	0	0
			Defines the register addresses of the WD trigger bit(s)					
WD bit pos 2	1	1	0	0	0	0	0	0
			Defines the binary bit position					

<*WD bit pos 1*>: 44H; watchdog trigger bit located at address 04H (DCR4)

<*WD bit pos 2*>: C0H; watchdog trigger bit location is bit0

<*WD bit pos 3*>: 00H

5.2.3.3 *Device application registers (RAM)*

The *device application registers* are all registers accessible using OpCode ‘00’, ‘01’ and ‘10’.

6 Functional safety concept

The device is designed to offer a set of features to support applications that need to fulfill functional safety requirements as defined by ASIL classification in ISO26262-2018. The IC is developed for different applications, hence can be considered a SEooC (safety element out of context) as defined in the normative. Analysis of the IC's capability to reach the required safety level, should be made at system level under the user's responsibility.

6.1 Safety requirements

The SPSB100 must fulfill safety requirements for temperature, output current, output voltage, and system operation as in the following tables based on MCU modes.

6.1.1 MCU in RUN mode

The following figure shows the MCU in RUN mode.

Figure 38. PMIC + MCU in RUN mode

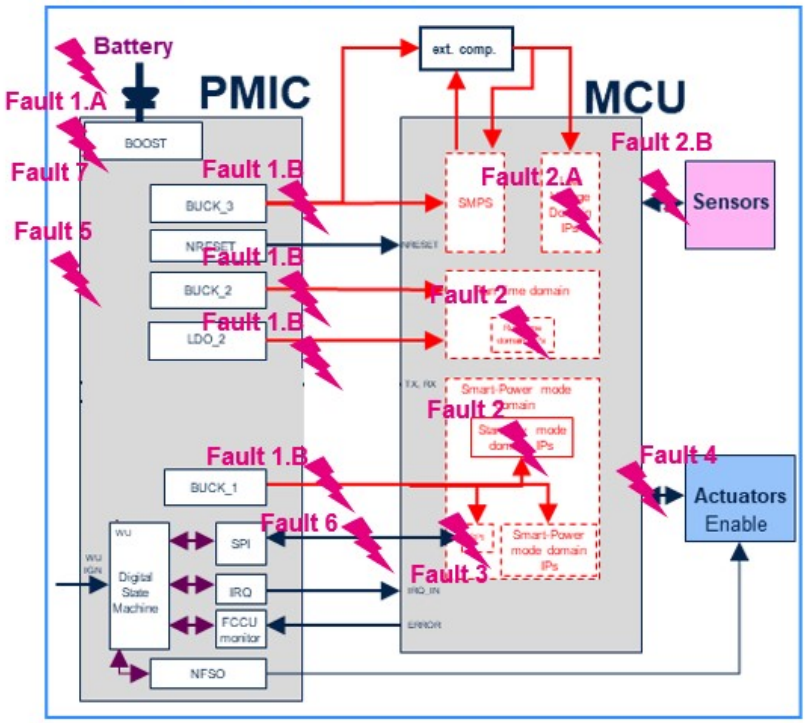


Table 19. Safety requirement list while MCU is in RUN mode

ID	Description	Safety state
SR1	While the MCU is in RUN mode the PMIC shall monitor the supply output voltages for the MCU and force a reset of the MCU in case of a voltage error.	Output regulators are stopped, NRESET and NFSO pins are asserted. SPSB100 tries to power-up again, if the fault is confirmed for 3 successive power-up then output regulators are stopped, NRESET and NFSO pins are asserted and SPSB100 reaches DEEP-SLEEP state.
SR2	While the MCU is in RUN mode the PMIC shall monitor the MCU error pin and force a reset of the MCU based on an error indication.	NRESET and NFSO pins are asserted, output regulators are set back to their state resulting from a power-up sequence, then NRESET assertion is maintained for few ms then released. SPSB100 is in RECOVERY-1 state.

ID	Description	Safety state
SR3	While the MCU is in RUN mode the PMIC shall monitor the MCU communication and force a reset of the MCU in case of error.	NRESET and NFSO pins are asserted, output regulators are set back to their state resulting from a power-up sequence, then NRESET assertion is maintained for a few ms then released. SPSB100 is in RECOVERY-1 state. If the MCU communication fault persists then SPSB100 executes a power-down/power-up sequence. If the MCU communication fault persists further then output regulators are stopped, NRESET and NFSO pins are asserted and SPSB100 reaches DEEP-SLEEP state.
SR4	The PMIC shall monitor the local temperature of each supply regulator and force a shut-down of the supply regulators in case of temperature runaway.	Output regulators are stopped, NRESET and NFSO pins are asserted. SPSB100 waits that the regulator temperature decrease then tries to power-up again, if the fault is confirmed for 3 successive power-up then output regulators are stopped, NRESET and NFSO pins are asserted and SPSB100 reaches DEEP-SLEEP state.
SR5	The PMIC shall monitor the power dissipation of BOOST external transistors and avoid their destruction in case of runaway.	BOOST is stopped, error is signaled to MCU, SPSB100 state is unchanged.

Note: More details about functional safety can be found in the device safety manual, provided only upon customers request.

6.1.2 MCU in Smart-Power mode

The following figure shows MCU in Smart-Power mode.

Figure 39. PMIC + MCU in Smart-Power mode

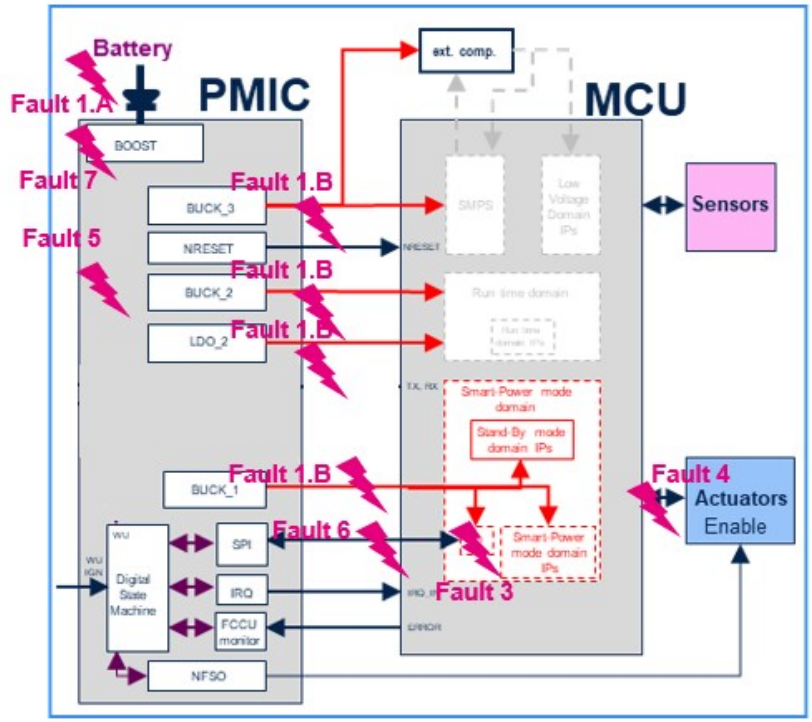


Table 20. Safety requirement list while MCU is in Smart-Power mode

ID	Description	Safe state
SR1	While MCU is in Smart-Power mode the PMIC shall monitor the supply output voltages for the MCU and force a reset of the MCU in case of a voltage error.	Output regulators are stopped, NRESET and NFSO pins are asserted. SPSB100 tries to power-up again, if the fault is confirmed for 3 successive power-up then output regulators are stopped, NRESET and NFSO pins are asserted and SPSB100 reaches DEEP-SLEEP state.
SR2	The PMIC shall monitor the local temperature of each supply regulator and force a shut-down of the supply regulator in case of temperature runaway.	Output regulators are stopped, NRESET and NFSO pins are asserted. SPSB100 waits that the regulator temperature decreases then tries to power-up again, if the fault is confirmed for 3 successive power-up then output regulators are stopped, NRESET and NFSO pins are asserted and SPSB100 reaches DEEP-SLEEP state.
SR3	The PMIC shall monitor the power dissipation of BOOST external transistors and avoid their destruction in case of runaway.	BOOST is stopped, error is signaled to MCU, SPSB100 state is unchanged.

Note: More details about functional safety can be found in the device safety manual, provided only upon customers request.

6.1.3 MCU in Stand-by mode

The following figure shows MCU in Stand-by mode.

Figure 40. PMIC + MCU in Stand-By mode

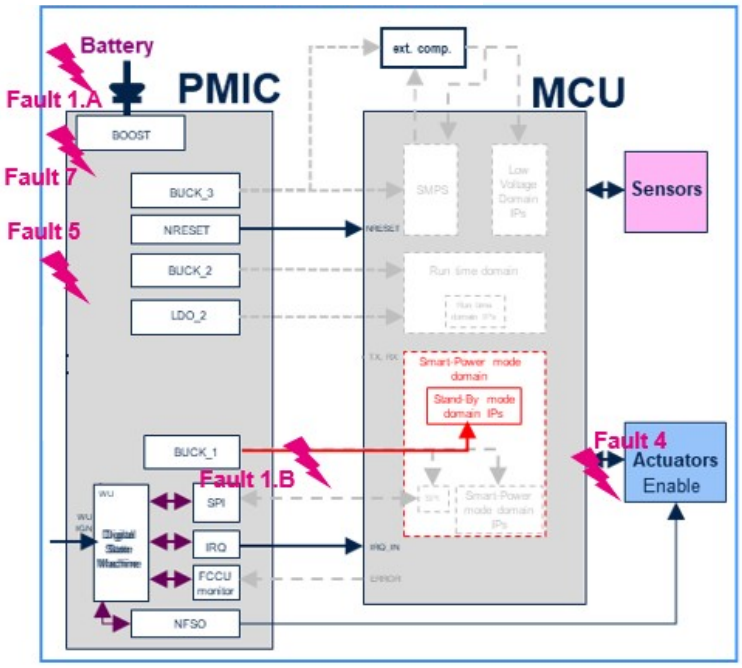


Table 21. Safety requirement list while MCU is in Stand-By mode

ID	Description	Safe state
SR1	While MCU is in Stand-By mode the PMIC shall monitor the supply output voltages for the MCU and force a reset of the MCU in case of a voltage error.	Output regulators are stopped, NRESET and NFSO pins are asserted. SPSB100 tries to power-up again, if the fault is confirmed for 3 successive power-up then output regulators are stopped, NRESET and NFSO pins are asserted and SPSB100 reaches DEEP-SLEEP state.
SR2	The PMIC shall monitor the local temperature of each supply regulator and force a shut-down of the supply regulator in case of temperature runaway.	Output regulators are stopped, NRESET and NFSO pins are asserted. SPSB100 waits that the regulator temperature decreases then tries to power-up again, if the fault is confirmed for 3 successive power-up then output regulators are stopped, NRESET and NFSO pins are asserted and SPSB100 reaches DEEP-SLEEP state.
SR3	The PMIC shall monitor the power dissipation of BOOST external transistors and avoid their destruction in case of runaway.	BOOST is stopped, error is signaled to MCU, SPSB100 state is unchanged.

Note: More details about functional safety can be found in the device safety manual, provided only upon customers request.

6.2 Safety mechanisms

Safety mechanisms implemented in SPSB100 are described in the Section 4: Protection, diagnosis and monitoring signals, more details about functional safety can be found in the device safety manual, provided only upon customers request.

7 Electrical characteristics

7.1 Supply monitoring

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
3 V < V_S < 29 V, 6 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 22. Supply and supply monitoring

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{FBB\_OK\_R1}$	V_{FBB} OK rising threshold	If BUCK1 and BUCK2 voltage setting = 3.3 V	6.9	7.2	7.5	V
$V_{FBB\_OK\_F1}$	V_{FBB} OK falling threshold	If BUCK1 and BUCK2 voltage setting = 3.3 V	6.4	6.7	7.0	V
$V_{FBB\_OK\_R2}$	V_{FBB} OK rising threshold	If BUCK1 or BUCK2 voltage setting are above 3.3 V (5.0 or 6.5 V)	8.65	9.0	9.25	V
$V_{FBB\_OK\_F2}$	V_{FBB} OK falling threshold	If BUCK1 or BUCK2 voltage setting are above 3.3 V (5.0 or 6.5 V)	8.15	8.5	8.75	V
$V_{FBB\_OK\_LP\_R1}$	Low power V_{FBB} OK rising threshold	If BUCK1 and BUCK2 voltage setting = 3.3 V	6.65	7.0	7.25	V
$V_{FBB\_OK\_LP\_F1}$	Low power V_{FBB} OK falling threshold	If BUCK1 and BUCK2 voltage setting = 3.3 V	6.15	6.5	6.75	V
$V_{FBB\_OK\_LP\_R2}$	Low power V_{FBB} OK rising threshold	If BUCK1 or BUCK2 voltage setting are above 3.3 V (5.0 or 6.5 V)	8.4	8.75	9.0	V
$V_{FBB\_OK\_LP\_F2}$	Low power V_{FBB} OK falling threshold	If BUCK1 or BUCK2 voltage setting are above 3.3 V (5.0 or 6.5 V)	7.9	8.25	8.5	V
$V_{FBB\_OK\_HYS}$	V_{FBB} OK hysteresis		0.4	0.5	0.6	V
$T_{F\_FBB\_OK}$	Digital filter time on FBB OK	Covered by scan	12	15	22	µs
V_{FBB_OV}	V_{FBB} overvoltage threshold	V_{FBB} increasing/decreasing	29	31	33	V
$V_{FBB\_OV\_HYS}$	V_{FBB} overvoltage hysteresis		0.1	0.15	0.25	V
$T_{F\_FBB\_OV}$	digital filter time on FBB overvoltage	Covered by scan	12	15	22	µs
$V_{FBB\_OV\_EW}$	V_{FBB} overvoltage early warning threshold	FBB_OV_EW_TH = [0…3] Step = 1 V	24	-	38	V
$V_{FBB\_UV\_EW\_TH}$	V_{FBB} undervoltage early warning range	FBB_UV_EW_TH = [0…3] Step = 0.24 V	5	-	8.36	V
$V_{VS\_UV\_EW\_TH}$	V_S undervoltage early warning range	VS_UV_EW_TH = [0…4] Step = 0.24 V	2.6	-	9.8	V
$V_{VIO\_UV\_R}$	V_{IO} undervoltage rising V_{IO} voltage		2.75	2.9	3.05	V
$V_{VIO\_UV\_F}$	On a falling V_{IO} voltage		2.7	2.85	3.0	V
$V_{VIO\_UV\_HYS}$	Hysteresis V_{IO} monitoring		0.005	0.035	0.065	V
$T_{F\_VIO\_UV}$	Digital filter time on comparator output	Covered by scan	12	15	22	µs
$I_{V(act)}$[(1)]	Current consumption in active-full power mode	V_S = 13.5 V BUCK1, 2, 3 ON LDO1, LDO2 ON	-	25	40	mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		No load on regulator $BUCK_{1,2\_freq}$ = 400 kHz				
I_{VS_LP1}[1]	Current consumption in active-low power mode	V_S = 13.5 V BUCK1 ON in LP BUCK1_REFRESH_FREQ = 1 BUCK2, 3 OFF LDO1, 2 OFF BUCK1 load = 5 mA V_{OUT_BUCK1} = 3.3 V $BUCK_{1\_freq}$ = 400 kHz, IRQ and NFSO high	-	2	3.2	mA
I_{VS_LP2}[1]	Current consumption in active-low power mode	V_S = 13.5 V BUCK1 ON in LP BUCK1_REFRESH_FREQ = 1 BUCK2, 3 OFF LDO1, 2 OFF BUCK1 load = 50 µA V_{OUT_BUCK1} = 3.3 V WDC, OUT_HS, cyclic sense, cyclic wake up, no SPI communication $BUCK_{2\_freq}$ = 400 kHz, IRQ and NFSO high	-	300	600	µA
I_{VS_DP}[2][3]	Current consumption in DEEP-SLEEP mode	V_S = 13.5 V BUCK1, 2, 3 OFF LDO1, 2 OFF OUT_HS, cyclic sense, cyclic wake-up, NFSO high Ta = 0 °C to 85 °C	-	20	40	µA
$I_{VS\_DP\_T}$[2][3]	Current consumption in DEEP-SLEEP mode	V_S = 13.5 V BUCK1, 2, 3 OFF LDO1, 2 OFF OUT_HS, cyclic sense, cyclic wake-up, NFSO high Full temperature range	-	-	55	µA
I_{QCW}	Current consumption adder for cyclic wake-up	V_S = 13.5 V In active-low power mode or DEEP-SLEEP state	-	60	90	µA
I_{QCS}	Current consumption adder for cyclic sense	V_S = 13.5 V In active-low power mode or DEEP-SLEEP state T_{period} = 50 ms, t_{ON} = 100 µs	-	60	90	µA
IQ_{OUT_HS}[3]	Additional bias quiescent current for switched ON OUT_HS	V_S = 13.5 V In active-low power mode or DEEP-SLEEP state No load	-	140	220	µA
$I_{VS\_BUCK2\_LP}$[3]	Additional bias quiescent current for BUCK2 in low power mode	V_S = 13.5 V BUCK2 ON in LP BUCK2_REFRESH_FREQ = 1 V_{out} = 5 V No load	-	90	400	µA

1. *Guaranteed by bench measurements. Performances verified in applicative conditions.*
2. *Current consumption in DEEP-SLEEP mode is calculated as IVS_DP + wake-up current consumption contributions.*
3. *Guaranteed by design.*

7.2 Power ground loss monitoring

Table 23. Power ground loss monitoring

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{Gnd\_Loss\_th}$	Ground Loss threshold		150	300	470	mV
$t_{Gnd\_Loss\_FILT}$[1]	Ground Loss filter time		12	15	22	µs

1. *Digital implementation is guaranteed by scan test.*

Ground loss protection parameter depends mainly on the implementation. This monitor measures a ground shift between GND and SGND pins.

7.3 Oscillator

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 24. Oscillator

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$F_{CLK800K}$	Oscillation frequency		640	800	960	kHz
$F_{CLK33M6\_MAIN}$	Oscillation frequency		26.88	33.6	40.32	MHz
$F_{CLK33M6\_MON}$	Oscillation frequency		26.88	33.6	40.32	MHz

7.4 Power-on reset

All outputs open; T_j = -40 °C to 150 °C, unless otherwise specified.

Table 25. Power-on reset

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PORVS_R}	V_S POR rising threshold		4.5	4.85	5.2	V
V_{PORVS_F}(1)	V_S POR falling threshold		1.9	2.1	2.3	V
V_{PORVS_HYS}	V_S POR hysteresis		2.5	2.75	3	V

1. *This threshold is valid if V_S had already reached $V_{PORVS\_R(max)}$ previously.*

7.5 LDO1 voltage regulator

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 26. LDO1

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LDO1}	Output voltage tolerance. Including line and load regulation	I_{LOAD} = 100 µA to 120 mA 6.0 V ≤ V_{FBB} ≤ 29 V	4.9	5.0	5.15	V
V_{LDO1_PG}	Power-good rising threshold	V_{LDO1} increasing	4.6	4.8	4.9	V
V_{LDO1_UV}	Undervoltage falling threshold	V_{LDO1} decreasing	3.8	4.0	4.1	V
$t_{LDO1\_PG\_TO}$(1)	LDO1 timeout for power-good		4.8	6	7.5	ms
t_{LDO1_UV}(1)	Undervoltage filter time		12	15	22	µs
V_{LDO1_DP}	Drop-out voltage	I_{LOAD} = 120 mA	-	-	0.8	V
I_{LDO1_Cmax}	Short circuit output current (to GND)	Current limitation	130	175	250	mA
C_{LDO1}(2)	Load capacitor1	Ceramic (±20%)	1	-	10	µF

1. *Digital implementation is guaranteed by scan test.*
2. *Nominal capacitor value required for stability of the regulator. Tested with 1 µF ceramic (± 20%). The capacitor must be located close to the regulator output pin. A 2.2 µF capacitor value is recommended to minimize the DPI (Direct power injection) stress in the application.*

7.6 LDO2 voltage regulator

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.
The same parameter values in both 5 V and 3.3 V conditions applies unless otherwise specified.

Table 27. LDO2

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{LDO2_5}	Output voltage	V_S ≥ 6.0 V	4.9	5.0	5.15	V
V_{LDO2_33}	Output voltage	V_S ≥ 6.0 V	3.23	3.3	3.399	V
$V_{LDO2\_ACC\_25}$(1)	Output voltage tracking accuracy	I_{LOAD} = 100 µA to 5 mA V_{FBB} = 8 V to 18 V T_j = 25 °C	-10	-	10	mV
$V_{LDO2\_ACC\_130}$	Output voltage tracking accuracy	I_{LOAD} = 100 µA to 5 mA V_{FBB} = 8 V to 18 V T_j = 130 °C	-20	-	20	mV
V_{LDO2_OV}	Overvoltage threshold for LDO2		105	108.5	112	%
t_{LDO2_OV}(2)	LDO2 overvoltage filter time		12	15	22	µs
V_{LDO2_PG}	Power-good voltage threshold for LDO2		91.5	95	98.5	%
V_{LDO2_UV}	Undervoltage threshold for LDO2		88	91.5	95	%
$tLDO_{LDO2\_UV}$(2)	LDO2 undervoltage filter time		12	15	22	µs
$t_{LDO2\_PG\_TO}$(2)	LDO2 timeout for power-good		4.8	6	7.5	ms
V_{LDO2_DP}	Drop-out voltage	I_{LOAD} = 10 mA	-	0.5	1.0	V
I_{LDO2_CCmax}	Short circuit output current (to GND)	Current limitation	15	30	45	mA
C_{LDO2}(3)	Load capacitor1	Ceramic (± 20%)	1	-	10	µF

1. *Guarantee by design.*
2. *Digital implementation is guaranteed by scan test.*
3. *Nominal capacitor value required for stability of the regulator. Tested with 1 µF ceramic (±20%). The capacitor must be located close to the regulator output pin. A 2.2 µF capacitor value is recommended to minimize the DPI (Direct power injection) stress in the application.*

7.7 Boost controller

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
3 V ≤ V_S ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 28. Boost controller

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{FBB\_UV\_R}$	BOOST rising enable threshold	Input voltage required on initial start-up to enable the boost	5.0	5.25	5.5	V
$V_{FBB\_UV\_F}$	BOOST falling disable threshold	Power down threshold	4.65	4.9	5.15	V
$V_{FBB\_UV\_HYS}$	Boost enable hysteresis		0.2	0.35	0.5	V
$T_{F\_FBB\_UV}$(1)	digital filter time on FBB POR		12	15	22	µs
V_{FBB_REG1}	VFBB regulation threshold	If BUCK1 and BUCK2 voltage settings are = 3.3 V	7.7	8.0	8.3	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{FBB_REG2}	VFBB regulation threshold	If BUCK1 or BUCK2 voltage settings are above 3.3 V (5.0 or 6.5 V)	9.2	9.5	9.8	V
F_{sw_BOOST}	Switching frequency	Guaranteed by scan	320	400	480	kHz
Boost_DC_Max(1)	Boost duty cycle max	0 V < V_S < V_{S_LOW} t_{ON} = 63 cycles of 33.6 MHz main clk	34	75	83	%
Boost_DC_High(1)	Boost duty cycle high	V_{S_LOW} < V_S < V_{S_MID} t_{ON} = 55 cycles of 33.6 MHz main clk	30	65.5	73	%
Boost_DC_Low(1)	Boost duty cycle low	V_{S_MID} < V_S < V_{S_HIGH} t_{ON} = 46 cycles of 33.6 MHz main clk	25	54.8	61	%
Boost_DC_Min(1)	Boost duty cycle min	V_{S_HIGH} < V_S t_{ON} = 38 cycles of 33.6 MHz main clk	21	45.2	50	%
Boost_DC_LP(1)	Boost duty cycle in low power mode	V_{S_HIGH} < V_S t_{ON} = 2 cycles of 800 kHz	27	50.0	66	%
$V_{S\_Low\_R}$	V_S comparator threshold V_{S_LOW} Rising		4.25	4.5	4.75	V
$V_{S\_Low\_F}$	V_S comparator threshold V_{S_LOW} Falling		3.75	4.0	4.25	V
$V_{S\_Low\_HYS}$	V_S comparator threshold V_{S_LOW} Hysteresis		0.4	0.5	0.6	V
$V_{S\_Mid\_R}$	V_S comparator threshold V_{S_MID} Rising		5.7	6.0	6.3	V
$V_{S\_Mid\_F}$	V_S comparator threshold V_{S_MID} Falling		5.2	5.5	5.8	V
$V_{S\_Mid\_HYS}$	V_S comparator threshold V_{S_MID} Hysteresis		0.4	0.5	0.6	V
$V_{S\_High\_R}$	V_S comparator threshold V_{S_HIGH} Rising		7.1	7.5	7.9	V
$V_{S\_High\_F}$	V_S comparator threshold V_{S_HIGH} Falling		6.6	7	7.4	V
$V_{S\_High\_HYS}$	V_S comparator threshold V_{S_HIGH} Hysteresis		0.4	0.5	0.6	V
V_{Boost_rip}(2)	Boost voltage_ripple	Ripple at 20 kHz All characteristics of all blocks supplied by FBB are guaranteed with external components defined in the Table 50	-	-	2.5	Vpp
I_{Boost}(2)	Boost current capability	Guaranteed with external components defined in the Table 50	0.05	-	4.2	A
$I_{Boost\_LS\_sink1}$	LS driver sink current	V_{FBB} = V_{GLB} = 8.5 V	70	100	130	mA
$I_{Boost\_HS\_source1}$	HS driver source current	V_{FBB} = 8.5 V V_{GLB} = 0 V	70	100	130	mA
$I_{Boost\_LS\_sink2}$	LS driver sink current	V_{FBB} = 8.5 V V_{GLB} = 0.5 V	20	35	55	mA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{Boost\_HS\_source2}$	HS driver source current	V_{FBB} = 8.5 V V_{GLB} = 8 V	10	25	45	mA
$R_{Boost\_gate\_pulldown}$	Resistive gate pull-down	BOOST_DIS = 1	3	5	8	kΩ
$I_{VS\_\_stdby}$	Current leakage on V_S pin in stdby		-	-	2	µA
I_{VS_Sense}	Sink current on V_S active mode		120	180	250	µA
V_{BOOST_VDSM1}	Boost drain-source rising threshold voltage	BOOST_DSMON_TH = 000	220	250	280	mV
V_{BOOST_VDSM2}	Boost drain-source rising threshold voltage	BOOST_DSMON_TH = 001	420	450	480	mV
V_{BOOST_VDSM3}	Boost drain-source rising threshold voltage	BOOST_DSMON_TH = 010	610	650	680	mV
V_{BOOST_VDSM4}	Boost drain-source rising threshold voltage	BOOST_DSMON_TH = 011	800	850	900	mV
V_{BOOST_VDSM5}	Boost drain-source rising threshold voltage	BOOST_DSMON_TH = 100	1.04	1.1	1.16	V
V_{BOOST_VDSM6}	Boost drain-source rising threshold voltage	BOOST_DSMON_TH = 101	1.24	1.3	1.36	V
V_{BOOST_VDSM7}	Boost drain-source rising threshold voltage	BOOST_DSMON_TH = 110	1.35	1.5	1.65	V
V_{BOOST_VDSM8}	Boost drain-source rising threshold voltage	BOOST_DSMON_TH = 111	1.53	1.7	1.87	V
$V_{BOOST\_VDSM\_HYS\_H}$	Boost drain-source threshold voltage hysteresis for high VDSM codes	BOOST_DSMON_TH = 1xx	75	100	125	mV
$V_{BOOST\_VDSM\_HYS\_L}$	Boost drain-source threshold voltage hysteresis for low VDSM codes	BOOST_DSMON_TH = 0xx	25	50	75	mV
$V_{TH\_BYPASS\_R1}$	Bypass external MOSFET enable comparator rising threshold, rising V_{VS}	If BUCK1 and BUCK2 voltage settings are = 3.3 V	8.65	9	9.35	V
$V_{TH\_BYPASS\_F1}$	Bypass external MOSFET disable comparator falling threshold, rising V_{VS}	If BUCK1 and BUCK2 voltage settings are = 3.3 V	8.4	8.75	9.1	V
$V_{TH\_BYPASS\_R2}$	Bypass external MOSFET enable comparator rising threshold, rising V_{VS}	If BUCK1 or BUCK2 voltage settings are above 3.3 V (5.0 or 6.5 V)	10.15	10.50	10.85	V
$V_{TH\_BYPASS\_F2}$	Bypass external MOSFET disable comparator falling threshold, rising V_{VS}	If BUCK1 or BUCK2 voltage settings are above 3.3 V (5.0 or 6.5 V)	9.9	10.25	10.60	V
$T_{F\_BYPASS\_EN}$ (1)	digital filter time on bypass external MOSFET enable comparator output		12	15	22	µs
$T_{F\_BYPASS\_DIS}$ (1)	digital filter time on bypass external MOSFET disable comparator output		0	0.24	0.4	µs
V_{BYPASS_VDSM1}	Bypass drain-source rising threshold voltage	BYPASS_DSMON_TH = 000	75	125	175	mV
V_{BYPASS_VDSM2}	Bypass drain-source rising threshold voltage	BYPASS _DSMON_TH = 001	125	165	225	mV
V_{BYPASS_VDSM3}	Bypass drain-source rising threshold voltage	BYPASS _DSMON_TH = 010	175	225	275	mV

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BYPASS_VDSM4}	Bypass drain-source rising threshold voltage	BYPASS _DSMON_TH =011	225	275	325	mV
V_{BYPASS_VDSM5}	Bypass drain-source rising threshold voltage	BYPASS _DSMON_TH = 100	275	325	375	mV
V_{BYPASS_VDSM6}	Bypass drain-source rising threshold voltage	BYPASS _DSMON_TH =101	325	375	425	mV
V_{BYPASS_VDSM7}	Bypass drain-source rising threshold voltage	BYPASS _DSMON_TH = 110	375	425	475	mV
V_{BYPASS_VDSM8}	Bypass drain-source rising threshold voltage	BYPASS _DSMON_TH = 111	425	475	525	mV
$V_{BYPASS\_VDSM\_HYS}$	Bypass drain-source threshold voltage hysteresis	BYPASS_DSMON_TH = xxx	25	50	75	mV
$T_{F\_BYPASS\_VDSM}$(1)	Digital filter time on bypass drain-source threshold		12	15	22	µs
$T_{B\_BYPASS\_VDSM}$(1)	Blanking time on bypass drain-source comparator		90	110	142	µs
$R_{bypass\_gate\_discharge}$	Bypass gate discharge resistor	FBB - GBY = 2 V FBB = 7 and GBY = 5 turn OFF	100	220	600	Ω
$I_{bypass\_gate\_charge}$	Bypass gate charge current	GBY = 5 V FBB = 13.5 V	0.4	1.2	2	mA

1. *Digital implementation is guaranteed by scan test.*
2. *Guaranteed by design.*

7.8 BUCK1 converter

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
8.5 V ≤ V_{IN12} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 29. BUCK1 converter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN12_H}	Input voltage range	V_{out_buck1} = 6.5 V	9.2	14	29	V
V_{IN12_M}	Input voltage range	V_{out_buck1} = 5 V	7.7	14	29	V
V_{IN12_L}	Input voltage range	V_{out_buck1} = 3.3 V	6	14	29	V
$V_{out\_buck1\_33}$(1)	Output voltage	BUCK1_PU_VALUE = 00 Transients and ripple not included V_{IN12} = 8.5 V to 16 V I_{load} = 50 mA to 1.5 A Freq. = 400 kHz	3.23	3.3	3.399	V
$V_{out\_buck1\_5}$(1)	Output voltage	BUCK1_PU_VALUE = 01 Transients and ripple not included V_{IN12} = 8.5 V to 16 V I_{load} = 50 mA to 1.5 A Freq. = 400 kHz	4.9	5	5.15	V
$V_{out\_buck1\_65}$(1)	Output voltage	BUCK1_PU_VALUE = 1x Transients and ripple not included V_{IN12} = 8.5 V to 16 V I_{load} = 50 mA to 1.5 A Freq. = 400 kHz	6.37	6.5	6.695	V
$V_{out\_UV\_buck1\_err}$	Output undervoltage threshold monitor range		86	90	94	%

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{out\_PG\_buck1}$	Output power-good threshold monitor range		88	92	96	%
$V_{out\_OV\_buck1\_err}$	Output overvoltage threshold monitor range		103	107	111	%
$t_{buck1\_PG\_TO}$ (2)	Output power-good time-out		4.8	6	7.5	ms
$t_{buck1\_UV\_TO}$ (2)	V_{out} undervoltage time-out filter		25	30	41	µs
$t_{buck1\_OV\_TO}$ (2)	V_{out} overvoltage time-out filter		25	30	41	µs
$R_{DSON\_HS\_buck1\_25}$ (3)	HS switch ON resistance at 1.5 A	V_{IN12} = 14 V T_j = 25 °C	-	0.095	0.12	Ω
$R_{DSON\_HS\_buck1\_130}$	HS switch ON resistance at 1.5 A	V_{IN12} = 14 V T_j = 130 °C	-	-	0.165	Ω
$R_{DSON\_LS\_buck1\_25}$	LS switch ON resistance at 1.5 A	V_{IN12} = 14 V T_j = 25 °C	-	0.095	0.12	Ω
$R_{DSON\_LS\_buck1\_130}$	LS switch ON resistance at 1.5 A	V_{IN12} = 14 V T_j = 130 °C	-	-	0.165	Ω
$I_{limit\_buck1\_000}$	Peak switching current limit at V_{IN12} = 14 V	BUCK1_IPEAK = 000	1.7	2	2.3	A
$I_{limit\_buck1\_001}$	Peak switching current limit at V_{IN12} = 14 V	BUCK1_IPEAK = 001	2.125	2.5	2.875	A
$I_{limit\_buck1\_010}$	Peak switching current limit at V_{IN12} = 14 V	BUCK1_IPEAK = 010	2.55	3	3.45	A
$I_{limit\_buck1\_011}$	Peak switching current limit at V_{IN12} = 14 V	BUCK1_IPEAK = 011	2.975	3.5	4.025	A
$I_{limit\_buck1\_100}$	Peak switching current limit at V_{IN12} = 14 V	BUCK1_IPEAK = 100	3.2	4	4.6	A
$I_{limit\_buck1\_101}$	Peak switching current limit at V_{IN12} = 14 V	BUCK1_IPEAK = 101	3.5	4.5	5.175	A
$I_{limit\_buck1\_11X}$	Peak switching current limit at V_{IN12} = 14 V	BUCK1_IPEAK = 11X	3.75	5	5.75	A
$t_{buck1\_OC\_TO}$ (2)	Over current filter time		125	150	200	µs
$T_{softstart\_buck1\_00}$ (3)	Soft start time slope when start-up	BUCK1_SS_VALUE = 00	9.9	16.5	23.1	V/ms
$T_{softstart\_buck1\_01}$ (3)	Soft start time slope when start-up	BUCK1_SS_VALUE = 01	4.95	8.25	11.9	V/ms
$T_{softstart\_buck1\_10}$ (3)	Soft start time slope when start-up	BUCK1_SS_VALUE = 10	1.98	3.3	4.62	V/ms
$T_{softstart\_buck1\_11}$ (3)	Soft start time slope when start-up	BUCK1_SS_VALUE = 11	0.99	1.65	2.31	V/ms
$F_{sw\_buck1\_0}$	Switching frequency	BUCK1_FREQ = 0	2.0	2.4	2.8	MHz
$F_{sw\_buck1\_1}$	Switching frequency	BUCK1_FREQ = 1	333	400	470	kHz
$F_{spread\_buck1\_24}$ (3)	Spread spectrum range (Enable/ disable by BUCK1_SPREAD_ENA)	F_{sw_buck1} = 2.4 MHz	-8	-	+8	%
$F_{spread\_buck1\_04}$ (3)	Spread spectrum range (enable/ disable by BUCK1_SPREAD_ENA)	F_{sw_buck1} = 400 kHz	-20	-	+20	%
RPD_OFF_buck1	Pull-down resistor in off	V_{out} = 3.3 V	60	75	90	Ω
I_{buck1_LP}	Output current in low power mode	V_{IN12} = 14 V	-	-	100	mA
$V_{buck1\_LP\_00}$	Output voltage in low power mode	BUCK1_PU_VALUE = 00 Line/load transients not included	3.08	3.3	3.51	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		Ripple included V_{IN12} = 8.5 V to 16 V I_{load} = 50 µA to I_{Buck1_LP}				
$V_{buck1\_LP\_01}$	Output voltage in low power mode	BUCK1_PU_VALUE = 01 Line/load transients not included Ripple included V_{IN12} = 8.5 V to 16 V I_{load} = 50 µA to I_{Buck1_LP}	4.75	5	5.25	V
$V_{buck1\_LP\_1X}$	Output voltage in low power mode	BUCK1_PU_VALUE = 1x Line/load transients not included Ripple included V_{IN12} = 8.5 V to 16 V I_{load} = 50 µA to I_{Buck1_LP}	6.22	6.5	6.78	V
$I_{sw\_limit\_buck1\_LP}$	Peak current limit in LP mode		750	1000	1250	mA
$V_{out\_UV\_buck1\_LP\_33}$	Output undervoltage threshold monitor in LP mode	V_{out} = 3.3 V	2.8	2.9	3.05	V
$V_{out\_UV\_buck1\_LP\_5}$	Output undervoltage threshold monitor in LP mode	V_{out} = 5 V	4.15	4.35	4.65	V
$V_{out\_UV\_buck1\_LP\_65}$	Output undervoltage threshold monitor in LP mode	V_{out} = 6.5 V	5.45	5.65	5.85	V
$V_{out\_OV\_\_buck1\_LP\_33}$	Output overvoltage threshold monitor in LP mode	V_{out} = 3.3 V	3.55	3.7	3.8	V
$V_{out\_OV\_buck1\_LP\_5}$	Output overvoltage threshold monitor in LP mode	V_{out} = 5 V	5.4	5.65	5.85	V
$V_{out\_OV\_buck1\_LP\_65}$	Output overvoltage threshold monitor in LP mode	V_{out} = 6.5 V	6.9	7.2	7.5	V
$R_{DSON\_HS\_buck1\_LP\_25}$	HS switch ON resistance at 0.1 A	V_{IN12} = 14 V T_j = 25 °C	-	0.72	0.9	Ω
$R_{DSON\_HS\_buck1\_LP\_130}$	HS switch ON resistance at 0.1 A	V_{IN12} = 14 V T_j = 130 °C	-	-	1.3	Ω
$R_{DSON\_LS\_buck1\_LP\_25}$	LS switch ON resistance at 0.1 A	V_{IN12} = 14 V T_j = 25 °C	-	0.2	0.3	Ω
$R_{DSON\_LS\_buck1\_LP\_130}$	LS switch ON resistance at 0.1 A	V_{IN12} = 14 V T_j = 130 °C	-	-	0.4	Ω

1. *Guaranteed by bench measurements. Performances verified in applicative conditions. Tested in static load conditions (I_{load} = 150 mA at 400 kHz and 2.4 MHz).*
2. *Digital implementation is guaranteed by scan test.*
3. *Guaranteed by design.*

7.9 BUCK2 converter

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
8.5 V ≤ V_{IN12} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.
BUCK2 shares the same input as BUCK1.

Table 30. BUCK2 converter

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN12_H}	Input voltage range	V_{out_buck2} = 6.5 V	9.2	14	29	V
V_{IN12_M}	Input voltage range	V_{out_buck2} = 5 V	7.7	14	29	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN12_L}	Input voltage range	V_{out_buck2} = 3.3 V	6	14	29	V
$V_{out\_buck2\_33}$ (1)	Output voltage	BUCK2_PU_VALUE = 00 Transients and ripple not included V_{IN12} = 8.5 V to 16 V I_{load} = 50 mA to 1.5 A Freq. = 400 kHz	3.23	3.3	3.399	V
$V_{out\_buck2\_5}$ (1)	Output voltage	BUCK2_PU_VALUE = 01 Transients and ripple not included V_{IN12} = 8.5 V to 16 V I_{load} = 50 mA to 1.5 A Freq. = 400 kHz	4.9	5	5.15	V
$V_{out\_buck2\_65}$ (1)	Output voltage	BUCK2_PU_VALUE = 1x Transients and ripple not included V_{IN12} = 8.5 V to 16 V I_{load} = 50 mA to 1.5 A Freq. = 400 kHz	6.37	6.5	6.695	V
$V_{out\_UV\_buck2\_err}$	Output undervoltage threshold monitor range		86	90	94	%
$V_{out\_PG\_buck2}$	Output power-good threshold monitor range		88	92	96	%
$V_{out\_OV\_buck2\_err}$	Output overvoltage threshold monitor range		103	107	111	%
$t_{buck2\_PG\_TO}$ (2)	Output power-good time-out		4.8	6	7.5	ms
$t_{buck2\_UV\_TO}$ (2)	Vout undervoltage time-out filter		25	30	41	µs
$t_{buck2\_OV\_TO}$ (2)	Vout overvoltage time-out filter		25	30	41	µs
$R_{DSON\_HS\_buck2\_25}$	HS switch ON resistance at 1.5 A	V_{IN12} = 14 V T_j = 25 °C	-	0.095	0.12	Ω
$R_{DSON\_HS\_buck2\_130}$	HS switch ON resistance at 1.5 A	V_{IN12} = 14 V T_j = 130 °C	-	-	0.165	Ω
$R_{DSON\_LS\_buck2\_25}$	LS switch ON resistance at 1.5 A	V_{IN12} = 14 V T_j = 25 °C	-	0.095	0.12	Ω
$R_{DSON\_LS\_buck2\_130}$	LS switch ON resistance at 1.5 A	V_{IN12} = 14 V T_j = 130 °C	-	-	0.165	Ω
$I_{limit\_buck2\_000}$	Peak switching current limit at V_{IN12} = 14 V	BUCK2_IPEAK = 000	1.7	2	2.3	A
$I_{limit\_buck2\_001}$	Peak switching current limit at V_{IN12} = 14 V	BUCK2_IPEAK = 001	2.125	2.5	2.875	A
$I_{limit\_buck2\_010}$	Peak switching current limit at V_{IN12} = 14 V	BUCK2_IPEAK = 010	2.55	3	3.45	A
$I_{limit\_buck2\_011}$	Peak switching current limit at V_{IN12} = 14 V	BUCK2_IPEAK = 011	2.975	3.5	4.025	A
$I_{limit\_buck2\_100}$	Peak switching current limit at V_{IN12} = 14 V	BUCK2_IPEAK = 100	3.2	4	4.6	A
$I_{limit\_buck2\_101}$	Peak switching current limit at V_{IN12} = 14 V	BUCK2_IPEAK = 101	3.5	4.5	5.175	A
$I_{limit\_buck2\_11x}$	Peak switching current limit at V_{IN12} = 14 V	BUCK2_IPEAK = 11x	3.75	5	5.75	A
$t_{buck2\_OC\_TO}$ (2)	Over current filter time		125	150	200	µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{softstart\_buck2\_00}$ (3)	Soft start time slope when start-up	BUCK2_SS_VALUE = 00	9.9	16.5	23.1	V/ms
$T_{softstart\_buck2\_01}$ (3)	Soft start time slope when start-up	BUCK2_SS_VALUE = 01	4.95	8.25	11.9	V/ms
$T_{softstart\_buck2\_10}$ (3)	Soft start time slope when start-up	BUCK2_SS_VALUE = 10	1.98	3.3	4.62	V/ms
$T_{softstart\_buck2\_11}$ (3)	Soft start time slope when start-up	BUCK2_SS_VALUE = 11	0.99	1.65	2.31	V/ms
$F_{sw\_buck2\_0}$	Switching frequency	BUCK2_FREQ = 0	2.0	2.4	2.8	MHz
$F_{sw\_buck2\_1}$	Switching frequency	BUCK2_FREQ = 1	333	400	470	kHz
$F_{spread\_buck2\_24}$ (3)	Spread spectrum range (enable/ disable by BUCK2_SPREAD_ENA)	F_{sw_buck2} = 2.4 MHz	-8	-	+8	%
$F_{spread\_buck2\_04}$ (3)	Spread spectrum range (enable/ disable by BUCK2_SPREAD_ENA)	F_{sw_buck2} = 400 kHz	-20	-	+20	%
PHI_buck2 (3)(2)	Phase shift to BUCK1		-	225	-	deg
$R_{PD\_OFF\_buck2}$	Pull-down resistor in off	V_{out} = 3.3 V	60	75	90	Ω
I_{buck2_LP}	Output current in low power mode	V_{IN12} = 14 V	-	-	100	mA
$V_{buck2\_LP\_00}$	Output voltage in low power mode	BUCK2_PU_VALUE = 00 Line/load transients not included Ripple included V_{IN12} = 8.5 V to 16 V I_{load} = 50 µA to I_{Buck2_LP}	3.08	3.3	3.51	V
$V_{buck2\_LP\_01}$	Output voltage in low power mode	BUCK2_PU_VALUE = 01 Line/load transients not included Ripple included V_{IN12} = 8.5 V to 16 V I_{load} = 50 µA to I_{Buck2_LP}	4.75	5	5.25	V
$V_{buck2\_LP\_1X}$	Output voltage in low power mode	BUCK2_PU_VALUE = 1x Line/load transients not included Ripple included V_{IN12} = 8.5 V to 16 V I_{load} = 50 µA to I_{Buck2_LP}	6.22	6.5	6.78	V
$I_{sw\_limit\_buck2\_LP}$	Peak current limit in LP mode		750	1000	1250	mA
$V_{out\_UV\_buck2\_LP\_33}$	Output undervoltage threshold monitor in LP mode	V_{out} = 3.3 V	2.8	2.9	3.05	V
$V_{out\_UV\_buck2\_LP\_5}$	Output undervoltage threshold monitor in LP mode	V_{out} = 5 V	4.15	4.35	4.65	V
$V_{out\_UV\_buck2\_LP\_65}$	Output undervoltage threshold monitor in LP mode	V_{out} = 6.5 V	5.45	5.65	5.85	V
$V_{out\_OV\_buck2\_LP\_33}$	Output overvoltage threshold monitor in LP mode	V_{out} = 3.3 V	3.55	3.7	3.8	V
$V_{out\_OV\_buck2\_LP\_5}$	Output overvoltage threshold monitor in LP mode	V_{out} = 5 V	5.4	5.65	5.85	V
$V_{out\_OV\_buck2\_LP\_65}$	Output overvoltage threshold monitor in LP mode	V_{out} = 6.5 V	6.9	7.2	7.5	V
$R_{DSON\_HS\_buck2\_LP\_25}$	HS switch ON resistance at 0.1 A	V_{IN12} = 14 V T_j = 25 °C	-	0.72	0.9	Ω
$R_{DSON\_HS\_buck2\_LP\_130}$	HS switch ON resistance at 0.1 A	V_{IN12} = 14 V T_j = 130 °C	-	-	1.3	Ω
$R_{DSON\_LS\_buck2\_LP\_25}$	LS switch ON resistance at 0.1 A	V_{IN12} = 14 V T_j = 25 °C	-	0.25	0.3	Ω

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$R_{DSON\_LS\_buck2\_LP\_130}$	LS switch ON resistance at 0.1 A	V_{IN12} = 14 V T_j = 130 °C	-	-	0.4	Ω

1. *Guaranteed by bench measurements. Performances verified in applicative conditions. Tested in static load conditions (I_{load} = 150 mA at 400 kHz and 2.4 MHz).*
2. *Digital implementation is guaranteed by scan test.*
3. *Guaranteed by design.*

Below are the efficiency curves for BUCK1 and BUCK2:

Figure 41. V_{out} = 6.5 V and V_{IN12} = 10 V at 400 kHz

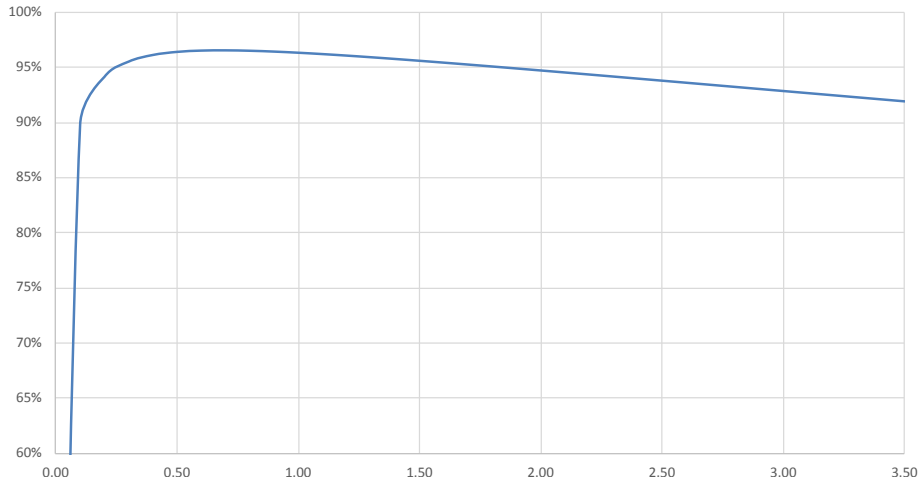


Figure 42. V_{out} = 5.0 V and V_{IN12} = 10 V at 400 kHz

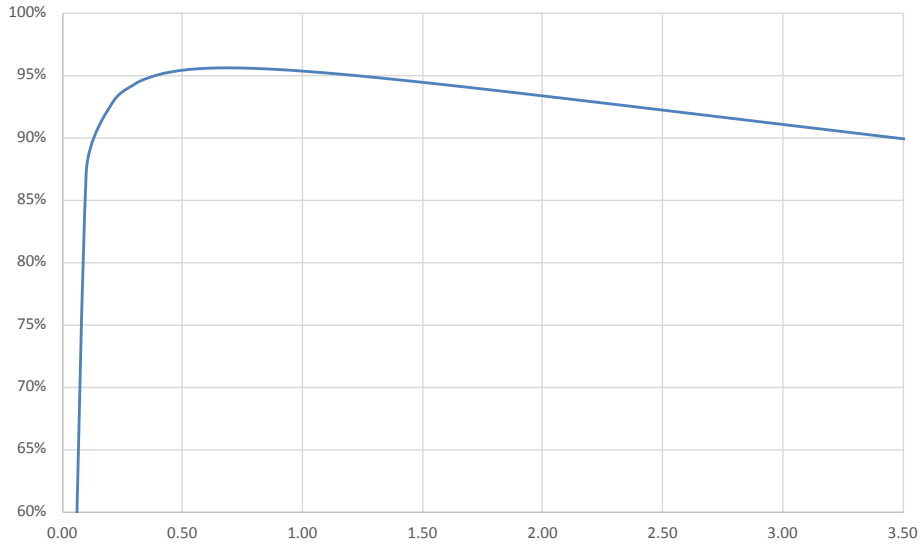


Figure 43. V_{out} = 3.3 V and V_{IN12} = 10 V at 400 kHz

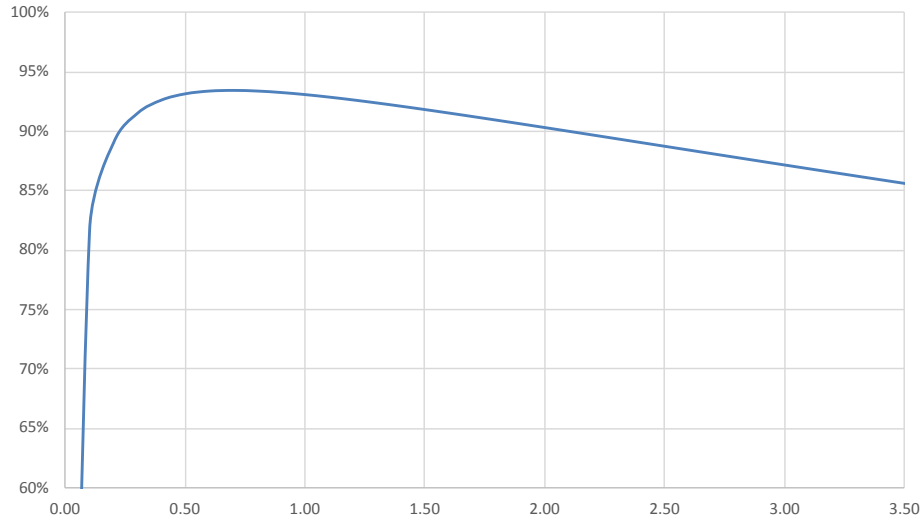


Figure 44. V_{out} = 6.5 V and V_{IN12} = 10 V at 2.4 MHz

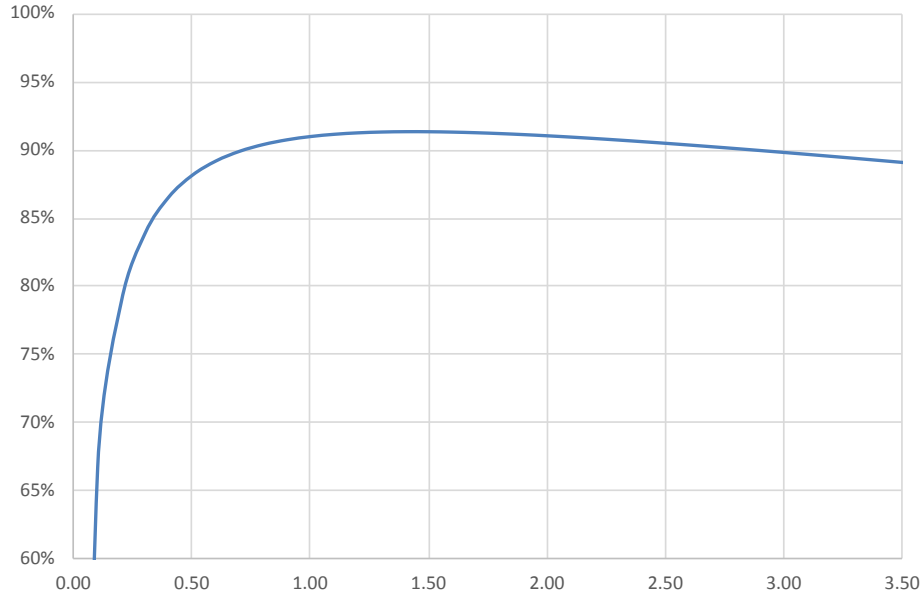


Figure 45. V_{out} = 5.0 V and V_{IN12} = 10 V at 2.4 MHz

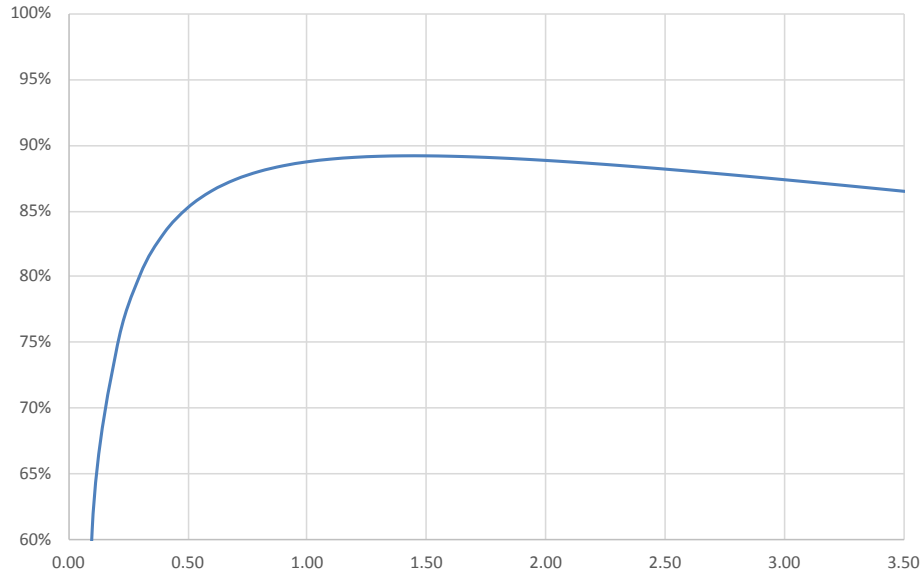
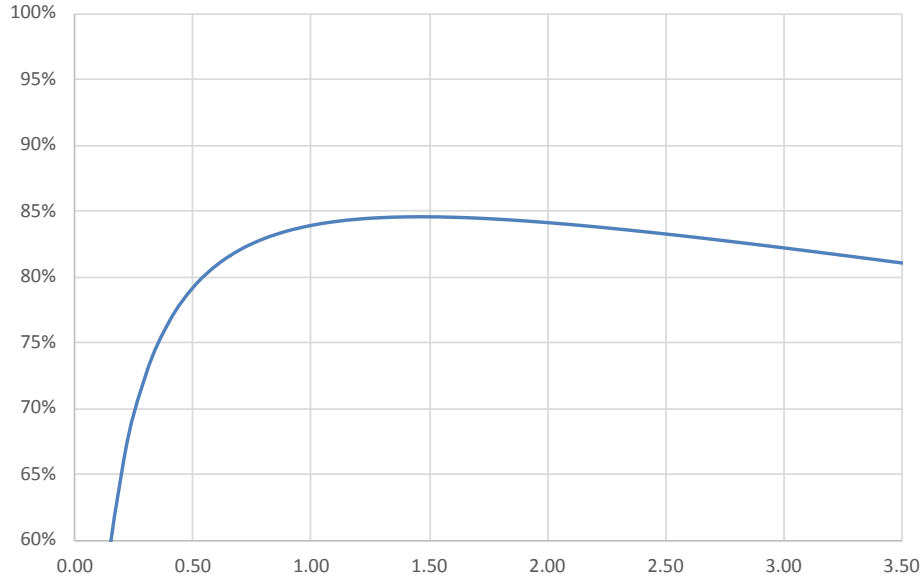
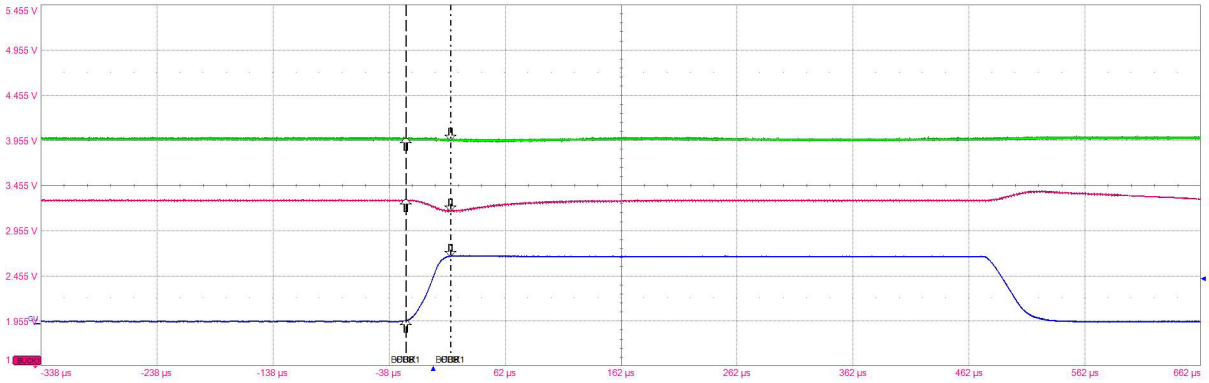


Figure 46. V_{out} = 3.3 V and V_{IN12} = 10 V at 2.4 MHz



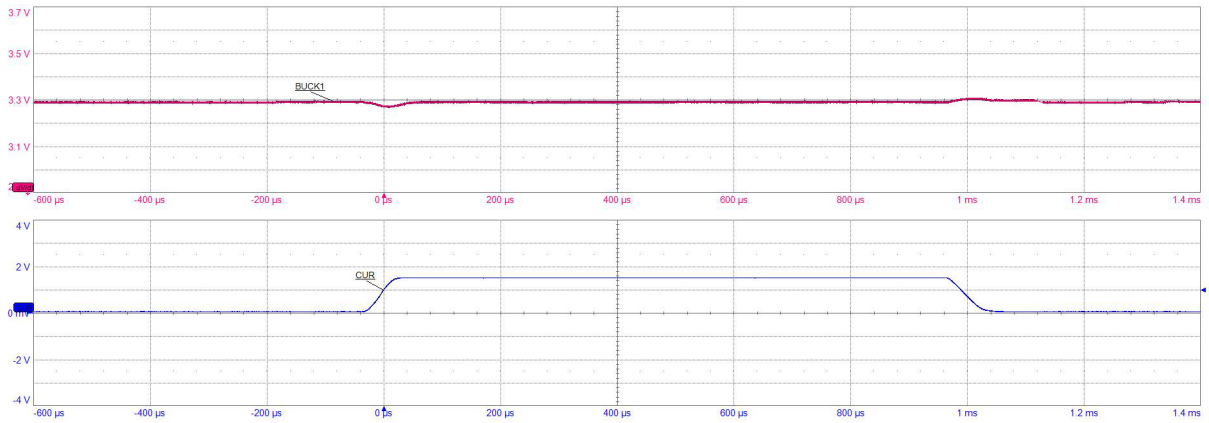
Following load and line transient curves for BUCK1, 2:

Figure 47. Load transient curve for BUCK1, 2 at 3.3 V, f = 400 kHz



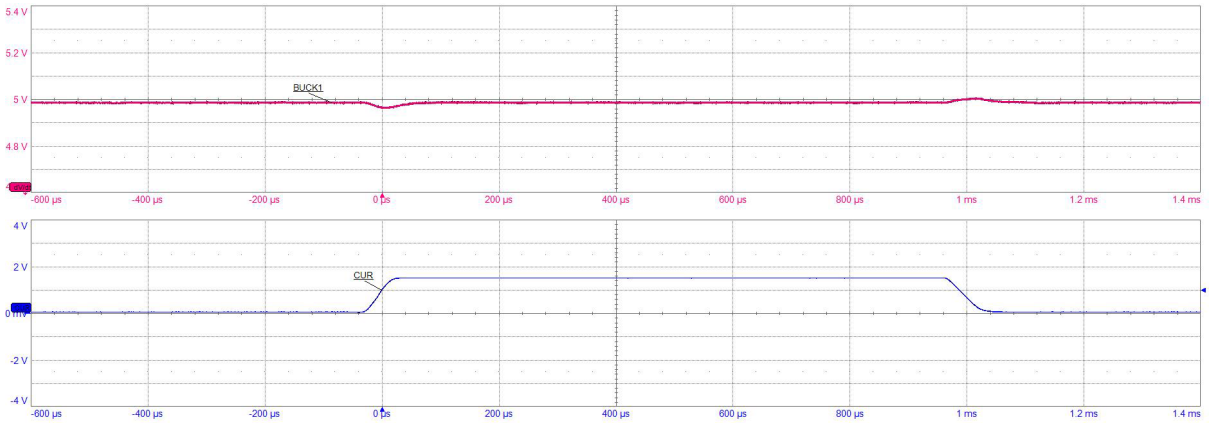
Note: V_{IN12} = 14 V, load current: 65 mA to 1.5 A at 30 A/ms.

Figure 48. Load transient curve for BUCK1, 2 at 3.3 V, f = 2.4 MHz



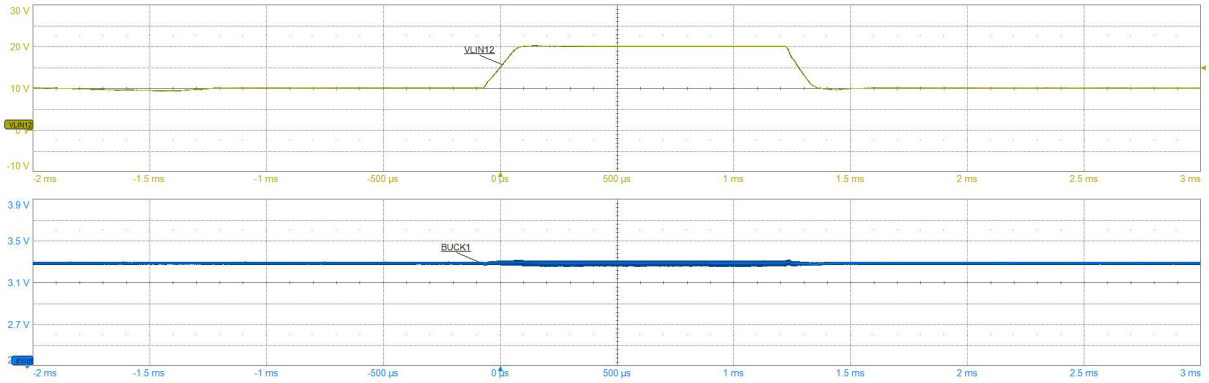
Note: V_{IN12} = 14 V, load current: 65 mA to 1.5 A at 30 A/ms.

Figure 49. Load transient curve for BUCK1, 2 at 5 V, f = 2.4 MHz



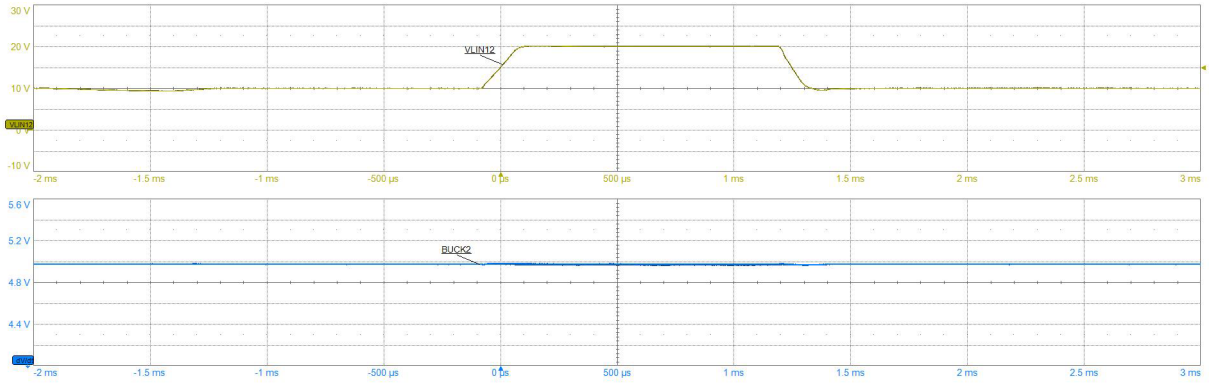
Note: V_{IN12} = 14 V, load current: 65 mA to 1.5 A at 30 A/ms.

Figure 50. Line transient curve for BUCK1, 2 at 3.3 V



Note: I_{load} = 1.5 A, line voltage: 10 V to 20 V at 50 V/ms.

Figure 51. Line transient curve for BUCK1, 2 at 5 V



Note: I_{load} = 1.5 A, line voltage: 10 V to 20 V at 50 V/ms.

Following current limitation curves for BUCK1, 2 based on different input voltages:

Figure 52. Current limitation curves of BUCK1, 2 for V_{out} 3.3 V

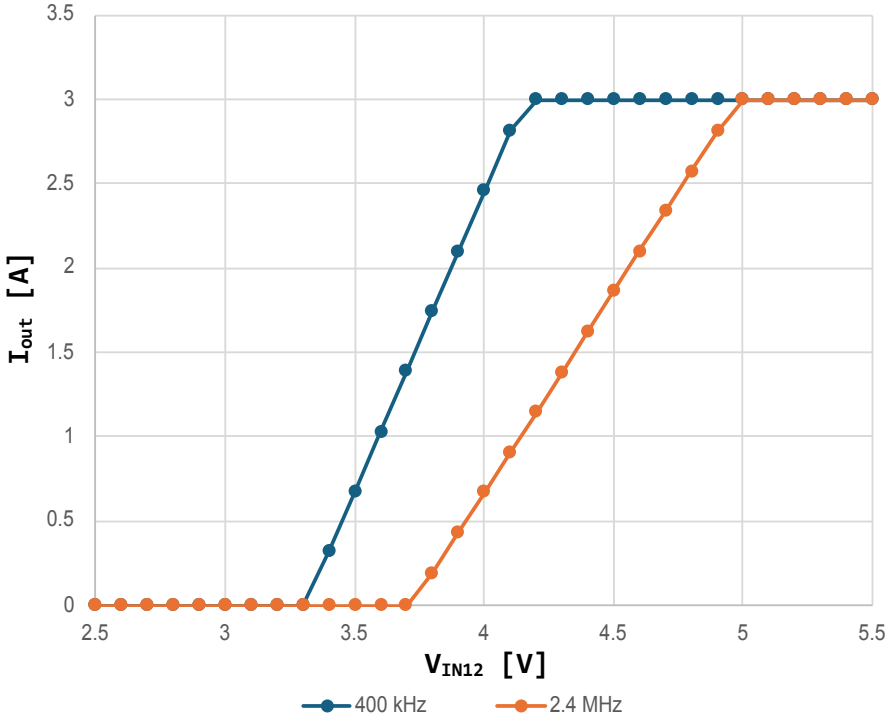


Figure 53. Current limitation curves of BUCK1, 2 for V_{out} 5 V

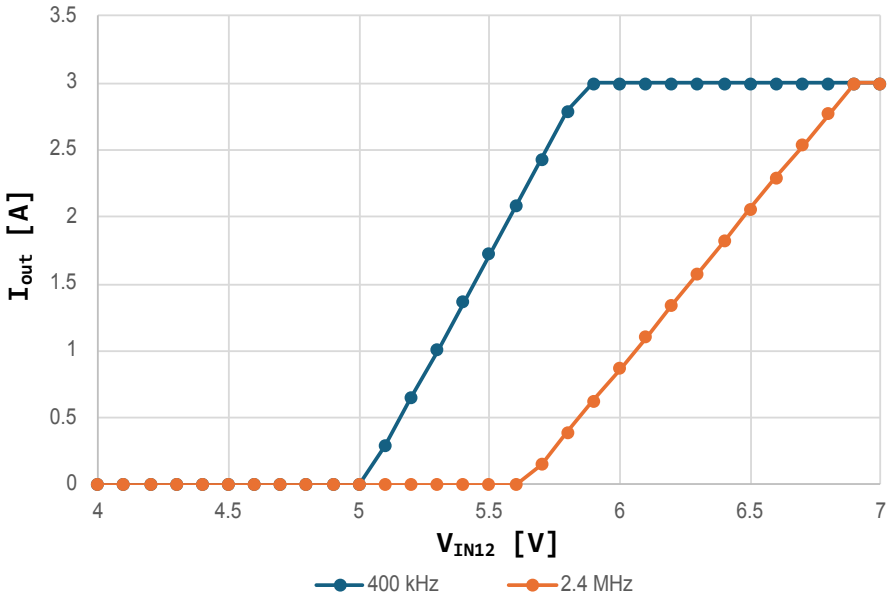
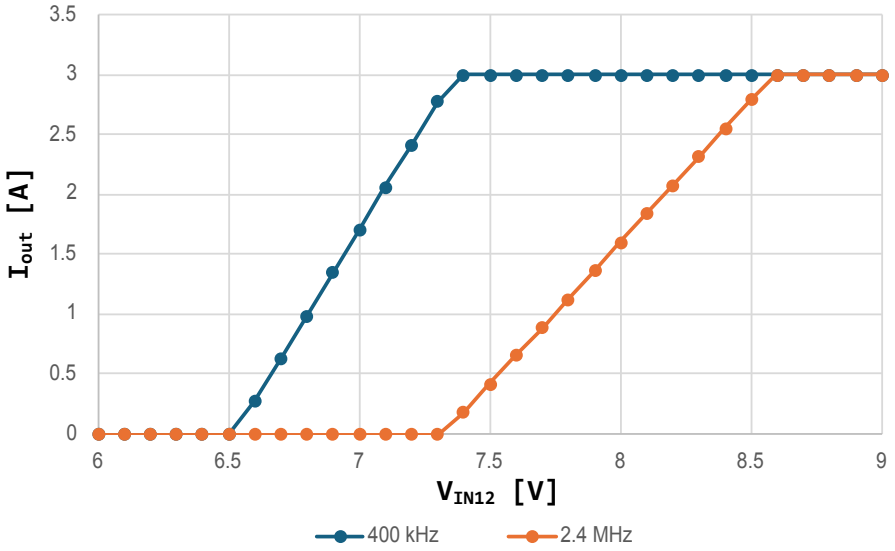


Figure 54. **Current limitation curves of BUCK1, 2 for V_{out} 6.5 V**



7.10 BUCK3 converter

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
3 V ≤ V_{IN13} ≤ 7 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 31. **BUCK3 converter**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{in3_L} (1)(2)	Input voltage range	V_{out_buck3} = 1.25 V or below	3	-	5.25	V
V_{in3_H} (1)(2)	Input voltage range	V_{out_buck3} = 3.3 V	4.85	-	7	V
$V_{out\_buck3\_11X}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 001 BUCK3_FTUNE = 11X V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	0.9215	0.95	0.9785	V
$V_{out\_buck3\_101}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 001 BUCK3_FTUNE = 101 V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	0.9312	0.96	0.9888	V
$V_{out\_buck3\_100}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 001 BUCK3_FTUNE = 100 V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	0.9409	0.97	0.9991	V
$V_{out\_buck3\_000}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 001 BUCK3_FTUNE = 000 V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	0.9506	0.98	1.0094	V
$V_{out\_buck3\_001}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 001 BUCK3_FTUNE = 001 V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	0.9603	0.99	1.0197	V
$V_{out\_buck3\_010}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 001 BUCK3_FTUNE = 010 V_{IN3} = 3 V to 5.5 V	0.97	1.0	1.03	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		I_{load} = 50 mA to 3 A				
$V_{out\_buck3\_011}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 001 BUCK3_FTUNE = 011 V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	0.9797	1.01	1.0403	V
$V_{out\_buck3\_1V1}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 010 V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	1.056	1.1	1.144	V
$V_{out\_buck3\_1V2}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 011 V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	1.152	1.2	1.248	V
$V_{out\_buck3\_1V25}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 100 V_{IN3} = 3 V to 5.5 V I_{load} = 50 mA to 3 A	1.2	1.25	1.3	V
$V_{out\_buck3\_3V3}$ (1)(2)	Output voltage	BUCK3_PU_VALUE = 101 or 11x V_{IN3} = 4.8 V to 7.0 V I_{load} = 50 mA to 3 A	3.168	3.3	3.432	V
$V_{out\_UV\_buck3}$	Output undervoltage threshold monitor range	For all BUCK3_PU_VALUE except 001	85	90	95	%
$V_{out\_PG\_buck3}$	Output power-good threshold monitor range		87	92	96	%
$V_{out\_OV\_buck3}$	Output overvoltage threshold monitor range	For all BUCK3_PU_VALUE except 001	104	107.5	111	%
$V_{out\_UV\_buck3}$	Output undervoltage threshold monitor range for fine-tune	BUCK3_PU_VALUE = 001	0.8	-	0.9	V
$V_{out\_PG\_buck3\_FT}$	Output power-good threshold monitor range for fine-tune	BUCK3_PU_VALUE = 001	0.82	-	0.92	V
$V_{out\_OV\_buck3\_FT}$	Output overvoltage threshold monitor range for fine-tune	BUCK3_PU_VALUE = 001	1.04	-	1.125	V
$t_{buck3\_PG\_TO}$ (3)	Output power-good timeout		4.8	6	7.5	ms
$t_{buck3\_UV\_TO}$ (3)	Vout undervoltage time-out filter		25	30	41	µs
$t_{buck3\_OV\_TO}$ (3)	Vout overvoltage time-out filter		25	30	41	µs
$R_{DSON\_HS\_buck3\_25}$	HS switch ON resistance at 3 A	V_{IN3} = 5 V T_J = 25 °C	-	0.04	0.08	Ω
$R_{DSON\_HS\_buck3\_130}$	HS switch ON resistance at 3 A	V_{IN3} = 5 V T_J = 130 °C	-	-	0.1	Ω
$R_{DSON\_LS\_buck3\_25}$	LS switch ON resistance at 3 A	V_{IN3} = 5 V T_J = 25 °C	-	0.04	0.08	Ω
$R_{DSON\_LS\_buck3\_130}$		V_{IN3} = 5 V T_J = 130 °C	-	-	0.1	Ω
$I_{limit\_buck3\_00}$	Peak switching current limit	BUCK3_IPEAK = 00	3.4	4	4.6	A
$I_{limit\_buck3\_01}$	Peak switching current limit	BUCK3_IPEAK = 01	4.25	5	5.75	A
$I_{limit\_buck3\_10}$	Peak switching current limit	BUCK3_IPEAK = 10	5.1	6	6.9	A
$I_{limit\_buck3\_11}$	Peak switching current limit	BUCK3_IPEAK = 11	5.95	7	8.05	A
$t_{buck3\_OC\_TO}$ (3)	Over current filter time		125	150	200	µs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{softstart\_buck\_00}$(1)	Soft start time slope when start-up	BUCK3_SS_VALUE = 00	5.28	8.7	12.32	V/ms
$T_{softstart\_buck\_01}$(1)	Soft start time slope when start-up	BUCK3_SS_VALUE = 01	2.64	4.35	6.16	V/ms
$T_{softstart\_buck\_10}$(1)	Soft start time slope when start-up	BUCK3_SS_VALUE = 10	1.08	1.75	2.52	V/ms
$T_{softstart\_buck\_11}$(1)	Soft start time slope when start-up	BUCK3_SS_VALUE = 11	0.552	0.87	1.288	V/ms
F_{sw_buck3}	Switching frequency		2.0	2.4	2.8	MHz
F_{spread_buck3}(1)	Spread spectrum range		-8	-	+8	%
PHI_buck3(1)(3)	Phase shift to BUCK1		200	250	300	deg
RPD_OFF_Buck3	Pull-down resistor in off	V_{out} = 3.3 V	120	150	180	Ω

1. *Guaranteed by design.*
2. *Guaranteed by bench measurements. Performances verified in applicative conditions. Tested in static load conditions (I_{load} = 150 mA).*
3. *Digital implementation is guaranteed by scan test.*

Below are the efficiency curves for BUCK3:

Figure 55. V_{out} = 3.3 V and V_{IN3} = 5 V

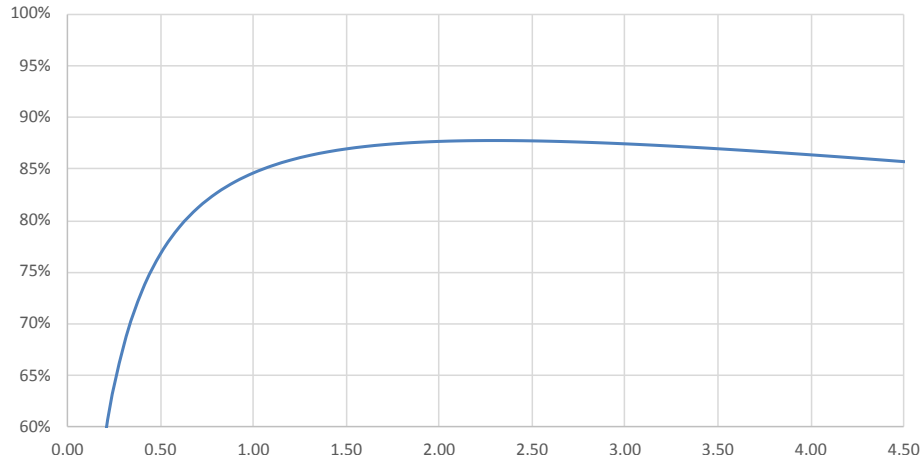


Figure 56. V_{out} = 1.25 V and V_{IN3} = 3.3 V

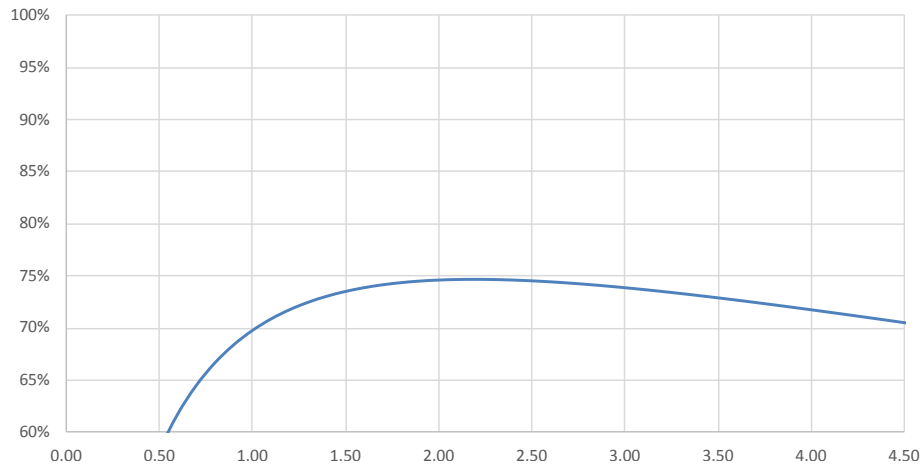


Figure 57. V_{out} = 1.2 V and V_{IN3} = 3.3 V

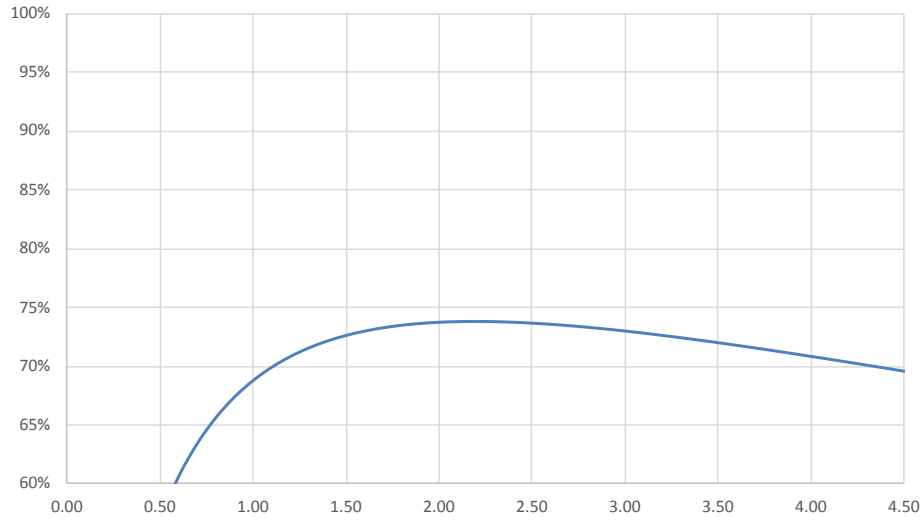


Figure 58. V_{out} = 1.1 V and V_{IN3} = 3.3 V

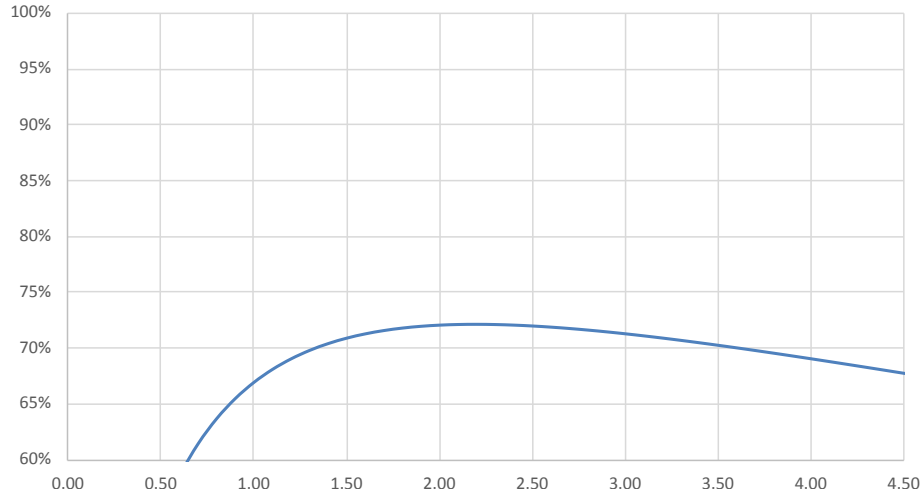
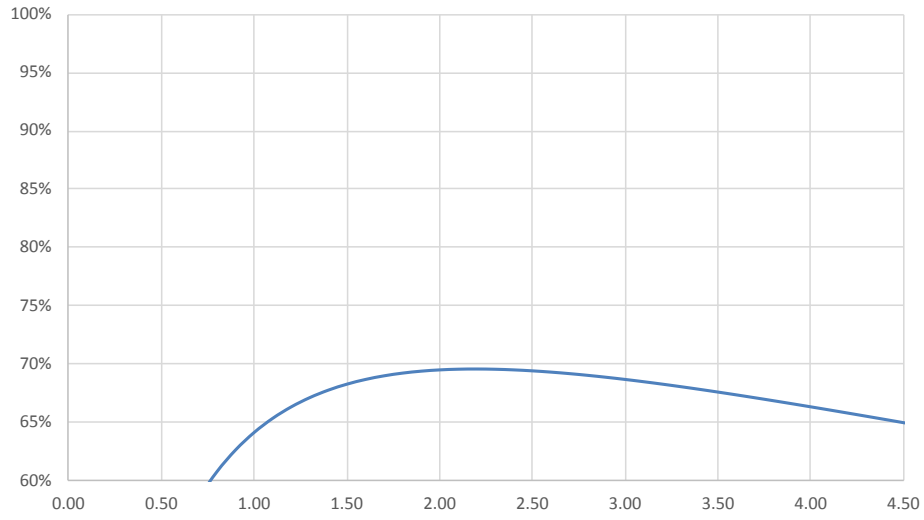
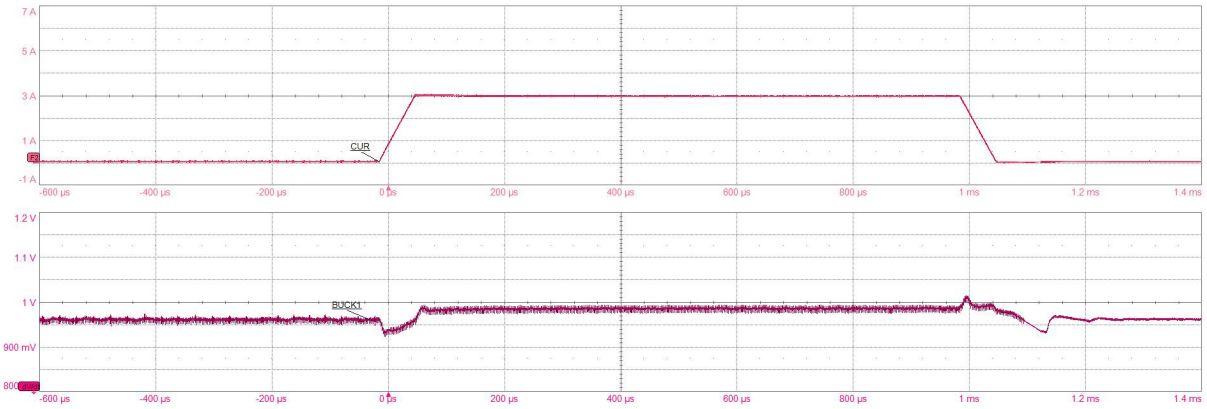


Figure 59. V_{out} = 0.98 V and V_{IN3} = 3.3 V



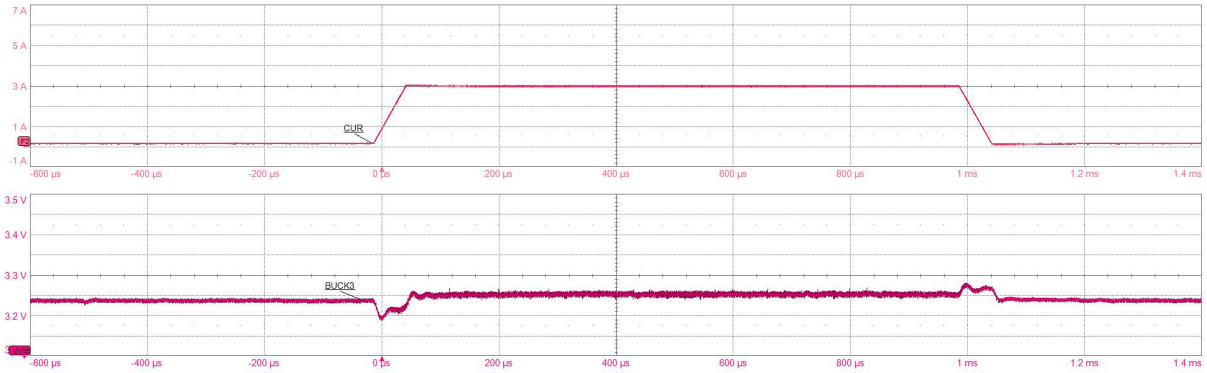
Following load and line transient curves for BUCK3:

Figure 60. Load transient BUCK3 at 0.98 V



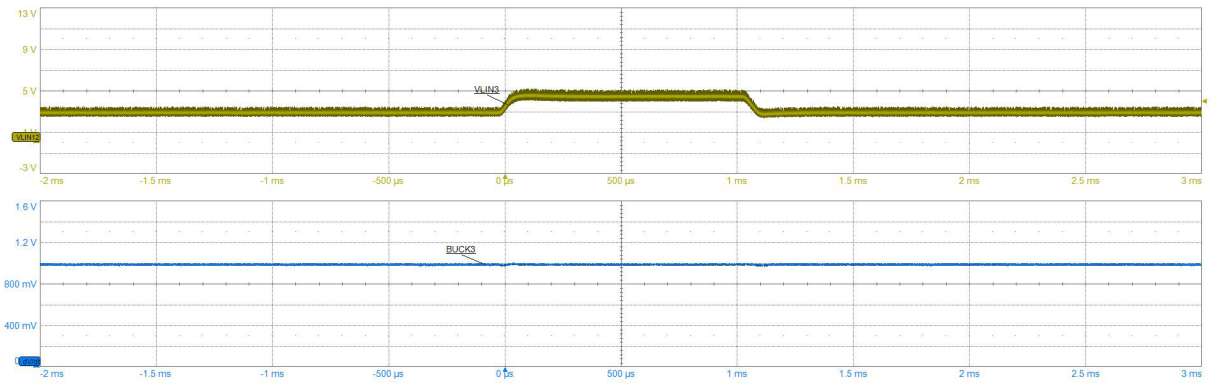
Note: V_{IN3} = 3.3 V, load current: 65 mA to 3 A at 60 A/ms.

Figure 61. Load transient BUCK3 at 3.3 V



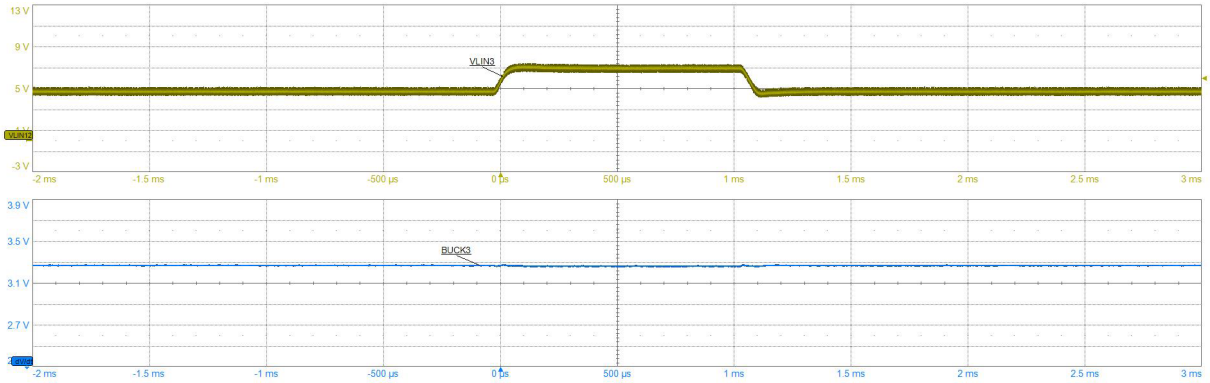
Note: V_{IN3} = 5 V, load current: 65 mA to 3 A at 60 A/ms.

Figure 62. Line transient BUCK3 at 0.98 V



Note: I_{load} = 3 A, line voltage: 3 V to 4.5 V at 30 V/ms.

Figure 63. **Line transient BUCK3 at 3.3 V**



Note: *I_{load} = 3 A, line voltage: 4.75 V to 7 V at 30 V/ms.*

7.11 Watchdog

6.0 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

All watchdog timings are covered by scan.

Table 32. **Watchdog**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LW1}	Long open window 1	LOW_SET <3:0> : 0000	-	-	319	ms
t_{LW2}	Long open window 2	LOW_SET <3:0> : 0001	-	-	479	ms
t_{LW3}	Long open window 3	LOW_SET <3:0> : 0010	-	-	638	ms
t_{LW4}	Long open window 4	LOW_SET <3:0> : 0011	-	-	1025	ms
t_{LW5}	Long open window 5	LOW_SET <3:0> : 0100	-	-	115	ms
t_{LW6}	Long open window 6	LOW_SET <3:0> : 0101	-	-	159	ms
t_{LW7}	Long open window 7	LOW_SET <3:0> : 0110	-	-	230	ms
t_{LW8}	Long open window 8	LOW_SET <3:0> : 0111	-	-	460	ms
t_{LW12}	Long open window 12	LOW_SET <3:0> : 1000-1011	-	-	2300	ms
t_{LW13}	Long open window 13	LOW_SET <3:0> : 1100	-	-	4600	ms
tLW14	Long open window 14	LOW_SET <3:0> : 1101	-	-	6900	ms
t_{LW15}	Long open window 15	LOW_SET <3:0> : 1110	-	-	9200	ms
t_{LW16}	Long open window 16	LOW_SET <3:0> : 1111	-	Infinite	-	-
T_{EFW1}	Early failure window 1	WD_TIME = 0000	-	-	2.8	ms
T_{LFW1}	Late failure window 1	WD_TIME = 0000	10	-	-	ms
T_{SW1}	Safe window 1	WD_TIME = 0000	4.5	-	5.4	ms
T_{EFW2}	Early failure window 2	WD_TIME = 0001 (default value)	-	-	5.3	ms
T_{LFW2}	Late failure window 2	WD_TIME = 0001 (default value)	20	-	-	ms
T_{SW2}	Safe window 2	WD_TIME = 0001 (default value)	8.4	-	11.5	ms
T_{EFW3}	Early failure window 3	WD_TIME = 0010	-	-	17.3	ms
T_{LFW3}	Late failure window 3	WD_TIME = 0010	50	-	-	ms
T_{SW3}	Safe window 3	WD_TIME = 0010	27.1	-	31.5	ms

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{EFW4}	Early failure window 4	WD_TIME = 0011	-	-	31.5	ms
T_{LFW4}	Late failure window 4	WD_TIME = 0011	90	-	-	ms
T_{SW4}	Safe window 4	WD_TIME = 0011	50.4	-	56.8	ms
T_{EFW5}	Early failure window 5	WD_TIME = 0100	-	-	96.2	ms
T_{LFW5}	Late failure window 5	WD_TIME = 0100	250	-	-	ms
T_{SW5}	Safe window 5	WD_TIME = 0100	151.1	-	159.3	ms
T_{EFW6}	Early failure window 6	WD_TIME = 0101	-	-	197.1	ms
T_{LFW6}	Late failure window 6	WD_TIME = 0101	500	-	-	ms
T_{SW6}	Safe window 6	WD_TIME = 0101	308.4	-	319.3	ms
T_{EFW7}	Early failure window 7	WD_TIME = 0110	-	-	299.6	ms
T_{LFW7}	Late failure window 7	WD_TIME = 0110	750	-	-	ms
T_{SW7}	Safe window 7	WD_TIME = 0110	468.1	-	479.4	ms
T_{EFW8}	Early failure window 8	WD_TIME = 0111	-	-	402.1	ms
T_{LFW8}	Late failure window 8	WD_TIME = 0111	1000	-	-	ms
T_{SW8}	Safe window 8	WD_TIME = 0111	627.8	-	638.7	ms
T_{EFW9}	Early failure window 9	WD_TIME = 1000	-	-	630.8	ms
T_{LFW9}	Late failure window 9	WD_TIME = 1000	1600	-	-	ms
T_{SW9}	Safe window 9	WD_TIME = 1000	984	-	1025.1	ms
T_{EFW10}	Early failure window 10	WD_TIME = 1001-1111	-	-	3.2	ms
T_{LFW10}	Late failure window 10	WD_TIME = 1001-1111	78	-	-	ms
T_{SW10}	Safe window 10	WD_TIME = 1001-1111	5	-	50	ms

Figure 64. **Watchdog early, late and safe windows**

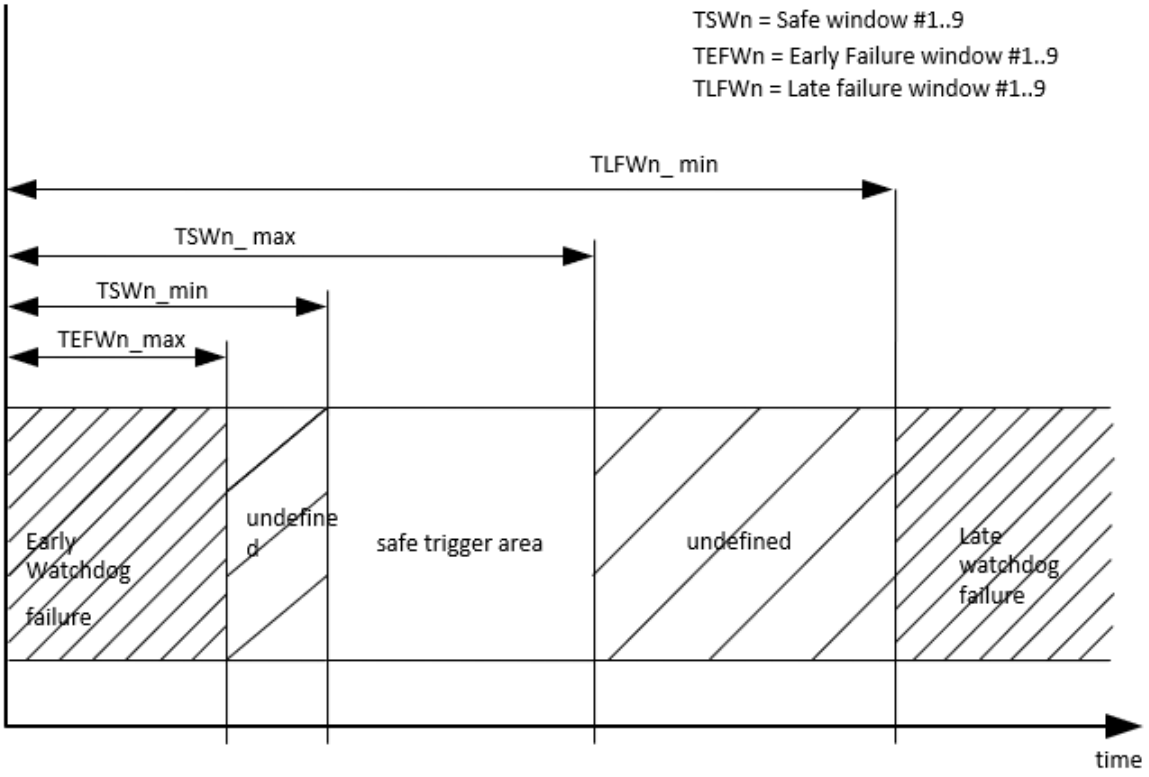
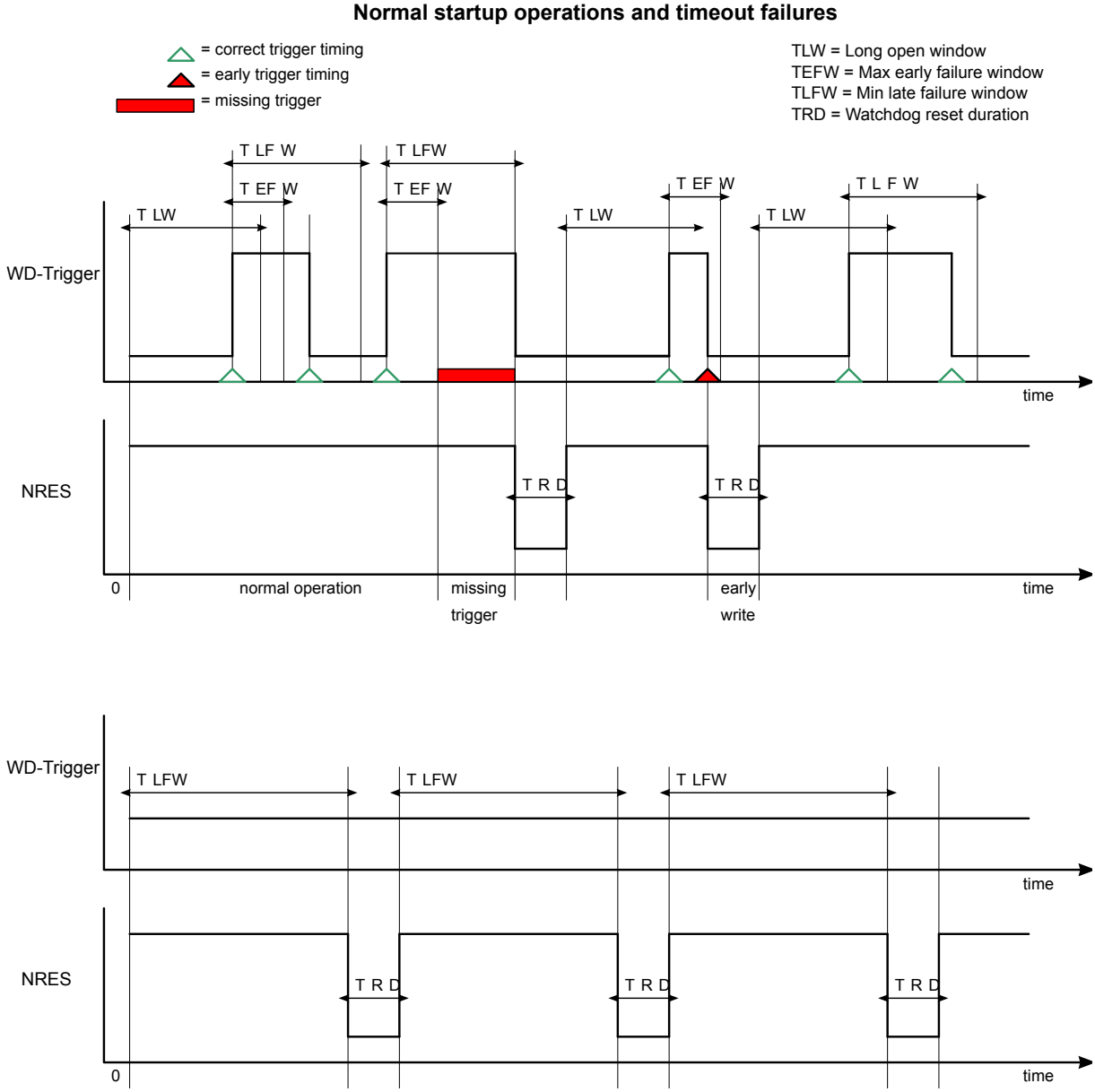


Figure 65. **Watchdog timing**



7.12 High side output OUT_HS

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6.0 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 33. **High side output OUT_HS**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$r_{ON\_OUT\_HS\_25}$	Static drain source On-resistance	V_{FBB} = 13.5 V I_{load} = -15 mA T_{amb} = +25 °C	-	55	80	Ω
$r_{ON\_OUT\_HS\_130}$	Static drain source On-resistance	V_{FBB} = 13.5 V I_{load} = -15 mA T_{amb} = +130 °C	-	-	130	Ω

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{OC\_OUT\_HS}$	Overcurrent threshold	V_{FBB} = 13.5 V	25	33	40	mA
$t_{OC\_OUT\_HS}$(1)	Overcurrent filter time		16	28	40	µs
$t_{BLK\_OC\_OUT\_HS}$(1)	Blanking time of overcurrent	In case of short at enable (to be added to filter time for the minimum t_{ON})	32	46	60	µs
$I_{OLD\_OUT\_HS}$	Open load detection current	V_{FBB} = 13.5 V	0.25	0.7	1.2	mA
$t_{OLD\_OUT\_HS}$(1)	Open load detection time		45	70	95	µs
dV_{OUT_HS}/dt	Slew rate	V_{FBB} = 13.5 V R_{load} = 620 Ω C_{load} = 47 nF from 20% to 80%	0.05	0.8	2	V/µs
$t_{DON\_OUT\_HS}$	Switch ON delay time	V_{FBB} = 13.5 V (from CSN rising 50% to OUT 80%) R_{load} = 620 Ω C_{load} = 47 nF	5	20	40	µs
$t_{DOFF\_OUT\_HS}$	Switch OFF delay time	V_{FBB} = 13.5 V (from CSN rising 50% to OUT 20%) R_{load} = 620 Ω C_{load} = 47 nF	10	60	100	µs
$I_{QLH\_OUT\_HS\_LP}$	Switched-off output Current in low power	V_{OUT_HS} = 0 V Active low power or DEEP-SLEEP modes	-5	-	-	µA
$I_{QLH\_OUT\_HS\_FP}$	Switched-off output Current in full power	V_{OUT_HS} = 0 V Active full power mode	-10	-	-	µA

1. *Digital implementation is guaranteed by scan test.*

7.13 NFSO1 fail safe output

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6.0 V ≤ V_{FBB} ≤ 40 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 34. Low side outputs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{NFSO1_L}	Output low level	I_{NFSO1} = 4 mA	-	-	0.5	V
I_{NFSO1_LK}	Tristate leakage current	V_{NFSO1} = 40 V	-	-	10	µA
t_{NFSO1_rt}	Detection reaction time		-	-	200	µs
R_{NFSO1_PU}	External pull-up resistor		-	30	-	kΩ
$t_{NFSO\_ECHO\_FILT}$	Echo error filter time	On falling edge	91	100	150	µs

7.14 Wake up inputs (WU, IGN)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6.0 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 35. Wake-up Inputs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{WUthp}	Wake-up negative edge threshold voltage	$V_{thp\ min}$ = V_{FBB} * 0.4 $V_{thp\ typ}$ = V_{FBB} * 0.45	5.6	6.3	7	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
		$V_{thp\ max} = V_{FBB} * 0.5$ Value for V_{FBB} = 14 V				
V_{IGNthp}	Wake-up negative edge threshold voltage	$V_{thp\ min} = V_{FBB} * 0.4$ $V_{thp\ typ} = V_{FBB} * 0.45$ $V_{thp\ max} = V_{FBB} * 0.5$ Value for V_{FBB} = 14 V	5.6	6.3	7	V
V_{WUthn}	Wake-up positive edge threshold voltage	$V_{thp\ min} = V_{FBB} * 0.5$ $V_{thp\ typ} = V_{FBB} * 0.55$ $V_{thp\ max} = V_{FBB} * 0.6$ Value for V_{FBB} = 14 V	7	7.7	8.4	V
V_{IGNthn}	Wake-up positive edge threshold voltage	$V_{thp\ min} = V_{FBB} * 0.5$ $V_{thp\ typ} = V_{FBB} * 0.55$ $V_{thp\ max} = V_{FBB} * 0.6$ Value for V_{FBB} = 14 V	7	7.7	8.4	V
V_{HYST_WU}	Hysteresis	$V_{thp\ min} = V_{FBB} * 0.05$ $V_{thp\ typ} = V_{FBB} * 0.1$ $V_{thp\ max} = V_{FBB} * 0.15$ Value for V_{FBB} = 14 V	0.7	1.4	2.1	V
V_{HYST_IGN}	Hysteresis	$V_{thp\ min} = V_{FBB} * 0.05$ $V_{thp\ typ} = V_{FBB} * 0.1$ $V_{thp\ max} = V_{FBB} * 0.15$ Value for V_{FBB} = 14 V	0.7	1.4	2.1	V
t_{WU_stat}(1)	Static wake filter time		50	64	85	µs
t_{IGN_stat}(1)	Static wake filter time		50	64	85	µs
I_{WU_stdby}	Input current in DEEP-SLEEP or active low power mode	V_{WU} < 1 V or V_{WU} > (V_{FBB} - 1.5 V) WU_ENA = 0	-	-	3	µA
I_{IGN_stdby}	Input current in DEEP-SLEEP or active low power mode	V_{IGN} < 1 V or V_{IGN} > (V_{FBB} - 1.5 V) IGN_ENA = 0	-	-	3	µA
$I_{WU\_stdby\_PD}$	Pull-down current in DEEP-SLEEP or active low power modes	V_{WU} < 1 V or V_{WU} > (V_S - 1.5 V) WU_ENA = 1	5	20	60	µA
$I_{WU\_stdby\_PU}$	Pull-up current in DEEP-SLEEP or active low power modes	V_{WU} < 1 V or V_{WU} > (V_S - 1.5 V) WU_ENA = 1	-60	-20	-5	µA
$I_{IGN\_stdby\_PD}$	Pull-down current in DEEP-SLEEP or active low power modes	V_{IGN} < 1 V or V_{IGN} > (V_S - 1.5 V) IGN_ENA = 1	5	20	60	µA
$I_{IGN\_stdby\_PU}$	Pull-up current in DEEP-SLEEP or active low power modes	V_{WU} < 1 V or V_{WU} > (V_S - 1.5 V) WU_ENA = 1	-60	-20	-5	µA
R_{WU_act}	Input resistor to GND in active mode and in DEEP-SLEEP or active low power mode during wake-up input sensing		80	180	300	kΩ
R_{IGN_act}	Input resistor to GND in active mode and in DEEP-SLEEP or active low power mode during wake-up input sensing		80	180	300	kΩ
t_{WU_cyc}(1)	Cyclic wake filter time		12	16	29	µs
t_{IGN_cyc}(1)	Cyclic wake filter time		12	16	29	µs

1. *Digital implementation is guaranteed by scan test.*

7.15 SPI

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
3 V ≤ V_{IO} ≤ 5.4 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 36. Input: CSN

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CSN_L}	Input voltage low threshold		1.0	-	-	V
V_{CSN_H}	Input voltage high threshold		-	-	2.3	V
V_{CSN_HYS}	V_{CSN_H} - V_{CSN_L}		0.2	0.4	-	V
R_{CSN_PU}	CSN pull-up resistor	$V^{(1)}$ = 1.0 V	13	29	55	kΩ
$C_{CSN}^{(1)}$		0 V < $V^{(1)}$ < 5.3 V	-	10	15	pF

1. *The value of input capacity is not measured in production test. Parameter guaranteed by design.*

Table 37. Inputs: CLK, SDI

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CLK_L}	CLK input low threshold		1.0	-	-	V
V_{SDI_L}	SDI input low threshold		1.0	-	-	V
V_{CLK_H}	CLK input high threshold		-	-	2.3	V
V_{SDI_H}	SDI input high threshold		-	-	2.3	V
V_{CLK_HYS}	CLK input hysteresis		0.2	-	-	V
V_{SDI_HYS}	SDI input hysteresis		0.2	-	-	V
I_{CLK}	CLK pull-down current at input	V_{CLK} = 1.0 V	5	20	60	µA
I_{SDI}	SDI pull-down current at input	V_{SDI} = 1.0 V	5	20	60	µA
$C_{in}^{(1)}$	Input capacitance at input CLK, and SDI	0 V < $V_{CLK,SDI}$ < 5.3 V	-	10	15	pF
f_{CLK}	SPI input frequency at CLK		-	-	6	MHz

1. *The value of input capacity is not measured in production test. Parameter guaranteed by design.*

Table 38. SDI, CLK and CSN timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{CLK}	Clock period		166	-	-	ns
t_{CLK_H}	Clock high time		58	-	-	ns
t_{CLK_L}	Clock low time		58	-	-	ns
t_{set_CSN}	CSN setup time, CSN low before rising edge of CLK in active full power mode		150	-	-	ns
$t_{set\_CSN\_LP}$	CSN setup time, CSN low before rising edge of CLK in active low power mode		10000	-	-	ns
t_{set_CLK}	CLK setup time, CLK high before rising edge of CSN		150	-	-	ns
t_{set_SDI}	SDI setup time		25	-	-	ns
t_{hold_SDI}	SDI hold time		25	-	-	ns
$t_{r\_in}^{(1)}$	Rise time of input signal SDI, CLK, CSN			-	25	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{f_in} (1)	Fall time of input signal SDI, CLK, CSN			-	25	ns

1. *Guaranteed by design.*

Table 39. Output: SDO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SDO_L}	Output low level	V_{IO} = 5.0 V I_{SDO} = +4 mA	-	-	0.5	V
V_{SDO_H}	Output high level	V_{IO} = 5.0 V I_{SDO} = -4 mA	4.5	-	-	V
I_{SDO_LK}	Tristate leakage current	V_{IO} = 5.0 V 0 V < V_{SDO} < V_{IO}	-10	-	10	µA

Table 40. SDO timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
t_{r_SDO} (1)	SDO rise time	C_L = 50 pF I_{load} = -4 mA 20% to 80%		-	25	ns	B.026
t_{f_SDO} (1)	SDO fall time	C_L = 50 pF I_{load} = 4 mA 20% to 80%		-	25	ns	B.027
$t_{en\_SDO\_tri\_L}$ (1)	SDO enable time from high impedance to low level	C_L = 50 pF I_{load} = 4 mA Pull-up load to V_{IO}		50	100	ns	B.028
$t_{dis\_SDO\_tri\_L}$ (1)	SDO disable time from low level to high impedance	C_L = 50 pF I_{load} = 4 mA Pull-up load to V_{IO}		50	100	ns	B.029
$t_{en\_SDO\_tri\_H}$ (1)	SDO enable time from high impedance to high level	C_L = 50 pF I_{load} = -4 mA Pull-down load to GND		50	100	ns	B.030
$t_{dis\_SDO\_H\_tri}$ (1)	SDO disable time from high level to high impedance	C_L = 50 pF I_{load} = -4 mA		50	100	ns	
t_{d_SDO} (1)	SDO delay time	V_{SDO} < 0.2 *V_{IO} or V_{SDO} > 0.8 *V_{IO} C_L = 50 pF		30	60	ns	B.031

1. *Guaranteed by design.*

Note: See the Figure 67.

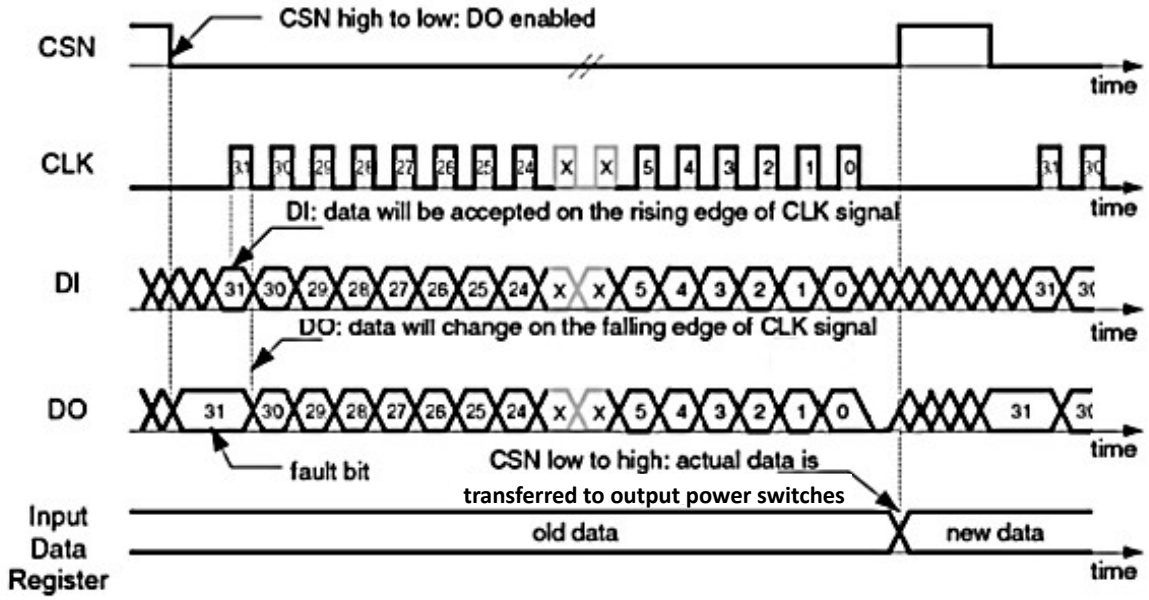
Table 41. CSN timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
t_{CSN_HI,min_act} (1)	Minimum CSN high time, active mode	Transfer of SPI-command to input register	0.5	-	-	µs	B.032
t_{CSN_HI,min_lp} (1)	Minimum CSN high time, low power modes	Transfer of SPI-command to input register	5	-	-	µs	-
$t_{CSNfail}$ (1)	CSN low timeout		20	35	50	ms	B.033

1. *Covered by scan.*

Note: See the Figure 68.

Figure 66. SPI - Transfer timing diagram



The SPI can be driven by a microcontroller with its SPI peripheral running in the following modes:

- CPOL = 0
- CPHA = 0

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

Figure 67. SPI - Input timing

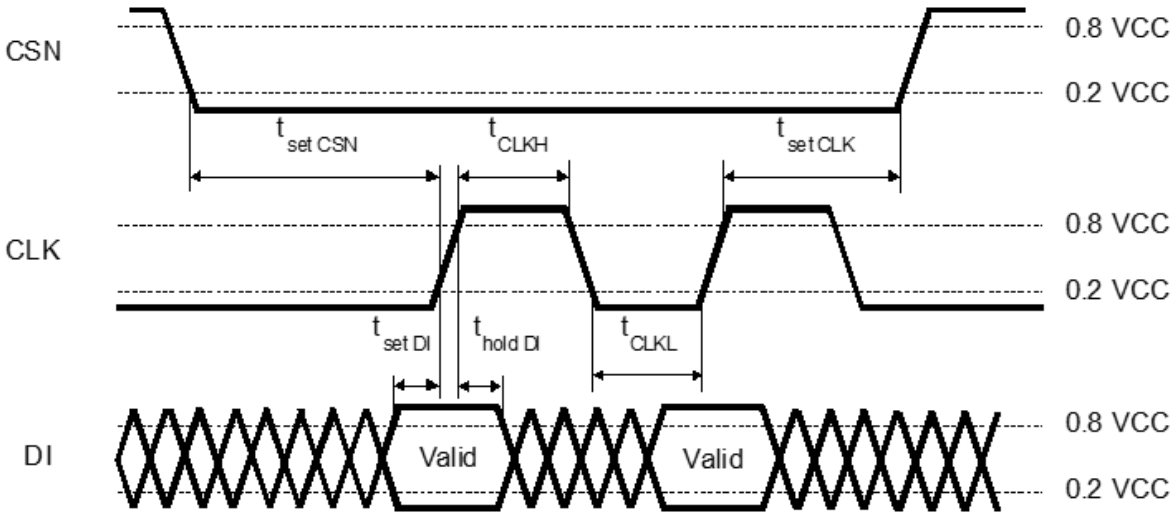


Figure 68. **SPI - Output timing**

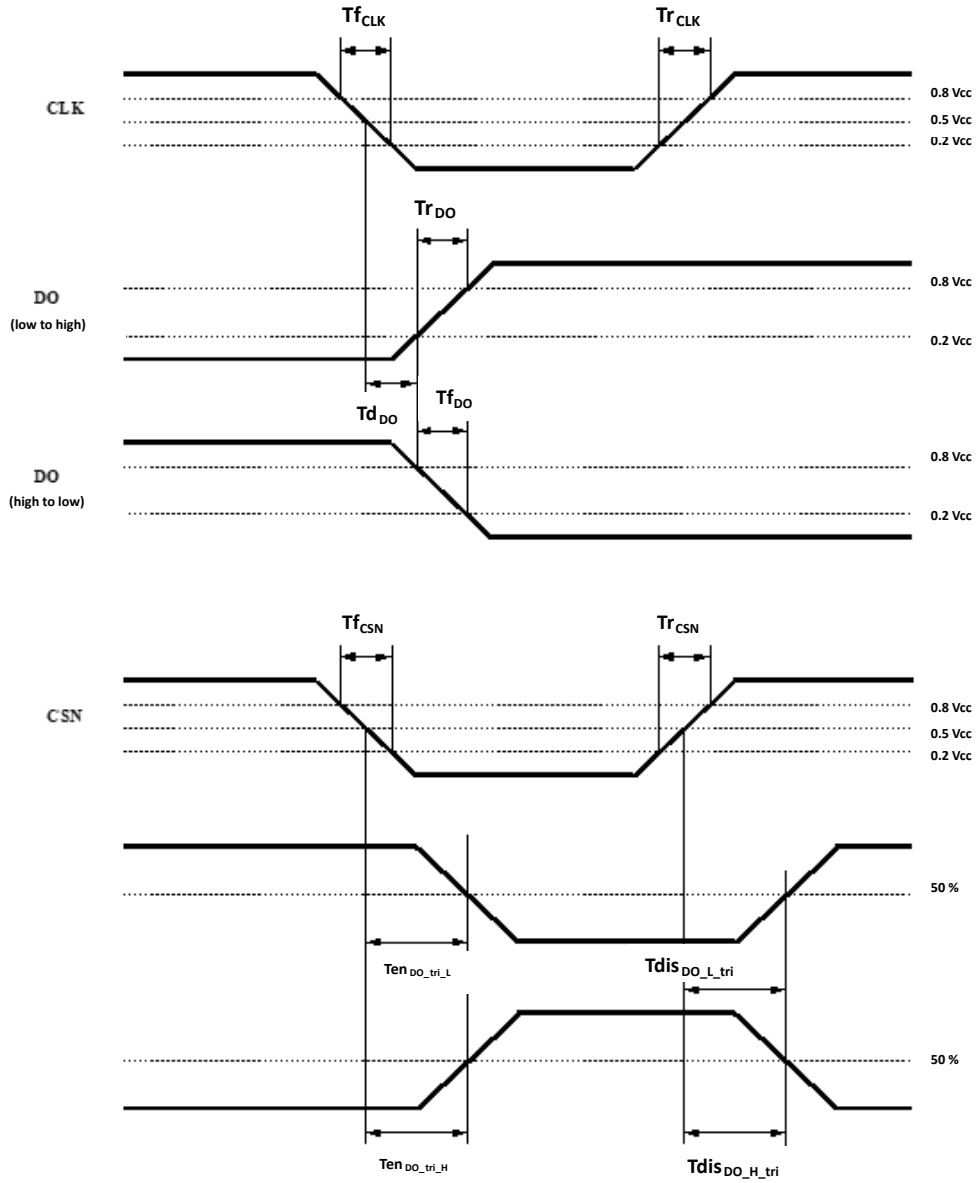


Figure 69. **SPI CSN - Output timing**

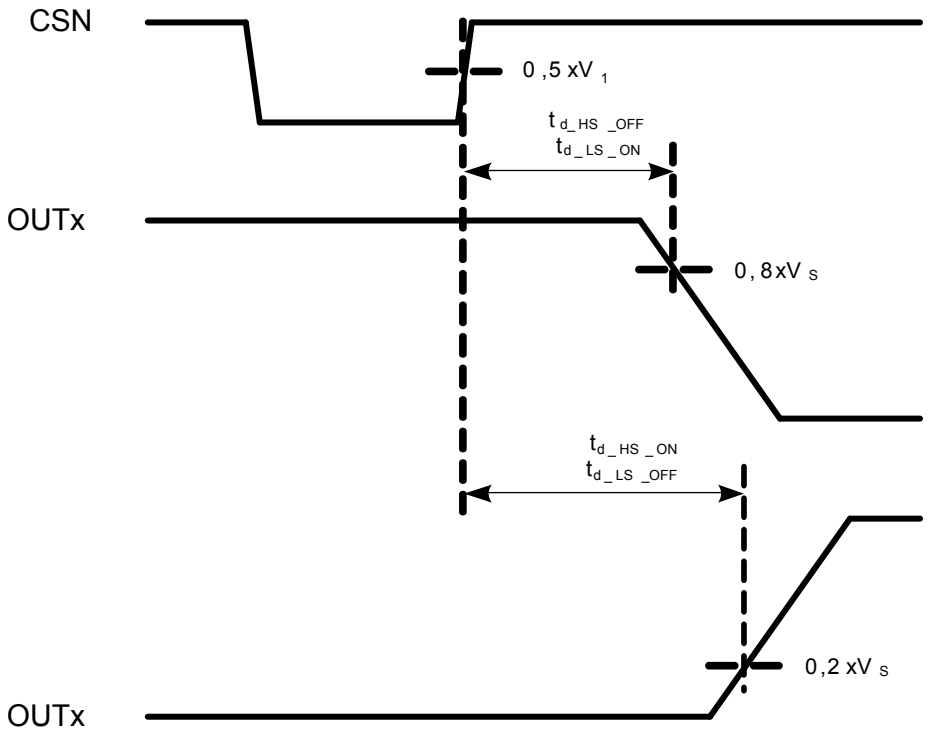
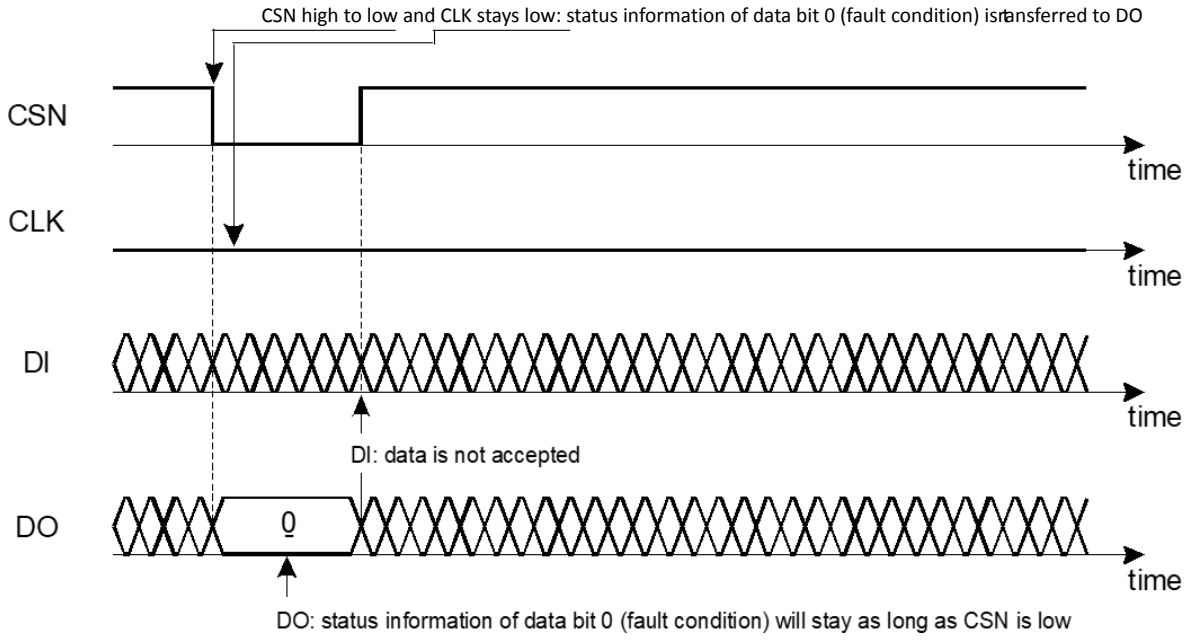


Figure 70. **SPI - CSN low to high transition and global status bit access**



7.16 SWDBG input

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
3 V ≤ V_{FBB} ≤ 20 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 42. **SWDBG input**

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{SWDBG_L}	Input voltage low threshold		1.0	-	-	V
V_{SWDBG_H}	Input voltage high threshold for WDC disable		-	-	2.3	V
V_{SWDBG_HYS}	Input hysteresis		0.2	-	-	V
t_{SWDBG_TO}(1)	Software-debug timeout		8.3	10	12.6	s
R_{SWDBG_PD}	Pull-down resistor	V_{SWDBG} = 6 to 20 V	13	29	55	kΩ
$V_{NVM\_EMU\_L}$	Input low threshold for NVM emulation exit		6.1	-	-	V
$V_{NVM\_EMU\_H}$	Input voltage high threshold for transition to NVM emulation		-	-	9.4	V
$V_{NVM\_EMU\_HYS}$	Input hysteresis for NVM emulation		0.3	-	-	V
C_{SWDBG}(2)	SWDBG input capacitance		-	-	15	pF

1. *Digital implementation is guaranteed by scan test.*
2. *Guaranteed by design.*

7.17 ADC characteristics

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6.0 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 43. ADC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{con}	Conversion time for 1 channel	Tested by scan	2.49	3	3.51	µs
t_{con_2ADC}	Conversion time between 2 ADC measurements	Tested by scan	32.3	39	45.6	µs
f_{ADC}	Clock frequency	Tested by scan	6.72	8.4	10.08	MHz
Acc(1)	Accuracy	Voltage divider+reference	-2	-	2	%
Acc22	Accuracy	Overall accuracy for WU input: V_{WU} = 22 V	-3	-	3	%
Acc18	Accuracy	Overall accuracy for WU input: V_{WU} = 18 V	-3.5	-	3.5	%
Acc6	Accuracy	Overall accuracy for WU input: V_{WU} = 6 V	-6	-	6	%
Acc4	Accuracy	Overall accuracy for WU input: V_{WU} = 4.5 V	-8	-	8	%
$IE_I I$	Integral linearity error		-	4	6	LSB
$IE_D I$	Differential linearity error		-	2	4	LSB
V_{AINVS}	Conversion voltage range (WU and IGN)		1	-	40	V
LSB_T	Thermal LSB		0.471	0.496	0.521	°C
LSB_V	Voltage LSB (WU, IGN, VS and FBB)		38	40	42	mV

1. *Guaranteed by design.*

7.18 IRQ interrupt

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
3.0 V ≤ V_{IO} ≤ 5.5 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 44. Interrupt output

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IRQ_L}	output low level	I_{IRQ} = +4 mA	-	-	0.5	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IRQ_LK}	Leakage current	V_{IRQ} = 20 V V_{IO} = 3.3 V	-	-	100	µA
$I_{IRQ\_LK\_5V}$	Leakage current when IRQ is disabled	V_{IRQ} = 5.0 V V_{IO} = 5.0 V	-	-	1	µA
R_{IRQ_PU}	IRQ internal pull-up resistor for echo	V_{IRQ} = 1 V	13	29	55	kΩ
t_{IRQ_react} (1)	Interrupt reaction time		-	-	40	µs
$t_{IRQ\_ECHO\_FILT}$	IRQ echo error filter time		91	100	150	µs

1. *Guaranteed by scan.*

7.19 FIN1 input

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
3.0 V ≤ V_{IO} ≤ 5.5 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 45. FIN1 input

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{FIN1_L}	Input voltage low threshold		1.0	-	-	V
V_{FIN1_H}	Input voltage high threshold		-	-	2.3	V
V_{FIN1_HYS}	Input voltage hysteresis		0.2	-	-	V
R_{FIN1_PU}	FIN1 pull-up resistor to V_{IO}	V_{IO} = 5.0 V V_{FIN1} = 1.0 V Defined by CR FCCU_STATIC_ERROR bit	13	29	55	kΩ
R_{FIN1_PD}	FIN1 pull-down resistor to GND	V_{IO} = 5.0 V V_{FIN1} = 1.0 V Defined by CR FCCU_STATIC_ERROR bit	13	29	55	kΩ
C_{FIN1} (1)	FIN1 input capacitance		-	-	15	pF

1. *Guaranteed by design.*

7.20 Timer

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
6.0 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.
All timer timings are covered by scan.

Table 46. Timer values

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{ON1}	Timer on time	T1_ENA = 000 (default value)	0.08	0.1	0.14	ms
t_{ON2}	Timer on time	T1_ENA = 001	0.25	0.3	0.39	ms
t_{ON3}	Timer on time	T1_ENA = 010	0.83	1	1.27	ms
t_{ON4}	Timer on time	T1_ENA = 011	8.3	10	12.5	ms
t_{ON5}	Timer on time	T1_ENA = 1xx	16.6	20	25	ms
T1	Timer period	T1_PER = 000 (default value)	8.3	10	12.5	ms
T2	Timer period	T1_PER = 001	16.6	20	25	ms

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T3	Timer period	T1_PER = 010	41.6	50	62.5	ms
T4	Timer period	T1_PER = 011	83	100	125	ms
T5	Timer period	T1_PER = 100	166	200	250	ms
T6	Timer period	T1_PER = 101	416	500	625	ms
T7	Timer period	T1_PER = 110	830	1000	1250	ms
T8	Timer period	T1_PER = 110	1660	2000	2500	ms

7.21 Reset output (NRST)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
3.0 V ≤ V_{IO} ≤ 5.5 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 47. Reset output

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{NRST_L}	Output low level	I_{NRST} = +4 mA	-	-	0.5	V
I_{NRST_LK}	Leakage current	V_{NRST} = 20.0 V V_{IO} = 3.3 V	-	-	100	µA
$I_{NRST\_LK\_5V}$	Leakage current when NRST is disabled	V_{NRST} = 5.0 V V_{IO} = 5.0 V	-	-	1	µA
R_{NRST_PU}	NRST internal pull-up resistor for echo	V_{NRST} = 1.0 V	13	29	55	kΩ
t_{NRST_rt}(1)	Reset reaction time		-	-	40	µs
t_{NRST_WDR}(1)	Low pulse duration time	In case of WD error	3.2	-	-	ms
t_{NRST_FCCU}(1)	Low pulse duration time	In case of FCCU error	4.8	-	-	ms
$t_{NRST\_ECHO\_FILT}$(1)	NRST echo error filter time		91	100	150	µs

1. *Guaranteed by scan.*

7.22 VREG voltage regulator

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
7.5 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 48. VREG

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{VREG}	Output voltage	In active-Full power V_{FBB} ≥ 7.5 V I_{load} = 150 mA	3.2	3.3	3.4	V
V_{VREG_LP}	Output voltage	In active-Low power V_{FBB} ≥ 7.5 V I_{load} = 15 mA	3.2	3.3	3.4	V
V_{VREG_OV}	Overvoltage threshold for V_{REG}		3.45	3.6	3.8	V
$V_{VREG\_OV\_LP}$	Overvoltage threshold for V_{REG} in LP		3.45	3.6	3.8	V
t_{VREG_OV}(1)	V_{REG} overvoltage filter time		12	15	22	µs
V_{VREG_UV}	Under voltage threshold for V_{REG}		2.7	2.85	3.05	V
$V_{VREG\_UV\_LP}$	Undervoltage threshold for V_{REG} in LP		2.7	2.85	3	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{VREG_UV}(1)	V_{REG} undervoltage filter time		12	15	22	µs
t_{VREG_stup}(1)	V_{REG} max start-up delay time for power-good		1.6	2	2.51	ms
I_{VREG_CCmax}	Short circuit output current (to GND)	Current limitation in active-full power	125	260	380	mA
C_{VREG}(2)	Load capacitor	Ceramic	3	4.7	10	µF

1. *Digital implementation guaranteed by scan test.*
2. *Nominal capacitor value required for stability of the regulator. Tested with 4.7 µF ceramic (±20%). The capacitor must be located close to the regulator output pin.*

7.23 BIST timing

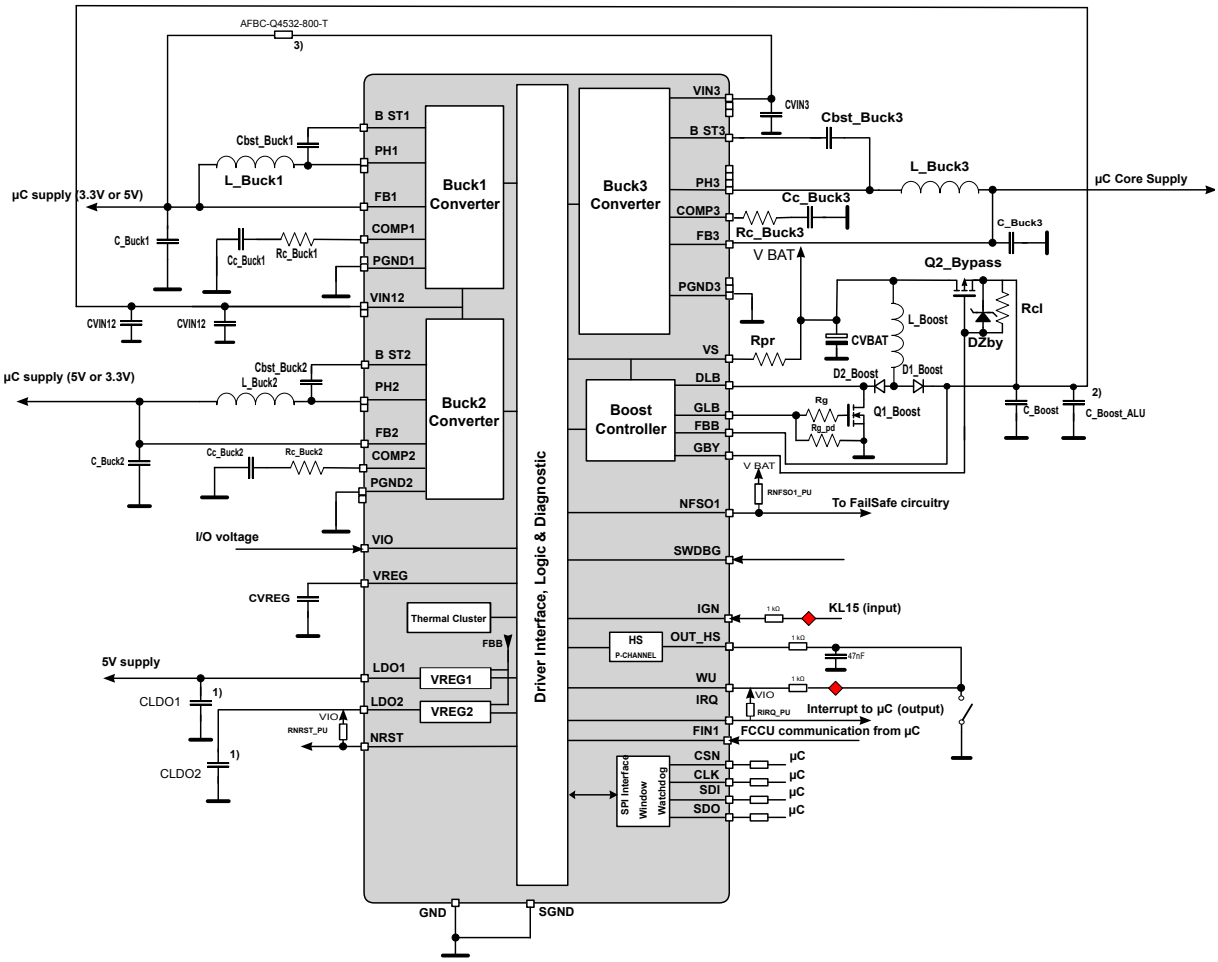
The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
7.5 V ≤ V_{FBB} ≤ 29 V, T_j = -40 °C to 150 °C, unless otherwise specified.

Table 49. BIST timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{LBIST}	Logical BIST execution timing	Covered by scan	12.1	14.6	18.3	ms
T_{ABIST}	Analog BIST execution timing	Covered by scan	83	100	188	µs

8 Application circuit

Figure 71. **Typical application circuit**



1)For EMC optimization purposes, capacitance could be redimensioned (2.2 µF recommended)
2)Optional to improve ripple on boost voltage
3)Only needed for EMC performances

ESD Protection for ECU pins

8.1 External components

Table 50. **External components (referred to pictures in the related sections)**

Component	Block/Usage	Min	Typ	Max	Unit	Note
C_{VBAT}(1)	Capacitance at V_{bat}	40	50	-	µF	ESR: < 15 mΩ Capacitance change or temperature coefficient: < | 22%| Rated voltage: > 40 VDC X7S SMD Choice: GCJ32EC71H106KA01
$C_{\_Boost}$(1)	Capacitance at FBB	40	50	150	µF	ESR: < 15 mΩ Capacitance change or temperature coefficient: < | 22%| Rated voltage: > 40 VDC

Component	Block/Usage	Min	Typ	Max	Unit	Note
						X7S SMD Choice: GCJ32EC71H106KA01
$C_{\_Boost\_ALU}$(1)	Option ALU capacitance at FBB	0	100	150	µF	ESR: < 30 mΩ Capacitance change or temperature coefficient: < | 32%| Rated voltage: > 40 VDC AL ELEC CAP SMD Choice: GYC1H101MCQ1GS
$Q1_{\_Boost}$	-	-	-	-	-	$R_{DS(ON)}$: < 10 mΩ $V_{(BR)DSS}$: > 40 V V_{GS}: ±20 V $I_{D\ (continuous)}$: > 20 A $I_{D\ (pulse)}$: > 40 A V_{GS_TH}: < 3 V Choice: STL105N4LF7AG
$D1_{\_Boost}$ $D2_{\_Boost}$	-	-	-	-	-	Schottky $I_{F(AV)}$: > 25 A V_{RRM}: > 40 V $V_{F(max)}$: < 0.7 V Choice: STPS3045DJF
$L_{\_Boost}$	BOOST inductance	0.8	1	1.2	µH	DCR: < 10 mΩ I_{sat}: > 20 A Derating < 40% Choice: IHLP-4040DZ-11
R_{pr}	Resistor for VS pin protection	0.95	1	1.05	K Ω	-
R_g	Serial gate resistor of $Q1_{\_BOOST}$	2.09	2.2	2.31	Ω	-
R_{g_pd}	Pull-down resistor of $Q1_{\_BOOST}$ gate	142.5	150	157.5	kΩ	-
$Q2_{\_Bypass}$	-	-	-	-	—	$R_{DS(ON)}$: < 10 mΩ $V_{(BR)DSS}$: > 40 V V_{GS}: ±20 V $I_{D\ (continuous)}$: > 20 A $I_{D\ (pulse)}$: > 40 A V_{GS_TH}: < 3 V Choice: STD45P4LLF6AG
D_{Zby}	Zener diode to clamp V_{GS} of Q2 bypass	-	-	-	-	Voltage clamp = 18 V Choice: SM4T18AY
R_{cl}	Discharge resistor to short V_{GS} of Q2 bypass in OFF STATE	20.9	22	23.1	KΩ	-
$C_{\_Buck1\_24}$(1) $C_{\_Buck2\_24}$(1) $C_{\_Buck3}$(1)	Output capacitor at 2.4 MHz T = 27 °C V_{out_buck1} = 3.3 V	17	22	27	µF	ESR: < 15 mΩ Rated voltage: > 10 VDC X7R [±15% temperature characteristics] SMD Choice: CGA6P1X7R1C226M250AC
$L_{\_Buck1\_24}$ $L_{\_Buck2\_24}$	Output inductor at 2.4 MHz I_{out} = 3 A	2.2	3.3	4	µH	Rdc: < 25 mΩ Isat > 8 A SRF > 15 MHz SMD Choice: XAL6030-332ME

Component	Block/Usage	Min	Typ	Max	Unit	Note
C_{bst_Buck1}[1] C_{bst_Buck2}[1]	Bootstrap capacitor	37.6	47	56.4	nF	-
C_{bst_Buck3}[1]	Bootstrap capacitor	80	100	120	nF	-
$L_{\_Buck3}$	Output inductor I_{out} = 6 A	2.2	3.3	4	µH	Rdc: < 15 mΩ Isat > 10 A SRF > 15 MHz SMD Choice: SPM10040T-3R3M-HZ
$C_{c\_Buck1\_24}$[1] $C_{c\_Buck2\_24}$[1]	F = 2.4 MHz	1.2	1.5	1.8	nF	-
C_{c_Buck3}[1]	-	3.76	4.7	5.64	nF	-
$R_{c\_Buck1\_24}$ $R_{c\_Buck2\_24}$	F = 2.4 MHz	14.25	15	15.75	kΩ	-
R_{c_Buck3}	-	0.95	1	1.05	kΩ	-
$C_{\_Buck1\_04}$[1] $C_{\_Buck2\_04}$[1]	Output capacitor at 400 kHz T = 27 °C V_{out_buck1} = 3.3 V	33	47	56	µF	ESR: < 15 mΩ Rated voltage: > 10 VDC X7R [±15% temperature characteristics] Choice: CGA6P1X7R1A476M250AC
$L_{\_Buck1\_04}$ $L_{\_Buck2\_04}$	Output inductor at 400 kHz I_{out} = 3 A	11	15	18	µH	Rdc : < 40mΩ Isat > 8 A SRF > 4 MHz SMD Choice: SPM12565VT-150M-D
$C_{c\_Buck1\_04}$[1] $C_{c\_Buck2\_04}$[1]	F = 400 kHz	8	10	12	nF	-
$R_{c\_Buck1\_04}$ $R_{c\_Buck2\_04}$	F = 400 kHz	4.84	5.1	5.35	kΩ	-
C_{VREG}[1]	-	3	4.7	10	µF	max ESR < 0.1 Ω Rated voltage > 5 V X7R Choice: CGA4J3X7R1A475K125AB
C_{LDO1}[1]	-	-	2.2	-	µF	-
C_{LDO2}[1]	-	-	2.2	-	µF	-
R_{NFSO1_PU}	Pull-up resistor to V_{bat}	28.5	30	31.5	KΩ	-
R_{IRQ_PU}	Pull-up resistor to V_{IO}	28.5	30	31.5	KΩ	-
R_{NRST_PU}	Pull-up resistor to V_{IO}	28.5	30	31.5	KΩ	-
C_{VIN12}[1]	BUCK1, 2 input capacitor	-	22	-	µF	-
C_{VIN3}[1]	BUCK3 input capacitor	-	47	-	µF	-

1. *Capacitance to be dimensioned, for example, according to voltage drop out requirements.*

8.2 External components calculation

8.2.1 BUCK1 and BUCK2 inductor

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. For the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of maximum load current.

For example, if:

$$\Delta I_L = IRipple = 0.3 I_{OUT(MAX)} \quad (1)$$

Where $I_{OUT(MAX)}$ is the maximum output current.

Then, the inductor value can be estimated by the following equation:

$$L > \frac{1}{f_{SW} X \Delta I_L} X V_{OUT} X \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Where f_{SW} is the switching frequency and $V_{IN(max)}$ is the maximum input voltage.

The peak current flowing in the inductor is:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

If the inductor value decreases, the peak current increases. The peak current has to be lower than the current limit of the device. The inductor should have a saturation current higher than the device current limit.

Note: To meet slope compensation, L needs to meet the following equation:

$$L > \frac{1}{2} X \frac{V_{OUT}}{I_{slope}}$$

With I_{slope} = 650 mA × f_{SW}.

8.2.2 BUC3 inductor

The value of the output inductor is usually calculated to satisfy the peak-to-peak ripple current requirement. For the best compromise of cost, size and performance, it is suggested to keep the inductor current ripple between 20% and 40% of maximum load current.

For example, if:

$$\Delta I_L = IRipple = 0.3 I_{OUT(MAX)} \quad (2)$$

Where $I_{OUT(MAX)}$ is the maximum output current.

Then, the inductor value can be estimated by the following equation:

$$L > \frac{1}{f_{SW} X \Delta I_L} X V_{OUT} X \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (3)$$

Where f_{SW} is the switching frequency and $V_{IN(max)}$ is the maximum input voltage.

The peak current flowing in the inductor is:

$$I_{L(PEAK)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \quad (4)$$

If the inductor value decreases, the peak current increases. The peak current has to be lower than the current limit of the device. The inductor should have a saturation current higher than the device current limit.

Note: To meet slope compensation, L needs to meet the following equation:

$$L > \frac{1}{2} X \frac{V_{OUT}}{I_{slope}} \quad (5)$$

With I_{slope} = 325 mA × f_{SW}.

9 SPI registers

9.1 Global status byte GSB

Table 51. Global status byte GSB

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
1 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
GSBN	RSTB	SPIE	RES	FE1	DE	GW	FS
Global status bit inverted	Reset	SPI error	Reserved	Functional error bit 1	Device error	Global warning	Fail-safe

Table 52. Global status byte GSB description

Bit	Name	Description
31	GSBN	**Global status bit inverted** The GSBN is a logically NOR combination of GSB bits 0 to bit 6(1). This bit can also be used as a global status flag without starting a complete communication frame as it is present at SDO directly after pulling CSN low. 0: Error detected (one or several GSB bits from 0 to 6 are set) 1: No error detected (default after power-on) Specific fault detection may be masked in the configuration registers 0x3F. A masked fault detection will still be reported in the GSB by the related fault flag, however it is not reflected in the GSBN (see the Section 5.2.2: Communication protocol for masks).
30	RSTB	**Reset** The RSTB indicates that the NRESET output has been asserted low, this flag is set in case of: • Power-down sequence • WDFAIL (SR3 - 0x23) • FCCU fail (SR3 - 0x23) 0: No reset signal has been generated (default) 1: Reset signal has been generated RSTB is cleared by a read and Clear command to all bits in status register 1 causing the reset event.
29	SPIE	**SPI error bit** The SPIE indicates errors related to a wrong SPI communication. • SPI_SDI_STUCK_HIGH (SR4 - 0x24) • SPI_SDI_STUCK_LOW (SR4 - 0x24) • SPI_CSN_TIMEOUT (SR4 - 0x24) • SPI_CRC_ERR (SR4 - 0x24) • SPI_UNDEF_ADD (SR4 - 0x24) • SPI_STATUS_WRT (SR4 - 0x24) • SPI_CLK_CNT (SR4 - 0x24) • SPI_LBISTED (SR4 - 0x24) 0: No error (default) 1: Error detected
28	RES	Reserved
27	FE1	**Functional error bit 1** The FE1 is a logical OR combination of errors coming from functional blocks. • OUTHS_OC (SR2 - 0x22) • OUTHS_OL (SR2 - 0x22) • BUCK1_UV (SR1 - 0x21) • BUCK2_UV (SR1 - 0x21)

Bit	Name	Description
		• BUCK3_UV (SR1 - 0x21) • BUCK1_OV (SR1 - 0x21) • BUCK2_OV (SR1 - 0x21) • BUCK3_OV (SR1 - 0x21) • BUCK1_OC (SR1 - 0x21) • BUCK2_OC (SR1 - 0x21) • BUCK3_OC (SR1 - 0x21) • LDO2_UV (SR1 - 0x21) • LDO2_OV (SR1 - 0x21) • BUCKX_PG_TIMEOUT from SPI request (SR1 - 0x21) • LDO2_PG_TIMEOUT from SPI request (SR1 - 0x21) 0: No error (default) 1: Error detected FE1 is cleared by a read and clear command to all related bits in status registers 3, 5 and 6
26	DE	**Device error bit** DE is a logical OR combination of global errors related to the device. • FBB_OV (SR2 - 0x22) • FBB_UV (SR2 - 0x22) • VIO_UV (SR2 - 0x22) • TSD_CLx (SR2 - 0x22) • WD_ENA_ECHO_ERROR (SR2 - 0x22) • FCCU_ENA_ECHO_ERROR (SR2 - 0x22) • NFSO1_ECHO_ERROR (SR2 - 0x22) • IRQ_ECHO_ERROR (SR2 - 0x22) • NRST_ECHO_ERROR (SR2 - 0x22) 0: No error (default) 1: Error detected DE is cleared by a read and clear command to all related bits in status registers 2, 4 and 7
25	GW	**Global warning bit** GW is a logical OR combination of warning flags. Warning bits do not lead to any device state change or switch off of functions. • FBB_UV_EW (SR4 - 0x24) • FBB_OV_EW (SR4 - 0x24) • VS_UV_EW (SR4 - 0x24) • TW_CLx (SR4 - 0x24) 0: No error (default) 1: Error detected GW is cleared by a read and clear command to all related bits in status register 2 and 4
24	FS	**Fail-safe** The FS bit indicates that the device was forced into DEEP-SLEEP, RECOVERY-1 or -2 state due to the following fault conditions: • FCCUFAIL (SR3 - 0x23) • WDFAIL (SR3 - 0x23) • FORCED_SLEEP_TSD (SR3 - 0x23) • FORCED_SLEEP_POWUP (SR5 - 0x25) • GNDLOSS (SR3 - 0x23) • INT_REG_UV (SR3 - 0x23) • INT_REG_OV (SR3 - 0x23) • CURRENT_MISMATCH (SR3 - 0x23) • OSC_ERROR (SR3 - 0x23) • ABIST_ERROR (SR3 - 0x23) • LBIST_ERROR (SR3 - 0x23) • NVM_COMP_ERROR (SR3 - 0x23) • NVM_CRC_ERROR (SR3 - 0x23) • SPI_REG_COMP_ERROR (SR3 - 0x23)

Bit	Name	Description
		• FSM_COMP_ERROR (SR3 - 0x23) All control registers are set to default Control registers are blocked for WRITE access except the following bits: • Error flags • Wake-up settings • Timer setting 1: Fail-safe active FS is cleared by a read and clear command to all related bits in status register SR3 and SR5

9.2 Control register overview

Table 53. Control register overview (bit 31...28) upper nibbles

			Bit				Mode
			31	30	29	28	
OpCode + address			OC1	OC2	A5	A4	R/W
Control register			Bit				Mode
Addr			23	22	21	20	
			15	14	13	12	
			7	6	5	4	
0x00		MSB	Reserved				
			Reserved				
		LSB	Reserved				
0x01	DCR1	MSB	RES	RES	RES	RES	R/W
			WD_TIME_1	WD_TIME_0	VBUCK3_ENA	VBUCK2_ENA	
		LSB	WD_LP_ENA	DO_POWER_DOWN	U-NVM_PROG	DO_POWER_CYCLE	
0x02	DCR2	MSB	RES	RES	NFSO_ASSERT_LOW	LBIST	R/W
			FCCU_COUNTER_10	FCCU_COUNTER_9	FCCU_COUNTER_8	FCCU_COUNTER_7	
		LSB	FCCU_COUNTER_2	FCCU_COUNTER_1	FCCU_COUNTER_0	FCCU_ENA	
0x03	DCR3	MSB	RES	RES	BUCK3_SPREAD_ENA	BUCK2_SPREAD_ENA	R/W
			BUCK3_FTUNE_1	BUCK3_FTUNE_0	BOOST_OFF	FBB_OV_EW_TH_3	
		LSB	FBB_UV_EW_TH_2	FBB_UV_EW_TH_1	FBB_UV_EW_TH_0	SPI_PROTECT_ACCESS	
0x04	DCR4	MSB	RES	BOOST_DSMON_TH_2	BOOST_DSMON_TH_1	BOOST_DSMON_TH_0	R/W
			VS_UV_EW_TH_1	VS_UV_EW_TH_0	FCCU_PROTOCOL	FCCU_STATIC_ERROR	
		LSB	BYPASS_DSMON_TH_0	CLR_REG_FAIL_CNT	KILL_SWDBG_TIMEOUT	WD_TRIG	
0x05	DCR5	MSB	RES	CLR_REC2_FROM_DO_POWER_CYCLE	CLR_DEEP_SLEEP_FROM_DO_POWER_DOWN	CLR_POWUP_RETRY_COUNT	R/W
			T1_PER_1	T1_PER_0	TIMER_WAKE_ENA	IGN_CONFIG	
		LSB	WU_ENA	WU_PU	WU_FILT	TIMER_ENA	
0x06	DCR6	MSB	RES	MASK_BUCK3_PG_TIMEOUT_IRQ	MASK_BUCK3_OC_IRQ	MASK_BUCK3_PG_IRQ	R/W
			MASK_BUCK2_IRQ	MASK_BUCK1_PG_TIMEOUT_IRQ	MASK_BUCK1_OC_IRQ	MASK_BUCK1_PG_IRQ	
		LSB	MASK_FBB_UV_EW_IRQ	MASK_LDO2_PG_IRQ	MASK_LDO2_PG_TIMEOUT_IRQ	MASK_LDO2_IRQ	
0x07	DCR7	MSB	RES	MASK_LDO1_PG_IRQ	MASK_LDO1_PG_TIMEOUT_IRQ	MASK_LDO1_IRQ	R/W
			MASK_VS_EW_IRQ	RES	MASK_CL4_TW_IRQ	MASK_CL3_TW_IRQ	
		LSB	MASK_SPI_ERROR_IRQ	MASK_NFSO1_ECHO_ERROR_IRQ	MASK_WD_ENA_ECHO_ERROR_IRQ	MASK_FCCU_ENA_ECHO_ERROR_IRQ	
0x08	DCR8	MSB	RES	MASK_SWDBG_VIO_IRQ	MASK_LP_READY_IRQ	CLR_TSD_CNT_FAIL	R/W
			MASK_BUCK2_UV_POWER_OFF	MASK_BUCK1_UV_POWER_OFF	MASK_TW_GW	MASK_OL_GSB	
		LSB	RES	RES	RES	GO_INIT	

Table 54. Control register overview (bit 27...24) lower nibbles

			Bit				Mode
			27	26	25	24	
OpCode + address			A3	A2	A1	A0	R/W
Control register			Bit				Mode
Addr			19	18	17	16	
			11	10	9	8	

			Bit				Mode
Addr			CRC 3	CRC 2	CRC 1	CRC 0	
0x00		MSB	Reserved				
			Reserved				
		LSB	Reserved				
0x01	DCR1	MSB	RES	RES	WD_TIME_3	WD_TIME_2	R/W
			VBUCK1_ENA	LDO1_ENA	LDO2_ENA	LOW_POWER_SET	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x02	DCR2	MSB	ABIST	RES	FCCU_COUNTER_12	FCCU_COUNTER_11	R/W
			FCCU_COUNTER_6	FCCU_COUNTER_5	FCCU_COUNTER_4	FCCU_COUNTER_3	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x03	DCR3	MSB	BUCK1_SPREAD_ENA	CLR_WDFAIL_CNT	RES	BUCK3_FTUNE_2	R/W
			FBB_OV_EW_TH_2	FBB_OV_EW_TH_1	FBB_OV_EW_TH_0	FBB_UV_EW_TH_3	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x04	DCR4	MSB	SWDBG_EXIT	VS_UV_EW_TH_4	VS_UV_EW_TH_3	VS_UV_EW_TH_2	R/W
			OUTHS_1	OUTHS_0	BYPASS_DSMON_TH_2	BYPASS_DSMON_TH_1	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x05	DCR5	MSB	T1_ENA_2	T1_ENA_1	T1_ENA_0	T1_PER_2	R/W
			IGN_FILT	IGN_ENA	IGN_PU	WU_CONFIG	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x06	DCR6	MSB	MASK_BUCK3_IRQ	MASK_BUCK2_PG_TIMEOUT_IRQ	MASK_BUCK2_OC_IRQ	MASK_BUCK2_PG_IRQ	R/W
			MASK_BUCK1_IRQ	MASK_FBB_OV_IRQ	MASK_FBB_UV_IRQ	MASK_FBB_OV_EW_IRQ	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x07	DCR7	MSB	MASK_BOOST_IN_LP_IRQ	MASK_BYPASS_VDSMON_IRQ	MASK_BOOST_VDSMON_IRQ	IRQ_REQUEST	R/W
			MASK_CL2_TW_IRQ	MASK_CL1_TW_IRQ	MASK_CL0_TW_IRQ	MASK_OUTHS_IRQ	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x08	DCR8	MSB	MASK_BUCK3_OC_POWER_OFF	MASK_BUCK2_OC_POWER_OFF	MASK_BUCK1_OC_POWER_OFF	MASK_BUCK3_UV_POWER_OFF	R/W
			RES	MASK_GW_GSB	RES	RES	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	

9.3 U_NVM register overview

Table 55. U_NVM register overview (bit 31...28) upper nibbles

			Bit				Mode
			31	30	29	28	
OpCode + address			OC1	OC2	A5	A4	R/W
U_NVM register			Bit				Mode
Addr.			23	22	21	20	
			15	14	13	12	
			7	6	5	4	
0x0A	DCR10	MSB	RES	RES	RES	RES	R/W
			BUCK1_PU_STEP_ENA_1	BUCK1_PU_STEP_ENA_0	BUCK1_PD_STEP_OFF_2	BUCK1_PD_STEP_OFF_1	
		LSB	BUCK1_REGFAIL_GO_REC	BUCK1_SS_VALUE_1	BUCK1_SS_VALUE_0	BUCK1_REFRESH_FREQ	
0x0B	DCR11	MSB	RES	RES	RES	RES	R/W
			BUCK2_PU_STEP_ENA_1	BUCK2_PU_STEP_ENA_0	BUCK2_PD_STEP_OFF_2	BUCK2_PD_STEP_OFF_1	
		LSB	BUCK2_REGFAIL_GO_REC	BUCK2_SS_VALUE_1	BUCK2_SS_VALUE_0	BUCK2_REFRESH_FREQ	
0x0C	DCR12	MSB	RES	RES	RES	RES	R/W
			BUCK3_PU_STEP_ENA_2	BUCK3_PU_STEP_ENA_1	BUCK3_PU_STEP_ENA_0	BUCK3_PD_STEP_OFF_2	
		LSB	BUCK3_REGFAIL_GO_REC	BUCK3_SS_VALUE_1	BUCK3_SS_VALUE_0	BUCK3_REFRESH_FREQ	
0x0D	DCR13	MSB	RES	RES	RES	RES	R/W
			U_NVM_D_11	U_NVM_D_10	U_NVM_D_9	U_NVM_D_8	
		LSB	U_NVM_D_3	U_NVM_D_2	U_NVM_D_1	U_NVM_D_0	
0x0E	DCR14	MSB	RES	RES	RES	RES	R/W
			LDO2_PD_STEP_OFF_2	LDO2_PD_STEP_OFF_1	LDO2_PD_STEP_OFF_0	LDO2_PU_STEP_ENA_2	

			Bit				Mode
0x0E	DCR14	LSB	LDO1_PD_STEP_OFF_0	LDO1_PU_STEP_ENA_2	LDO1_PU_STEP_ENA_1	LDO1_PU_STEP_ENA_0	R/W
0x0F	DCR15	MSB	RES	RES	RES	RES	R/W
			PU_WAIT_DEL_ENA_6_1	PU_WAIT_DEL_ENA_6_0	PU_WAIT_DEL_ENA_5_1	PU_WAIT_DEL_ENA_5_0	
		LSB	PU_WAIT_DEL_ENA_2_1	PU_WAIT_DEL_ENA_2_0	PU_WAIT_DEL_ENA_1_1	PU_WAIT_DEL_ENA_1_0	
0x!0	DCR16	MSB	RES	RES	RES	RES	R/W
			NRESET_PD_STEP_ASSERT_1	NRESET_PD_STEP_ASSERT_0	NRESET_PU_STEP_DEASSERT_2	NRESET_PU_STEP_DEASSERT_1	
		LSB	PU_WAIT_PG_ENA_4	PU_WAIT_PG_ENA_3	PU_WAIT_PG_ENA_2	PU_WAIT_PG_ENA_1	
0x11	DCR17	MSB	RES	RES	RES	RES	R/W
			U_NVM_CRC0_3	U_NVM_CRC0_2	U_NVM_CRC0_1	U_NVM_CRC0_0	
		LSB	NFSO_STATE_IN_DEEP_SLEEP	U_NVM_H_2	U_NVM_H_1	BOOST_DIS	
0x12	DCR18	MSB	RES	RES	RES	RES	R/W
			PD_WAIT_DEL_OFF_6_1	PD_WAIT_DEL_OFF_6_0	PD_WAIT_DEL_OFF_5_1	PD_WAIT_DEL_OFF_5_0	
		LSB	PD_WAIT_DEL_OFF_2_1	PD_WAIT_DEL_OFF_2_0	PD_WAIT_DEL_OFF_1_1	PD_WAIT_DEL_OFF_1_0	
0x13	DCR19	MSB	RES	RES	RES	RES	R/W
			U_NVM_RELEASE_11	U_NVM_RELEASE_10	U_NVM_RELEASE_9	U_NVM_RELEASE_8	
		LSB	U_NVM_RELEASE_3	U_NVM_RELEASE_2	U_NVM_RELEASE_1	U_NVM_RELEASE_0	
0x14	DCR20	MSB	RES	RES	RES	RES	R/W
			U_NVM_K_11	U_NVM_K_10	U_NVM_K_9	U_NVM_K_8	
		LSB	LOW_SET_3	LOW_SET_2	LOW_SET_1	LOW_SET_0	
0x15	DCR21	MSB	RES	RES	RES	RES	R/W
			U_NVM_L_11	U_NVM_L_10	U_NVM_L_9	U_NVM_L_8	
		LSB	U_NVM_L_3	U_NVM_L_2	U_NVM_L_1	U_NVM_L_0	
0x16	DCR22	MSB	RES	RES	RES	RES	R/W
			U_NVM_M_11	U_NVM_M_10	U_NVM_M_9	U_NVM_M_8	
		LSB	U_NVM_M_3	U_NVM_M_2	U_NVM_M_1	U_NVM_M_0	
0x17	DCR23	MSB	RES	RES	RES	RES	R/W
			U_NVM_N_11	U_NVM_N_10	U_NVM_N_9	U_NVM_N_8	
		LSB	U_NVM_N_3	U_NVM_N_2	U_NVM_N_1	U_NVM_N_0	
0x18	DCR24	MSB	RES	RES	RES	RES	R/W
			U_NVM_O_11	U_NVM_O_10	U_NVM_O_9	U_NVM_O_8	
		LSB	U_NVM_O_3	U_NVM_O_2	U_NVM_O_1	U_NVM_O_0	
0x19	DCR25	MSB	RES	RES	RES	RES	R/W
			U_NVM_CRC1_3	U_NVM_CRC1_2	U_NVM_CRC1_1	U_NVM_CRC1_0	
		LSB	U_NVM_P_3	U_NVM_P_2	U_NVM_P_1	U_NVM_P_0	
0x1C	DCR28	MSB	RES	TEST_REG_PAGE_FUNC	RES	RES	R/W
			RES	RES	RES	RES	
		LSB	RES	RES	RES	RES	

Table 56. U_NVM register overview (bit 27...24) lower nibbles

			Bit				Mode
			27	26	25	24	
OpCode + address			A3	A2	A1	A0	R/W
U_NVM register			Bit				Mode
Addr.			19	18	17	16	
			11	10	9	8	
			CRC 3	CRC 2	CRC 1	CRC 0	
0x0A	DCR10	MSB	BUCK1_FREQ	BUCK1_PU_VALUE_1	BUCK1_PU_VALUE_0	BUCK1_PU_STEP_ENA_2	R/W
			BUCK1_PD_STEP_OFF_0	BUCK1_IPEAK_2	BUCK1_IPEAK_1	BUCK1_IPEAK_0	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x0B	DCR11	MSB	BUCK2_FREQ	BUCK2_PU_VALUE_1	BUCK2_PU_VALUE_0	BUCK2_PU_STEP_ENA_2	R/W
			BUCK2_PD_STEP_OFF_0	BUCK2_IPEAK_2	BUCK2_IPEAK_1	BUCK2_IPEAK_0	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x0C	DCR12	MSB	BYPASS_DIS	BUCK3_PU_VALUE_2	BUCK3_PU_VALUE_1	BUCK3_PU_VALUE_0	R/W
			BUCK3_PD_STEP_OFF_1	BUCK3_PD_STEP_OFF_0	BUCK3_IPEAK_1	BUCK3_IPEAK_0	

			Bit				Mode
0x0C	DCR12	LSB	CRC 3	CRC 2	CRC 1	CRC 0	R/W
0x0D	DCR13	MSB	U_NVM_D_15	U_NVM_D_14	U_NVM_D_13	U_NVM_D_12	R/W
			U_NVM_D_7	U_NVM_D_6	U_NVM_D_5	U_NVM_D_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x0E	DCR14	MSB	PU_LOOP_FOR_EVER	LDO2_REGFAIL_GO_REC	LDO2_TRK_1	LDO2_TRK_0	R/W
			LDO2_PU_STEP_ENA_1	LDO2_PU_STEP_ENA_0	LDO1_PD_STEP_OFF_2	LDO1_PD_STEP_OFF_1	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x0F	DCR15	MSB	U_NVM_F_15	U_NVM_F_14	PU_WAIT_DEL_ENA_7_1	PU_WAIT_DEL_ENA_7_0	R/W
			PU_WAIT_DEL_ENA_4_1	PU_WAIT_DEL_ENA_4_0	PU_WAIT_DEL_ENA_3_1	PU_WAIT_DEL_ENA_3_0	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x!0	DCR16	MSB	U_NVM_G_15	U_NVM_G_14	U_NVM_G_13	NRESET_PD_STEP_ASSERT_2	R/W
			NRESET_PU_STEP_DEASSERT_0	PU_WAIT_PG_ENA_7	PU_WAIT_PG_ENA_6	PU_WAIT_PG_ENA_5	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x11	DCR17	MSB	U_NVM_CRC0_7	U_NVM_CRC0_6	U_NVM_CRC0_5	U_NVM_CRC0_4	R/W
			U_PROG0_1	U_PROG0_0	U_NVM_H_5	U_NVM_H_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x12	DCR18	MSB	PD_WAIT_VREG_DEL_OFF_1	PD_WAIT_VREG_DEL_OFF_0	PD_WAIT_DEL_OFF_7_1	PD_WAIT_DEL_OFF_7_0	R/W
			PD_WAIT_DEL_OFF_4_1	PD_WAIT_DEL_OFF_4_0	PD_WAIT_DEL_OFF_3_1	PD_WAIT_DEL_OFF_3_0	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x13	DCR19	MSB	U_NVM_RELEASE_15	U_NVM_RELEASE_14	U_NVM_RELEASE_13	U_NVM_RELEASE_12	R/W
			U_NVM_RELEASE_7	U_NVM_RELEASE_6	U_NVM_RELEASE_5	U_NVM_RELEASE_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x14	DCR20	MSB	U_NVM_K_15	U_NVM_K_14	U_NVM_K_13	U_NVM_K_12	R/W
			U_NVM_K_7	U_NVM_K_6	U_NVM_K_5	U_NVM_K_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x15	DCR21	MSB	U_NVM_L_15	U_NVM_L_14	U_NVM_L_13	U_NVM_L_12	R/W
			U_NVM_L_7	U_NVM_L_6	U_NVM_L_5	U_NVM_L_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x16	DCR22	MSB	U_NVM_M_15	U_NVM_M_14	U_NVM_M_13	U_NVM_M_12	R/W
			U_NVM_M_7	U_NVM_M_6	U_NVM_M_5	U_NVM_M_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x17	DCR23	MSB	U_NVM_N_15	U_NVM_N_14	U_NVM_N_13	U_NVM_N_12	R/W
			U_NVM_N_7	U_NVM_N_6	U_NVM_N_5	U_NVM_N_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x18	DCR24	MSB	U_NVM_O_15	U_NVM_O_14	U_NVM_O_13	U_NVM_O_12	R/W
			U_NVM_O_7	U_NVM_O_6	U_NVM_O_5	U_NVM_O_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x19	DCR25	MSB	U_NVM_CRC1_7	U_NVM_CRC1_6	U_NVM_CRC1_5	U_NVM_CRC1_4	R/W
			U_PROG1_1	U_PROG1_0	U_NVM_P_5	U_NVM_P_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x1C	DCR28	MSB	RES	RES	RES	RES	R/W
			RES	RES	RES	RES	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	

9.4 Status register overview

Table 57. Status register overview (bit 31...28) upper nibbles

			Bit				Mode
			31	30	29	28	
Global status			GSBN	RSTB	SPIE	RES	R
Status register			Bit				Mode
Addr.			23	22	21	20	
			15	14	13	12	
			7	6	5	4	
0x21	DSR1	MSB	RES	RES	FORCED_SLEEP_WDFAIL	BUCK3_OC	R
			BUCK2_OV	BUCK2_UV	BUCK2_PG_TIMEOUT	BUCK1_OC	
		LSB	LDO2_UV	LDO2_OV	LDO1_PG_TIMEOUT	LDO1_UV	
0x22	DSR2	MSB	RES	OUTHS_OL	OUTHS_OC	BOOST_IN_LP	R
			IRQ_ECHO_ERROR	FCCU_ENA_ECHO_ERROR	NFSO1_ECHO_ERROR	WD_ENA_ECHO_ERROR	
		LSB	TSD_CL2	TSD_CL1	TSD_CL0	TSD	
0x23	DSR3	MSB	RES	LBIST_STOPPED	BUCK3_INT_FAIL	BUCK2_INT_FAIL	R
			CURRENT_MISMATCH	FORCED_SLEEP_TSD	FCCUFAIL	WDFAIL	
		LSB	GNDLOSS	OSC_ERROR	SPI_REG_COMP_ERROR	FSM_COMP_ERROR	
0x24	DSR4	MSB	RES	SPI_ALL_WAKEUP_DISABLE	SPI_CLK_CNT	SPI_CSN_TIMEOUT	R
			SPI_STATUS_WRT	SPI_LBISTED	FBB_OV_EW	FBB_UV_EW	
		LSB	TW_CL2	TW_CL1	TW_CL0	TW	
0x25	DSR5	MSB	RES	FP_READY	BOOST_LEVEL_SET	BOOST_ENA_STATUS	R
			DEV_STATE_5	DEV_STATE_4	DEV_STATE_3	DEV_STATE_2	
		LSB	FORCED_SLEEP_POWUP	FSM_TO_REC2	REC2_FROM_DO_POWER_CYCLE_1	REC2_FROM_DO_POWER_CYCLE_0	
0x26	DSR6	MSB	RES	LP_READY	SWDBG_VIO	SWDBG_STATE	R
			RES	FIN1_STATE	IGN_STATE	WU_STATE	
		LSB	IRQ_ECHO	NRST_ECHO	IRQ_SENT	NFSO1_ECHO	
0x27	DSR7	MSB	RES	VPOR	LDO1_PG_OK	LDO2_ENA_STATUS	R
			WD_TIMER_STATE_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	
		LSB	POWUP_RETRY_CNT_0	RES	NVM_PROG_OK	NVM_PROG_DONE	
0x28	DSR8	MSB	RES	FCCU_LAST_STABLE_12	FCCU_LAST_STABLE_11	FCCU_LAST_STABLE_10	R
			FCCU_LAST_STABLE_5	FCCU_LAST_STABLE_4	FCCU_LAST_STABLE_3	FCCU_LAST_STABLE_2	
		LSB	REG_FAIL_CNT_0	ABIST_BOOST_IGNORED	LBIST_COMPLETE	ABIST_COMPLETE	
0x29	DSR9	MSB	RES	RES	RES	RES	R
			RES	RES	TEMP_CL0_9	TEMP_CL0_8	
		LSB	TEMP_CL0_3	TEMP_CL0_2	TEMP_CL0_1	TEMP_CL0_0	
0x2A	DSR10	MSB	RES	RES	RES	RES	R
			RES	RES	TEMP_CL1_9	TEMP_CL1_8	
		LSB	TEMP_CL1_3	TEMP_CL1_2	TEMP_CL1_1	TEMP_CL1_0	
0x2B	DSR11	MSB	RES	RES	RES	RES	R
			RES	RES	TEMP_CL2_9	TEMP_CL2_8	
		LSB	TEMP_CL2_3	TEMP_CL2_2	TEMP_CL2_1	TEMP_CL2_0	
0x2C	DSR12	MSB	RES	RES	RES	RES	R
			RES	RES	TEMP_CL3_9	TEMP_CL3_8	
		LSB	TEMP_CL3_3	TEMP_CL3_2	TEMP_CL3_1	TEMP_CL3_0	
0x2D	DSR13	MSB	RES	RES	RES	RES	R
			RES	RES	TEMP_CL4_9	TEMP_CL4_8	
		LSB	TEMP_CL4_3	TEMP_CL4_2	TEMP_CL4_1	TEMP_CL4_0	
0x2E	DSR14	MSB	RES	RES	RES	RES	R
			RES	RES	VS_9	VS_8	
		LSB	VS_3	VS_2	VS_1	VS_0	
0x2F	DSR15	MSB	RES	RES	RES	RES	R
			RES	RES	WU_9	WU_8	
		LSB	WU_3	WU_2	WU_1	WU_0	

			Bit				Mode
0x30	DSR16	MSB	RES	RES	RES	RES	R
			RES	RES	IGN_9	IGN_8	
		LSB	IGN_3	IGN_2	IGN_1	IGN_0	
0x31	DSR17	MSB	RES	RES	RES	RES	R
			RES	RES	FBB_9	FBB_8	
		LSB	FBB_3	FBB_2	FBB_1	FBB_0	
0x32	DSR18	MSB	RES	RES	RES	BUCK2_FBLOSS	R
			WD_TIME_STATUS_1	WD_TIME_STATUS_0	VBUCK3_ENA_STATUS	VBUCK2_ENA_STATUS	
		LSB	BOOST_ENA_STATUS	FCCU_ENA_STATUS	RES	RES	

Table 58. Status register overview (bit 27...24) lower nibbles

			Bit				Mode
			27	26	25	24	
Global status			FE1	DE	GW	FS	R
Status register			Bit				Mode
Addr.			19	18	17	16	
			11	10	9	8	
			CRC 3	CRC 2	CRC 1	CRC 0	
0x21	DSR1	MSB	BUCK3_OV	BUCK3_UV	BUCK3_PG_TIMEOUT	BUCK2_OC	R
			BUCK1_OV	BUCK1_UV	BUCK1_PG_TIMEOUT	LDO2_PG_TIMEOUT	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x22	DSR2	MSB	BYPASS_VDSMON_ERROR	BOOST_VDSMON_ERROR	FBB_OV	FBB_UV	R
			NRST_ECHO_ERROR	VIO_UV	TSD_CL4	TSD_CL3	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x23	DSR3	MSB	BUCK1_INT_FAIL	LBIST_ERROR_1	LBIST_ERROR_0	ABIST_ERROR	R
			INT_REG_UV	INT_REG_OV	NVM_COMP_ERROR	NVM_CRC_ERROR	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x24	DSR4	MSB	SPI_CRC_ERR	SPI_SDI_STUCK_HIGH	SPI_SDI_STUCK_LOW	SPI_UNDEF_ADD	R
			VS_UV_EW	RES	TW_CL4	TW_CL3	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x25	DSR5	MSB	BYPASS_STATUS	BUCK3_PG_OK	BUCK2_PG_OK	BUCK1_PG_OK	R
			DEV_STATE_1	DEV_STATE_0	DEEP-SLEEP_FROM_DO_POWER_DOWN_1	DEEP-SLEEP_FROM_DO_POWER_DOWN_0	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x26	DSR6	MSB	RES	RES	RES	RES	R
			IGN_WAKE	WU_WAKE	RES	TIMER_WAKE	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x27	DSR7	MSB	LDO2_PG_OK	FCCU_ENA_ECHO	WD_ENA_ECHO	WD_TIMER_STATE_1	R
			WDFAIL_CNT_0	TSD_CNT_FAIL_1	TSD_CNT_FAIL_0	POWUP_RETRY_CNT_1	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x28	DSR8	MSB	FCCU_LAST_STABLE_9	FCCU_LAST_STABLE_8	FCCU_LAST_STABLE_7	FCCU_LAST_STABLE_6	R
			FCCU_LAST_STABLE_1	FCCU_LAST_STABLE_0	FORCED_SLEEP_REGFAIL	REG_FAIL_CNT_1	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x29	DSR9	MSB	RES	RES	RES	RES	R
			TEMP_CL0_7	TEMP_CL0_6	TEMP_CL0_5	TEMP_CL0_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x2A	DSR10	MSB	RES	RES	RES	RES	R
			TEMP_CL1_7	TEMP_CL1_6	TEMP_CL1_5	TEMP_CL1_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x2B	DSR11	MSB	RES	RES	RES	RES	R
			TEMP_CL2_7	TEMP_CL2_6	TEMP_CL2_5	TEMP_CL2_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x2C	DSR12	MSB	RES	RES	RES	RES	R
			TEMP_CL3_7	TEMP_CL3_6	TEMP_CL3_5	TEMP_CL3_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	

			Bit				Mode
0x2D	DSR13	MSB	RES	RES	RES	RES	R
			TEMP_CL4_7	TEMP_CL4_6	TEMP_CL4_5	TEMP_CL4_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x2E	DSR14	MSB	RES	RES	RES	RES	R
			VS_7	VS_6	VS_5	VS_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x2F	DSR15	MSB	RES	RES	RES	RES	R
			WU_7	WU_6	WU_5	WU_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x30	DSR16	MSB	RES	RES	RES	RES	R
			IGN_7	IGN_6	IGN_5	IGN_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x31	DSR17	MSB	RES	RES	RES	RES	R
			FBB_7	FBB_6	FBB_5	FBB_4	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	
0x32	DSR18	MSB	BUCK1_FBLOSS	NVM_COMPARE_ENA_STATUS	WD_TIME_STATUS_3	WD_TIME_STATUS_2	R
			VBUCK1_ENA_STATUS	LDO1_ENA_STATUS	OUTHS_ENA_STATUS	LOW_STATUS	
		LSB	CRC 3	CRC 2	CRC 1	CRC 0	

9.5 Control registers

Table 59. **DCR1 (0x01) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	0 (R/W)	0 (R/W)
RES	RES	RES	RES	RES	RES	WD_TIME_3	WD_TIME_2
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Watchdog trigger time 3	Watchdog trigger time 2

Table 60. **DCR1 (0x01) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	WD_TIME_3	Watchdog trigger time 0000: Window 1 0001: Window 2 (default window once WD kick) 0010: Window 3 0011: Window 4 0100: Window 5 0101: Window 6 0110: Window 7 0111: Window 8 1000: Window 9 1001-1110: Window 10 → 5-50 ms window 1111: Stop watchdog The modified WD trigger time is valid after the next WD trig (CSN transition low-high) protected by SPI_PROTECT_ACCESS bit
16	WD_TIME_2	

Table 61. **DCR1 (0x01)**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	1 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
WD_TIME_1	WD_TIME_0	VBUCK3_ENA	VBUCK2_ENA	VBUCK1_ENA	LDO1_ENA	LDO2_ENA	LOW_POWER_SET
Watchdog trigger time 1	Watchdog trigger time 0	BUCK3 enable bit	BUCK2 enable bit	BUCK1 enable bit	LDO1 enable bit	LDO2 enable bit	Set low power mode

Table 62. **DCR1 (0x01) description**

Bit	Name	Description
15	WD_TIME_1	
14	WD_TIME_0	
13	VBUCK3_ENA	BUCK3 enable bit (default value link to start up sequence setting)

Bit	Name	Description
		1: Enable Protected by SPI_PROTECT_ACCESS bit 0: Disabled Note that, after the first power-up is needed to align the live bit associated in DSR18 (VBUCK3_ENA_STATUS) with the current value associated in DCR1
12	VBUCK2_ENA	BUCK2 enable bit (default value link to start up sequence setting) 1: Enable Protected by SPI_PROTECT_ACCESS bit 0: Disabled Note that, after the first power-up is needed to align the live bit associated in DSR18 (VBUCK2_ENA_STATUS) with the current value associated in DCR1
11	VBUCK1_ENA	BUCK1 enable bit (default value link to start up sequence setting) 1: Enable Protected by SPI_PROTECT_ACCESS bit 0: Disabled Note that, after the first power-up is needed to align the live bit associated in DSR18 (VBUCK1_ENA_STATUS) with the current value associated in DCR1
10	LDO1_ENA	LDO1 enable bit (default value link to start up sequence setting) 1: Enable 0: Disabled Protected by SPI_PROTECT_ACCESS bit Note that, after the first power-up is needed to align the live bit associated in DSR18 (LDO1_ENA_STATUS) with the current value associated in DCR1
9	LDO2_ENA	LDO2 enable bit (default value link to start up sequence setting) 1: Enable 0: Disabled Protected by SPI_PROTECT_ACCESS bit Note that, after the first power-up is needed to align the live bit associated in DSR18 (LDO2_ENA_STATUS) with the current value associated in DCR1
8	LOW_POWER_SET	Set low power mode 1: Go to low power 0: Back to full power Protected by SPI_PROTECT_ACCESS bit

Table 63. DCR1 (0x01) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
WD_LP_ENA	DO_POWER_DOWN	U-NVM_PROG	DO_POWER_CYCLE	CRC3	CRC2	CRC1	CRC0
Watchdog in low power mode enable bit	Power-down sequence bit	User NVM program bit	Power cycle bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 64. DCR1 (0x01) LSB description

Bit	Name	Description
7	WD_LP_ENA	1: Watchdog is enabled in low power mode (default)

Bit	Name	Description
		Is taken into account as soon the LOW_POWER_SET bit is set to "1" 0: Watchdog is disabled in Low power mode Is taken into account as soon the LOW_POWER_SET bit is set to "1" Protected by SPI_PROTECT_ACCESS bit
6	DO_POWER_DOWN	1: Execute power down sequence Bit is reset after entry in DEEP-SLEEP state This bit is automatically cleared and always read low 0: No action (default) Protected by SPI_PROTECT_ACCESS bit
5	U-NVM_PROG	To start a user NVM program 0: No action Protected by SPI_PROTECT_ACCESS bit
4	DO_POWER_CYCLE	This bit is automatically cleared and always read low Protected by SPI_PROTECT_ACCESS bit
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 65. DCR2 (0x02) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-(R0)	-(R0)	1 (R/W)	0 (R/W)	0 (R/W)	- (R0)	0 (R/W)	0 (R/W)
RES	RES	NFSO_ASSERT_LOW	LBIST	ABIST	RES	FCCU_COUNTER_12	FCCU_COUNTER_11
Reserved	Reserved	NFSO low bit	Logical bist request bit	Analog bist request bit	Reserved	FCCU counter bit 12	FCCU counter bit 11

Table 66. DCR2 (0x02) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	NFSO_ASSERT_LOW	Force low NFSO pin Protected by SPI_PROTECT_ACCESS bit
20	LBIST	Logical bist request This bit is automatically cleared and always read low Protected by SPI_PROTECT_ACCESS bit
19	ABIST	Analog bist request This bit is automatically cleared and always read low Protected by SPI_PROTECT_ACCESS bit
18	RES	Reserved
17	FCCU_COUNTER_12	FCCU counter value selection Protected by SPI_PROTECT_ACCESS bit

Bit	Name	Description
16	FCCU_COUNTER_11	

Table 67. DCR2 (0x02)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
FCCU_COUNTER_10	FCCU_COUNTER_9	FCCU_COUNTER_8	FCCU_COUNTER_7	FCCU_COUNTER_6	FCCU_COUNTER_5	FCCU_COUNTER_4	FCCU_COUNTER_3
FCCU counter bit 10	FCCU counter bit 9	FCCU counter bit 8	FCCU counter bit 7	FCCU counter bit 6	FCCU counter bit 5	FCCU counter bit 4	FCCU counter bit 3

Table 68. DCR2 (0x02) description

Bit	Name	Description
15	FCCU_COUNTER_10	
14	FCCU_COUNTER_9	
13	FCCU_COUNTER_8	
12	FCCU_COUNTER_7	
11	FCCU_COUNTER_6	
10	FCCU_COUNTER_5	
9	FCCU_COUNTER_4	
8	FCCU_COUNTER_3	

Table 69. DCR2 (0x02) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
FCCU_COUNTER_2	FCCU_COUNTER_1	FCCU_COUNTER_0	FCCU_ENA	CRC3	CRC2	CRC1	CRC0
FCCU counter bit 2	FCCU counter bit 1	FCCU counter bit 0	FCCU monitor enable bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 70. DCR2 (0x02) LSB description

Bit	Name	Description
7	FCCU_COUNTER_2	
6	FCCU_COUNTER_1	
5	FCCU_COUNTER_0	
4	FCCU_ENA	Enable FCCU monitor 1: Enabled 0: Disabled (pull-up/down defined by FCCU_STATIC_ERROR) Protected by SPI_PROTECT_ACCESS bit
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 71. DCR3 (0x03) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-(R0)	-(R0)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	-(R0)	0 (R/W)
RES	RES	BUCK3_SPREAD_ENA	BUCK2_SPREAD_ENA	BUCK1_SPREAD_ENA	CLR_WDFAIL_CNT	RES	BUCK3_FTUNE_2
Reserved	Reserved	BUCK3 spread enable bit	BUCK2 spread enable bit	BUCK1 spread enable bit	Clear WDFAIL_CNT bits	reserved	BUCK3 fine-tune bit 2

Table 72. DCR3 (0x03) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	BUCK3_SPREAD_ENA	Frequency spread selection 1: Enabled 0: Disabled (default)
20	BUCK2_SPREAD_ENA	Frequency spread selection 1: Enabled 0: Disabled (default)
19	BUCK1_SPREAD_ENA	Frequency spread selection 1: Enabled 0: Disabled (default)
18	CLR_WDFAIL_CNT	Clear WDFAIL_CNT to 0 This bit is always read low
17	RES	Reserved
16	BUCK3_FTUNE_2	

Table 73. DCR3 (0x03)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
BUCK3_FTUNE_1	BUCK3_FTUNE_0	BOOST_OFF	FBB_OV_EW_TH_3	FBB_OV_EW_TH_2	FBB_OV_EW_TH_1	FBB_OV_EW_TH_0	FBB_UV_EW_TH_3
BUCK3 fine-tune bit 1	BUCK3 fine-tune bit 0	BOOST disable bit	FBB overvoltage early warning threshold bit 3	FBB overvoltage early warning threshold bit 2	FBB overvoltage early warning threshold bit 1	FBB overvoltage early warning threshold bit 0	FBB undervoltage early warning threshold bit 3

Table 74. DCR3 (0x03) description

Bit	Name	Description
15	BUCK3_FTUNE_1	
14	BUCK3_FTUNE_0	Valid only if U-NVM bits BUCK3_PU_VALUE = 001 11x: 0.95 V 101: 0.96 V 100: 0.97 V 000: 0.98 V (default) 001: 0.99 V 010: 1.00 V 011: 1.01 V
13	BOOST_OFF	Boost disable 1: Boost is disabled 0: Boost feature define by BOOST_DIS U-NVM bit (default)

Bit	Name	Description
12	FBB_OV_EW_TH_3	FBB over voltage early warning threshold At FBB > FBB_OV_EW_TH, an interrupt is generated on IRQ pin and status bit FBB_OV_EW in SR4 is set (in active mode) 0000: (default) feature deactivated 0001: 17 V ... (1 V step) 1111: 31 V
11	FBB_OV_EW_TH_2	
10	FBB_OV_EW_TH_1	
9	FBB_OV_EW_TH_0	
8	FBB_UV_EW_TH_3	FBB undervoltage early warning threshold. At FBB < FBB_UV_EW_TH, an interrupt is generated on IRQ pin and status bit FBB_UV_EW in SR4 is set (in active mode) 0000: (default) feature deactivated 0001: 5 V ... (0.25 V step) 1111: 8.5 V

Table 75. DCR3 (0x03) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
FBB_UV_EW_TH_2	FBB_UV_EW_TH_1	FBB_UV_EW_TH_0	SPI_PROTECT_ACCESS	CRC3	CRC2	CRC1	CRC0
FBB undervoltage early warning threshold bit 2	FBB undervoltage early warning threshold bit 1	FBB undervoltage early warning threshold bit 0	SPI protect access bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 76. DCR3 (0x03) LSB description

Bit	Name	Description
7	FBB_UV_EW_TH_2	
6	FBB_UV_EW_TH_1	
5	FBB_UV_EW_TH_0	
4	SPI_PROTECT_ACCESS	1: Allows write access to protected SPI bits on next write SPI frame This bit is automatically cleared on the next write SPI frame but can be read high before the next write SPI frame 0: Access to protected SPI bits is blocked
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 77. DCR4 (0x04) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	1 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
RES	BOOST_DSMON_TH_2	BOOST_DSMON_TH_1	BOOST_DSMON_TH_0	SWDBG_EXIT	VS_UV_EW_TH_4	VS_UV_EW_TH_3	VS_UV_EW_TH_2

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved	BOOST monitor threshold bit 2	BOOST monitor threshold bit 1	BOOST monitor threshold bit 0	Software debug exit bit	V_S undervoltage early warning threshold bit 4	V_S undervoltage early warning threshold bit 3	V_S undervoltage early warning threshold bit 2

Table 78. DCR4 (0x04) MSB description

Bit	Name	Description
23	RES	Reserved
22	BOOST_DSMON_TH_2	Control BOOST_VDMON_TH 000: 0.3 V 001: 0.5 V 010: 0.7 V 011: 0.9 V 100: 1.1 V 101: 1.3 V 110: 1.5 V 111: 1.7 V
21	BOOST_DSMON_TH_1	
20	BOOST_DSMON_TH_0	
19	SWDBG_EXIT	This bit is active in software debug mode 1: Forces the device to exit software debug mode Watchdog restarts with a LOW 0: No action (default)
18	VS_UV_EW_TH_4	V_S undervoltage early warning threshold At V_S < VS_EW_TH, an interrupt is generated on IRQ pin and the status bit VS_UV_EW in SR4 is set (in active mode) 00000: Feature deactivated (default) 00001: 2.5 V … (0.25 V step) 11111: 10 V
17	VS_UV_EW_TH_3	
16	VS_UV_EW_TH_2	

Table 79. DCR4 (0x04)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	1 (R/W)	0 (R/W)
VS_UV_EW_TH_1	VS_UV_EW_TH_0	FCCU_PROTOCOL	FCCU_STATIC_ERROR	OUTHS_1	OUTHS_0	BYPASS_DSMON_TH_2	BYPASS_DSMON_TH_1
V_S undervoltage early warning threshold bit 1	V_S undervoltage early warning threshold bit 0	FCCU protocol bit	FCCU static error bit	OUTHS configuration bit 1	OUTHS configuration bit 0	BYPASS monitor threshold bit 2	BYPASS monitor threshold bit 1

Table 80. DCR4 (0x04) description

Bit	Name	Description
15	VS_UV_EW_TH_1	
14	VS_UV_EW_TH_0	
13	FCCU_PROTOCOL	1: Toggle (pull-up/down defined by FCCU_STATIC_ERROR) 0: Static (error state defined by FCCU_STATIC_ERROR)

Bit	Name	Description
12	FCCU_STATIC_ERROR	1: Error when FIN1 = 1 (→ pull-up active) 0: Error when FIN1 = 0 (→ pull-down active)
11	OUTHS_1	OUTHS configuration bits 00: Off (default) 01: On 1x: Timer 1
10	OUTHS_0	
9	BYPASS_DSMON_TH_2	
8	BYPASS_DSMON_TH_1	

Table 81. DCR4 (0x04) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
BYPASS_DSMON_TH_0	CLR_REG_FAIL_CNT	KILL_SWDBG_TIMEOUT	WD_TRIG	CRC3	CRC2	CRC1	CRC0
BYPASS monitor threshold bit 0	Clear REG_FAIL_CNT bits	Kill software debug timeout bit	Watchdog trigger bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 82. DCR4 (0x04) LSB description

Bit	Name	Description
7	BYPASS_DSMON_TH_0	
6	CLR_REG_FAIL_CNT	Clear REG_FAIL_CNT to 0 This bit is always read low
5	KILL_SWDBG_TIMEOUT	Kill the 10s timeout that runs when the SWDBG pin is shorted to VIO at start-up. With this bit at '1' the timeout is killed → state machine exits from SWDBG state and transits to REC-1 and the watchdog is started with a LOW. SWDBG mode is then NOT entered. This feature allows the MCU to take control of SPSB100 in case of hardware fault without waiting the 10 s timeout to elapse.
4	WD_TRIG	Watchdog trig alternatively with 0 and 1. First trig has to be with 1 Watchdog trig alternatively with 0 and 1
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 83. DCR5 (0x05) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
RES	CLR_REC2_FROM_DO_POWER_CYCLE	CLR_DEEP_SLEEP_FROM_DO_POWER_DOWN	CLR_POWUP_RETRY_COUNT	T1_ENA_2	T1_ENA_1	T1_ENA_0	T1_PER_2
Reserved	Clear REC2_FROM_DO_POWER_CYCLE bit	Clear DEEP_SLEEP_FROM_DO_POWER_DOWN bit	Clear POWUP_RETRY_COUNT bit	Timer 1 enable bit 2	Timer 1 enable bit 1	Timer 1 enable bit 0	Timer 1 period bit 2

Table 84. DCR5 (0x05) MSB description

Bit	Name	Description
23	RES	Reserved
22	CLR_REC2_FROM_DO_POWER_CYCLE	Clear REC2_FROM_DO_POWER_CYCLE to 0

Bit	Name	Description
		This bit is always read low
21	CLR_DEEP_SLEEP_FROM_DO_POWER_DOWN	Clear DEEP-SLEEP_FROM_DO_POWER_DOWN to 0 This bit is always read low
20	CLR_POWUP_RETRY_COUNT	Clear POWUP_RETRY_CNT to 0 This bit is always read low
19	T1_ENA_2	Configuration of timer 1 ON duration 000: t_{ON1} - 0.1 ms (default) 001: t_{ON2} - 0.3 ms 010: t_{ON3} - 1 ms 011: t_{ON4} - 10 ms 1xx: t_{ON5} - 20 ms
18	T1_ENA_1	
17	T1_ENA_0	
16	T1_PER_2	Configuration of timer 1 period 000: T1 - 10 ms (default) 001: T2 - 20 ms 010: T3 - 50 ms 011: T4 - 100 ms 100: T5 - 200 ms 101: T6 - 500 ms 110: T7 - 1000 ms 111: T8 - 2000 ms

Table 85. DCR5 (0x05)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	1 (R/W)	0 (R/W)	0 (R/W)
T1_PER_1	T1_PER_0	TIMER_WAKE_ENA	IGN_CONFIG	IGN_FILT	IGN_ENA	IGN_PU	WU_CONFIG
Timer 1 period bit 1	Timer 1 period bit 0	Timer wake-up enable bit	IGN configuration bit	IGN filter configuration bit	IGN enable bit	IGN pull-up/ down configuration bit	Wake-up configuration bit

Table 86. DCR5 (0x05) description

Bit	Name	Description
15	T1_PER_1	
14	T1_PER_0	
13	TIMER_WAKE_ENA	Timer wake up enable 1: Wake after timer period 0: No timer wake up capability
12	IGN_CONFIG	Configuration of input pin IGN input configured as wake-up input 1: IGN voltage measurement enabled 0: IGN configured as wake-up input (default)
11	IGN_FILT	IGN filter configuration bits

Bit	Name	Description
		1: IGN input monitored in cyclic mode with Timer1 (filter time: tIGN_cyc, blanking time 80% of timer ON time) 0: IGN input monitored in static mode (filter time tGN_stat) (default)
10	IGN_ENA	IGN input enable: 1: Device wake-up capability by IGN pin enabled (default) 0: No wake-up possible by IGN pin
9	IGN_PU	IGN Pull-up/down configuration 1: PULL-UP 0: PULL-DOWN
8	WU_CONFIG	Configuration of input pin WU input configured as wake-up input 1: WU voltage measurement enabled 0: WU configured as wake-up input (default)

Table 87. DCR5 (0x05) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
WU_ENA	WU_PU	WU_FILT	TIMER_ENA	CRC3	CRC2	CRC1	CRC0
Wake-up enable bit	Wake-up pull-up/down configuration bit	Wake-up filter configuration bit	Timer enable bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 88. DCR5 (0x05) LSB description

Bit	Name	Description
7	WU_ENA	WU input enable: 1: Device wake-up capability by WU pin enabled (default) 0: No wake-up possible by WU pin
6	WU_PU	WU pull-up/down configuration 1: PULL-UP 0: PULL-DOWN
5	WU_FILT	WU filter configuration bits 1: WU input monitored in cyclic mode with Timer1 (filter time: tWU_cyc, blanking time 80% of timer ON time) 0: WU input monitored in static mode (filter time tWU_stat) (default)
4	TIMER_ENA	Enables timer counting 1: Allow counting 0: Counter stopped
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 89. DCR6 (0x06) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
RES	MASK_BUCK3_PG_TIMEOUT_IRQ	MASK_BUCK3_OC_IRQ	MASK_BUCK3_PG_IRQ	MASK_BUCK3_IRQ	MASK_BUCK2_PG_TIMEOUT_IRQ	MASK_BUCK2_OC_IRQ	MASK_BUCK2_PG_IRQ
Reserved	Mask BUCK3 PG timeout interrupt bit	Mask BUCK3 over current interrupt bit	Mask BUCK3 PG interrupt bit	Mask BUCK3 interrupt bit	Mask BUCK2 PG timeout interrupt bit	Mask BUCK2 over current interrupt bit	Mask BUCK2 PG interrupt bit

Table 90. DCR6 (0x06) MSB description

Bit	Name	Description
23	RES	Reserved
22	MASK_BUCK3_PG_TIMEOUT_IRQ	Mask BUCK PG timeout interruption when turned on by SPI command When turned on by a power-up sequence, IRQ is never masked 1: IRQ signal is not generated 0: IRQ signal is generated (default)
21	MASK_BUCK3_OC_IRQ	Mask BUCK over current interruption 1: IRQ signal is not generated 0: IRQ signal is generated (default)
20	MASK_BUCK3_PG_IRQ	Mask BUCK power-good interruption when turned ON through SPI 1: IRQ signal is not generated 0: IRQ signal is generated when the regulator is turned ON through SPI (default)
19	MASK_BUCK3_IRQ	Mask BUCK interruption for over voltage, undervoltage and for buck internal OV or UV in high or low power 1: IRQ signal is not generated 0: IRQ signal is generated (default)
18	MASK_BUCK2_PG_TIMEOUT_IRQ	Mask BUCK PG timeout interruption when turned on by SPI command When turned on by power-up sequence, IRQ is never masked 1: IRQ signal is not generated 0: IRQ signal is generated (default)
17	MASK_BUCK2_OC_IRQ	Mask BUCK over current interruption 1: IRQ signal is not generated 0: IRQ signal is generated (default)
16	MASK_BUCK2_PG_IRQ	reserved

Table 91. DCR6 (0x06)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
MASK_BUCK2_IRQ	MASK_BUCK1_PG_TIMEOUT_IRQ	MASK_BUCK1_OC_IRQ	MASK_BUCK1_PG_IRQ	MASK_BUCK1_IRQ	MASK_FBB_OV_IRQ	MASK_FBB_UV_IRQ	MASK_FBB_OV_EW_IRQ
Mask BUCK2 interrupt bit	Mask BUCK1 PG timeout interrupt bit	Mask BUCK1 overcurrent interrupt bit	Mask BUCK1 PG interrupt bit	Mask BUCK1 interrupt bit	Mask FBB overvoltage interrupt bit	Mask FBB undervoltage interrupt bit	Mask FBB overvoltage early warning interrupt bit

Table 92. DCR6 (0x06) description

Bit	Name	Description
15	MASK_BUCK2_IRQ	Mask BUCK interruption for over voltage, undervoltage and for buck internal OV or UV in high or low power 1: IRQ signal is not generated 0: IRQ signal is generated (default)
14	MASK_BUCK1_PG_TIMEOUT_IRQ	Mask BUCK PG timeout interruption when turned on by SPI command When turned on by a power-up sequence, IRQ is never masked 1: IRQ signal is not generated

Bit	Name	Description
		0: IRQ signal is generated (default)
13	MASK_BUCK1_OC_IRQ	Mask BUCK overcurrent interruption 1: IRQ signal is not generated 0: IRQ signal is generated (default)
12	MASK_BUCK1_PG_IRQ	Mask BUCK power-good interruption when turned ON through SPI 1: IRQ signal is not generated 0: IRQ signal is generated when the regulator is turned ON through SPI (default)
11	MASK_BUCK1_IRQ	Mask BUCK interruption for overvoltage, undervoltage and for BUCK internal OV or UV in high or low power 1: IRQ signal is not generated 0: IRQ signal is generated (default)
10	MASK_FBB_OV_IRQ	1: IRQ masked 0: IRQ not masked
9	MASK_FBB_UV_IRQ	1: IRQ masked 0: IRQ not masked
8	MASK_FBB_OV_EW_IRQ	1: IRQ masked 0: IRQ not masked

Table 93. DCR6 (0x06) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
MASK_FBB_UV_EW_IRQ	MASK_LDO2_PG_IRQ	MASK_LDO2_PG_TIMEOUT_IRQ	MASK_LDO2_IRQ	CRC3	CRC2	CRC1	CRC0
Mask FBB undervoltage early warning interrupt bit	Mask LDO2 PG interrupt bit	Mask LDO2 PG timeout interrupt bit	Mask LDO2 interrupt bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 94. DCR6 (0x06) LSB description

Bit	Name	Description
7	MASK_FBB_UV_EW_IRQ	1: IRQ masked 0: IRQ not masked
6	MASK_LDO2_PG_IRQ	Mask regulator power-good interruption when turned ON through SPI No interrupt generated when turned on by power-up sequence 1: IRQ signal is not generated 0: IRQ signal is generated when the regulator is turned ON through SPI (default)
5	MASK_LDO2_PG_TIMEOUT_IRQ	Mask LDO2 power-good timeout when turned on by SPI request No interrupt generated when turned on by power-up sequence 1: IRQ signal is not generated 0: IRQ signal is generated (default)
4	MASK_LDO2_IRQ	Mask LDO2 overvoltage or undervoltage interruption 1: IRQ signal is not generated 0: IRQ signal is generated (default)
3	CRC3	
2	CRC2	
1	CRC1	

Bit	Name	Description
0	CRC0	

Table 95. DCR7 (0x07) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
RES	MASK_LDO1_PG_IRQ	MASK_LDO1_PG_TIMEOUT_IRQ	MASK_LDO1_IRQ	MASK_BOOST_IN_LP_IRQ	MASK_BYPASS_VDSMON_IRQ	MASK_BOOST_VDSMON_IRQ	IRQ_REQUEST
Reserved	Mask LDO1 PG interrupt bit	Mask LDO1 PG timeout interrupt bit	Mask LDO1 interrupt bit	Mask BOOST in Low power mode interrupt bit	Mask bypass VDSMON interrupt bit	Mask BOOST VDSMON interrupt bit	Interrupt request bit

Table 96. DCR7 (0x07) MSB description

Bit	Name	Description
23	RES	Reserved
22	MASK_LDO1_PG_IRQ	Mask regulator power-good interruption when turned ON through SPI No interrupt generated when turned on by power-up sequence 1: IRQ signal is not generated 0: IRQ signal is generated when the regulator is turned ON through SPI (default)
21	MASK_LDO1_PG_TIMEOUT_IRQ	Mask LDO1 power-good timeout when turned on by SPI request No interrupt generated when turned on by power-up sequence 1: IRQ signal is not generated 0: IRQ signal is generated (default)
20	MASK_LDO1_IRQ	Mask LDO1 undervoltage interruption 1: IRQ signal is not generated 0: IRQ signal is generated (default)
19	MASK_BOOST_IN_LP_IRQ	1: IRQ masked 0: IRQ not masked
18	MASK_BYPASS_VDSMON_IRQ	1: IRQ masked 0: IRQ not masked
17	MASK_BOOST_VDSMON_IRQ	1: IRQ masked 0: IRQ not masked
16	IRQ_REQUEST	1: Send IRQ to MCU This bit is automatically cleared and always read low 0: No action

Table 97. DCR7 (0x07)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
MASK_VS_EW_IRQ	RES	MASK_CL4_TW_IRQ	MASK_CL3_TW_IRQ	MASK_CL2_TW_IRQ	MASK_CL1_TW_IRQ	MASK_CL0_TW_IRQ	MASK_OUTHS_IRQ
Mask V_S early warning interrupt bit	Reserved bit	Mask current limitation 4 thermal warning interrupt bit	Mask current limitation 3 thermal warning interrupt bit	Mask current limitation 2 thermal warning interrupt bit	Mask current limitation 1 thermal warning interrupt bit	Mask current limitation 0 thermal warning interrupt bit	Mask out high side interrupt bit

Table 98. DCR7 (0x07) description

Bit	Name	Description
15	MASK_VS_EW_IRQ	1: IRQ masked 0: IRQ not masked

Bit	Name	Description
14	RES	Reserved
13	MASK_CL4_TW_IRQ	1: IRQ masked 0: IRQ not masked
12	MASK_CL3_TW_IRQ	1: IRQ masked 0: IRQ not masked
11	MASK_CL2_TW_IRQ	1: IRQ masked 0: IRQ not masked
10	MASK_CL1_TW_IRQ	1: IRQ masked 0: IRQ not masked
9	MASK_CL0_TW_IRQ	1: IRQ masked 0: IRQ not masked
8	MASK_OUTHS_IRQ	1: IRQ masked 0: IRQ not masked

Table 99. DCR7 (0x07) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
MASK_SPI_ERROR_IRQ	MASK_NFSO1_ECHO_ERROR_IRQ	MASK_WD_ENA_ECHO_ERROR_IRQ	MASK_FCCU_ENA_ECHO_ERROR_IRQ	CRC3	CRC2	CRC1	CRC0
Mask SPI error interrupt bit	Mask NFSO1 echo error interrupt bit	Mask watchdog enable echo error interrupt bit	Mask FCCU enable echo error interrupt bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 100. DCR7 (0x07) LSB description

Bit	Name	Description
7	MASK_SPI_ERROR_IRQ	1: IRQ masked 0: IRQ not masked
6	MASK_NFSO1_ECHO_ERROR_IRQ	1: IRQ masked 0: IRQ not masked
5	MASK_WD_ENA_ECHO_ERROR_IRQ	1: IRQ masked 0: IRQ not masked
4	MASK_FCCU_ENA_ECHO_ERROR_IRQ	1: IRQ masked 0: IRQ not masked
3	CRC3	
2	CRC2	
1	CRC1	
0	CRC0	

Table 101. DCR8 (0x08) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
RES	MASK_SWDBG_VIO_IRQ	MASK_LP_READY_IRQ	CLR_TSD_CNT_FAIL	MASK_BUCK3_OC_POWER_OFF	MASK_BUCK2_OC_POWER_OFF	MASK_BUCK1_OC_POWER_OFF	MASK_BUCK3_UV_POWER_OFF
Reserved	Mask software debug VIO interrupt bit	Mask low power mode ready interrupt bit	Clear TSD_CNT_FAIL bit	Mask BUCK3 overcurrent power off bit	Mask BUCK2 overcurrent power off bit	Mask BUCK1 overcurrent power off bit	Mask BUCK3 undervoltage power off bit

Table 102. DCR8 (0x08) MSB description

Bit	Name	Description
23	RES	reserved
22	MASK_SWDBG_VIO_IRQ	Mask IRQ when SWDBG is still at V_{IO} at the end of timeout detection. In this case, watchdog is restarted with a long open window and SWDBG is ignored. 1: IRQ is masked 0: IRQ not masked
21	MASK_LP_READY_IRQ	Mask IRQ when FSM goes to low power state. 1: IRQ is masked 0: IRQ not masked
20	CLR_TSD_CNT_FAIL	Clear TSD_CNT_FAIL to 0 This bit is always read low
19	MASK_BUCK3_OC_POWER_OFF	Mask regulator over current as source of its power off 1: Regulator is not turned off after an over current occurs 0: Regulator is turned off after an over current occurs
18	MASK_BUCK2_OC_POWER_OFF	Mask regulator over current as source of its power off 1: Regulator is not turned off after an over current occurs 0: Regulator is turned off after an over current occurs
17	MASK_BUCK1_OC_POWER_OFF	Mask regulator over current as source of its power off 1: Regulator is not turned off after an over current occurs 0: Regulator is turned off after an over current occurs
16	MASK_BUCK3_UV_POWER_OFF	Mask regulator under voltage as source of its power off 1: Regulator is not turned off after an under voltage occurs 0: Regulator is turned off after an under voltage occurs

Table 103. DCR8 (0x08)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
MASK_BUCK2_UV_POWER_OFF	MASK_BUCK1_UV_POWER_OFF	MASK_TW_GW	MASK_OL_GSB	RES	MASK_GW_GSB	RES	RES
Mask BUCK2 undervoltage power off bit	Mask BUCK1 undervoltage power off bit	Mask thermal warning GW bit	Mask open load GSB bit	RES	Mask global warning GSB bit	RES	Reserved

Table 104. DCR8 (0x08) description

Bit	Name	Description
15	MASK_BUCK2_UV_POWER_OFF	Mask regulator undervoltage as source of its power off 1: Regulator is not turned off after an undervoltage occurs 0: Regulator is turned off after an undervoltage occurs
14	MASK_BUCK1_UV_POWER_OFF	Mask regulator undervoltage as source of its power off 1: Regulator is not turned off after an undervoltage occurs 0: Regulator is turned off after an undervoltage occurs
13	MASK_TW_GW	Mask thermal Warnings 1: Thermal warnings are masked in GW 0: Thermal warnings are not masked (default)
12	MASK_OL_GSB	Mask open-load 1: Open-load condition at OUTHS is masked It is reported as a functional error 1 (GSB bit 3) but not as a global error (GSB bit 7)

Bit	Name	Description
		0: Open-load condition at OUTHS is not masked (default)
11	RES	Reserved
10	MASK_GW_GSB	Mask global warning 1: Global warning conditions are masked It is reported as a global warning (GSB bit 1) but not as a global error (GSB bit 7) 0: Global warning conditions are not masked (default)
9	RES	Reserved
8	RES	Reserved

Table 105. DCR8 (0x08) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R/W)	0 (R/W)	1 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)	0 (R/W)
RES	RES	RES	GO_INIT	CRC3	CRC2	CRC1	CRC0
Reserved	Reserved	Reserved	NVM init bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 106. DCR8 (0x08) LSB description

Bit	Name	Description
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	GO_INIT	1: NVM emulation and load phases are completed and INIT state can be executed (valid only in USER_NVM_PROG state) This bit is automatically cleared and always read low and always read low 0: (default)
3	CRC3	
2	CRC2	
1	CRC1	
0	CRC0	

9.6 U_NVM registers

During the emulation mode (described in the Section 3.8.2: USER-NVM emulation) U_NVM SPI registers from DCR10 to DRC28 can be R/W, instead after valid USER-NVM programming procedure the U_NVM SPI registers from DCR10 to DRC28 can be only readable as showed below.

Table 107. DCR10 (0x0A) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	BUCK1_FREQ	BUCK1_PU_VALUE_1	BUCK1_PU_VALUE_0	BUCK1_PU_STEP_ENA_2
Reserved	Reserved	Reserved	Reserved	BUCK1 frequency bit	BUCK1 pull-up value bit 1	BUCK1 pull-up value bit 0	BUCK1 pull-up step enables bit 2

Table 108. DCR10 (0x0A) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	BUCK1_FREQ	BUCK1 frequency: 1: 0.4 MHz 0: 2.4 MHz
18	BUCK1_PU_VALUE_1	BUCK1 voltage setting 00: 3.3 V 01: 5.0 V 1X: 6.5 V
17	BUCK1_PU_VALUE_0	
16	BUCK1_PU_STEP_ENA_2	

Table 109. DCR10 (0x0A)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
BUCK1_PU_STEP_ENA_1	BUCK1_PU_STEP_ENA_0	BUCK1_PD_STEP_OFF_2	BUCK1_PD_STEP_OFF_1	BUCK1_PD_STEP_OFF_0	BUCK1_IPEAK_2	BUCK1_IPEAK_1	BUCK1_IPEAK_0
BUCK1 pull-up step enables bit 1	BUCK1 pull-up step enables bit 0	BUCK1 power-down step off bit 2	BUCK1 power-down step off bit 1	BUCK1 power-down step off bit 0	BUCK1 peak limitation current bit 2	BUCK1 peak limitation current bit 1	BUCK1 peak limitation current bit 0

Table 110. DCR10 (0x0A) description

Bit	Name	Description
15	BUCK1_PU_STEP_ENA_1	
14	BUCK1_PU_STEP_ENA_0	To define BUCK1 turn-on steps 000: BUCK is not turned ON 001: Step 1 010: Step 2 011: Step 3 100: Step 4 101: Step 5 110: Step 6 111: Step 7

Bit	Name	Description
13	BUCK1_PD_STEP_OFF_2	
12	BUCK1_PD_STEP_OFF_1	
11	BUCK1_PD_STEP_OFF_0	To define BUCK1 turn-off steps 000: Step 1 001: Step 2 010: Step 3 011: Step 4 100: Step 5 101: Step 6 11X: Step 7
10	BUCK1_IPEAK_2	
9	BUCK1_IPEAK_1	
8	BUCK1_IPEAK_0	BUCK1 peak limitation current 000: 2.0 A 001: 2.5 A 010: 3.0 A 011: 3.5 A 100: 4.0 A 101: 4.5 A 11X: 5.0 A

Table 111. DCR10 (0x0A) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
BUCK1_REGFAIL_GO_REC	BUCK1_SS_VALUE_1	BUCK1_SS_VALUE_0	BUCK1_REFRESH_FREQ	CRC3	CRC2	CRC1	CRC0
BUCK1 regulator fail receive bit	BUCK1 soft start value bit 1	BUCK1 soft start value bit 0	BUCK1 refresh frequency bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 112. DCR10 (0x0A) LSB description

Bit	Name	Description
7	BUCK1_REGFAIL_GO_REC	1: A fail on BUCK1 regulator initiates a power-down sequence and moves the state machine to REC-2 state 0: A fail on BUCK1 regulator sends an IRQ (UV, OV, PG_nok, TW are maskable by SPI, but not TSD), and turns the regulator OFF if the fail is unmasked (UV, PG_nok are maskable by SPI, but not OV and TSD. TW never turns the regulator OFF)
6	BUCK1_SS_VALUE_1	
5	BUCK1_SS_VALUE_0	BUCK1 soft start setting 00: 16.5 V/ms 01: 8.25 V/ms 10: 3.3 V/ms 11: 1.65 V/ms
4	BUCK1_REFRESH_FREQ	1: Refresh frequency 1 kHz 0: Refresh frequency 25 kHz
3	CRC3	
2	CRC2	

Bit	Name	Description
1	CRC1	
0	CRC0	

Table 113. DCR11 (0x0B) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	BUCK2_FREQ	BUCK2_PU_VALUE_1	BUCK2_PU_VALUE_0	BUCK2_PU_STEP_ENA_2
Reserved	Reserved	Reserved	Reserved	BUCK2 frequency bit	BUCK2 pull-up value bit 1	BUCK2 pull-up value bit 0	BUCK2 pull-up step enables bit 2

Table 114. DCR11 (0x0B) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	BUCK2_FREQ	BUCK2 frequency 1: 0.4 MHz 0: 2.4 MHz
18	BUCK2_PU_VALUE_1	BUCK2 voltage setting 00: 3.3 V 01: 5.0 V 1X: 6.5 V
17	BUCK2_PU_VALUE_0	
16	BUCK2_PU_STEP_ENA_2	

Table 115. DCR11 (0x0B)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
BUCK2_PU_STEP_ENA_1	BUCK2_PU_STEP_ENA_0	BUCK2_PD_STEP_OFF_2	BUCK2_PD_STEP_OFF_1	BUCK2_PD_STEP_OFF_0	BUCK2_IPEAK_2	BUCK2_IPEAK_1	BUCK2_IPEAK_0
BUCK2 pull-up step enables bit 1	BUCK2 pull-up step enables bit 0	BUCK2 pull-down step off bit 2	BUCK2 pull-down step off bit 1	BUCK2 pull-down step off bit 0	BUCK2 peak limitation current bit 2	BUCK2 peak limitation current bit 1	BUCK2 peak limitation current bit 0

Table 116. DCR11 (0x0B) description

Bit	Name	Description
15	BUCK2_PU_STEP_ENA_1	
14	BUCK2_PU_STEP_ENA_0	To define BUCK2 turn-on steps 000: BUCK is not turned ON 001: Step 1 010: Step 2 011: Step 3 100: Step 4 101: Step 5 110: Step 6 111: Step 7

Bit	Name	Description
13	BUCK2_PD_STEP_OFF_2	
12	BUCK2_PD_STEP_OFF_1	
11	BUCK2_PD_STEP_OFF_0	To define BUCK2 turn-off steps 000: Step 1 001: Step 2 010: Step 3 011: Step 4 100: Step 5 101: Step 6 11X: Step 7
10	BUCK2_IPEAK_2	
9	BUCK2_IPEAK_1	
8	BUCK2_IPEAK_0	BUCK2 peak limitation current 000: 2.0 A 001: 2.5 A 010: 3.0 A 011: 3.5 A 100: 4.0 A 101: 4.5 A 11X: 5.0 A

Table 117. DCR11 (0x0B) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
BUCK2_REGFAIL_GO_REC	BUCK2_SS_VALUE_1	BUCK2_SS_VALUE_0	BUCK2_REFRESH_FREQ	CRC3	CRC2	CRC1	CRC0
BUCK2 regulator fail receive bit	BUCK2 soft start value bit 1	BUCK2 soft start value bit 0	BUCK2 refresh frequency bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 118. DCR11 (0x0B) LSB description

Bit	Name	Description
7	BUCK2_REGFAIL_GO_REC	1: A fail on BUCK2 regulator initiates a power-down sequence and moves the state machine to REC-2 state 0: A fail on BUCK2 regulator sends an IRQ (UV, OV, PG_nok, TW are maskable by SPI, but not TSD), and turns the regulator OFF if the fail is unmasked (UV, PG_nok are maskable by SPI, but not OV and TSD. TW never turns the regulator OFF)
6	BUCK2_SS_VALUE_1	
5	BUCK2_SS_VALUE_0	BUCK2 soft start setting 00: 16.5 V/ms 01: 8.25 V/ms 10: 3.3 V/ms 11: 1.65 V/ms
4	BUCK2_REFRESH_FREQ	1: Refresh frequency 1 kHz 0: Refresh frequency 25 kHz
3	CRC3	
2	CRC2	

Bit	Name	Description
1	CRC1	
0	CRC0	

Table 119. DCR12 (0x0C) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
-(R0)	-(R0)	-(R0)	-(R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	BYPASS_DIS	BUCK3_PU_VALUE_2	BUCK3_PU_VALUE_1	BUCK3_PU_VALUE_0
Reserved	Reserved	Reserved	Reserved	Bypass disable bit	BUCK3 pull-up value bit 2	BUCK3 pull-up value bit 1	BUCK3 pull-up value bit 0

Table 120. DCR12 (0x0C) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	BYPASS_DIS	If bit BYPASS_DIS = 1: BYPASS will always be OFF If bit BYPASS_DIS = 0: BYPASS will be ON and OFF based on the sensed Vbat value
18	BUCK3_PU_VALUE_2	
17	BUCK3_PU_VALUE_1	
16	BUCK3_PU_VALUE_0	BUCK3 voltage setting 001: 0.98 V 010: 1.1 V 011: 1.2 V 100: 1.25 V 101: 3.3 V 11X: 3.3 V

Table 121. DCR12 (0x0C)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
BUCK3_PU_STEP_ENA_2	BUCK3_PU_STEP_ENA_1	BUCK3_PU_STEP_ENA_0	BUCK3_PD_STEP_OFF_2	BUCK3_PD_STEP_OFF_1	BUCK3_PD_STEP_OFF_0	BUCK3_IPEAK_1	BUCK3_IPEAK_0
BUCK3 pull-up step enables bit 2	BUCK3 pull-up step enables bit 1	BUCK3 pull-up step enables bit 0	BUCK3 pull-down step off bit 2	BUCK3 pull-down step off bit 1	BUCK3 pull-down step off bit 0	BUCK3 peak switching current bit 1	BUCK3 peak switching current bit 0

Table 122. DCR12 (0x0C) description

Bit	Name	Description
15	BUCK3_PU_STEP_ENA_2	
14	BUCK3_PU_STEP_ENA_1	
13	BUCK3_PU_STEP_ENA_0	To define BUCK3 turn-on steps 000: BUCK is not turned ON 001: Step 1 010: Step 2

Bit	Name	Description
		011: Step 3 100: Step 4 101: Step 5 110: Step 6 111: Step 7
12	BUCK3_PD_STEP_OFF_2	To define BUCK3 turn-off steps 000: Step 1 001: Step 2 010: Step 3 011: Step 4 100: Step 5 101: Step 6 11X: Step 7
11	BUCK3_PD_STEP_OFF_1	
10	BUCK3_PD_STEP_OFF_0	
9	BUCK3_IPEAK_1	BUCK3 peak switching current 00: 4.0 A 01: 5.0 A 10: 6.0 A 11: 7.2 A
8	BUCK3_IPEAK_0	

Table 123. DCR12 (0x0C) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
BUCK3_REGFAIL_GO_REC	BUCK3_SS_VALUE_1	BUCK3_SS_VALUE_0	BUCK3_REFRESH_FREQ	CRC3	CRC2	CRC1	CRC0
BUCK3 regulator fail go receiver bit	BUCK3 soft start value bit 1	BUCK3 soft start value bit 0	BUCK3 refresh frequency bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 124. DCR12 (0x0C) LSB description

Bit	Name	Description
7	BUCK3_REGFAIL_GO_REC	1: A fail on BUCK3 regulator initiates a power-down sequence and moves the state machine to REC-2 state 0: A fail on BUCK3 regulator sends an IRQ (UV, OV, PG_nok, TW are maskable by SPI, but not TSD), and turns the regulator OFF if the fail is unmasked (UV, PG_nok are maskable by SPI, but not OV and TSD. TW never turns the regulator OFF)
6	BUCK3_SS_VALUE_1	BUCK3 soft start setting 00: 8.V/ms 01: 4.3 V/ms 10: 1.7 V/ms 11: 0.8 V/ms
5	BUCK3_SS_VALUE_0	
4	BUCK3_REFRESH_FREQ	1: Refresh frequency 1 kHz 0: Refresh frequency 25 kHz
3	CRC 3	

Bit	Name	Description
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 125. DCR13 (0x0D) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_D_15	U_NVM_D_14	U_NVM_D_13	U_NVM_D_12
Reserved	Reserved	Reserved	Reserved	User NVM D register bit 15	User NVM D register bit 14	User NVM D register bit 13	User NVM D register bit 12

Table 126. DCR13 (0x0D) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_D_15	User NVM regs Can be emulated when FSM in U_PROG_1 state
18	U_NVM_D_14	
17	U_NVM_D_13	
16	U_NVM_D_12	

Table 127. DCR13 (0x0D)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_D_11	U_NVM_D_10	U_NVM_D_9	U_NVM_D_8	U_NVM_D_7	U_NVM_D_6	U_NVM_D_5	U_NVM_D_4
User NVM D register bit 11	User NVM D register bit 10	User NVM D register bit 9	User NVM D register bit 8	User NVM D register bit 7	User NVM D register bit 6	User NVM D register bit 5	User NVM D register bit 4

Table 128. DCR13 (0x0D) description

Bit	Name	Description
15	U_NVM_D_11	
14	U_NVM_D_10	
13	U_NVM_D_9	
12	U_NVM_D_8	
11	U_NVM_D_7	
10	U_NVM_D_6	
9	U_NVM_D_5	
8	U_NVM_D_4	

Table 129. **DCR13 (0x0D) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_D_3	U_NVM_D_2	U_NVM_D_1	U_NVM_D_0	CRC3	CRC2	CRC1	CRC0
User NVM D register bit 3	User NVM D register bit 2	User NVM D register bit 1	User NVM D register bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 130. **DCR13 (0x0D) LSB description**

Bit	Name	Description
7	U_NVM_D_3	
6	U_NVM_D_2	
5	U_NVM_D_1	
4	U_NVM_D_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 131. **DCR14 (0x0E) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	PU_LOOP_FOR_EVER	LDO2_REGFAIL_GO_REC	LDO2_TRK_1	LDO2_TRK_0
Reserved	Reserved	Reserved	Reserved	Pull-up infinite loop bit	LDO2 regulator fail go receiver bit	LDO2 tracker bit 1	LDO2 tracker bit 0

Table 132. **DCR14 (0x0E) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	PU_LOOP_FOR_EVER	User NVM regs Can be emulated when FSM in U_PROG_1 state
18	LDO2_REGFAIL_GO_REC	1: A fail on LDO2 regulator initiates a power-down sequence and moves the state machine to REC-2 state 0: A fail on LDO2 regulator sends an IRQ (UV, OV, PG_nok, TW are maskable by SPI, but not TSD), and turns the regulator OFF if the fail is unmasked (UV, PG_nok are maskable by SPI, but not OV and TSD. TW never turns the regulator OFF)
17	LDO2_TRK_1	
16	LDO2_TRK_0	

Table 133. DCR14 (0x0E)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
LDO2_PD_STEP_OFF_2	LDO2_PD_STEP_OFF_1	LDO2_PD_STEP_OFF_0	LDO2_PU_STEP_ENA_2	LDO2_PU_STEP_ENA_1	LDO2_PU_STEP_ENA_0	LDO1_PD_STEP_OFF_2	LDO1_PD_STEP_OFF_1
LDO2 pull-down step off bit 2	LDO2 pull-down step off bit 1	LDO2 pull-down step off bit 0	LDO2 pull-up step enables bit 2	LDO2 pull-up step enables bit 1	LDO2 pull-up step enables bit 0	LDO1 pull-down step off bit 2	LDO1 pull-down step off bit 1

Table 134. DCR14 (0x0E) description

Bit	Name	Description
15	LDO2_PD_STEP_OFF_2	To define LDO2 turn-off steps 000: Step 1 001: Step 2 010: Step 3 011: Step 4 100: Step 5 101: Step 6 11X: Step 7
14	LDO2_PD_STEP_OFF_1	
13	LDO2_PD_STEP_OFF_0	
12	LDO2_PU_STEP_ENA_2	To define LDO2 turn-on steps 000: LDO2 is not turned ON 001: Step 1 010: Step 2 011: Step 3 100: Step 4 101: Step 5 110: Step 6 111: Step 7
11	LDO2_PU_STEP_ENA_1	
10	LDO2_PU_STEP_ENA_0	
9	LDO1_PD_STEP_OFF_2	To define LDO1 turn-off steps 000: Step 1 001: Step 2 010: Step 3 011: Step 4 100: Step 5 101: Step 6 11X: Step 7
8	LDO1_PD_STEP_OFF_1	

Table 135. DCR14 (0x0E) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
LDO1_PD_STEP_OFF_0	LDO1_PU_STEP_ENA_2	LDO1_PU_STEP_ENA_1	LDO1_PU_STEP_ENA_0	CRC3	CRC2	CRC1	CRC0
LDO1 pull-down step off bit 0	LDO1 pull-up step enables bit 2	LDO1 pull-up step enables bit 1	LDO1 pull-up step enables bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 136. **DCR14 (0x0E) LSB description**

Bit	Name	Description
7	LDO1_PD_STEP_OFF_0	
6	LDO1_PU_STEP_ENA_2	To define LDO1 turn-on steps 000: LDO1 is not turned ON 001: Step 1 010: Step 2 011: Step 3 100: Step 4 101: Step 5 110: Step 6 111: Step 7
5	LDO1_PU_STEP_ENA_1	
4	LDO1_PU_STEP_ENA_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 137. **DCR15 (0x0F) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_F_15	U_NVM_F_14	PU_WAIT_DEL_ENA_7_1	PU_WAIT_DEL_ENA_7_0
Reserved	Reserved	Reserved	Reserved	User NVM F register bit 15	User NVM F register bit 14	Pull-up wait delay enable 7 bit 1	Pull-up wait delay enable 7 bit 0

Table 138. **DCR15 (0x0F) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_F_15	User NVM regs Can be emulated when FSM in U_PROG_1 state
18	U_NVM_F_14	
17	PU_WAIT_DEL_ENA_7_1	Power up delay at step 7 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
16	PU_WAIT_DEL_ENA_7_0	

Table 139. DCR15 (0x0F)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
PU_WAIT_DEL_ENA_6_1	PU_WAIT_DEL_ENA_6_0	PU_WAIT_DEL_ENA_5_1	PU_WAIT_DEL_ENA_5_0	PU_WAIT_DEL_ENA_4_1	PU_WAIT_DEL_ENA_4_0	PU_WAIT_DEL_ENA_3_1	PU_WAIT_DEL_ENA_3_0
Pull-up wait delay enable 6 bit 1	Pull-up wait delay enable 6 bit 0	Pull-up wait delay enable 5 bit 1	Pull-up wait delay enable 5 bit 0	Pull-up wait delay enable 4 bit 1	Pull-up wait delay enable 4 bit 0	Pull-up wait delay enable 3 bit 1	Pull-up wait delay enable 3 bit 0

Table 140. DCR15 (0x0F) description

Bit	Name	Description
15	PU_WAIT_DEL_ENA_6_1	Power up delay at step 6 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
14	PU_WAIT_DEL_ENA_6_0	
13	PU_WAIT_DEL_ENA_5_1	Power up delay at step 5 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
12	PU_WAIT_DEL_ENA_5_0	
11	PU_WAIT_DEL_ENA_4_1	Power up delay at step 4 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
10	PU_WAIT_DEL_ENA_4_0	
9	PU_WAIT_DEL_ENA_3_1	Power up delay at step 3 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
8	PU_WAIT_DEL_ENA_3_0	

Table 141. DCR15 (0x0F) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
PU_WAIT_DEL_ENA_2_1	PU_WAIT_DEL_ENA_2_0	PU_WAIT_DEL_ENA_1_1	PU_WAIT_DEL_ENA_1_0	CRC3	CRC2	CRC1	CRC0
Pull-up wait delay enable 2 bit 1	Pull-up wait delay enable 2 bit 0	Pull-up wait delay enable 1 bit 1	Pull-up wait delay enable 1 bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 142. DCR15 (0x0F) LSB description

Bit	Name	Description
7	PU_WAIT_DEL_ENA_2_1	Power up delay at step 2 00: 0 ms 01: 2 ms

Bit	Name	Description
		10: 5 ms 11: 10 ms
6	PU_WAIT_DEL_ENA_2_0	
5	PU_WAIT_DEL_ENA_1_1	Power up delay at step 1 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
4	PU_WAIT_DEL_ENA_1_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 143. DCR16 (0x10) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_G_15	U_NVM_G_14	U_NVM_G_13	NRESET_PD_STEP_ASSERT_2
Reserved	Reserved	Reserved	Reserved	User NVM G register bit 15	User NVM G register bit 14	User NVM G register bit 13	NRESET pull-down step assertion bit 2

Table 144. DCR16 (0x10) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_G_15	User NVM regs Can be emulated when FSM in U_PROG_1 state
18	U_NVM_G_14	
17	U_NVM_G_13	
16	NRESET_PD_STEP_ASSERT_2	To define NRESET assertion steps 000: Step 1 001: Step 2 010: Step 3 011: Step 4 100: Step 5 101: Step 6 11x: Step 7

Table 145. DCR16 (0x10)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
NRESET_PD_STEP_ASSERT_1	NRESET_PD_STEP_ASSERT_0	NRESET_PU_STEP_DEASSERT_2	NRESET_PU_STEP_DEASSERT_1	NRESET_PU_STEP_DEASSERT_0	PU_WAIT_PG_ENA_7	PU_WAIT_PG_ENA_6	PU_WAIT_PG_ENA_5
NRESET pull-down step assertion bit 1	NRESET pull-down step assertion bit 0	NRESET pull-up step deassertion bit 2	NRESET pull-up step deassertion bit 1	NRESET pull-up step deassertion bit 0	Pull-up wait power good enable bit 7	Pull-up wait power good enable bit 6	Pull-up wait power good enable bit 5

Table 146. DCR16 (0x10) description

Bit	Name	Description
15	NRESET_PD_STEP_ASSERT_1	
14	NRESET_PD_STEP_ASSERT_0	
13	NRESET_PU_STEP_DEASSERT_2	To define NRESET deassertion and WD start step 000: End of step 7 001: Step 1 010: Step 2 011: Step 3 100: Step 4 101: Step 5 110: Step 6 111: Step 7
12	NRESET_PU_STEP_DEASSERT_1	
11	NRESET_PU_STEP_DEASSERT_0	
10	PU_WAIT_PG_ENA_7	1: At power-up step 7 waits for power-good signal 0: At power-up step 7 does not wait for a power-good signal
9	PU_WAIT_PG_ENA_6	1: At power-up step 6 waits for power-good signal 0: At power-up step 6 does not wait for a power-good signal
8	PU_WAIT_PG_ENA_5	1: At power-up step 5 waits for power-good signal 0: At power-up step 5 does not wait for a power-good signal

Table 147. DCR16 (0x10) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
PU_WAIT_PG_ENA_4	PU_WAIT_PG_ENA_3	PU_WAIT_PG_ENA_2	PU_WAIT_PG_ENA_1	CRC3	CRC2	CRC1	CRC0
Pull-up wait power-good enable bit 4	Pull-up wait power-good enable bit 3	Pull-up wait power-good enable bit 2	Pull-up wait power-good enable bit 1	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 148. DCR16 (0x10) LSB description

Bit	Name	Description
7	PU_WAIT_PG_ENA_4	1: At power-up step 4 waits for power-good signal 0: At power-up step 4 does not wait for a power-good signal
6	PU_WAIT_PG_ENA_3	1: At power-up step 3 waits for power-good signal 0: At power-up step 3 does not wait for a power-good signal
5	PU_WAIT_PG_ENA_2	1: At power-up step 2 waits for power-good signal 0: At power-up step 2 does not wait for a power-good signal
4	PU_WAIT_PG_ENA_1	1: At power-up step 1 waits for power-good signal 0: At power-up step 1 does not wait for a power-good signal

Bit	Name	Description
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 149. DCR17 (0x11) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_CRC0_7	U_NVM_CRC0_6	U_NVM_CRC0_5	U_NVM_CRC0_4
Reserved	Reserved	Reserved	Reserved	User NVM CRC 0 bit 7	User NVM CRC 0 bit 6	User NVM CRC 0 bit 5	User NVM CRC 0 bit 4

Table 150. DCR17 (0x11) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_CRC0_7	
18	U_NVM_CRC0_6	
17	U_NVM_CRC0_5	
16	U_NVM_CRC0_4	

Table 151. DCR17 (0x11)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_CRC0_3	U_NVM_CRC0_2	U_NVM_CRC0_1	U_NVM_CRC0_0	U_PROG0_1	U_PROG0_1	U_NVM_H_5	U_NVM_H_4
User NVM CRC 0 bit 3	User NVM CRC 0 bit 2	User NVM CRC 0 bit 1	User NVM CRC 0 bit 0	User program 0 bit 1	User program 0 bit 0	User NVM H register bit 5	User NVM H register bit 4

Table 152. DCR17 (0x11) description

Bit	Name	Description
15	U_NVM_CRC0_3	
14	U_NVM_CRC0_2	
13	U_NVM_CRC0_1	
12	U_NVM_CRC0_0	
11	U_PROG0_1	Not accessible by user but programmed by NVM controller during user programming
10	U_PROG0_0	Not accessible by user but programmed by NVM controller during user programming
9	U_NVM_H_5	
8	U_NVM_H_4	

Table 153. DCR17 (0x11) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
NFSO_STATE_IN_DEEP_SLEEP	U_NVM_H_2	U_NVM_H_1	BOOST_DIS	CRC3	CRC2	CRC1	CRC0
Set NFSO default state in DEEP-SLEEP bit	User NVM H register bit 2	User NVM H register bit 1	BOOST disable bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 154. DCR17 (0x11) LSB description

Bit	Name	Description
7	NFSO_STATE_IN_DEEP_SLEEP	1: NFSO pin is high when FSM is in DEEP-SLEEP state 0: NFSO pin is low when FSM is in DEEP-SLEEP state
6	U_NVM_H_2	
5	U_NVM_H_1	
4	BOOST_DIS	1: Disable boost 0: Boost is not disabled and depends on BOOST_OFF control bit
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 155. DCR18 (0x12) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	PD_WAIT_VREG_DEL_OFF_1	PD_WAIT_VREG_DEL_OFF_0	PD_WAIT_DEL_OFF_7_1	PD_WAIT_DEL_OFF_7_0
Reserved	Reserved	Reserved	Reserved	Pull-down wait VREG delay off bit 1	Pull-down wait VREG delay off bit 0	Pull-down wait delay off 7 bit 1	Pull-down wait delay off 7 bit 0

Table 156. DCR18 (0x12) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	PD_WAIT_VREG_DEL_OFF_1	Power-down delay for Vreg 00: 2 ms 01: 5 ms 10: 10 ms 11: 20 ms
18	PD_WAIT_VREG_DEL_OFF_0	
17	PD_WAIT_DEL_OFF_7_1	Power-down delay at step 7 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms

Bit	Name	Description
16	PD_WAIT_DEL_OFF_7_0	

Table 157. DCR18 (0x12)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
PD_WAIT_DEL_OFF_6_1	PD_WAIT_DEL_OFF_6_0	PD_WAIT_DEL_OFF_5_1	PD_WAIT_DEL_OFF_5_0	PD_WAIT_DEL_OFF_4_1	PD_WAIT_DEL_OFF_4_0	PD_WAIT_DEL_OFF_3_1	PD_WAIT_DEL_OFF_3_0
Pull-down wait delay off 6 bit 1	Pull-down wait delay off 6 bit 0	Pull-down wait delay off 5 bit 1	Pull-down wait delay off 5 bit 0	Pull-down wait delay off 4 bit 1	Pull-down wait delay off 4 bit 0	Pull-down wait delay off 3 bit 1	Pull-down wait delay off 3 bit 0

Table 158. DCR18 (0x12) description

Bit	Name	Description
15	PD_WAIT_DEL_OFF_6_1	Power-down delay at step 6 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
14	PD_WAIT_DEL_OFF_6_0	
13	PD_WAIT_DEL_OFF_5_1	Power-down delay at step 5 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
12	PD_WAIT_DEL_OFF_5_0	
11	PD_WAIT_DEL_OFF_4_1	Power-down delay at step 4 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
10	PD_WAIT_DEL_OFF_4_0	
9	PD_WAIT_DEL_OFF_3_1	Power-down delay at step 3 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
8	PD_WAIT_DEL_OFF_3_0	

Table 159. DCR18 (0x12) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
PD_WAIT_DEL_OFF_2_1	PD_WAIT_DEL_OFF_2_0	PD_WAIT_DEL_OFF_1_1	PD_WAIT_DEL_OFF_1_0	CRC3	CRC2	CRC1	CRC0
Pull-down wait delay off 2 bit 1	Pull-down wait delay off 2 bit 0	Pull-down wait delay off 1 bit 1	Pull-down wait delay off 1 bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 160. DCR18 (0x12) LSB description

Bit	Name	Description
7	PD_WAIT_DEL_OFF_2_1	Power-down delay at step 2 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
6	PD_WAIT_DEL_OFF_2_0	
5	PD_WAIT_DEL_OFF_1_1	Power-down delay at step 1 00: 0 ms 01: 2 ms 10: 5 ms 11: 10 ms
4	PD_WAIT_DEL_OFF_1_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 161. DCR19 (0x13) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_RELEASE_15	U_NVM_RELEASE_14	U_NVM_RELEASE_13	U_NVM_RELEASE_12
Reserved	Reserved	Reserved	Reserved	User NVM release bit 15	User NVM release bit 14	User NVM release bit 13	User NVM release bit 12

Table 162. DCR19 (0x13) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_RELEASE_15	User NVM regs Can be emulated when FSM in U_PROG_1 state (available for customer to identify the user NVM release)
18	U_NVM_RELEASE_14	
17	U_NVM_RELEASE_13	
16	U_NVM_RELEASE_12	

Table 163. DCR19 (0x13)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_RELEASE_11	U_NVM_RELEASE_10	U_NVM_RELEASE_9	U_NVM_RELEASE_8	U_NVM_RELEASE_7	U_NVM_RELEASE_6	U_NVM_RELEASE_5	U_NVM_RELEASE_4
User NVM release bit 11	User NVM release bit 10	User NVM release bit 9	User NVM release bit 8	User NVM release bit 7	User NVM release bit 6	User NVM release bit 5	User NVM release bit 4

Table 164. DCR19 (0x13) description

Bit	Name	Description
15	U_NVM_RELEASE_11	
14	U_NVM_RELEASE_10	
13	U_NVM_RELEASE_9	
12	U_NVM_RELEASE_8	
11	U_NVM_RELEASE_7	
10	U_NVM_RELEASE_6	
9	U_NVM_RELEASE_5	
8	U_NVM_RELEASE_4	

Table 165. DCR19 (0x13) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_RELEASE_3	U_NVM_RELEASE_2	U_NVM_RELEASE_1	U_NVM_RELEASE_0	CRC3	CRC2	CRC1	CRC0
User NVM release bit 3	User NVM release bit 2	User NVM release bit 1	User NVM release bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 166. DCR19 (0x13) LSB description

Bit	Name	Description
7	U_NVM_RELEASE_3	
6	U_NVM_RELEASE_2	
5	U_NVM_RELEASE_1	
4	U_NVM_RELEASE_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 167. DCR20 (0x14) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_K_15	U_NVM_K_14	U_NVM_K_13	U_NVM_K_12
Reserved	Reserved	Reserved	Reserved	User NVM K register bit 15	User NVM K register bit 14	User NVM K register bit 13	User NVM K register bit 12

Table 168. DCR20 (0x14) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_K_15	User NVM regs

Bit	Name	Description
		Can be emulated when FSM is in U_PROG_1 state
18	U_NVM_K_14	
17	U_NVM_K_13	
16	U_NVM_K_12	

Table 169. DCR20 (0x14)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_K_11	U_NVM_K_10	U_NVM_K_9	U_NVM_K_8	U_NVM_K_7	U_NVM_K_6	U_NVM_K_5	U_NVM_K_4
User NVM K register bit 11	User NVM K register bit 10	User NVM K register bit 9	User NVM K register bit 8	User NVM K register bit 7	User NVM K register bit 6	User NVM K register bit 5	User NVM K register bit 4

Table 170. DCR20 (0x14) description

Bit	Name	Description
15	U_NVM_K_11	
14	U_NVM_K_10	
13	U_NVM_K_9	
12	U_NVM_K_8	
11	U_NVM_K_7	
10	U_NVM_K_6	
9	U_NVM_K_5	
8	U_NVM_K_4	

Table 171. DCR20 (0x14) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
LOW_SET_3	LOW_SET_2	LOW_SET_1	LOW_SET_0	CRC3	CRC2	CRC1	CRC0
LOW set bit 3	LOW set bit 2	LOW set bit 1	LOW set bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 172. DCR20 (0x14) LSB description

Bit	Name	Description
7	LOW_SET_3	Long open window duration 0000: 319 ms max 0001: 479 ms max 0010: 638 ms max 0011: 1025 ms max 0100: 115 ms max 0101: 159 ms max 0110: 230 ms max 0111: 460 ms max 1000-1011: 2300 ms max

Bit	Name	Description
		1100: 4600 ms max 1101: 6900 ms max 1110: 9200 ms max 1111: Infinite
6	LOW_SET_2	
5	LOW_SET_1	
4	LOW_SET_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 173. DCR21 (0x15) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_L_15	U_NVM_L_14	U_NVM_L_13	U_NVM_L_12
Reserved	Reserved	Reserved	Reserved	User NVM L register bit 15	User NVM L register bit 14	User NVM L register bit 13	User NVM L register bit 12

Table 174. DCR21 (0x15) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_L_15	User NVM regs Can be emulated when FSM in U_PROG_1 state
18	U_NVM_L_14	
17	U_NVM_L_13	
16	U_NVM_L_12	

Table 175. DCR21 (0x15)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_L_11	U_NVM_L_10	U_NVM_L_9	U_NVM_L_8	U_NVM_L_7	U_NVM_L_6	U_NVM_L_5	U_NVM_L_4
User NVM L register bit 11	User NVM L register bit 10	User NVM L register bit 9	User NVM L register bit 8	User NVM L register bit 7	User NVM L register bit 6	User NVM L register bit 5	User NVM L register bit 4

Table 176. DCR21 (0x15) description

Bit	Name	Description
15	U_NVM_L_11	
14	U_NVM_L_10	

Bit	Name	Description
13	U_NVM_L_9	
12	U_NVM_L_8	
11	U_NVM_L_7	
10	U_NVM_L_6	
9	U_NVM_L_5	
8	U_NVM_L_4	

Table 177. DCR21 (0x15) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_L_3	U_NVM_L_2	U_NVM_L_1	U_NVM_L_0	CRC3	CRC2	CRC1	CRC0
User NVM L register bit 3	User NVM L register bit 2	User NVM L register bit 1	User NVM L register bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 178. DCR21 (0x15) LSB description

Bit	Name	Description
7	U_NVM_L_3	
6	U_NVM_L_2	
5	U_NVM_L_1	
4	U_NVM_L_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 179. DCR22 (0x16) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_M_15	U_NVM_M_14	U_NVM_M_13	U_NVM_M_12
Reserved	Reserved	Reserved	Reserved	User NVM M register bit 15	User NVM M register bit 14	User NVM M register bit 13	User NVM M register bit 12

Table 180. DCR22 (0x16) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_M_15	User NVM regs Can be emulated when FSM is in U_PROG_1 state

Bit	Name	Description
18	U_NVM_M_14	
17	U_NVM_M_13	
16	U_NVM_M_12	

Table 181. DCR22 (0x16)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_M_11	U_NVM_M_10	U_NVM_M_9	U_NVM_M_8	U_NVM_M_7	U_NVM_M_6	U_NVM_M_5	U_NVM_M_4
User NVM M register bit 11	User NVM M register bit 10	User NVM M register bit 9	User NVM M register bit 8	User NVM M register bit 7	User NVM M register bit 6	User NVM M register bit 5	User NVM M register bit 4

Table 182. DCR22 (0x16) description

Bit	Name	Description
15	U_NVM_M_11	
14	U_NVM_M_10	
13	U_NVM_M_9	
12	U_NVM_M_8	
11	U_NVM_M_7	
10	U_NVM_M_6	
9	U_NVM_M_5	
8	U_NVM_M_4	

Table 183. DCR22 (0x16) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_M_3	U_NVM_M_2	U_NVM_M_1	U_NVM_M_0	CRC3	CRC2	CRC1	CRC0
User NVM M register bit 3	User NVM M register bit 2	User NVM M register bit 1	User NVM M register bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 184. DCR22 (0x16) LSB description

Bit	Name	Description
7	U_NVM_M_3	
6	U_NVM_M_2	
5	U_NVM_M_1	
4	U_NVM_M_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 185. **DCR23 (0x17) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_N_15	U_NVM_N_14	U_NVM_N_13	U_NVM_N_12
Reserved	Reserved	Reserved	Reserved	User NVM N register bit 15	User NVM N register bit 14	User NVM N register bit 13	User NVM N register bit 12

Table 186. **DCR23 (0x17) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_N_15	User NVM regs Can be emulated when FSM is in U_PROG_1 state
18	U_NVM_N_14	
17	U_NVM_N_13	
16	U_NVM_N_12	

Table 187. **DCR23 (0x17)**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_N_11	U_NVM_N_10	U_NVM_N_9	U_NVM_N_8	U_NVM_N_7	U_NVM_N_6	U_NVM_N_5	U_NVM_N_4
User NVM N register bit 11	User NVM N register bit 10	User NVM N register bit 9	User NVM N register bit 8	User NVM N register bit 7	User NVM N register bit 6	User NVM N register bit 5	User NVM N register bit 4

Table 188. **DCR23 (0x17) description**

Bit	Name	Description
15	U_NVM_N_11	
14	U_NVM_N_10	
13	U_NVM_N_9	
12	U_NVM_N_8	
11	U_NVM_N_7	
10	U_NVM_N_6	
9	U_NVM_N_5	
8	U_NVM_N_4	

Table 189. **DCR23 (0x17) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_N_3	U_NVM_N_2	U_NVM_N_1	U_NVM_N_0	CRC3	CRC2	CRC1	CRC0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
User NVM N register bit 3	User NVM N register bit 2	User NVM N register bit 1	User NVM N register bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 190. DCR23 (0x17) LSB

Bit	Name	Description
7	U_NVM_N_3	
6	U_NVM_N_2	
5	U_NVM_N_1	
4	U_NVM_N_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 191. DCR24 (0x18) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_O_15	U_NVM_O_14	U_NVM_O_13	U_NVM_O_12
Reserved	Reserved	Reserved	Reserved	User NVM O register bit 15	User NVM O register bit 14	User NVM O register bit 13	User NVM O register bit 12

Table 192. DCR24 (0x18) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	U_NVM_O_15	User NVM regs Can be emulated when FSM is in U_PROG_1 state
18	U_NVM_O_14	
17	U_NVM_O_13	
16	U_NVM_O_12	

Table 193. DCR24 (0x18)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_O_11	U_NVM_O_10	U_NVM_O_9	U_NVM_O_8	U_NVM_O_7	U_NVM_O_6	U_NVM_O_5	U_NVM_O_4
User NVM O register bit 11	User NVM O register bit 10	User NVM O register bit 9	User NVM O register bit 8	User NVM O register bit 7	User NVM O register bit 6	User NVM O register bit 5	User NVM O register bit 4

Table 194. **DCR24 (0x18) description**

Bit	Name	Description
15	U_NVM_O_11	
14	U_NVM_O_10	
13	U_NVM_O_9	
12	U_NVM_O_8	
11	U_NVM_O_7	
10	U_NVM_O_6	
9	U_NVM_O_5	
8	U_NVM_O_4	

Table 195. **DCR24 (0x18) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_O_3	U_NVM_O_2	U_NVM_O_1	U_NVM_O_0	CRC3	CRC2	CRC1	CRC0
User NVM O register bit 3	User NVM O register bit 2	User NVM O register bit 1	User NVM O register bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 196. **DCR24 (0x18) LSB description**

Bit	Name	Description
7	U_NVM_O_3	
6	U_NVM_O_2	
5	U_NVM_O_1	
4	U_NVM_O_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 197. **DCR25 (0x19) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)
RES	RES	RES	RES	U_NVM_CRC1_7	U_NVM_CRC1_6	U_NVM_CRC1_5	U_NVM_CRC1_4
Reserved	Reserved	Reserved	Reserved	User NVM CRC1 bit 7	User NVM CRC1 bit 6	User NVM CRC1 bit 5	User NVM CRC1 bit 4

Table 198. **DCR25 (0x19) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved

Bit	Name	Description
20	RES	Reserved
19	U_NVM_CRC1_7	User NVM regs Can be emulated when FSM is in U_PROG_1 state
18	U_NVM_CRC1_6	
17	U_NVM_CRC1_5	
16	U_NVM_CRC1_4	

Table 199. DCR25 (0x19)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_CRC1_3	U_NVM_CRC1_2	U_NVM_CRC1_1	U_NVM_CRC1_0	U_PROG1_1	U_PROG1_0	U_NVM_P_5	U_NVM_P_4
User NVM CRC1 bit 3	User NVM CRC1 bit 2	User NVM CRC1 bit 1	User NVM CRC1 bit 0	User program 1 bit 1	User program 1 bit 0	User NVM P register bit 5	User NVM P register bit 4

Table 200. DCR25 (0x19)

Bit	Name	Description
15	U_NVM_CRC1_3	
14	U_NVM_CRC1_2	
13	U_NVM_CRC1_1	
12	U_NVM_CRC1_0	
11	U_PROG1_1	Not accessible by user but programmed by NVM controller during user programming
10	U_PROG1_0	Not accessible by user but programmed by NVM controller during user programming
9	U_NVM_P_5	
8	U_NVM_P_4	

Table 201. DCR25 (0x19) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)	- (R)
U_NVM_P_3	U_NVM_P_2	U_NVM_P_1	U_NVM_P_0	CRC3	CRC2	CRC1	CRC0
User NVM P register bit 3	User NVM P register bit 2	User NVM P register bit 1	User NVM P register bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 202. DCR25 (0x19) LSB description

Bit	Name	Description
7	U_NVM_P_3	
6	U_NVM_P_2	
5	U_NVM_P_1	
4	U_NVM_P_0	
3	CRC 3	
2	CRC 2	

Bit	Name	Description
1	CRC 1	
0	CRC 0	

Table 203. DCR28 (0x1C) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 204. DCR28 (0x1C) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 205. DCR28 (0x1C)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 206. DCR28 (0x1C) description

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	RES	Reserved
12	RES	Reserved
11	RES	Reserved
10	RES	Reserved
9	RES	Reserved
8	RES	Reserved

Table 207. DCR28 (0x1C) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
- (R0)	- (R0)	- (R0)	- (R0)	- (R)	- (R)	- (R)	- (R)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RES	RES	RES	RES	CRC3	CRC2	CRC1	CRC0
Reserved	Reserved	Reserved	Reserved	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 208. DCR28 (0x1C) LSB description

Bit	Name	Description
7	RES	Reserved
6	RES	Reserved
5	RES	Reserved
4	RES	Reserved
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

9.7 Status registers

Table 209. **DSR1 (0x21) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
RES	RES	FORCED_SLEEP_WDFAIL	BUCK3_OC	BUCK3_OV	BUCK3_UV	BUCK3_PG_TIMEOUT	BUCK2_OC
Reserved	Reserved	Device enters in DEEP-SLEEP state after 15 WD fail bit	BUCK3 overcurrent bit	BUCK3 overvoltage bit	BUCK3 undervoltage bit	BUCK3 power-good timeout bit	BUCK2 overcurrent bit

Table 210. **DSR1 (0x21) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	FORCED_SLEEP_WDFAIL	1: state machine reaches DEEP-SLEEP after 15 watchdog fails 0: No transition to DEEP-SLEEP due to 15 consecutive watchdog fails
20	BUCK3_OC	1: BUCK3 overcurrent detected 0: No error
19	BUCK3_OV	1: BUCK3 overvoltage detected 0: No error
18	BUCK3_UV	1: BUCK3 undervoltage detected 0: No error
17	BUCK3_PG_TIMEOUT	BUCK3 power-good time out during power-up sequence 1: Indicates that the power-good is not reached at the end of timeout Bit is latched until a “read and clear” command
16	BUCK2_OC	1: BUCK2 overcurrent detected 0: No error

Table 211. **DSR1 (0x21)**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
BUCK2_OV	BUCK2_UV	BUCK2_PG_TIMEOUT	BUCK1_OC	BUCK1_OV	BUCK1_UV	BUCK1_PG_TIMEOUT	LDO2_PG_TIMEOUT
BUCK2 overvoltage bit	BUCK2 undervoltage bit	BUCK2 power-good timeout bit	BUCK1 overcurrent bit	BUCK1 overvoltage bit	BUCK1 undervoltage bit	BUCK1 power-good timeout bit	LDO2 power-good timeout bit

Table 212. **DSR1 (0x21) description**

Bit	Name	Description
15	BUCK2_OV	1: BUCK2 overvoltage detected 0: No error
14	BUCK2_UV	1: BUCK2 undervoltage detected 0: No error
13	BUCK2_PG_TIMEOUT	BUCK2 power-good time out during power-up sequence 1: Indicates that the power-good is not reached at the end of timeout Bit is latched until a “read and clear” command
12	BUCK1_OC	1: BUCK1 overcurrent detected

Bit	Name	Description
		0: No error
11	BUCK1_OV	1: BUCK1 overvoltage detected 0: No error
10	BUCK1_UV	1: BUCK1 undervoltage detected 0: No error
9	BUCK1_PG_TIMEOUT	BUCK1 power-good time out during power-up sequence 1: Indicates that the power-good is not reached at the end of timeout Bit is latched until a “read and clear” command
8	LDO2_PG_TIMEOUT	1: PG timeout occurs following a SPI request to tun on LDO2

Table 213. DSR1 (0x21) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
LDO2_UV	LDO2_OV	LDO1_PG_TIMEOUT	LDO1_UV	CRC3	CRC2	CRC1	CRC0
LDO2 undervoltage bit	LDO2 overvoltage bit	LDO1 power-good timeout bit	LDO1 undervoltage bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 214. DSR1 (0x21) LSB description

Bit	Name	Description
7	LDO2_UV	Indicates undervoltage condition at voltage regulator LDO2 (LDO2 < VRTx) 1: Undervoltage Bit is latched until a “read and clear” command
6	LDO2_OV	Indicates overvoltage condition at voltage regulator LDO2 1: Overvoltage Bit is latched until a “read and clear” command
5	LDO1_PG_TIMEOUT	1: PG timeout occurs following a SPI request to tun on LDO1
4	LDO1_UV	Indicates undervoltage condition at voltage regulator LDO1 (LDO1 < VRTx) 1: Undervoltage Bit is latched until a “read and clear” command
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 215. DSR2 (0x22) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
RES	OUTHS_OL	OUTHS_OC	BOOST_IN_LP	BYPASS_VDSMON_ERROR	BOOST_VDSMON_ERROR	FBB_OV	FBB_UV
Reserved	OUTHS open load bit	OUTHS overcurrent bit	BOOST in Low power mode bit	Bypass VDSMON error bit	BOOST VDSMON error bit	FBB overvoltage bit	FBB undervoltage bit

Table 216. DSR2 (0x22) MSB description

Bit	Name	Description
23	RES	Reserved
22	OUTHS_OL	Open-load 1: Indicates an open-load condition was detected at OUTHS output Bit is latched until a “read and clear” command
21	OUTHS_OC	Overcurrent 1: Indicates an overcurrent condition was detected at OUTHS output Bit is latched until a “read and clear” command
20	BOOST_IN_LP	Boost switched on in low power mode 1: Occurred
19	BYPASS_VDSMON_ERROR	BYPASS V_{ds} monitoring error 1: Error is detected 0: No error reported
18	BOOST_VDSMON_ERROR	BOOST V_{ds} monitoring error 1: Error is detected 0: No error reported
17	FBB_OV	FBB overvoltage 1: Indicates the voltage at FBB increased above the FBB overvoltage threshold In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ Bit is latched until a “read and clear” command
16	FBB_UV	FBB under voltage 1: Indicates the voltage at FBB decreased below the FBB undervoltage threshold In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ Bit is latched until a “read and clear” command

Table 217. DSR2 (0x22)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
IRQ_ECHO_ERROR	FCCU_ENA_ECHO_ERROR	NFSO1_ECHO_ERROR	WD_ENA_ECHO_ERROR	NRST_ECHO_ERROR	VIO_UV	TSD_CL4	TSD_CL3
Interrupt echo error bit	FCCU enable echo error bit	NFSO1 echo error bit	Watchdog enable echo error bit	NRESET echo error bit	VIO undervoltage bit	Thermal shutdown of cluster 4 bit	Thermal shutdown of cluster 3 bit

Table 218. DSR2 (0x22) description

Bit	Name	Description
15	IRQ_ECHO_ERROR	IRQ asserted but still high 1: Still high when asserted low
14	FCCU_ENA_ECHO_ERROR	1: The FCCU_ENA echo monitor reported an error 0: No error reported
13	NFSO1_ECHO_ERROR	1: The NFSO1 echo monitor reported an error 0: No error reported
12	WD_ENA_ECHO_ERROR	1: The WD_ENA echo monitor reported an error 0: No error reported
11	NRST_ECHO_ERROR	1: NRESET input high while NRESET output (expected) low after filter 0: No error

Bit	Name	Description
10	VIO_UV	V_{IO} under voltage 1: Indicates the voltage at VIO has reached the undervoltage threshold Bit is latched until a “read and clear” command
9	TSD_CL4	Thermal shutdown of cluster x 1: Indicates cluster x has reached the thermal shutdown threshold (TSD) and the output cluster was shut down Bit is latched until a “read and clear” command
8	TSD_CL3	

Table 219. DSR2 (0x22) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
TSD_CL2	TSD_CL1	TSD_CL0	TSD	CRC3	CRC2	CRC1	CRC0
Thermal shutdown of cluster 2 bit	Thermal shutdown of cluster 1 bit	Thermal shutdown of cluster 0 bit	Thermal shutdown bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 220. DSR2 (0x22) LSB description

Bit	Name	Description
7	TSD_CL2	
6	TSD_CL1	
5	TSD_CL0	Central thermal shutdown
4	TSD	Thermal shutdown was reached (Logical or combination of all TSD_CLx, see status register DSR6) This bit cannot be cleared directly. It is reset if the corresponding TSD_CLx bits in SR6 are cleared
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 221. DSR3 (0x23) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
RES	LBIST_STOPPED	BUCK3_INT_FAIL	BUCK2_INT_FAIL	BUCK1_INT_FAIL	LBIST_ERROR_1	LBIST_ERROR_0	ABIST_ERROR
Reserved	LBIST stopped bit	BUCK3 interrupt fail bit	BUCK2 interrupt fail bit	BUCK31 interrupt fail bit	Logic BIST error bit 1	Logic BIST error bit 0	Analog bist error bit

Table 222. DSR3 (0x23) MSB description

Bit	Name	Description
23	RES	Reserved
22	LBIST_STOPPED	1: Indicates that LBIST has been stopped due to fault events
21	BUCK3_INT_FAIL	BUCK3 internal fail that may be caused by LDO_BUCK3_OV or LDO_Buck3_UV 1: Indicates that an internal occurs on BUCK3 Bit is latched until a “read and clear” command
20	BUCK2_INT_FAIL	BUCK2 internal fail that may be caused by LDO_BUCK2_OV or LDO_BUCK2_UV

Bit	Name	Description
		1: Indicates that an internal occurs on BUCK2 Bit is latched until a “read and clear” command
19	BUCK1_INT_FAIL	BUCK1 internal fail that may be caused by LDO_BUCK1_OV or LDO_BUCK1_UV 1: Indicates that an internal occurs on buck1 Bit is latched until a “read and clear” command
18	LBIST_ERROR_1	1: The logic BIST2 reported an error
17	LBIST_ERROR_0	1: The logic BIST1 reported an error
16	ABIST_ERROR	1: The analog BIST reported an error

Table 223. DSR3 (0x23)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
CURRENT_MISMATCH	FORCED_SLEEP_TSD	FCCUFAIL	WDFAIL	INT_REG_UV	INT_REG_OV	NVM_COMP_ERROR	NVM_CRC_ERROR
Current mismatch bit	Forced sleep after TSD event bit	FCCU fail bit	Watchdog fail bit	Interrupt regulator undervoltage bit	Interrupt regulator overvoltage bit	NVM compare error bit	NVM CRC error bit

Table 224. DSR3 (0x23) description

Bit	Name	Description
15	CURRENT_MISMATCH	1: A current mismatch occurs between main and monitoring currents
14	FORCED_SLEEP_TSD	1: state machine reaches DEEP-SLEEP after 3 TSD events
13	FCCUFAIL	FCCU fault detection 1: A fault has been detected by the FCCU monitor bit is latched until a "Read and clear" command
12	WDFAIL	A WD trig fail event occurred Bit is latched until a "Read and clear" command Note that after 15 consecutive WD trig faults the device reach DEEP-SLEEP state where WDFAIL_CNT is cleared, while WDFAIL bit is kept at 1
11	INT_REG_UV	Internal regulator undervoltage 1: Indicates an internal regulator under voltage occurs on 3V3 This bit is latched until a “read and clear” command
10	INT_REG_OV	Internal regulator overvoltage 1: Indicates an internal regulator over voltage occurs on 3V3 This bit is latched until a “read and clear” command
9	NVM_COMP_ERROR	Indicates an error between NVM and mirror register
8	NVM_CRC_ERROR	Indicates a NVM CRC error at NVM download

Table 225. DSR3 (0x33) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
GNDLOSS	OSC_ERROR	SPI_REG_COMP_ERROR	FSM_COMP_ERROR	CRC3	CRC2	CRC1	CRC0
Ground Loss detection bit	Oscillators error bit	SPI registers compare error bit	Finite state machine compares error bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 226. DSR3 (0x33) LSB description

Bit	Name	Description
7	GNDLOSS	1: Digital or analog central ground loss detected 0: No error
6	OSC_ERROR	1: The oscillator monitor reported an error 0: No error reported
5	SPI_REG_COMP_ERROR	1: The SPI safety registers monitor reported an error 0: No error reported
4	FSM_COMP_ERROR	1: The Main finite state machine monitor reported an error 0: No error reported
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 227. DSR4 (0x24) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
RES	SPI_ALL_WAKEUP_DISABLE	SPI_CLK_CNT	SPI_CSN_TIMEOUT	SPI_CRC_ERR	SPI_SDI_STUCK_HIGH	SPI_SDI_STUCK_LOW	SPI_UNDEF_ADD
Reserved	SPI all wake up disable bit	SPI clock counter bit	SPI CSN timeout bit	SPI CRC error bit	SPI SDI Stuck high bit	SPI SDI Stuck Low bit	SPI undefined address bit

Table 228. DSR4 (0x24) MSB description

Bit	Name	Description
23	RES	Reserved
22	SPI_ALL_WAKEUP_DISABLE	SPI tentative occurs to disable all wake up sources. This tentative for last wake up disable has not been performed
21	SPI_CLK_CNT	SPI clock counter 1: Indicates an SPI frame with the wrong number of CLK cycles was detected bit is latched until a valid SPI frame
20	SPI_CSN_TIMEOUT	1: SPI CSN time-out error detected
19	SPI_CRC_ERR	1: SPI CRC error detected
18	SPI_SDI_STUCK_HIGH	1: SPI SDI stuck at high level
17	SPI_SDI_STUCK_LOW	1: SPI SDI stuck at low level
16	SPI_UNDEF_ADD	1: SPI access to undefined address

Table 229. DSR4 (0x24)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
SPI_STATUS_WRT	SPI_LBISTED	FBB_OV_EW	FBB_UV_EW	VS_UV_EW	RES	TW_CL4	TW_CL3
SPI status write bit	SPI LBIST test bit	FBB overvoltage early warning bit	FBB undervoltage early warning bit	VS undervoltage early warning bit	Reserved bit	Thermal warning of cluster 4 bit	Thermal warning of cluster 3 bit

Table 230. DSR4 (0x24) description

Bit	Name	Description
15	SPI_STATUS_WRT	1: SPI writes access to status register
14	SPI_LBISTED	1: SPI access while SPI is under LBIST test
13	FBB_OV_EW	FBB over voltage early warning 1: Indicates the voltage at FBB increased above the FBB over voltage early warning threshold (configured in CR3) In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ. Bit is latched until a “read and clear” command
12	FBB_UV_EW	FBB under voltage early warning 1: Indicates the voltage at FBB decreased below the FBB under voltage early warning threshold (configured in CR3) In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ Bit is latched until a “read and clear” command
11	VS_UV_EW	V_S early warning 1: Indicates the voltage at V_S decreased below the V_S early warning threshold (configured in CR3) In ACTIVE and REC-1 modes, an interrupt pulse is generated at IRQ. Bit is latched until a “read and clear” command
10	RES	Reserved
9	TW_CL4	Thermal warning of cluster x 1: Indicates cluster x has reached the thermal warning threshold (TSW) Bit is latched until a “read and clear” command
8	TW_CL3	

Table 231. DSR4 (0x24) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
TW_CL2	TW_CL1	TW_CL0	TW	CRC3	CRC2	CRC1	CRC0
Thermal warning of cluster 2 bit	Thermal warning of cluster 1 bit	Central thermal warning bit	Thermal warning bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 232. DSR4 (0x24) LSB description

Bit	Name	Description
7	TW_CL2	
6	TW_CL1	
5	TW_CL0	Central thermal warning
4	TW	Thermal warning 1: Indicates the temperature has reached the thermal warning threshold (logical OR combination of bits TW_CLx in DSR6)
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 233. DSR5 (0x25) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (RC1L)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)
RES	FP_READY	BOOST_LEVEL_SET	BOOST_ENA_STATUS	BYPASS_STATUS	BUCK3_PG_OK	BUCK2_PG_OK	BUCK1_PG_OK
Reserved	Full power Ready bit	BOOST Level set bit	BOOST enable status bit	Bypass status bit	BUCK3 power-good ok bit	BUCK2 power-good ok bit	BUCK1 power-good ok bit

Table 234. DSR5 (0x25) MSB description

Bit	Name	Description
23	RES	Reserved
22	FP_READY	1: Transition from Low power to full power occurred. IRQ generated when this occurs
21	BOOST_LEVEL_SET	1: 9.5 V 0: 8.0 V
20	BOOST_ENA_STATUS	1: Boost switching ON 0: Boost switching OFF Live bit
19	BYPASS_STATUS	1: Bypass ON 0: Bypass OFF Live bit
18	BUCK3_PG_OK	1: Power-good reached after the regulator has been turned ON by power-up sequence or through SPI 0: PG not reached
17	BUCK2_PG_OK	1: Power-good reached after the regulator has been turned ON by power-up sequence or through SPI 0: PG not reached
16	BUCK1_PG_OK	1: Power-good reached after the regulator has been turned ON by power-up sequence or through SPI 0: PG not reached

Table 235. DSR5 (0x25)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)
DEV_STATE_5	DEV_STATE_4	DEV_STATE_3	DEV_STATE_2	DEV_STATE_1	DEV_STATE_0	DEEP-SLEEP_FROM_DO_POWER_DOWN_1	DEEP-SLEEP_FROM_DO_POWER_DOWN_0
Device state bit 5	Device state bit 4	Device state bit 3	Device state bit 2	Device state bit 1	Device state bit 0	DEEP-SLEEP from power down bit 1	DEEP-SLEEP from power down bit 0

Table 236. DSR5 (0x25) description

Bit	Name	Description
15	DEV_STATE_5	
14	DEV_STATE_4	
13	DEV_STATE_3	
12	DEV_STATE_2	
11	DEV_STATE_1	
10	DEV_STATE_0	Current state of state machine 00000: INIT …

Bit	Name	Description
9	DEEP-SLEEP_FROM_DO_POWER_DOWN_1	00: Default 01: DEEP-SLEEP entered after a DO_POWER_DOWN command in ACTIVE state 1x: DEEP-SLEEP entered after a DO_POWER_DOWN command in REC-1 state
8	DEEP-SLEEP_FROM_DO_POWER_DOWN_0	

Table 237. DEV_STATE binary code for state machine states/modes

Digital FSM states	Spec states/modes	Binary
AA_START_UP	START-UP state	000000
ACTIVE_HP	ACTIVE FULL-POWER mode	000001
ACTIVE_LP	ACTIVE LOW-POWER mode	000010
ACTIVE_LP2HP1	LP2FP transition	000011
ACTIVE_LP2HP2		000100
ACTIVE_LP2HP3		000101
ACTIVE_LP2HP4		000110
ANA_TRIM	Not usable	000111
DEEPSLEEP_INIT1	DEEP-SLEEP state	001000
DEEPSLEEP_INIT2		001001
DEEPSLEEP_INIT3		001010
DEEPSLEEP_INIT4		001011
DEEPSLEEP_TO_START_SM		001100
DEEP_SLEEP		001101
INIT1	INIT state	001110
INIT2		001111
POWER_DOWN_FROM_PG_TIMEOUT	POWER-DOWN sequence	010001
POWER_DOWN_TO_DEEP_SLEEP		010010
POWER_DOWN_TO_REC_2		010011
NRESET_PULSE	POWER-UP sequence	010000
POWER_UP_FROM_FAIL		010100
POWER_UP_FROM_INIT		010101
PROD_TEST_MODE	Not usable	010110
READ_NVM_DL	U-NVM-DL state	010111
REC_1	REC-1 state	011000
REC_2	REC-2 state	011001
RESET_SPI_REG	START-SM state	011010
RISE_REF		011011
START_SM		011100
SWDBG	SWDBG	011101
SWDBG_SET		011110
USER_NVM_PROG_1	U-NVM-PROG-1	011111
USER_NVM_PROG_2	U-NVM-PROG-2	100000

Digital FSM states	Spec states/modes	Binary
USER_NVM_PROG_2_COMPLETE	U-NVM-PROG-2	100001
USER_NVM_PROG_3		100010
USER_NVM_PROG_3_COMPLETE		100011
USER_NVM_PROG_4		100100
USER_NVM_PROG_4_COMPLETE		100101

Table 238. DSR5 (0x25) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
FORCED_SLEEP_POWUP	FSM_TO_REC2	REC2_FROM_DO_POWER_CYCLE_1	REC2_FROM_DO_POWER_CYCLE_0	CRC3	CRC2	CRC1	CRC0
Forced sleep power up bit	Finite state machine to REC2 bit	REC2 from power cycle bit 1	REC2 from power cycle bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 239. DSR5 (0x25) LSB description

Bit	Name	Description
7	FORCED_SLEEP_POWUP	1: state machine reaches DEEP-SLEEP after 3 attend to power-up
6	FSM_TO_REC2	Functional state machine state before reaching REC2 1: REC1 Bit is latched until a “read and clear” command 0: ACTIVE
5	REC2_FROM_DO_POWER_CYCLE_1	00: Default 01: REC2 entered after a DO_POWER_CYCLE command in ACTIVE state 1x: REC2 entered after a DO_POWER_CYCLE command in REC-1 state
4	REC2_FROM_DO_POWER_CYCLE_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 240. DSR6 (0x26) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (RC1L)	0 (RC1L)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
RES	LP_READY	SWDBG_VIO	SWDBG_STATE	RES	RES	RES	RES
Reserved	Low power Ready bit	Software debug VIO bit	Software debug status	Reserved bit	Reserved bit	Reserved bit	Reserved bit

Table 241. DSR6 (0x26) MSB description

Bit	Name	Description
23	RES	Reserved
22	LP_READY	1: Transition from full power to low power occurred. IRQ generated and this bit set when this occurs if not masked by MASK_LP_READY_IRQ
21	SWDBG_VIO	SWDBG is linked to V_{IO} up to the end of the timeout following the power-up sequence. If not masked, IRQ is generated and the watchdog starts with L.O.W.
20	SWDBG_STATE	state of SWDBG input pin with VIO thresholds

Bit	Name	Description
		1: Input level is high The bit shows the current state of SWDBG and cannot be cleared (“live bit”) 0: Input level is low
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 242. DSR6 (0x26)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RC1L)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
RES	FIN1_STATE	IGN_STATE	WU_STATE	IGN_WAKE	WU_WAKE	RES	TIMER_WAKE
Reserved bit	FIN1 state bit	IGN state bit	Wake-up state bit	IGN wake up bit	Wake-up bit	Reserved bit	Timer wake up bit

Table 243. DSR6 (0x26) description

Bit	Name	Description
15	RES	Reserved
14	FIN1_STATE	state of FIN1 input 1: Input level is high The bit shows the current state of FIN1 and cannot be cleared (“live bit”) 0: Input level is low
13	IGN_STATE	state of IGN input 1: Input level is high The bit shows the momentary status of IGN and cannot be cleared (“live bit”) Note that the status is only valid if IGN is configured as wake-up input in configuration register (0x05). Otherwise this bit is read at its previous logic state 0: Input level is low
12	WU_STATE	state of WU input 1: Input level is high The bit shows the momentary status of WU and cannot be cleared (“live bit”) Note that the status is only valid if WU is configured as wake-up input in configuration register (0x05). Otherwise this bit is read at its previous logic state 0: Input level is low
11	IGN_WAKE	Wake-up by IGN: shows wake up source 1: Wake-up Bits are latched until a “read and clear” command
10	WU_WAKE	Wake-up by WU: shows wake up source 1: Wake-up Bits are latched until a “read and clear” command
9	RES	Reserved
8	TIMER_WAKE	Wake-up by timer: shows wake up source 1: Wake-up Bits are latched until a “read and clear” command

Table 244. DSR6 (0x26) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (RC1L)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
IRQ_ECHO	NRST_ECHO	IRQ_SENT	NFSO1_ECHO	CRC3	CRC2	CRC1	CRC0
Interrupt echo bit	NRST echo bit	Interrupt sent bit	NFSO1_echo bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 245. DSR6 (0x26) LSB description

Bit	Name	Description
7	IRQ_ECHO	Indicates current status of IRQ pin. 1: High It is a live bit
6	NRST_ECHO	Indicates current status of NRST pin. 1: High It is a live bit
5	IRQ_SENT	IRQ sent from IRQ_REQUEST rising 1: IRQ sent
4	NFSO1_ECHO	Indicates current status of NFSO1 pin. 1: High It is a live bit
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 246. DSR7 (0x27) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (RC1L)	0 (RC1L)	0 (R)	0 (RC1L)	0 (R)	0 (R)	0 (R)
RES	VPOR	LDO1_PG_OK	LDO2_ENA_STATUS	LDO2_PG_OK	FCCU_ENA_ECHO	WD_ENA_ECHO	WD_TIMER_STATE_1
Reserved	Vs power on reset bit	LDO1 power-good ok bit	LDO2 enable status bit	LDO2 power-good ok bit	FCCU enable echo bit	Watchdog enable echo bit	Watchdog timer state bit 1

Table 247. DSR7 (0x27) MSB description

Bit	Name	Description
23	RES	Reserved
22	VPOR	V_S power-on reset threshold (VPOR) reached bit is latched until a "Read and clear" command
21	LDO1_PG_OK	Indicates power-good LDO1 bit is latched until a “read and clear” command
20	LDO2_ENA_STATUS	LDO2 enable status bit. Live bit LDO2 is a tracker and when disabled by SPI or UV or OV, this bit indicates the enable status 1: Enabled 0: Disabled
19	LDO2_PG_OK	1: Power-good reached after the regulator has been turned ON by power-up sequence or through SPI 0: PG not reached

Bit	Name	Description
18	FCCU_ENA_ECHO	echo of FCCU enable signal at FCCU block input 1: Indicates that the FCCU is running Live bit 0: Indicates that FCCU block is disabled
17	WD_ENA_ECHO	echo of WD enable signal at WD block input 1: Indicates that the WD is running Live bit 0: Indicates that WD block is disabled It occurs in software debug or in test mode
16	WD_TIMER_STATE_1	Watchdog timer status 00: WD counter in too early window trig 01: WD counter in valid window trig 11: WD counter in too late window trig

Table 248. DSR7 (0x27)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)
WD_TIMER_STATE_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	TSD_CNT_FAIL_1	TSD_CNT_FAIL_0	POWUP_RETRY_CNT_1
Watchdog timer state bit 0	Watchdog fail count bit 3	Watchdog fail count bit 2	Watchdog fail count bit 1	Watchdog fail count bit 0	Thermal shutdown fail count bit 1	Thermal shutdown fail count bit 0	Power up retry count bit 1

Table 249. DSR7 (0x27) description

Bit	Name	Description
15	WD_TIMER_STATE_0	
14	WDFAIL_CNT_3	Indicates number of consecutive watchdog trig fault, from 1 to 15 Bits cannot be cleared, will be cleared with a valid watchdog trig during a long open window, or in DEEP-SLEEP
13	WDFAIL_CNT_2	
12	WDFAIL_CNT_1	
11	WDFAIL_CNT_0	
10	TSD_CNT_FAIL_1	Thermal shut down sequence retry counter
9	TSD_CNT_FAIL_0	
8	POWUP_RETRY_CNT_1	Power up sequence retry counter MCU must clear this counter in REC-1 or ACTIVE state

Table 250. DSR7 (0x27) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RC1L)	- (R0)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
POWUP_RETRY_CNT_0	RES	NVM_PROG_OK	NVM_PROG_DONE	CRC3	CRC2	CRC1	CRC0
Power up retry count bit 0	Reserved	NVM program ok bit	NVM program done bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 251. DSR7 (0x27) LSB description

Bit	Name	Description
7	POWUP_RETRY_CNT_0	
6	RES	
5	NVM_PROG_OK	U-NVM programming is completed without error
4	NVM_PROG_DONE	U-NVM programming is completed
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 252. DSR8 (0x28) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	FCCU_LAST_STABLE_12	FCCU_LAST_STABLE_11	FCCU_LAST_STABLE_10	FCCU_LAST_STABLE_9	FCCU_LAST_STABLE_8	FCCU_LAST_STABLE_7	FCCU_LAST_STABLE_6
Reserved	FCCU last stable bit 12	FCCU last stable bit 11	FCCU last stable bit 10	FCCU last stable bit 9	FCCU last stable bit 8	FCCU last stable bit 7	FCCU last stable bit 6

Table 253. DSR8 (0x28) MSB description

Bit	Name	Description
23	RES	Reserved
22	FCCU_LAST_STABLE_12	
21	FCCU_LAST_STABLE_11	
20	FCCU_LAST_STABLE_10	
19	FCCU_LAST_STABLE_9	
18	FCCU_LAST_STABLE_8	
17	FCCU_LAST_STABLE_7	
16	FCCU_LAST_STABLE_6	

Table 254. DSR8 (0x28)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
FCCU_LAST_STABLE_5	FCCU_LAST_STABLE_4	FCCU_LAST_STABLE_3	FCCU_LAST_STABLE_2	FCCU_LAST_STABLE_1	FCCU_LAST_STABLE_0	FORCED_SLEEP_REGFAIL	REG_FAIL_CNT_1
FCCU last stable bit 5	FCCU last stable bit 4	FCCU last stable bit 3	FCCU last stable bit 2	FCCU last stable bit 1	FCCU last stable bit 0	Forced sleep regulator fail bit	Regulator fail counter bit 1

Table 255. DSR8 (0x28) description

Bit	Name	Description
15	FCCU_LAST_STABLE_5	
14	FCCU_LAST_STABLE_4	
13	FCCU_LAST_STABLE_3	
12	FCCU_LAST_STABLE_2	
11	FCCU_LAST_STABLE_1	
10	FCCU_LAST_STABLE_0	FCCU monitor last stable value duration
9	FORCED_SLEEP_REGFAIL	1: When REG_FAIL_CNT = 3 then FSM transit from REC_2 to DEEP-SLEEP (similar to TSD_CNT_FAIL) and in DEEP-SLEEP

Bit	Name	Description
		0: No transition to DEEP-SLEEP due to REG_FAIL_CNT
8	REG_FAIL_CNT_1	

Table 256. DSR8 (0x28) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
REG_FAIL_CNT_0	ABIST_BOOST_IGNORED	LBIST_COMPLETE	ABIST_COMPLETE	CRC3	CRC2	CRC1	CRC0
Regulator fail counter bit 0	ABIST boost ignored bit			Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 257. DSR8 (0x28) LSB description

Bit	Name	Description
7	REG_FAIL_CNT_0	REG_FAIL_CNT is incremented when a reg_fail event occurs on any regulator having its REGFAIL_GO_REC = 1 (that is one counter for all regulators having REGFAIL_GO_REC = 1)
6	ABIST_BOOST_IGNORED	1: Boost PWM activity has been detected during the ABIST test. So the BOOST comparator has not been covered by ABIST not to signal a wrong ABIST error 0: Boost ABIST well run
5	LBIST_COMPLETE	Define logical BIST ending 1: LBIST is complete 0: LBIST not complete or not running
4	ABIST_COMPLETE	Define analog BIST ending 1: ABIST is complete 0: ABIST not complete or not running
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 258. DSR9 (0x29) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 259. DSR9 (0x29) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved

Bit	Name	Description
17	RES	Reserved
16	RES	Reserved

Table 260. DSR9 (0x29)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	TEMP_CL0_9	TEMP_CL0_8	TEMP_CL0_7	TEMP_CL0_6	TEMP_CL0_5	TEMP_CL0_4
Reserved	Reserved	Temperature central cluster bit 9	Temperature central cluster bit 8	Temperature central cluster bit 7	Temperature central cluster bit 6	Temperature central cluster bit 5	Temperature central cluster bit 4

Table 261. DSR9 (0x29) description

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	TEMP_CL0_9	Temperature cluster 0: Central cluster Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	TEMP_CL0_8	
11	TEMP_CL0_7	
10	TEMP_CL0_6	
9	TEMP_CL0_5	
8	TEMP_CL0_4	

Table 262. DSR9 (0x29) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
TEMP_CL0_3	TEMP_CL0_2	TEMP_CL0_1	TEMP_CL0_0	CRC3	CRC2	CRC1	CRC0
Temperature central cluster bit 3	Temperature central cluster bit 2	Temperature central cluster bit 1	Temperature central cluster bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 263. DSR9 (0x29) LSB description

Bit	Name	Description
7	TEMP_CL0_3	
6	TEMP_CL0_2	
5	TEMP_CL0_1	
4	TEMP_CL0_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	

Bit	Name	Description
0	CRC 0	

Table 264. DSR10 (0x2A) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 265. DSR10 (0x2A) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 266. DSR10 (0x2A)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	TEMP_CL1_9	TEMP_CL1_8	TEMP_CL1_7	TEMP_CL1_6	TEMP_CL1_5	TEMP_CL1_4
Reserved	Reserved	Temperature cluster 1 bit 9	Temperature cluster 1 bit 8	Temperature cluster 1 bit 7	Temperature cluster 1 bit 6	Temperature cluster 1 bit 5	Temperature cluster 1 bit 4

Table 267. DSR10 (0x2A) description

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	TEMP_CL1_9	Temperature cluster 1 Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	TEMP_CL1_8	
11	TEMP_CL1_7	
10	TEMP_CL1_6	
9	TEMP_CL1_5	
8	TEMP_CL1_4	

Table 268. **DSR10 (0x2A) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
TEMP_CL1_3	TEMP_CL1_2	TEMP_CL1_1	TEMP_CL1_0	CRC3	CRC2	CRC1	CRC0
Temperature cluster 1 bit 3	Temperature cluster 1 bit 2	Temperature cluster 1 bit 1	Temperature cluster 1 bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 269. **DSR10 (0x2A) LSB description**

Bit	Name	Description
7	TEMP_CL1_3	
6	TEMP_CL1_2	
5	TEMP_CL1_1	
4	TEMP_CL1_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 270. **DSR11 (0x2B) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 271. **DSR11 (0x2B) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 272. **DSR11 (0x2B)**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	TEMP_CL2_9	TEMP_CL2_8	TEMP_CL2_7	TEMP_CL2_6	TEMP_CL2_5	TEMP_CL2_4
Reserved	Reserved	Temperature cluster 2 bit 9	Temperature cluster 2 bit 8	Temperature cluster 2 bit 7	Temperature cluster 2 bit 6	Temperature cluster 2 bit 5	Temperature cluster 2 bit 4

Table 273. **DSR11 (0x2B) description**

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	TEMP_CL2_9	Temperature cluster 2 Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	TEMP_CL2_8	
11	TEMP_CL2_7	
10	TEMP_CL2_6	
9	TEMP_CL2_5	
8	TEMP_CL2_4	

Table 274. **DSR11 (0x2B) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
TEMP_CL2_3	TEMP_CL2_2	TEMP_CL2_1	TEMP_CL2_0	CRC3	CRC2	CRC1	CRC0
Temperature cluster 2 bit 3	Temperature cluster 2 bit 2	Temperature cluster 2 bit 1	Temperature cluster 2 bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 275. **DSR11 (0x2B) LSB description**

Bit	Name	Description
7	TEMP_CL2_3	
6	TEMP_CL2_2	
5	TEMP_CL2_1	
4	TEMP_CL2_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 276. **DSR12 (0x2C) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 277. **DSR12 (0x2C) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved

Bit	Name	Description
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 278. DSR12 (0x2C)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	TEMP_CL3_9	TEMP_CL3_8	TEMP_CL3_7	TEMP_CL3_6	TEMP_CL3_5	TEMP_CL3_4
Reserved	Reserved	Temperature cluster 3 bit 9	Temperature cluster 3 bit 8	Temperature cluster 3 bit 7	Temperature cluster 3 bit 6	Temperature cluster 3 bit 5	Temperature cluster 3 bit 4

Table 279. DSR12 (0x2C) description

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	TEMP_CL3_9	Temperature cluster 3 Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	TEMP_CL3_8	
11	TEMP_CL3_7	
10	TEMP_CL3_6	
9	TEMP_CL3_5	
8	TEMP_CL3_4	

Table 280. DSR12 (0x2C) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
TEMP_CL3_3	TEMP_CL3_2	TEMP_CL3_1	TEMP_CL3_0	CRC3	CRC2	CRC1	CRC0
Temperature cluster 3 bit 3	Temperature cluster 3 bit 2	Temperature cluster 3 bit 1	Temperature cluster 3 bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 281. DSR12 (0x2C) LSB description

Bit	Name	Description
7	TEMP_CL3_3	
6	TEMP_CL3_2	
5	TEMP_CL3_1	
4	TEMP_CL3_0	

Bit	Name	Description
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 282. DSR13 (0x2D) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 283. DSR13 (0x2D) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 284. DSR13 (0x2D)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	TEMP_CL4_9	TEMP_CL4_8	TEMP_CL4_7	TEMP_CL4_6	TEMP_CL4_5	TEMP_CL4_4
Reserved	Reserved	Temperature cluster 4 bit 9	Temperature cluster 4 bit 8	Temperature cluster 4 bit 7	Temperature cluster 4 bit 6	Temperature cluster 4 bit 5	Temperature cluster 4 bit 4

Table 285. DSR13 (0x2D) description

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	TEMP_CL4_9	Temperature cluster 4 Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	TEMP_CL4_8	
11	TEMP_CL4_7	
10	TEMP_CL4_6	
9	TEMP_CL4_5	
8	TEMP_CL4_4	

Table 286. **DSR13 (0x2D) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
TEMP_CL4_3	TEMP_CL4_2	TEMP_CL4_1	TEMP_CL4_0	CRC3	CRC2	CRC1	CRC0
Temperature cluster 4 bit 3	Temperature cluster 4 bit 2	Temperature cluster 4 bit 1	Temperature cluster 4 bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 287. **DSR13 (0x2D) LSB description**

Bit	Name	Description
7	TEMP_CL4_3	
6	TEMP_CL4_2	
5	TEMP_CL4_1	
4	TEMP_CL4_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 288. **DSR14 (0x2E) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 289. **DSR14 (0x2E) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 290. **DSR14 (0x2E)**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	VS_9	VS_8	VS_7	VS_6	VS_5	VS_4
Reserved	Reserved	VS voltage Level bit 9	VS voltage Level bit 8	VS voltage Level bit 7	VS voltage Level bit 6	VS voltage Level bit 5	VS voltage Level bit 4

Table 291. **DSR14 (0x2E)**

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	VS_9	Voltage level on V_S pin Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	VS_8	
11	VS_7	
10	VS_6	
9	VS_5	
8	VS_4	

Table 292. **DSR14 (0x2E) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
VS_3	VS_2	VS_1	VS_0	CRC3	CRC2	CRC1	CRC0
VS voltage Level bit 3	VS voltage Level bit 2	VS voltage Level bit 1	VS voltage Level bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 293. **DSR14 (0x2E) LSB description**

Bit	Name	Description
7	VS_3	
6	VS_2	
5	VS_1	
4	VS_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 294. **DSR15 (0x2F) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 295. **DSR15 (0x2F) MSB**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved

Bit	Name	Description
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 296. DSR15 (0x2F)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	WU_9	WU_8	WU_7	WU_6	WU_5	WU_4
Reserved	Reserved	Wake-up voltage level bit 9	Wake-up voltage level bit 8	Wake-up voltage level bit 7	Wake-up voltage level bit 6	Wake-up voltage level bit 5	Wake-up voltage level bit 4

Table 297. DSR15 (0x2F) description

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	WU_9	Voltage level on WU pin Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	WU_8	
11	WU_7	
10	WU_6	
9	WU_5	
8	WU_4	

Table 298. DSR15 (0x2F) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
WU_3	WU_2	WU_1	WU_0	CRC3	CRC2	CRC1	CRC0
Wake-up voltage level bit 3	Wake-up voltage level bit 2	Wake-up voltage level bit 1	Wake-up voltage level bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 299. DSR15 (0x2F) LSB description

Bit	Name	Description
7	WU_3	
6	WU_2	
5	WU_1	
4	WU_0	

Bit	Name	Description
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 300. DSR16 (0x30) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 301. DSR16 (0x30) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 302. DSR16 (0x30)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	IGN_9	IGN_8	IGN_7	IGN_6	IGN_5	IGN_4
Reserved	Reserved	IGN voltage level bit 9	IGN voltage level bit 8	IGN voltage level bit 7	IGN voltage level bit 6	IGN voltage level bit 5	IGN voltage level bit 4

Table 303. DSR16 (0x30) description

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	IGN_9	Voltage level on IGN pin Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	IGN_8	
11	IGN_7	
10	IGN_6	
9	IGN_5	
8	IGN_4	

Table 304. **DSR16 (0x30) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
IGN_3	IGN_2	IGN_1	IGN_0	CRC3	CRC2	CRC1	CRC0
IGN voltage level bit 3	IGN voltage level bit 2	IGN voltage level bit 1	IGN voltage level bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 305. **DSR16 (0x30) LSB description**

Bit	Name	Description
7	IGN_3	
6	IGN_2	
5	IGN_1	
4	IGN_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 306. **DSR17 (0x31) MSB**

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)	- (R0)
RES	RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 307. **DSR17 (0x31) MSB description**

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved
20	RES	Reserved
19	RES	Reserved
18	RES	Reserved
17	RES	Reserved
16	RES	Reserved

Table 308. **DSR17 (0x31)**

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	FBB_9	FBB_8	FBB_7	FBB_6	FBB_5	FBB_4
Reserved	Reserved	FBB voltage level bit 9	FBB voltage level bit 8	FBB voltage level bit 7	FBB voltage level bit 6	FBB voltage level bit 5	FBB voltage level bit 4

Table 309. DSR17 (0x31) description

Bit	Name	Description
15	RES	Reserved
14	RES	Reserved
13	FBB_9	Voltage level on FBB pin Bits cannot be cleared (a clear command generates a SPI_UNDEF_ADD flag)
12	FBB_8	
11	FBB_7	
10	FBB_6	
9	FBB_5	
8	FBB_4	

Table 310. DSR17 (0x31) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
FBB_3	FBB_2	FBB_1	FBB_0	CRC3	CRC2	CRC1	CRC0
FBB voltage Level bit 3	FBB voltage Level bit 2	FBB voltage Level bit 1	FBB voltage Level bit 0	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 311. DSR17 (0x31) LSB description

Bit	Name	Description
7	FBB_3	
6	FBB_2	
5	FBB_1	
4	FBB_0	
3	CRC 3	
2	CRC 2	
1	CRC 1	
0	CRC 0	

Table 312. DSR18 (0x32) MSB

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
- (R0)	- (R0)	- (R0)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
RES	RES	RES	BUCK2_FBLOSS	BUCK1_FBLOSS	NVM_COMPARE_ENA_STATUS	WD_TIME_STATUS_3	WD_TIME_STATUS_2
Reserved	Reserved	Reserved	BUCK2 feedback loss bit	BUCK1 feedback loss bit	NVM compare enable status bit	Watchdog time status bit 3	Watchdog time status bit 2

Table 313. DSR18 (0x32) MSB description

Bit	Name	Description
23	RES	Reserved
22	RES	Reserved
21	RES	Reserved

Bit	Name	Description
20	BUCK2_FBLOSS	1: BUCK2 FB pin detection 0: No error
19	BUCK1_FBLOSS	1: BUCK1 FB pin detection 0: No error
18	NVM_COMPARE_ENA_STATUS	1: Status bit from ST_NVM to NVM_COMPARE_DISABLE inverted bit for user read
17	WD_TIME_STATUS_3	Live bit
16	WD_TIME_STATUS_2	Live bit

Table 314. DSR18 (0x32)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
WD_TIME_STATUS_1	WD_TIME_STATUS_0	VBUCK3_ENA_STATUS	VBUCK2_ENA_STATUS	VBUCK1_ENA_STATUS	LDO1_ENA_STATUS	OUTHS_ENA_STATUS	LOW_STATUS
Watchdog time status bit 1	Watchdog time status bit 0	VBUCK3 enable status bit	VBUCK2 enable status bit	VBUCK1 enable status bit	LDO1 enable status bit	OUTHS enable status bit	LOW status bit

Table 315. DSR18 (0x32) description

Bit	Name	Description
15	WD_TIME_STATUS_1	Live bit
14	WD_TIME_STATUS_0	Live bit
13	VBUCK3_ENA_STATUS	Live bit
12	VBUCK2_ENA_STATUS	Live bit
11	VBUCK1_ENA_STATUS	Live bit
10	LDO1_ENA_STATUS	Live bit
9	OUTHS_ENA_STATUS	Live bit
8	LOW_STATUS	Live bit 1: Watchdog is counting in LOW. Current window is LOW_SET 0: Watchdog is not counting in LOW. Current window is WD_TIME_STATUS

Table 316. DSR18 (0x32) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (R)	0 (R)	0 (R)	0 (R)	0 (RC1L)	0 (RC1L)	0 (RC1L)	0 (RC1L)
BOOST_ENA_STATUS	FCCU_ENA_STATUS	RES	RES	CRC3	CRC2	CRC1	CRC0
Boost enable status bit	FCCU enable status bit	Reserved bit	Reserved bit	Cyclic redundancy checking bit 3	Cyclic redundancy checking bit 2	Cyclic redundancy checking bit 1	Cyclic redundancy checking bit 0

Table 317. DSR18 (0x32) LSB description

Bit	Name	Description
7	BOOST_ENA_STATUS	Live bit
6	FCCU_ENA_STATUS	Live bit
5	RES	Reserved
4	RES	Reserved
3	CRC 3	

Bit	Name	Description
2	CRC 2	
1	CRC 1	
0	CRC 0	

9.8 Status register that must be cleared to enter into active FP mode

Table 318. **Status register list to be cleared for active FP mode**

Register
abist_boost_ignored
abist_complete
boost_in_lp
boost_vdsmon_error
buck1_int_fail
buck1_oc
buck1_ov
buck1_pg_ok
buck1_pg_timeout
buck1_uv
buck2_int_fail
buck2_oc
buck2_ov
buck2_pg_ok
buck2_pg_timeout
buck2_uv
buck3_int_fail
buck3_oc
buck3_ov
buck3_pg_ok
buck3_pg_timeout
buck3_uv
bypass_vdsmon_error
current_mismatch
fbb_ov
fbb_uv
fccu_ena_echo_error
fccufail
forced_sleep_powup
fp_ready
fsm_comp_error
fsm_to_rec2
gndloss
ign_wake
int_reg_ov
int_reg_uv
irq_echo_error
irq_sent

Register
lbist_complete
lbist_stopped
ldo1_pg_ok
ldo1_pg_timeout
ldo1_uv
ldo2_ov
ldo2_pg_ok
ldo2_pg_timeout
ldo2_uv
lp_ready
nvm_comp_error
nvm_crc_error
osc_error
ouths_oc
ouths_ol
nrst_echo_error
spi_all_wakeup_disable
spi_clk_cnt
spi_crc_error
spi_csn_timeout
spi_reg_comp_error
spi_sdi_stuck_high
spi_sdi_stuck_low
spi_lbisted
spi_status_wrt
spi_undef_add
timer_wake
tsd_cl0
tsd_cl1
tsd_cl2
tsd_cl3
tsd_cl4
vio_uv
vpor
wdfail
wu_wake
forced_sleep_regfail

10 PCB layout recommendation

In designing devices embedding high frequency switching converters, PCB layout is very important because it affects noise pickup and can cause a good design to perform with results that are under the expectations.

Usually, the connections for the power components should be on the top layer with wide, copper-filled areas or shapes. Moreover, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

Output capacitors, inductors and the SPSB100 itself should be as close to each other as possible. This helps to reduce the EMI radiated by the Powertraces due to the high switching currents through them and avoid inserting any other additional components necessary to put in place a suitable filtering action.

Place the input capacitors directly at the VIN12 and VIN3 pins of SPSB100. The feedback parts of the system should be kept away from the inductors and other noise sources.

The critical bypass components such as capacitors for V_{INx} and V_{REG} should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to FBx and COMPx pins.

In a multilayer PCB, use at least one layer as a power ground plane, cause it is not always necessary to have a dedicated signal ground plane. In any case, it is a good practice to have sensitive analog signals referenced to a quiet ground location, to avoid any interferences with the high current loop. The QFN is a thermally enhanced package. To effectively remove heat from the device the exposed pad should be connected to the ground plane using via holes. Figures below illustrate the implementation of the layout guidelines outlined above, on the 4-layer demo board.

As shown in the PCB layout:

- Allow enough copper for V_{IN}, GND and PHx
- All bypass capacitors are placed as close as possible to their connecting pins
- Components for loop compensation are placed as close as possible to the COMP pin
- SGND as well as GND are connected to the inner PGND plane through via holes
- PHx nodes copper should only be routed on the top layer to minimize switching noises
- FBx trace routing is kept away from the software node
- Thermal via holes are placed on VINx and PGND pads to improve thermal dissipation

Figure 72. Assembly top

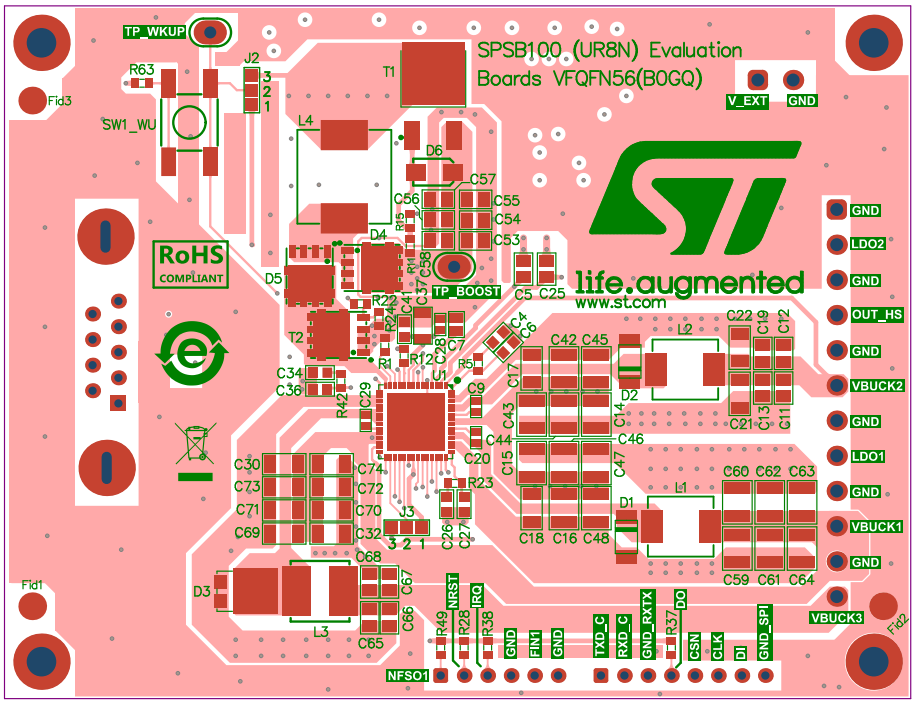


Figure 73. Inner 1 (ground)

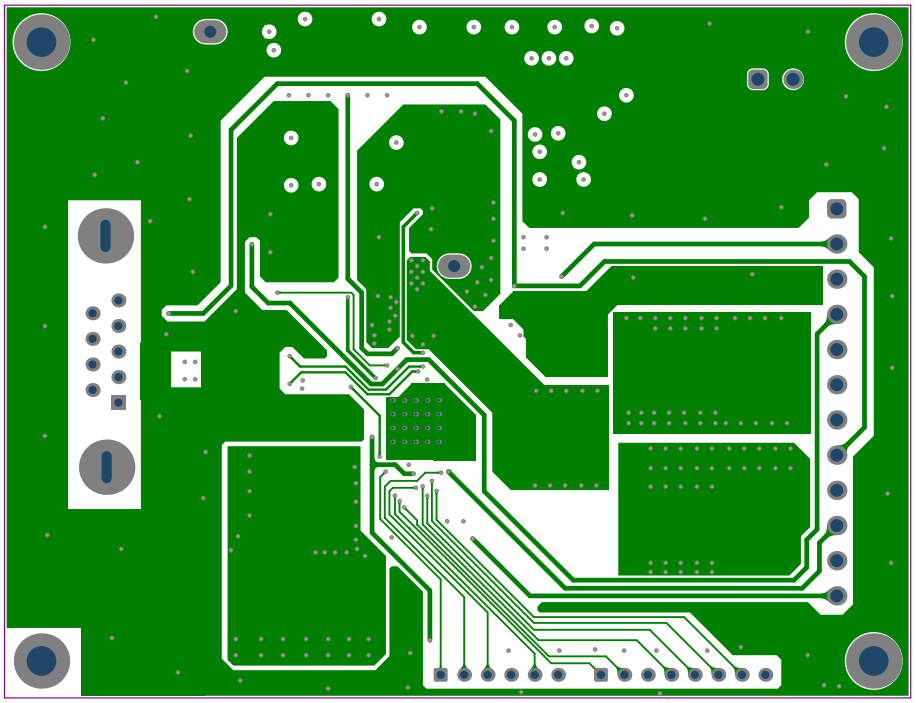


Figure 74. Inner 2 (ground and signal)

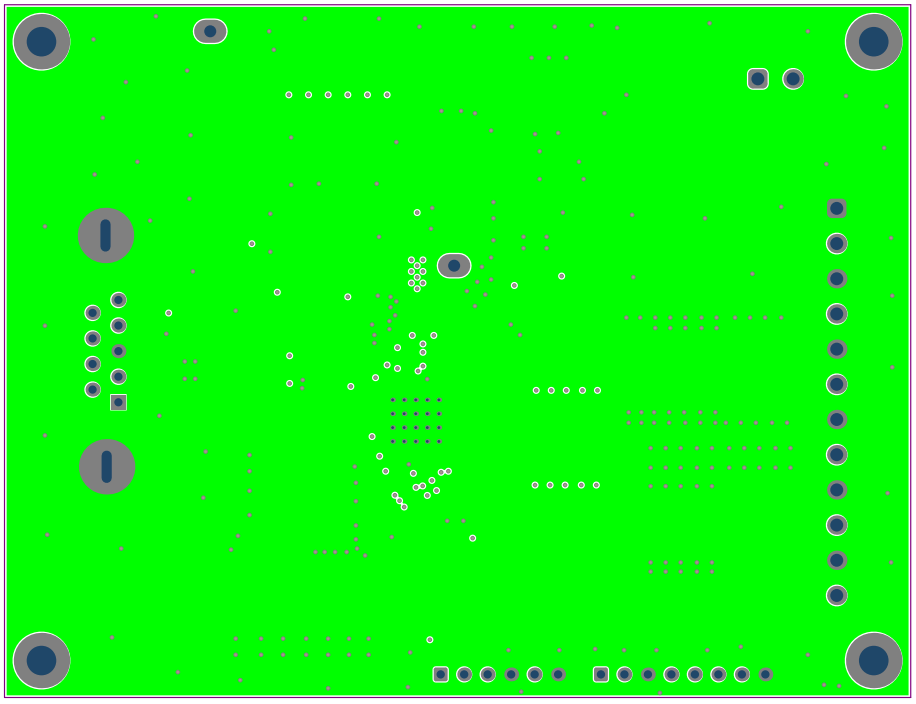
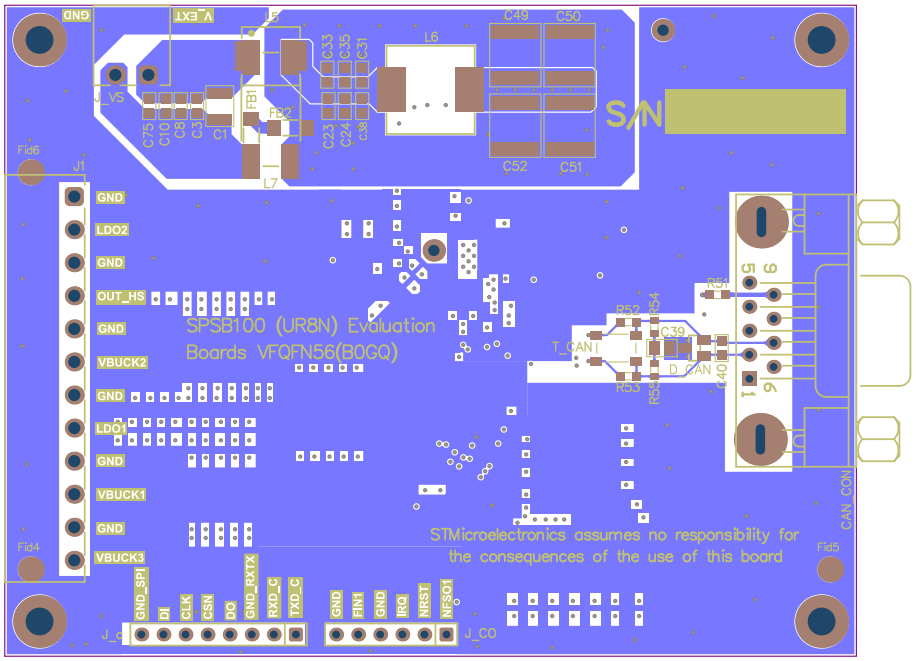


Figure 75. **Assembly bottom**



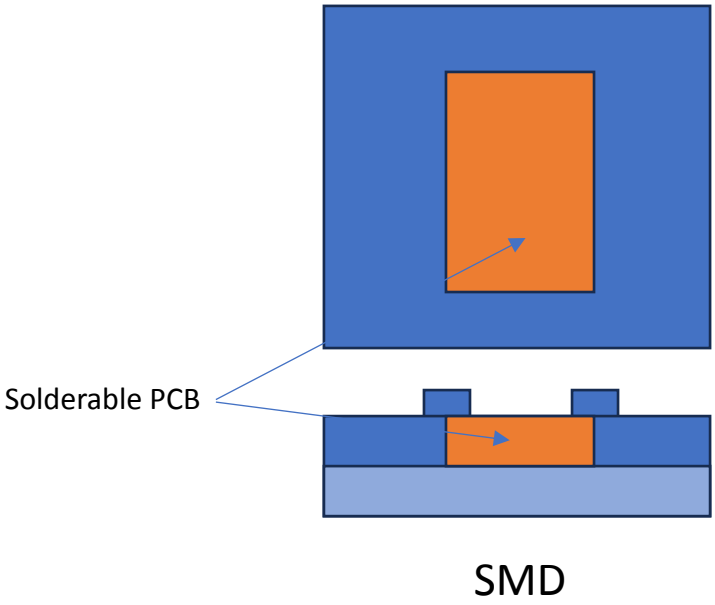
10.1 PCB metal and component placement

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout. QFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

10.2 Solder mask

We recommend that larger power or land area pads are solder mask defined (SMD). This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the openings in the solder mask. This allows for layers to be misaligned by up to 0.1 mm on both axes. Ensure that the solder resists in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

Figure 76. **Solder mask defined (SMD)**



10.3 Stencil design

Stencils for QFN packages can be used with thicknesses of 0.100 ~ 0.250 mm (0.004 ~ 0.010”) stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm ~ 0.200 mm (0.005 ~ 0.008”), with suitable reductions, give the best results. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

11 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 VFQFN56+4L (8x8x0.9 mm exp. pad down) package information

Figure 77. VFQFN56+4L (8x8x0.9 mm exp. pad down) package outline

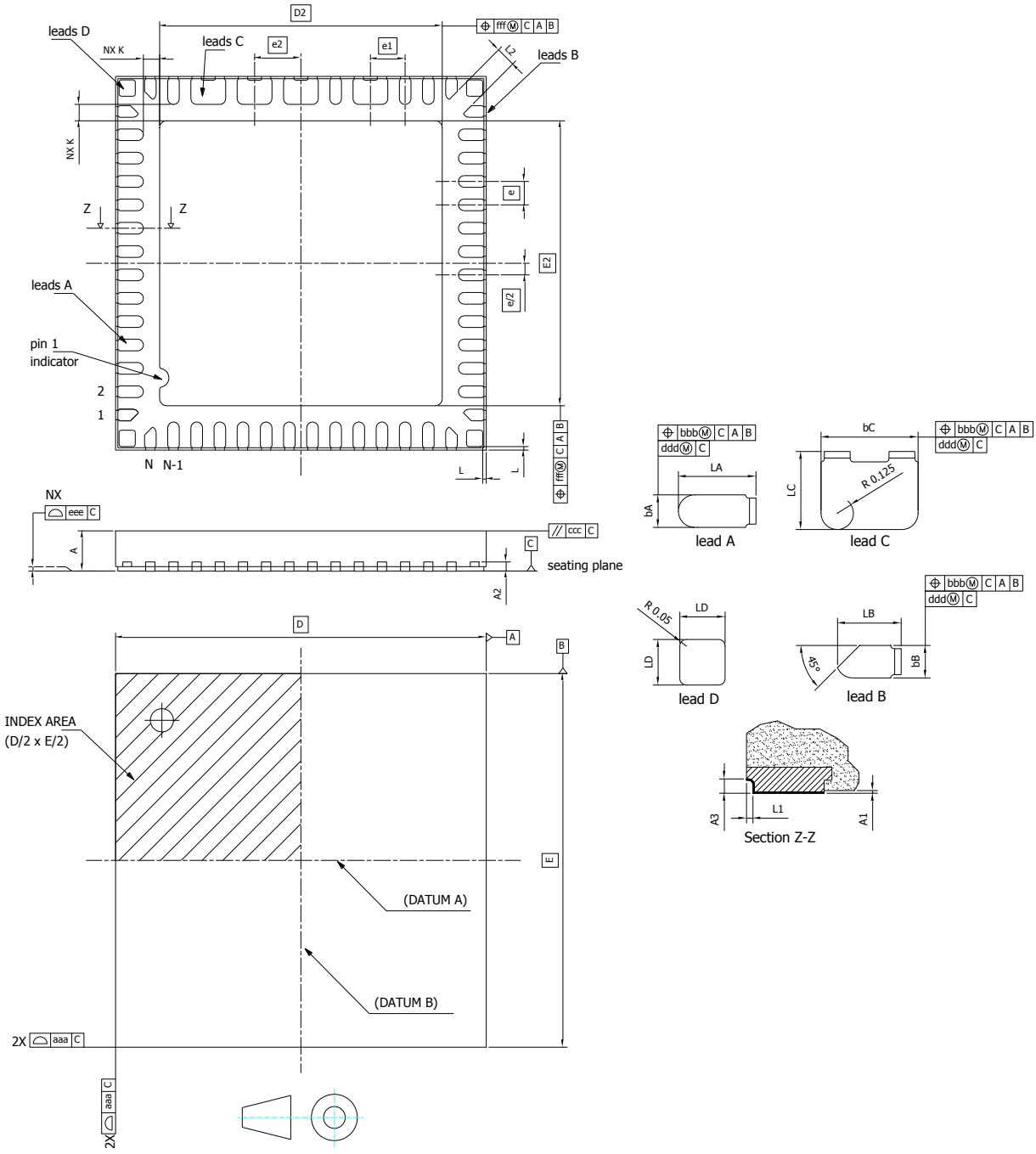


Table 319. **VFQFN56+4L (8x8x0.9 mm exp. pad down) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	-	0.05
A2		0.2 REF	
A3	0.10	-	-
D		8.00 BSC	
D2	6.00	6.10	6.20
E2	6.00	6.10	6.20
e		0.50 BSC	
e1		0.75 BSC	
e2		1.00 BSC	
L		0.075 RFE	
L1		0.05 REF	
L2	0.38	0.43	0.48
LA	0.55	0.60	0.65
bA	0.20	0.25	0.30
LB	0.44	0.49	0.54
bB	0.20	0.25	0.30
LC	0.55	0.60	0.65
bC	0.70	0.75	0.80
LD	0.30	0.35	0.40
K	0.20	-	-
N		56 + 4	
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		010	
REF		-	

Revision history

Table 320. **Document revision history**

Date	Version	Changes
04-Jun-2024	1	Initial release.
07-Oct-2024	2	Updated Table 50. External components (referred to pictures in the related sections), Table 52. Global status byte GSB description, Section 7.9: BUCK2 converter and Section 7.10: BUCK3 converter. Minor text changes in Table 8. IRQ events, Table 73. DCR3 (0x03), Table 78. DCR4 (0x04) MSB description and Table 86. DCR5 (0x05) description.

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