ACEPACK 1 and 2, SiC power modules: how to read our datasheet

Introduction

This technical note is intended to explain the parameters included in a power module datasheet and guide the customer toward the best choice according to their specific application. This document provides the designer with sufficient information to establish the limits of the device. The datasheet values listed are referred to the parameters tested in the characterization lab and at the production site.

For this document, an ACEPACK 2 power module has been chosen as a reference: A2F12M12W2-F1 datasheet is considered in the next paragraphs.

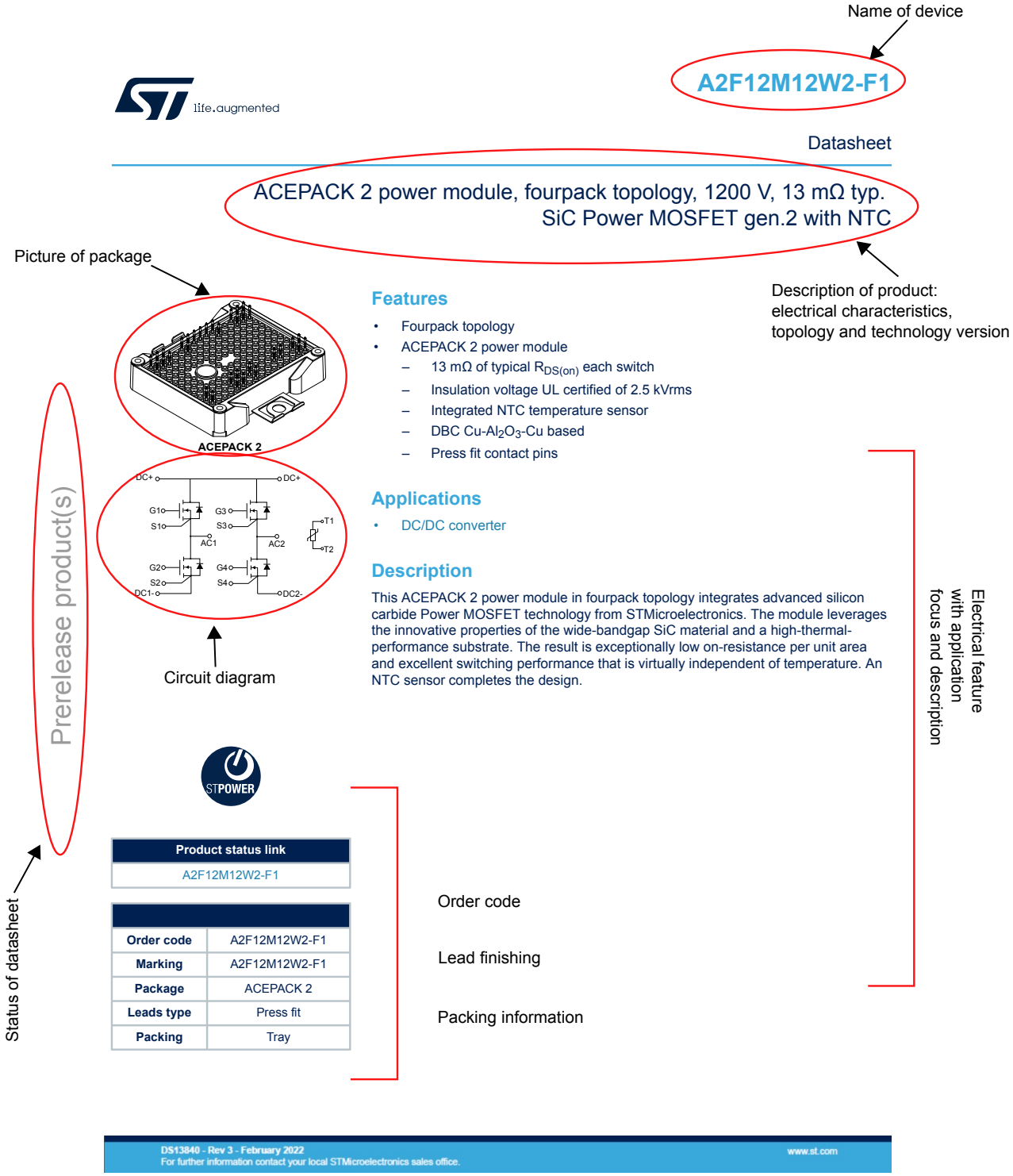
STMicroelectronics' datasheet for SiC based devices is structured as listed below:

- Datasheet general information, mainly listed in front page.
- Absolute maximum ratings of SiC MOSFET
- Electrical characteristics in operating conditions for single switch inside the module
- NTC thermistor characteristics
- Package features
- Circuit output and package outline

1 Datasheet general information

The first datasheet page shows the primary details regarding the power module.

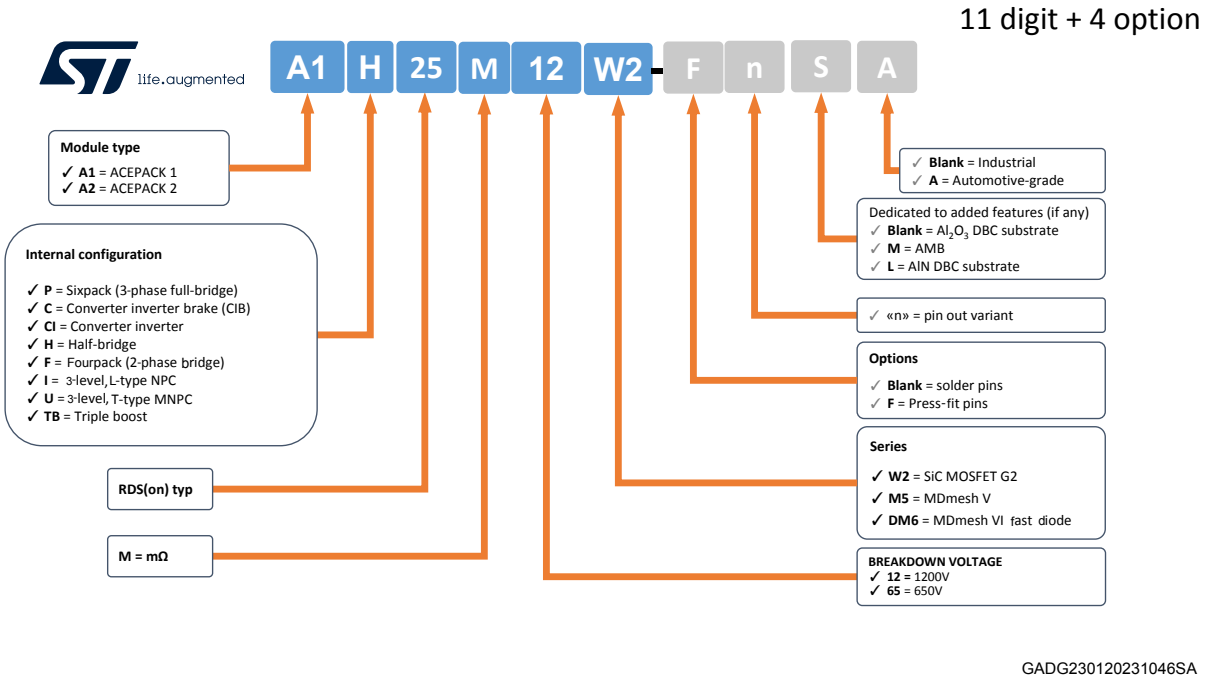
Figure 1. Datasheet layout



1.1 ACEPACK 1 and ACEPACK 2 nomenclature

The nomenclature of ACEPACK 1 and 2 is explained in Figure 2. Layout nomenclature.

Figure 2. Layout nomenclature



2 Electrical rating description

2.1 Absolute maximum rating description

Figure 3. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	
I_D	Drain current (continuous) at T_C = 25 °C	75	A
I_{DM}(1)	Repetitive peak drain current	150	A
T_J	Maximum junction temperature	175	°C
	Operating junction temperature range under switching conditions	-40 to 150	

1. *Pulse width limited by maximum junction temperature.*

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- **Drain-source voltage:** the allowable peak drain source voltage.
- **Gate-source voltage:** allowable gate source voltage range without damaging the gate oxide.
- **Gate-source voltage (recommended operating values):** recommended operating voltage gate drive for achieving the proper $R_{DS(on)}$.
- **The DC drain current:** this value is based on total power dissipation. The maximum drain current of a module can be calculated with equation

$$I_D = \sqrt{\frac{\left(T_J\max - T_C\right)}{R_{DS(on)} \cdot R_{thJC}}} \quad (1)$$

  Where:

  J = junction

  C = case
- **Repetitive peak drain current:** the nominal drain current that can be exceeded in an application for a short time. This is defined as the repetitive peak drain current and represents the maximum value of the pulsed current, which allows the device to stay within the SOA (safe operating area). From a theoretical point of view, these values can be derived from feasible power dissipation and the transient thermal impedance Z_{th} if the duration of the overcurrent condition is defined. However, this theoretical value does not consider any limitations of bond wires, bus bars or power connectors. Therefore, the datasheet value is quite low compared to a calculated value based on theory, but represents a safe operating parameter considering all the practical limitations of the power module.

2.2 Thermal data

Figure 4. **Thermal data**

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.43	°C/W

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This data shows the thermal junction-to-case resistance for each switch.

Thermal resistance relates to the heat conduction properties of the power module (temperature per unit of power, °C/W). The main power losses of the SiC module are dissipated from the die to the heat sink through different materials, as shown in Figure 5. Thermal resistance scheme for power module:

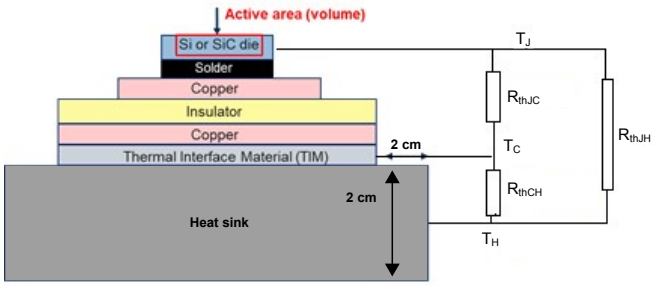
- **R_{thJC}:** thermal resistance from the die junction to the case. It is the thermal resistance when the module is mounted on the heat sink with specific thermal interface material (TIM).

$$R_{thJC} = \frac{T_J\max - T_C}{P\_appl} \quad (2)$$

- **R_{thJH}:** thermal resistance from the die to heat sink this is determined by:

$$R_{thJH} = \frac{T_J\max - T_{heat\ sink}}{P\_appl} \quad (3)$$

Figure 5. **Thermal resistance scheme for power module**



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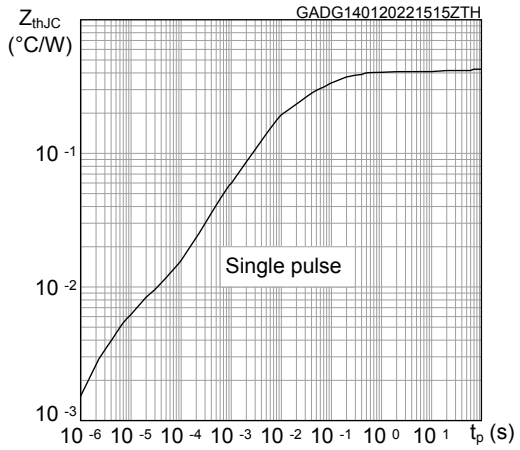
The thermal impedance behavior can therefore be modeled with the appropriate coefficients of the SiC module and represented in a Z_{thJC} (t) graph, as shown in Figure 6. Maximum transient thermal impedance:

Figure 6. **Maximum transient thermal impedance**



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2.3 Electrical characteristic

Figure 7. On/off state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V , I_D = 1 mA	1200			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 18 V , I_D = 75 A		13	17	mΩ
		V_{GS} = 18 V , I_D = 75 A,T_J = 150 °C		20		
$V_{GS(th)}$	Gate threshold voltage	I_D = 10 mA, V_{DS} = V_{GS}	1.9	3.0	4.9	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1200 V, V_{GS} = 0 V			200	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = -10 to 22 V			±1	µA
C_{iss}	Input capacitance	f = 1 MHz, V_{DS} = 800 V, V_{GS} = 0 V		7000		pF
C_{oss}	Output capacitance			440		pF
C_{rss}	Reverse transfer capacitance			56		pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A		1		Ω
Q_g	Total gate charge	V_{DD} = 800 V, V_{GS} = -5 to 18 V, I_D = 100 A		294		nC
Q_{gs}	Gate-source charge			65		nC
Q_{gd}	Gate-drain charge			109		nC

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$R_{DS(on)}$ characteristics

This parameter states the resistance between drain and source for a specified drain current. This value is temperature dependent. The $R_{DS(on)}$ of ACEPACK SiC MOSFET increases with temperature and decreases with V_{GS} . The typical drain-source on state resistance is determined by the output characteristic measurement at the same drain current I_D. During the output characteristics measurement, the voltage drop is measured. It is always measured on module pins. Figure 8. Typical output characteristics T_J = 25 °C and Figure 9. Typical output characteristics T_J = 150 °C show the output characteristic @ 25 °C and 150 °C. The drain-source on-state resistance is evaluated from the voltage drop with the following formula:

$$R_{DS(on)} = \frac{V_{DS}(V_{GS}fixed)}{I_D} \quad (4)$$

Figure 8. Typical output characteristics T_J = 25 °C

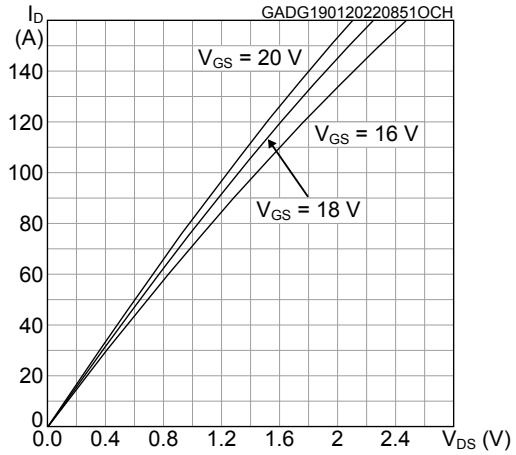

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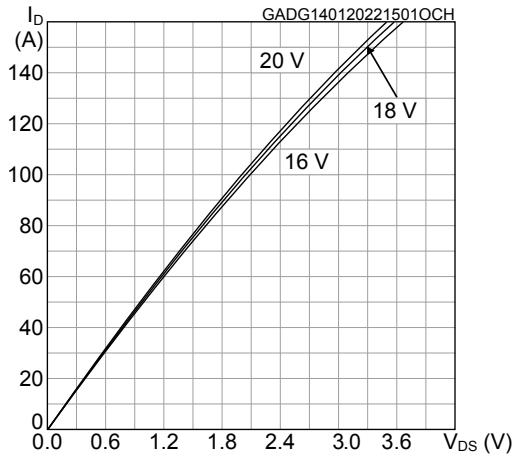
Figure 9. **Typical output characteristics T_J = 150 °C**



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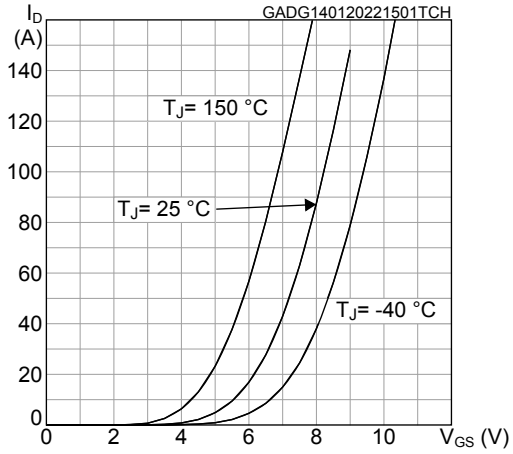
V_{GS} threshold voltage

The threshold voltage, $V_{GS(th)}$, is the gate-source voltage needed for current to start flowing through the channel of the device at a specific drain-to-source current. Figure 7. On/off state shows the threshold test condition. This threshold voltage $V_{GS(th)}$ is measured by applying V_{GS}=V_{DS} by forcing current I_{DS}=5 mA. From the results, the typical threshold voltage $V_{GS(th)}$ equals 3.1 V at 25 °C and I_{DS}=5 mA. The behavior of $V_{GS(th)}$ vs current and temperature is shown by the transfer charactheristic graph, see Figure 10. Typical transfer characteristics.

Figure 10. **Typical transfer characteristics**



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I_{DSS} e I_{GSS} leakage current

Two major types of leakage currents are shown in Figure 7. On/off state of the datasheet:

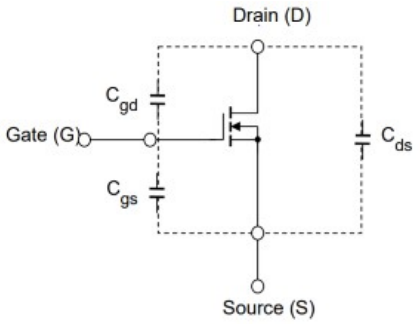
- I_{DSS}: the maximum drain-source cut-off current, which describes the leakage current between the drain and source when the SiC inside module is in blocking mode
- I_{GSS}: the gate-source leakage current gives some indication about the maximum leakage current between gate and source with drain-source short-circuited and maximum gate source voltage applied.

Capacitances (C_{iss}, C_{rss} and C_{oss})

In a SiC power MOSFET, the gate is insulated by a thin silicon oxide. Therefore, a SiC MOSFET has capacitances between the input and output terminal gate-drain, gate-source, and drain-source terminals. The gate-drain capacitance C_{gd} and the gate-source capacitance C_{gs} are mainly determined by the structure of the gate terminal, while the drain-source capacitance C_{ds} is determined by the capacitance of the vertical junction.

$$C_{iss} = C_{gs} + C_{gd} \quad (5)$$

Figure 11. Schematic parassitic capacitance



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The C_{oss}: the output capacitance is the sum of the drain-source capacitance and the gate-drain capacitance:

$$C_{oss} = C_{ds} + C_{gd} \quad (6)$$

The reverse transfer capacitance – C_{rss} reverse transfer capacitance:

$$C_{rss} = C_{gd} \quad (7)$$

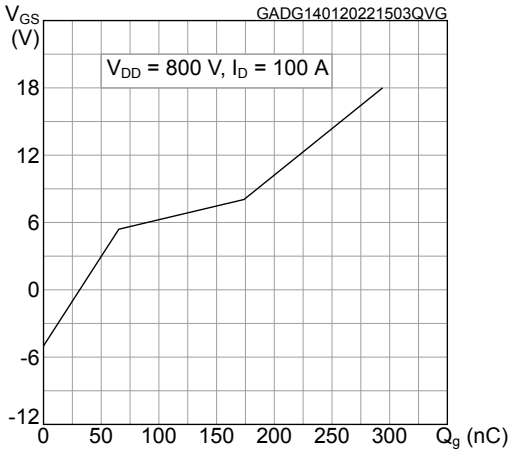
Gate resistance (R_G)

The internal gate resistance, R_G, is inversely proportional to die size and a given breakdown voltage. Since a SiC MOSFET die is much smaller than a silicon MOSFET die, internal gate resistance tends to be higher. The real benefit of the smaller SiC MOSFET die comes in the form of lower input capacitance, C_{ISS}, which translates to lower required gate charge, Q_G.

Gate charge (Q_g)

When V_{GS} is applied, a certain amount of charge is transferred to change the gate voltage between $V_{GS(MIN)}$ and $V_{GS(MAX)}$ (V_{DD}) as fast as possible. Since the MOSFET internal capacitances are non-linear, a V_{GS} versus gate charge (Q_g) curve is helpful to identify how much charge must be delivered for a given V_{GS} level. A typical gate charge curve for a SiC MOSFET is shown in Figure 12. Typical gate charge characteristics.

Figure 12. Typical gate charge characteristics



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2.4 Switching energy E_{on} and E_{off}

Figure 13. **Switching energy**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	V_{DD} = 800 V, I_D = 75 A,	-	1.48	-	mJ
E_{off}	Turn-off switching energy	V_{GS} = -5 to 18 V, R_G = 5.6 Ω	-	0.35	-	
E_{on}	Turn-on switching energy	V_{DD} = 800 V, I_D = 75 A,	-	1.51	-	mJ
E_{off}	Turn-off switching energy	V_{GS} = -5 to 18 V, R_G = 5.6 Ω T_J = 150 °C	-	0.32	-	

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This section describes the behavior of the device during the two transitional states: from off-state to on-state and from on-state to off-state. The switching characteristics of the SiC power module are evaluated using the double-pulse clamped inductive load test setup shown in the Figure 14. Testing circuit for switching energies. Parasitic inductance in the module depends on internal layout, so it must be considered in addition to the inductance of testing circuit.

Figure 14. **Testing circuit for switching energies**

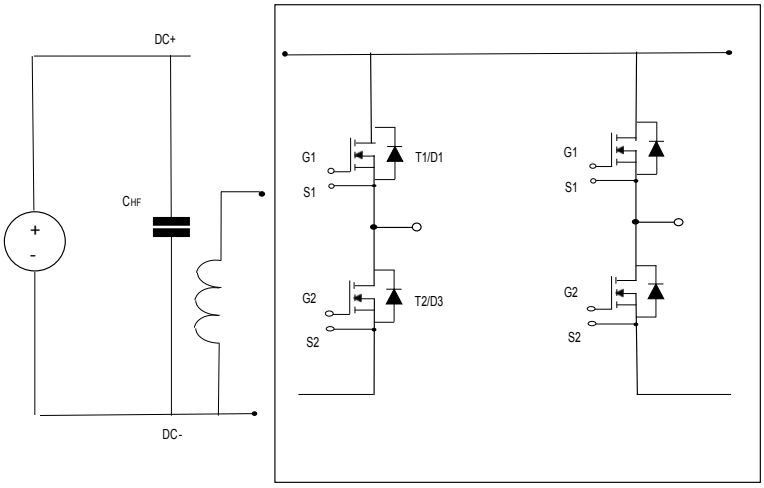

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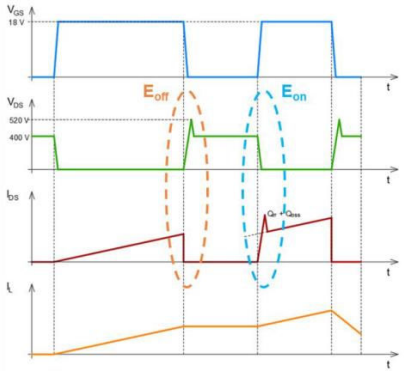
Figure 15. **Typical behavior of switching on and off**



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Compared to IGBT, SiC power modules are faster in terms of switching conditions. The SiC MOSFET has almost zero recovery loss E_{rr} thanks to the fast recovery performance of body diodes of SiC MOSFETs. Furthermore, they have exceptionally low E_{off} than IGBTs due to the absence of tail current. E_{on} and E_{off} tend to increase in proportion to currents (the proportionality varies with external R_g). Recovery current in Si MOSFETs and tail current in IGBTs become higher at high temperatures, whereas SiC modules using majority carrier devices exhibit exceptionally small change in switching losses with increasing temperature. Also, the threshold voltage of SiC devices decreases at high temperatures. The net effect is that SiC power modules tend to have lower E_{on} and slightly higher E_{off} as operating temperature increases. Figure 15. Typical behavior of switching on and off, Figure 16. Typical switching energy vs drain current (T_J = 25 °C), Figure 17. Typical switching energy vs gate resistance (T_J = 150 °C), Figure 18. Typical switching energy vs temperature and Figure 19. Typical switching energy vs V_{GS} (T_J = 150 °C) detail the changes in switching energy in relation to I_D, R_G, and T_J.

Figure 16. Typical switching energy vs drain current (T_J = 25 °C)

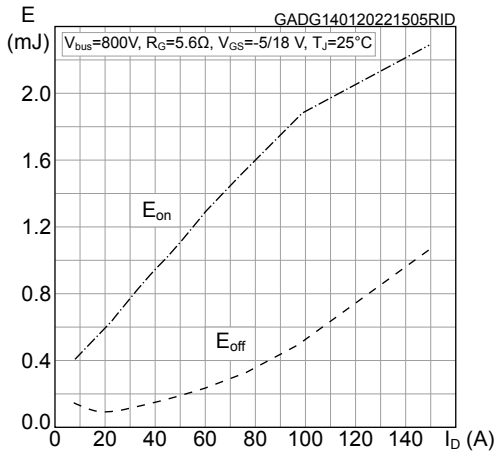

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Figure 17. Typical switching energy vs gate resistance (T_J = 150 °C)

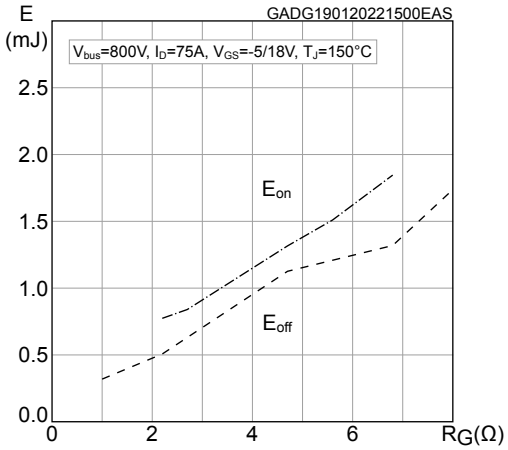

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Figure 18. Typical switching energy vs temperature

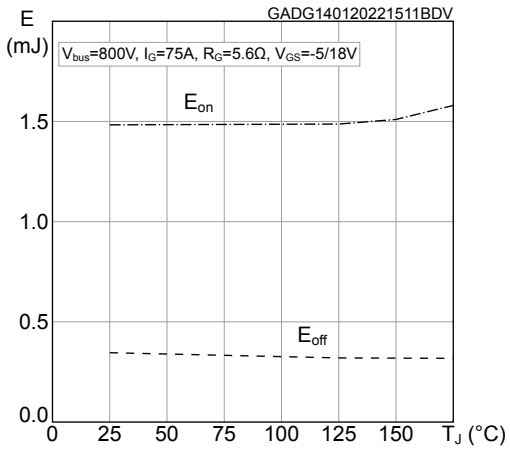

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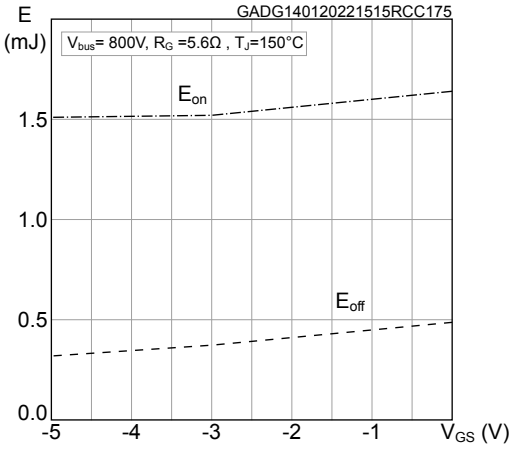
Figure 19. Typical switching energy vs V_{GS} (T_J = 150 °C)



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2.5 Source-drain body diode

Figure 20. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	V_{GS} = 0 V, I_{SD} = 75 A	-	2.9	-	V
t_{rr}	Reverse recovery time	I_{SD} = 75 A, V_{DD} = 800 V, V_{GS} = -5 V	-	42	-	ns
Q_{rr}	Reverse recovery charge		-	896	-	nC
I_{RRM}	Reverse recovery current		-	60	-	A
E_{rr}	Reverse recovery energy		-	336	-	µJ

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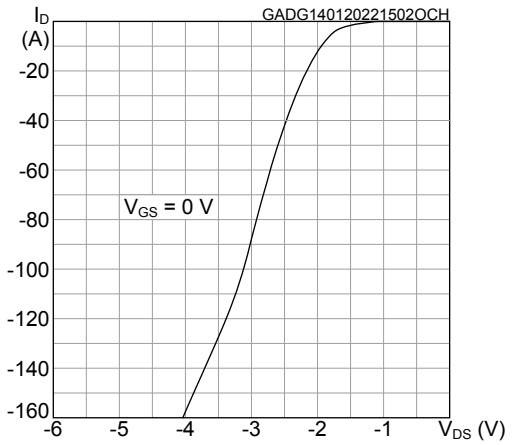
The Figure 20. Source-drain diode shows the characteristic of parasitic body diode of the SiC MOSFET formed in the P-N junction. However, the body diode of the SiC MOSFET has a high threshold voltage (around 3 V) and relatively large forward voltage drop (V_f) due to SiC having three times larger bandgap than Si. When connecting an external anti-parallel freewheeling diode to the Si MOSFET, an additional low-voltage blocking diode needs to be connected to the MOSFET in series to prevent conduction through the “slow” body diode. This is because the V_f of the Si MOSFET body diode is about the same as that of the external diode. This means more components and higher conduction loss. This arrangement is not needed with SiC MOSFETs as the V_f of their body diodes is sufficiently high compared to that of a typical external free-wheeling diode. The high V_f of the body diode can be reduced by turning on the gate voltage for reverse conducting, like synchronous rectification. Figure 21. Typical diode forward characteristics shows the body diode characteristic.

Figure 21. Typical diode forward characteristics



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2.6 NTC thermistor

Figure 22. Absolute maximum ratings for NTC temperature sensor, considered as standalone

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{25}	Resistance rating	T = 25 °C		5		kΩ
R_{100}	Resistance rating	T = 100 °C		493		Ω
$\Delta R_{100}/R$	Resistance tolerance		-5		5	%
B	B value	T = 25 to 50 °C		3375		K
		T = 25 to 85 °C		3411		
T	Operating temperature range		-40		150	°C

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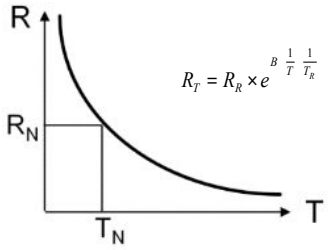
One of the most important parameters in power electronic devices is the chip temperature. The measurement of this temperature during operation is very difficult. One approach for estimating the real chip temperature in steady state is to use the NTC inside the SiC module. The NTC (negative temperature coefficient) is a thermistor with resistance that decreases as temperature increases. Several parameters are needed to describe the electrical behavior of a thermistor.

- R_{25}: this value specifies the nominal resistance value at a defined temperature of 25 °C under zero power conditions.
- R_{100}: is the resistance value at 100 °C. This value also shows the resistance values at the nominal tolerance.
- $\Delta R_{100}/R$: this is the tolerance of the resistance at 100 °C.

Figure 23. Resistance vs temperature



T	Temperature in [K]
R_T	Resistance in [Ω] at temperature T
T_R	Rated temperature in [K]
R_R	Resistance in [Ω] at T_N
B	B-value, material specific constant
e	Base of natural logarithm (e = 2.71828)

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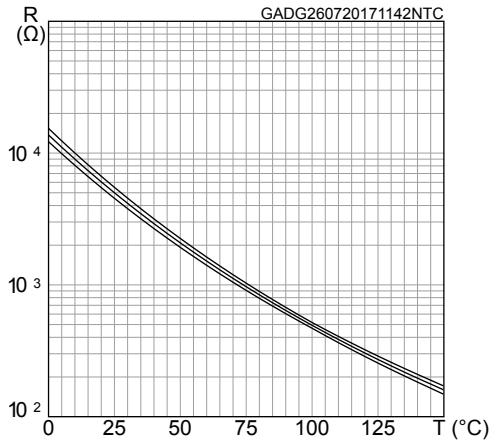
- The B value is determined by the ceramic material, and represents the slope of the R/T curve. The B value is given in [K]

$$B = \frac{T_1 \times T_2}{T_2 - T_1} \cdot \ln \frac{R_1}{R_2} \quad (8)$$

The B value can be determined by measuring the resistance (R_1, R_2) at two temperatures (T_1, T_2). The datasheet specifications refer to resistance values at 25 °C and 100 °C: $B_{25}/100$ and 25 °C and 80 °C: $B_{25}/80$.

Figure 24. NTC typical resistance vs temperature



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3 Package

Figure 25. **ACEPACK 2 package**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s)	2.5			kVrms
M_d	Mounting torque (M4 screw)	2.0		2.3	N•m
CTI	Comparative tracking index	200			V
L_s	Stray inductance module loop		12		nH
T_{stg}	Storage temperature range	-40		125	°C

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V_{ISO}: the insolation voltage is the minimum voltage a device has to withstand between the electrical connections and the base. This is also known as a high potential test. All main pins or terminals and control pins or terminals are connected during this test. The applied impulse voltage is a function of the working voltage and the overvoltage category. V_{ISO} is the RMS value of a 50 Hz AC voltage at which 100% of the modules are tested.

M_d: minimum and maximum values for the M4 fixing screws.

CTI: the resistance of ACEPACK insulating material is described by the CTI (comparative tracking index). The insulating materials are classed in four groups:

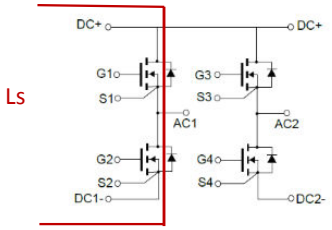
Table 1. **CTI description**

CTI group description		
CTI group	**CTI level (V)**	**Example**
1	≥600	Plastic material like PE-HD (polytetrafluoroethylene)
2	400-599	Printed circuit board (PCB) base material FR4 type KF
3a	175-399	Glass-filled PCB material FR4
3b	100-174	Foil material polymide (e.g. Kapton) or resins (e.g. phenolic)

L_S: stray inductance leads to transient overvoltage at the switching transient and are a major source of EMI.

This inductance, in combination with parasitic capacitances of the component, can lead to resonant circuits, which can cause voltage and current ringing at switching transients. The stray inductance depends on the SiC topology inside module. Typically, it is included in the loop between DC+ and DC-.

Figure 26. **Schematic for Ls**



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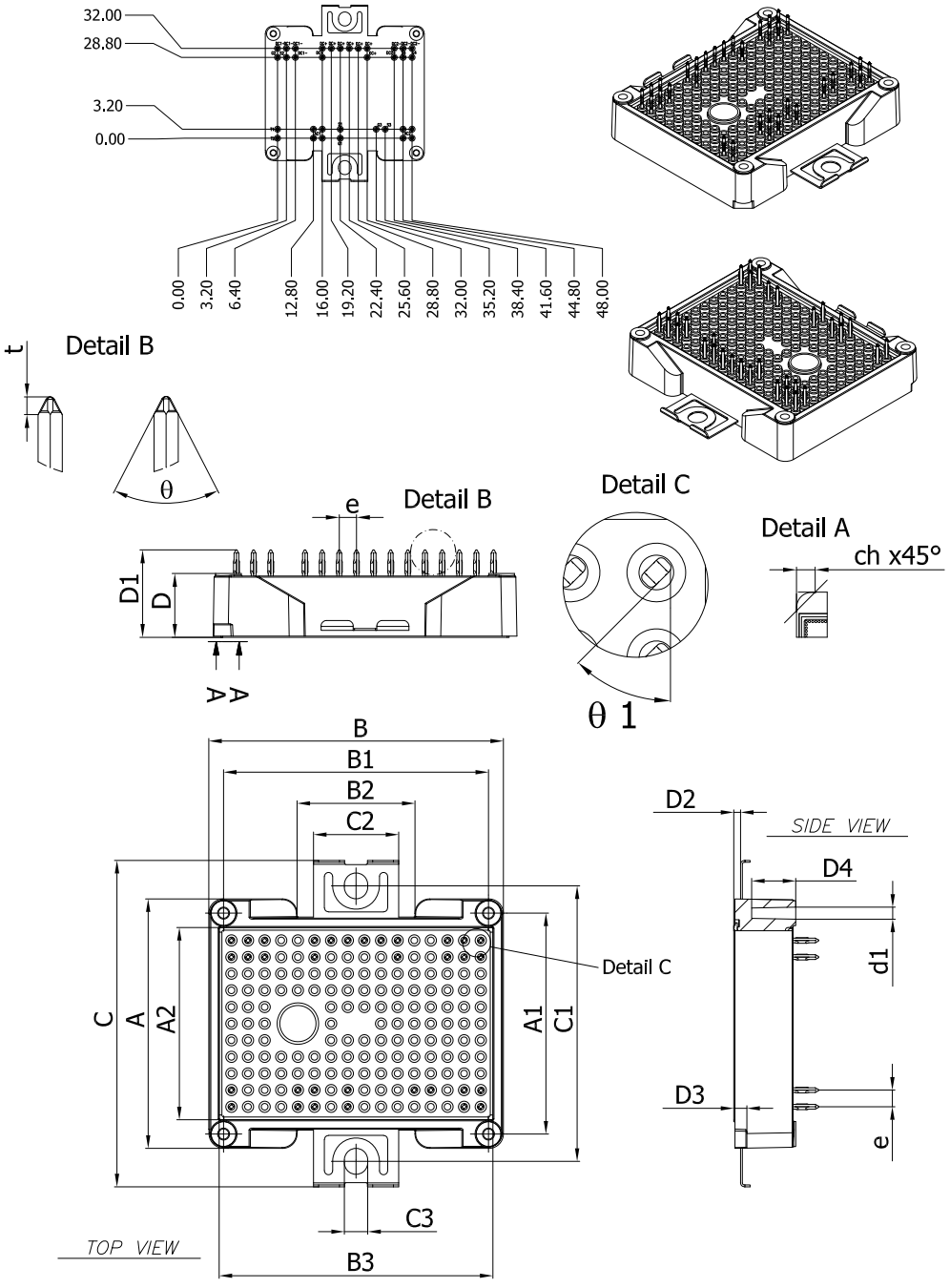
3.1 Schematic and pin descriptions

This section describes the output circuit and the pin descriptions. It shows the package output outline, with all measurements in mm.

Figure 27. ACEPACK 2 fourpack press fit package outline (dimensions are in mm)



8569722_12_fourpack_press_fit

4 References

- IEC 60112- *Method for the determination of comparative and proof tracking indices of solid insulating material*
- *AN4544 IGBT datasheet tutorial*
- *Datasheet A2F12M12W3-F1*
- *TN1250 technical note: Press-fit ACEPACK power modules mounting instructions*

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
06-Mar-2023	1	First release.

Contents