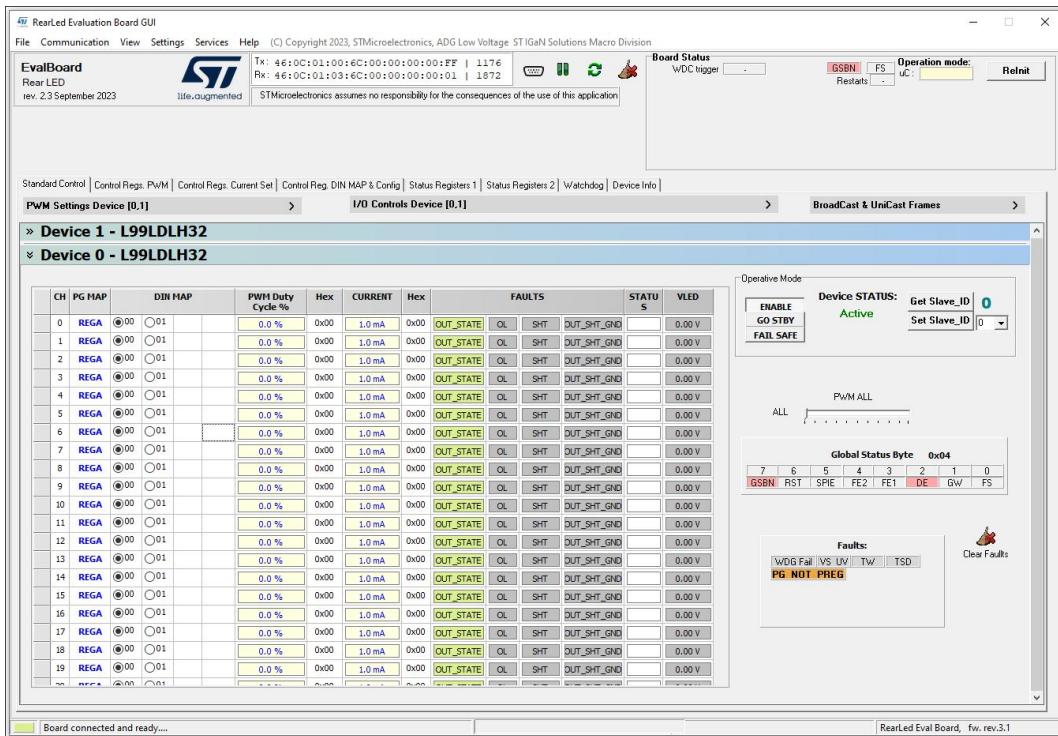


Graphical user interface (GUI) for EV-L99LDLH32GEN

Introduction

The STSW-EVLDLH32GEN is the graphical user interface (GUI) dedicated to set and control the L99LDLH32 device assembled in the corresponding evaluation board **EV-L99LDLH32GEN**. The STSW-EVLDLH32GEN has been developed by using Visual Studio/C sharp and it works with the board EVAL-SPC582B programmed with a dedicated firmware.

Figure 1. STSW-EVLDLH32GEN graphical user interface



1 Get software

Search on www.st.com, STSW-EVLDLH32GEN and in the “Tools & Software” section. To get the software (GUI + Firmware) follow the procedure below.

2 Software installation

2.1 Firmware

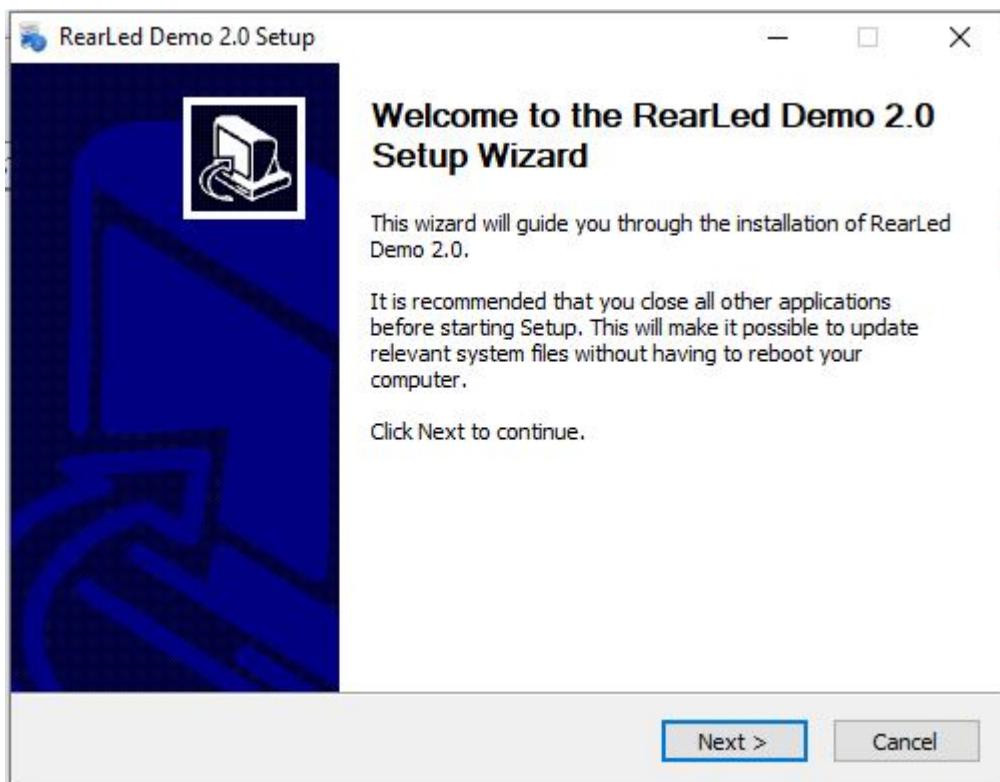
The board EVAL-SPC582B is programmed with a specific firmware.

2.2 GUI installation

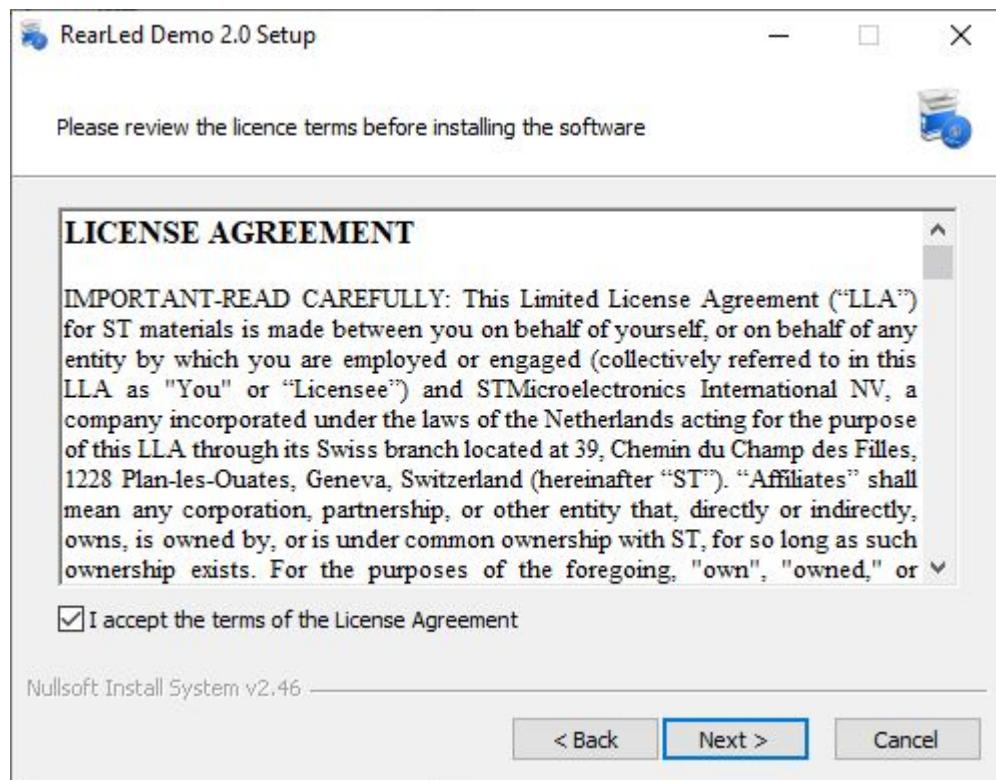
The GUI installation has the following steps:

- Launch SetupRearLed.exe

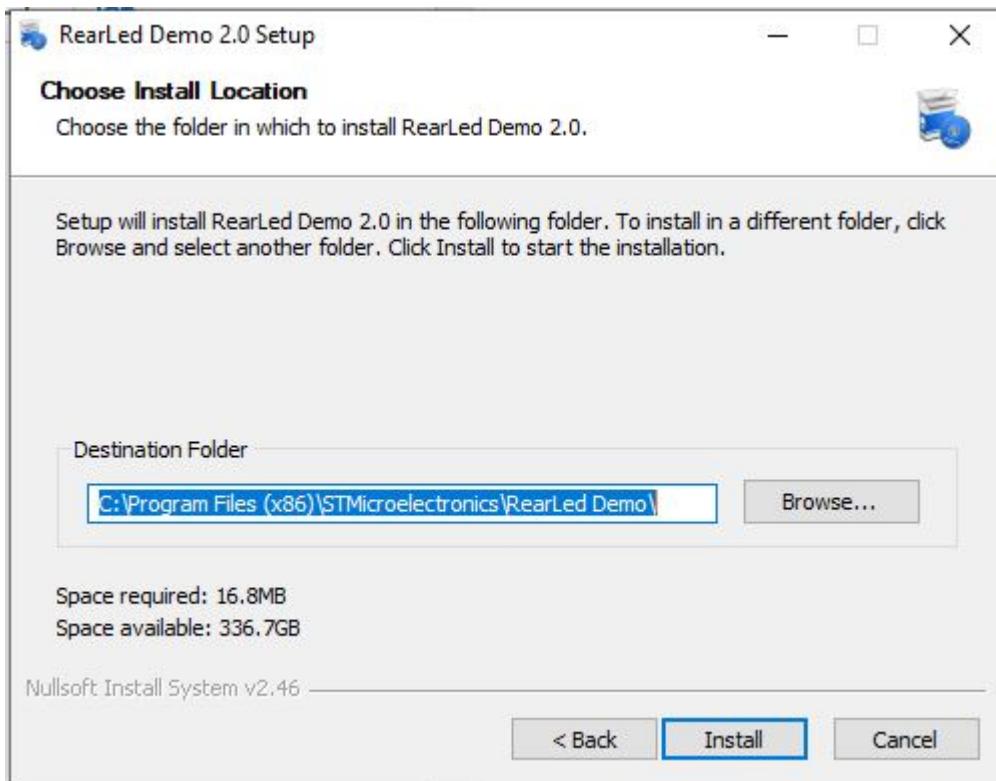
Figure 2. Setup wizard



- Following step by step the wizard you are able to install the GUI RearLed. To continue the installation you have to accept the terms of the license agreement:

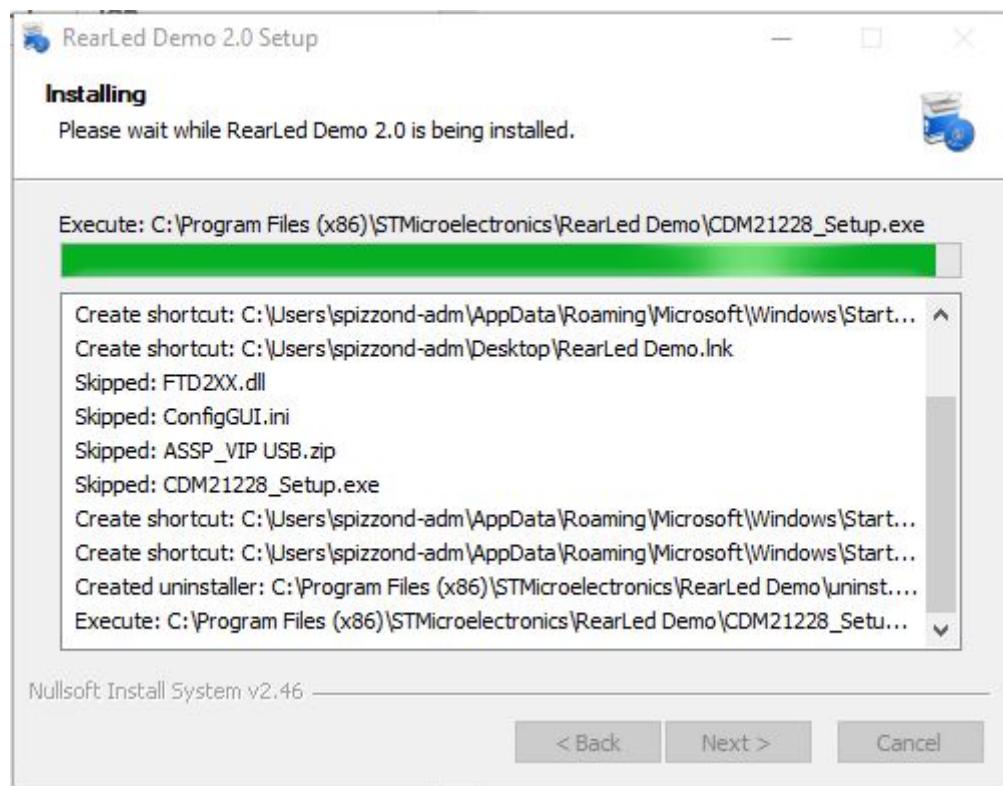
Figure 3. License agreement

- Next you have to choose the installation folder:

Figure 4. Installation folder setup

- The installation continues till the end:

Figure 5. Copying files



- Before ending the installation, it is proposed to install FTDI drivers. Skip this step if you want to install them at a different time (drivers could be obtained from the ftdichip website) or if they are already installed.

Figure 6. FTDI installation (1/4)

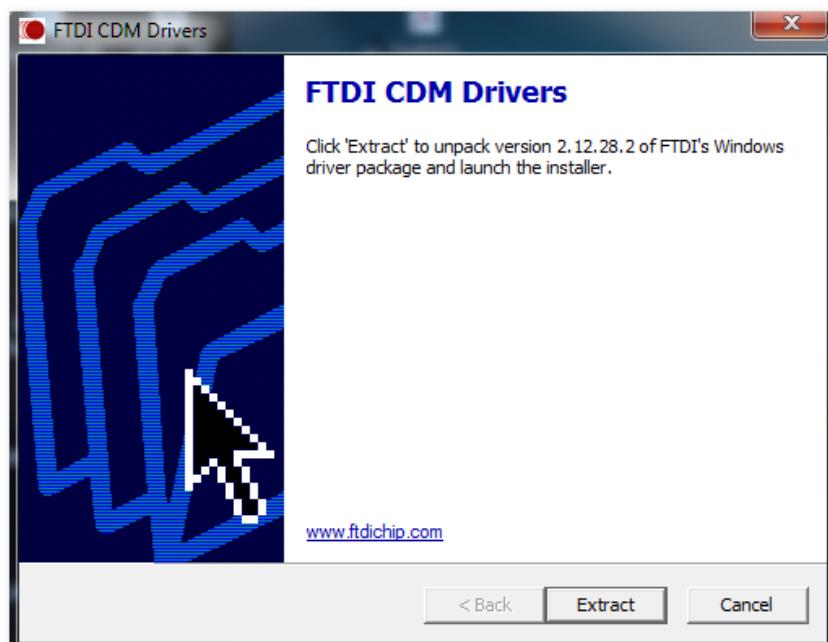
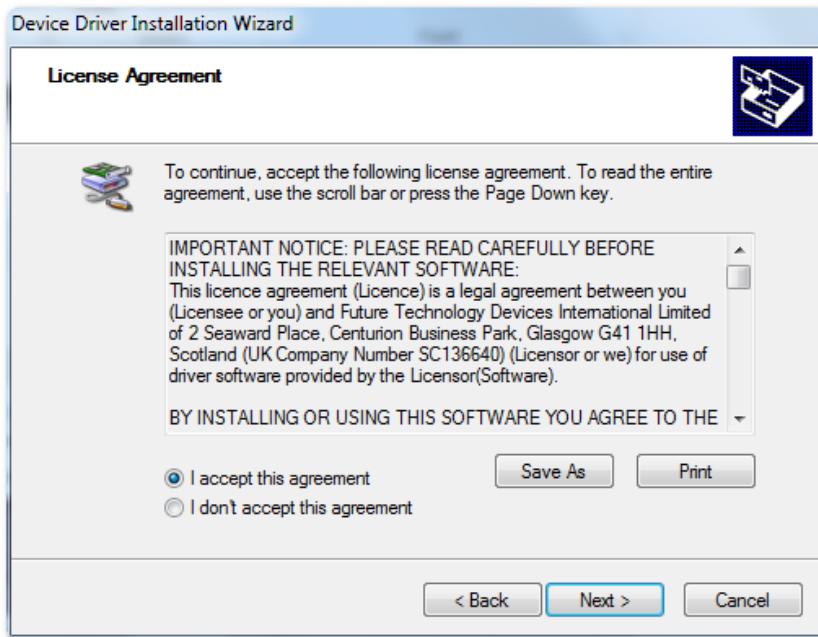


Figure 7. FTDI installation (2/4)

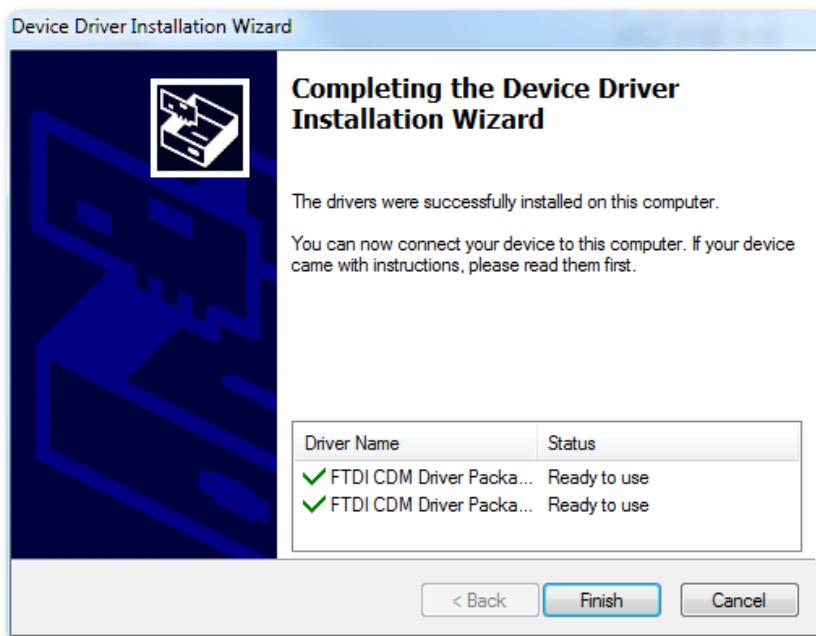


Figure 8. FTDI installation (3/4)



- To complete the FTDI installation the following dialog box is shown to confirm that the drivers were successfully installed.

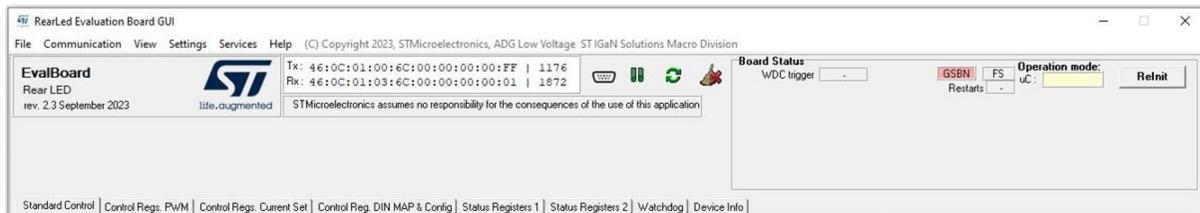
Figure 9. FTDI installation (4/4)



3 GUI description

The main form contains four tabs for device control.

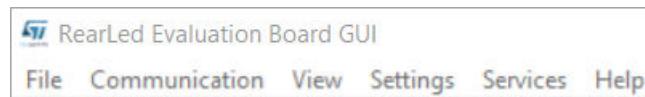
Figure 10. Tabs for device control



It is also embedded the communication traffic monitor, showing communicated data between GUI and MCU.

3.1 Main menu

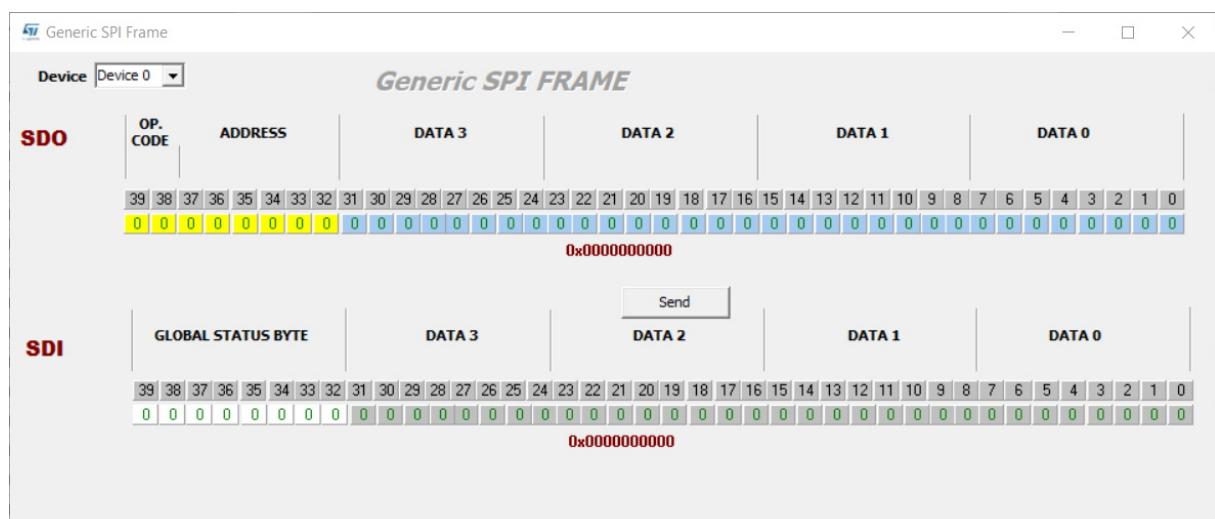
Figure 11. Main menu



It contains the following actions:

- Possibility to choose the communication interface
- View: SPI registers overview
- Settings: allow to configure periodical refresh of registers
- Service: generic SPI frame allows to send a customizable SPI frame to a specific device selected through a combo box

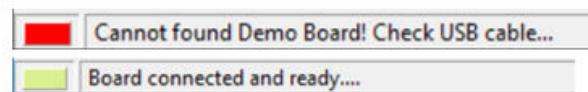
Figure 12. Generic SPI frame



3.2 Status strip

The icons show the interface status between FTDI and GUI.

Figure 13. Status strip

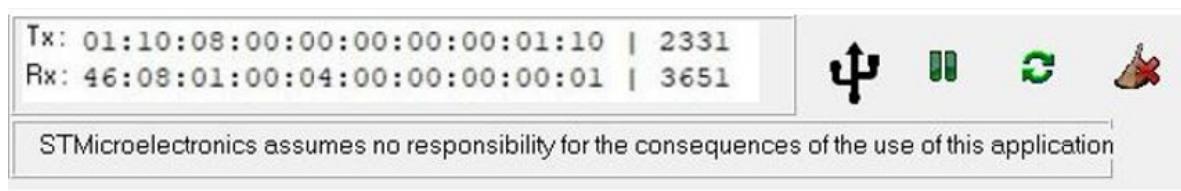


- board not connected
- normal application operation (communication between MCU and GUI correctly established)

3.3 Device diagnostic/communication

It shows SPI traffic detail (Tx and Rx).

Figure 14. Diagnostic/communication panel



Communication interface selection



Enable/Disable periodical reading of status registers and GSB



Refresh all registers (both control and status)

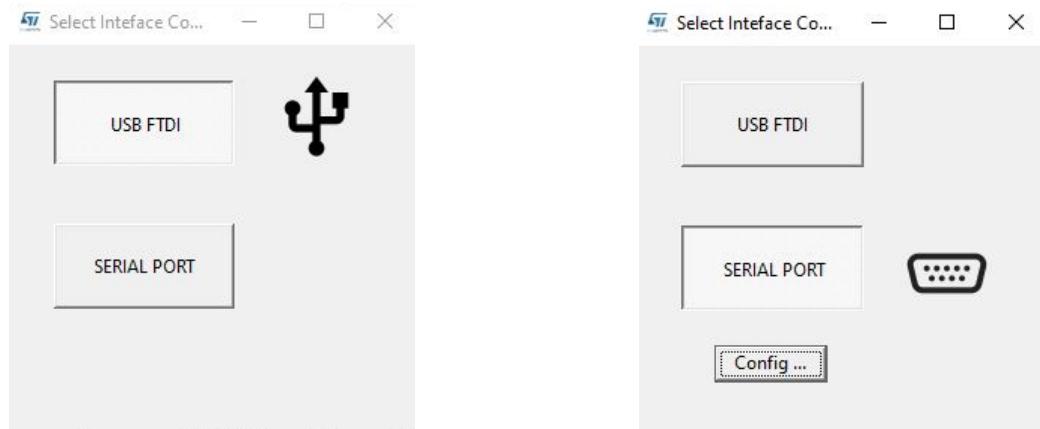


Clear all status registers

Board status section shows the status of the device pin HWLO and DIAG.

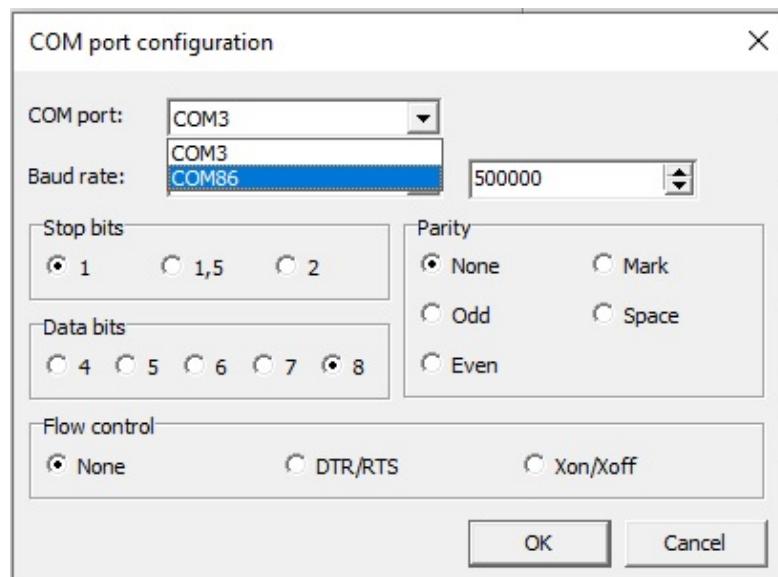
If you choose one of the two communication buttons, described before, an pop-up menu appears where you can choose the FTDI or the serial port communication.

Figure 15. Interface configuration



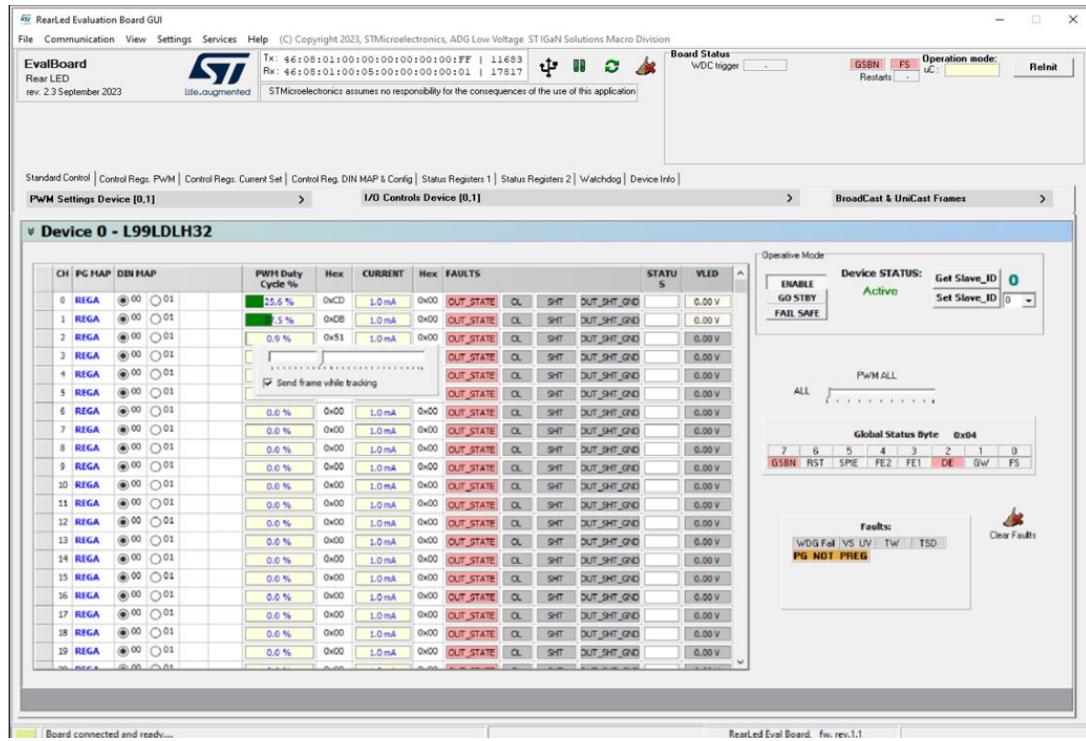
By choosing the serial port option, another pop-up appears to configure the com port. Closing all the pop-up the connection starts automatically.

Figure 16. Com port configuration



3.4 Standard control

Figure 17. Standard control



This main tab shows the main device features, giving the possibility to apply different device modes, enable HS gate, execute self-test, set different thresholds and select diagnostic data to be periodically read and displayed or stopped.

3.4.1 Device control panel

Figure 18. Device control panel

CH	PG MAP	DIN MAP	PWM Duty Cycle %	Hex	CURRENT	Hex	FAULTS	STATU S	VLED
0	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
1	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
2	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
3	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
4	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
5	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
6	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
7	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
8	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
9	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
10	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
11	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
12	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
13	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
14	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
15	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
16	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
17	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
18	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
19	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V
20	REGA	(●) 00 (○) 01	0.0 %	0x00	5.0 mA	0x49	OUT_STATE OL SHT DUT_SHT_GND		0.00 V

This table reports all the channels of the selected device. For each channel you can set:

- DIN MAP
- Duty cycle
- Current

There is also diagnostic info:

- OL (Open load)
- SHT (Short to GND)
- SHT_VPRE (Short to VPreg)
- VLED (V indication)

3.4.2 Operative mode

Figure 19. Operative mode

Operative Mode

Device STATUS: Active	Get Slave_ID: 0
ENABLE GO STBY FAIL SAFE	Set Slave_ID: 0

To change device status use buttons ENABLE, GO STBY and FAIL SAFE. The device ID is managed using the buttons Get or Set Slave_ID.

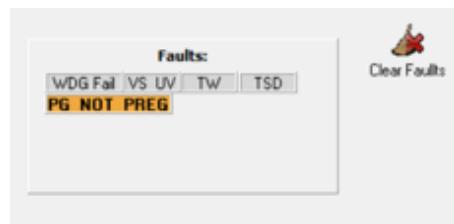
3.4.3 Global status byte

Here is reported the GSB value of the device:

Figure 20. Global status byte

Global Status Byte 0x04							
7	6	5	4	3	2	1	0
GSBN	RST	SPIE	FE2	FE1	DE	GW	FS

Figure 21. Faults



Here are reported the device warnings/errors:

- WDG fail (watchdog error)
- VS UV (undervoltage)
- TW (thermal warning)
- TSD (thermal shutdown)
- PG_NOT PREG (power not good for pre-regulator)

3.4.4 Add/Remove device form

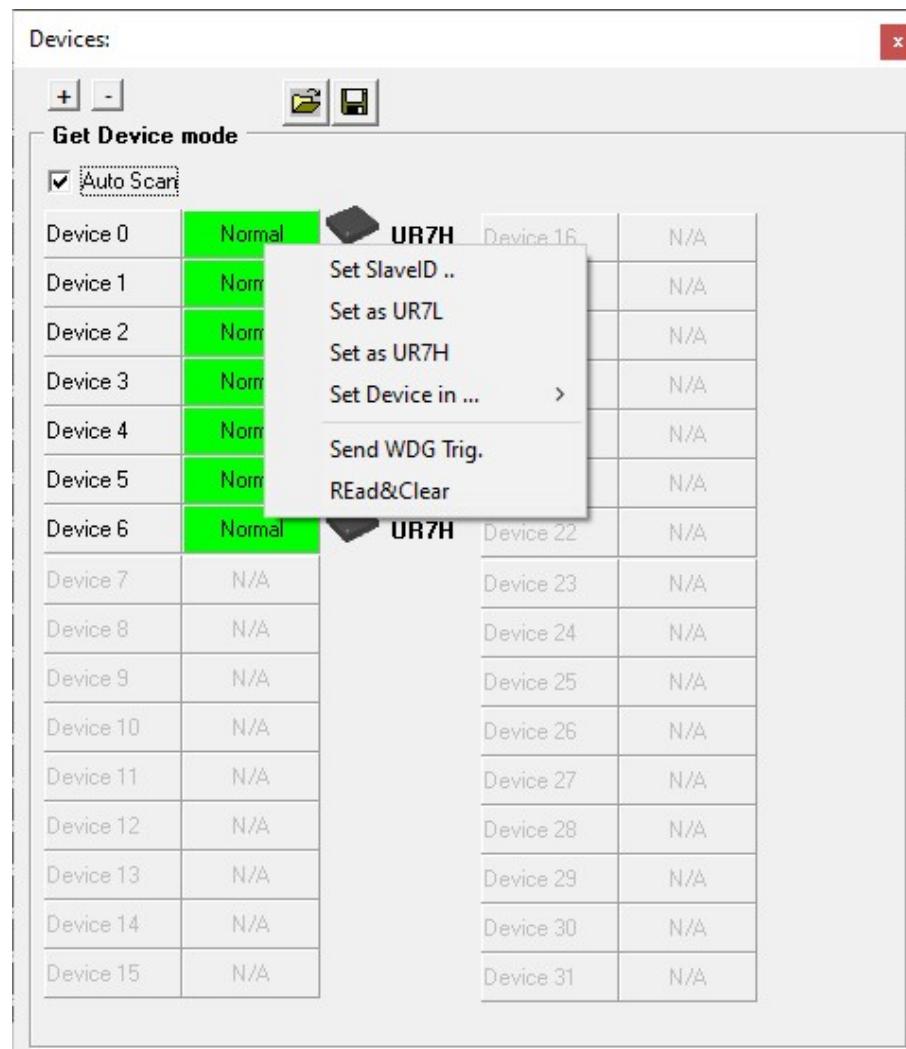
Figure 22. Add/Remove device form



- A new device can be added (+) or removed (-)
- Device status monitored until this checkbox “Autoscan” is checked
- Device status can be in 3 states:
 1. Green (normal mode)
 2. Red (failsafe mode)
 3. Yellow (standby mode)

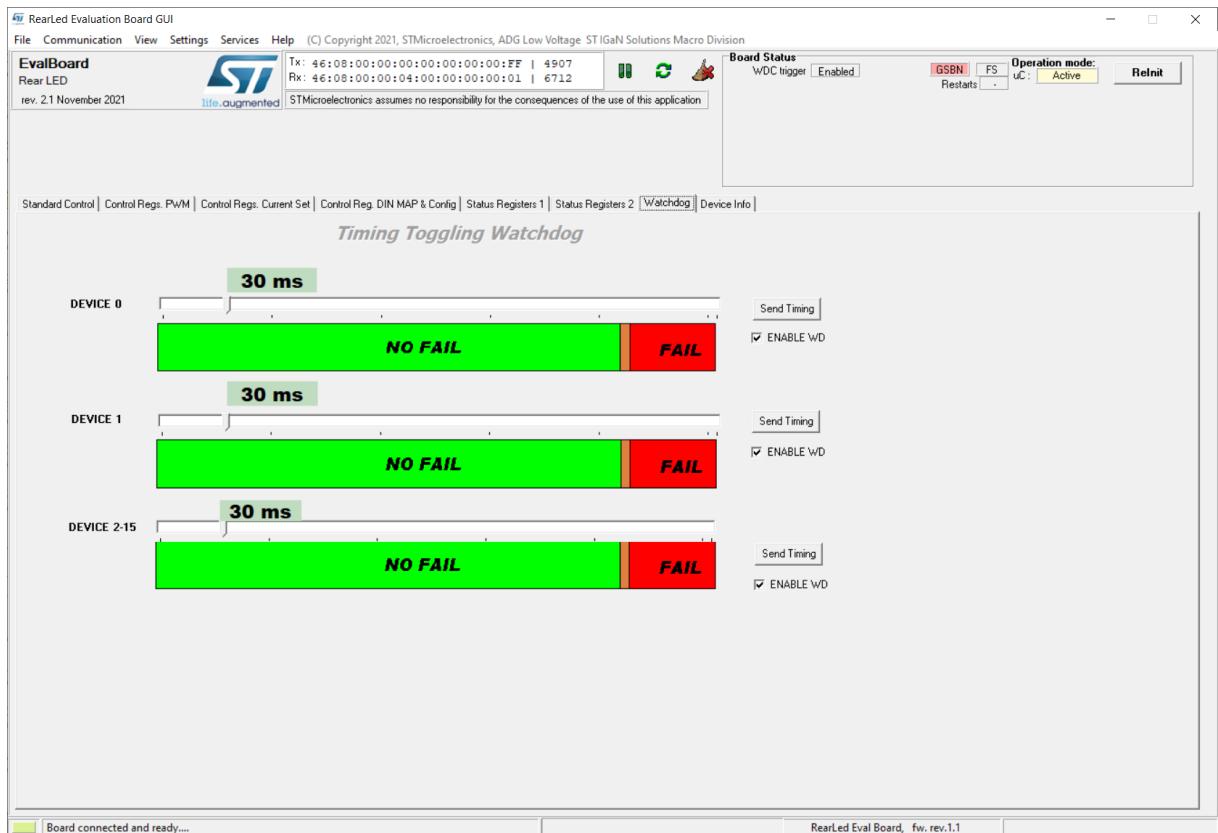
- For each device it can be set (by right click):
 1. Device ID
 2. Type
 3. Set device in normal, failsafe or standby mode
 4. Send watchdog trigger
 5. Read&Clear command

Figure 23. Device setting



3.5 Watchdog

Figure 24. Watchdog



Period for watchdog (WD) serving is adjustable by item “WDG TIME”.

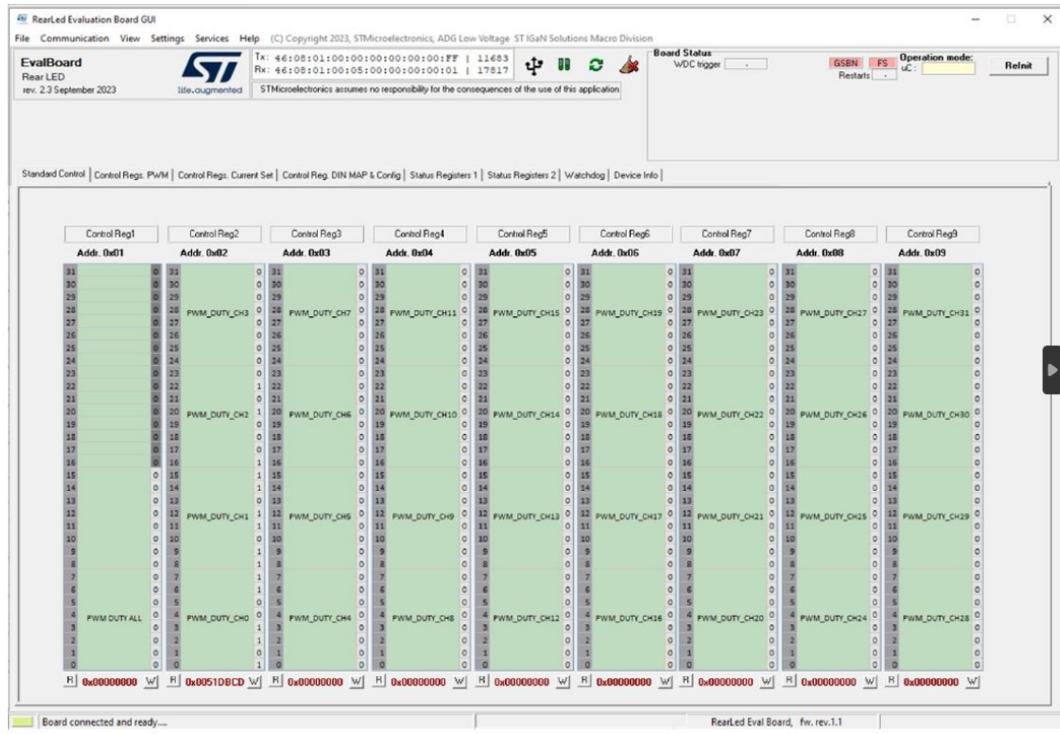
WD serving is applied by refreshing the WD_TRIG bit in one of the control registers.

Enabled WD—enable/disable WD serving by refreshing the WD_TRIG bit

There is also the possibility to set the WD refresh time sent by MCU through a dedicated bar and button (“Send Timing”). This allows the testing of device WD timeout failure.

3.6 Control register page

Figure 25. Control register page



This page displays the control registers for each device selected in the following combo box. It is possible for each column to change the values and read or write new values by clicking the related buttons

R or W

3.7 Status register page

Figure 26. Status register page

L99LDLH32											
Standard Control Control Regs: PWM Control Regs: Current Set Control Reg. DIN MAP & Config Status Registers 1 Status Registers 2 Watchdog Device Info											
Burst Read				Burst Read				Burst Read			
Addr. 0x27	OUT_STATUS	SHT	OL	DUTSHT_VPRE	VLEDON_RFR	STATUS 1	STATUS 2	STATUS 3	FTP_STATUS_1	FTP_STATUS_2	Addr. 0x30
Addr. 0x28	Addr. 0x28	Addr. 0x29	Addr. 0x2A	Addr. 0x2B	Addr. 0x2C	Addr. 0x2D	Addr. 0x2E	Addr. 0x2F			
31 OUT_STATUS_CH31	1 SHT_CH31	0 31 OLC_H31	0 31 OLC_H30	0 31 SHT_VPRE_CH31	0 31 VLEDON_RFR_CH31	0 31 Tj	0 31 NTC_ADC	0 31	0 31 FS_OUT_EN_CH31	0 31 FS_OUT_EN_CH30	0 31 FS_OUT_EN_CH30
30 OUT_STATUS_CH30	1 SHT_CH30	0 30 OLC_H30	0 30 SHT_VPRE_CH30	0 30 VLEDON_RFR_CH30	0 30	0 30 VLEDON_RFR_CH29	0 29	0 30	0 30 FS_OUT_EN_CH29	0 29 FS_OUT_EN_CH29	0 29 FS_OUT_EN_CH29
29 OUT_STATUS_CH29	1 SHT_CH29	0 29 OLC_H29	0 29 SHT_VPRE_CH29	0 29 VLEDON_RFR_CH29	0 29	0 29 Tj	0 29 VLEDON_RFR_CH28	0 28	0 29 FS_OUT_EN_CH28	0 28 FS_OUT_EN_CH28	0 28 FS_OUT_EN_CH28
28 OUT_STATUS_CH28	1 SHT_CH28	0 28 OLC_H28	0 28 SHT_VPRE_CH28	0 28 VLEDON_RFR_CH28	0 28	0 28 VLEDON_RFR_CH27	0 27	0 28 NTC_ADC	0 27 Tj	0 27 VLEDON_RFR_CH27	0 27 FS_OUT_EN_CH27
27 OUT_STATUS_CH27	1 SHT_CH27	0 27 OLC_H27	0 27 SHT_VPRE_CH27	0 27 VLEDON_RFR_CH27	0 27	0 27 VLEDON_RFR_CH26	0 26	0 27	0 27 FS_OUT_EN_CH26	0 26 VLEDON_RFR_CH26	0 26 FS_OUT_EN_CH26
26 OUT_STATUS_CH26	1 SHT_CH26	0 26 OLC_H26	0 26 SHT_VPRE_CH26	0 26 VLEDON_RFR_CH26	0 26	0 26 VLEDON_RFR_CH25	0 25	0 26	0 26 FS_OUT_EN_CH25	0 25 VLEDON_RFR_CH25	0 25 FS_OUT_EN_CH25
25 OUT_STATUS_CH25	1 SHT_CH25	0 25 OLC_H25	0 25 SHT_VPRE_CH25	0 25 VLEDON_RFR_CH25	0 25	0 25 VLEDON_RFR_CH24	0 24	0 25	0 25 FS_OUT_EN_CH24	0 24 VLEDON_RFR_CH24	0 24 FS_OUT_EN_CH24
24 OUT_STATUS_CH24	1 SHT_CH24	0 24 OLC_H24	0 24 SHT_VPRE_CH24	0 24 VLEDON_RFR_CH24	0 24	0 24 VLEDON_RFR_CH23	0 23	0 24	0 24 FS_OUT_EN_CH23	0 23 VLEDON_RFR_CH23	0 24 FS_OUT_EN_CH24
23 OUT_STATUS_CH23	1 SHT_CH23	0 23 OLC_H23	0 23 SHT_VPRE_CH23	0 23 VLEDON_RFR_CH23	0 23	0 23 VLEDON_RFR_CH22	0 22	0 23	0 23 FS_OUT_EN_CH22	0 22 VLEDON_RFR_CH22	0 23 FS_OUT_EN_CH23
22 OUT_STATUS_CH22	1 SHT_CH22	0 22 OLC_H22	0 22 SHT_VPRE_CH22	0 22 VLEDON_RFR_CH22	0 22	0 22 VLEDON_RFR_CH21	0 21	0 22	0 22 FS_OUT_EN_CH21	0 21 VLEDON_RFR_CH21	0 22 FS_OUT_EN_CH22
21 OUT_STATUS_CH21	1 SHT_CH21	0 21 OLC_H21	0 21 SHT_VPRE_CH21	0 21 VLEDON_RFR_CH21	0 21	0 21 VLEDON_RFR_CH20	0 20	0 21	0 21 FS_OUT_EN_CH20	0 20 POR_DELAY	0 21 FS_OUT_EN_CH21
20 OUT_STATUS_CH20	1 SHT_CH20	0 20 OLC_H20	0 20 SHT_VPRE_CH20	0 20 VLEDON_RFR_CH20	0 20	0 20 VLEDON_RFR_CH19	0 19	0 20	0 20 FS_OUT_EN_CH20	0 19 VLEDON_RFR_CH19	0 20 FS_OUT_EN_CH21
19 OUT_STATUS_CH19	1 SHT_CH19	0 19 OLC_H19	0 19 SHT_VPRE_CH19	0 19 VLEDON_RFR_CH19	0 19	0 19 VLEDON_RFR_CH18	0 18	0 19	0 19 FS_OUT_EN_CH19	0 18 WD_CONF	0 19 FS_OUT_EN_CH19
18 OUT_STATUS_CH18	1 SHT_CH18	0 18 OLC_H18	0 18 SHT_VPRE_CH18	0 18 VLEDON_RFR_CH18	0 18	0 18 VLEDON_RFR_CH17	0 17	0 18	0 18 FS_OUT_EN_CH18	0 17 WD_CONF	0 18 FS_OUT_EN_CH18
17 OUT_STATUS_CH17	1 SHT_CH17	0 17 OLC_H17	0 17 SHT_VPRE_CH17	0 17 VLEDON_RFR_CH17	0 17	0 17 VLEDON_RFR_CH16	0 16	0 17	0 17 FS_OUT_EN_CH17	0 17 REF_PRE_REG_MAV	0 17 FS_OUT_EN_CH17
16 OUT_STATUS_CH16	1 SHT_CH16	0 16 OLC_H16	0 16 SHT_VPRE_CH16	0 16 VLEDON_RFR_CH16	0 16	0 16 VLEDON_RFR_CH15	0 15	0 16	0 16 FS_OUT_EN_CH16	0 16 PWM_FS_ALL_EN	0 16 FS_OUT_EN_CH16
15 OUT_STATUS_CH15	1 SHT_CH15	0 15 OLC_H15	0 15 SHT_VPRE_CH15	0 15 VLEDON_RFR_CH15	0 15	0 15 VLEDON_RFR_CH14	0 14	0 15	0 15 FS_OUT_EN_CH15	0 15 WD_FAULT	0 15 FS_OUT_EN_CH15
14 OUT_STATUS_CH14	1 SHT_CH14	0 14 OLC_H14	0 14 SHT_VPRE_CH14	0 14 VLEDON_RFR_CH14	0 14	0 14 VLEDON_RFR_CH13	0 13	0 14	0 14 FS_OUT_EN_CH14	0 14 VS_UV	0 14 FS_OUT_EN_CH14
13 OUT_STATUS_CH13	1 SHT_CH13	0 13 OLC_H13	0 13 SHT_VPRE_CH13	0 13 VLEDON_RFR_CH13	0 13	0 13 VLEDON_RFR_CH12	0 12	0 13	0 13 FS_OUT_EN_CH13	0 13 VLEDON_RFR_CH12	0 13 FS_OUT_EN_CH13
12 OUT_STATUS_CH12	1 SHT_CH12	0 12 OLC_H12	0 12 SHT_VPRE_CH12	0 12 VLEDON_RFR_CH12	0 12	0 12 VLEDON_RFR_CH11	0 11	0 12	0 12 FS_OUT_EN_CH12	0 12 WD_STATUS	0 12 FS_OUT_EN_CH12
11 OUT_STATUS_CH11	1 SHT_CH11	0 11 OLC_H11	0 11 SHT_VPRE_CH11	0 11 VLEDON_RFR_CH11	0 11	0 11 VLEDON_RFR_CH10	0 10	0 11	0 11 FS_OUT_EN_CH11	0 11 DIN_STATUS	0 11 FS_OUT_EN_CH11
10 OUT_STATUS_CH10	1 SHT_CH10	0 10 OLC_H10	0 10 SHT_VPRE_CH10	0 10 VLEDON_RFR_CH10	0 10	0 10 VLEDON_RFR_CH9	0 9	0 10	0 10 FS_OUT_EN_CH10	0 9 NTC_FAULT	0 10 FS_OUT_EN_CH10
9 OUT_STATUS_CH9	1 SHT_CH9	0 9 OLC_H9	0 9 SHT_VPRE_CH9	0 9 VLEDON_RFR_CH9	0 9	0 9 VLEDON_RFR_CH8	0 8	0 9	0 9 FS_OUT_EN_CH9	0 8 NTC_DER_ACT	0 9 FS_OUT_EN_CH9
8 OUT_STATUS_CH8	1 SHT_CH8	0 8 OLC_H8	0 8 SHT_VPRE_CH8	0 8 VLEDON_RFR_CH8	0 8	0 8 VLEDON_RFR_CH7	0 7	0 8	0 8 FS_OUT_EN_CH8	0 7 OR_COL	0 8 FS_OUT_EN_CH8
7 OUT_STATUS_CH7	1 SHT_CH7	0 7 OLC_H7	0 7 SHT_VPRE_CH7	0 7 VLEDON_RFR_CH7	0 7	0 7 VLEDON_RFR_CH6	0 6	0 7	0 7 FS_OUT_EN_CH7	0 6 OR_SHT	0 6 FS_OUT_EN_CH6
6 OUT_STATUS_CH6	1 SHT_CH6	0 6 OLC_H6	0 6 SHT_VPRE_CH6	0 6 VLEDON_RFR_CH6	0 6	0 6 VLEDON_RFR_CH5	0 5	0 6	0 6 FS_OUT_EN_CH6	0 5 OR_OUTSHT_VPRE	0 5 FS_OUT_EN_CH5
5 OUT_STATUS_CH5	1 SHT_CH5	0 5 OLC_H5	0 5 SHT_VPRE_CH5	0 5 VLEDON_RFR_CH5	0 5	0 5 VLEDON_RFR_CH4	0 4	0 5	0 5 FS_OUT_EN_CH5	0 4 WM_DUTY_ALL_AL	0 4 FS_OUT_EN_CH4
4 OUT_STATUS_CH4	1 SHT_CH4	0 4 OLC_H4	0 4 SHT_VPRE_CH4	0 4 VLEDON_RFR_CH4	0 4	0 4 VLEDON_RFR_CH3	0 3	0 4	0 4 FS_OUT_EN_CH4	0 3 TW	0 4 FS_OUT_EN_CH3
3 OUT_STATUS_CH3	1 SHT_CH3	0 3 OLC_H3	0 3 SHT_VPRE_CH3	0 3 VLEDON_RFR_CH3	0 3	0 3 VLEDON_RFR_CH2	0 2	0 3	0 3 FS_OUT_EN_CH3	0 2 TSD	0 3 FS_OUT_EN_CH2
2 OUT_STATUS_CH2	1 SHT_CH2	0 2 OLC_H2	0 2 SHT_VPRE_CH2	0 2 VLEDON_RFR_CH2	0 2	0 2 VLEDON_RFR_CH1	0 1	0 2	0 2 FS_OUT_EN_CH2	0 1 PG_NOT_VPRE	0 2 FS_OUT_EN_CH1
1 OUT_STATUS_CH1	1 SHT_CH1	0 1 OLC_H1	0 1 SHT_VPRE_CH1	0 1 VLEDON_RFR_CH1	0 1	0 1 VLEDON_RFR_CH0	0 0	0 1	0 1 FS_OUT_EN_CH1	0 0 PG_NOT_VPRE	0 1 FS_OUT_EN_CH0
0 OUT_STATUS_CH0	1 SHT_CH0	0 0 OLC_H0	0 0 SHT_VPRE_CH0	0 0 VLEDON_RFR_CH0	0 0	0 0	0 0	0 0	0 0	0 0	0 0

This page displays the status registers for each device that you have selected in the following combo box



It is possible to read 4 status registers at the same time by clicking "Burst Read" button



is possible to read or clear some registers by clicking the related buttons



3.8

Device info

The form below shows the device ROM and can be refreshed with the dedicated button, and details about all the devices info stored in ROM:

- UR7H for L99LDLH32
 - UR7L for L99LDLL16

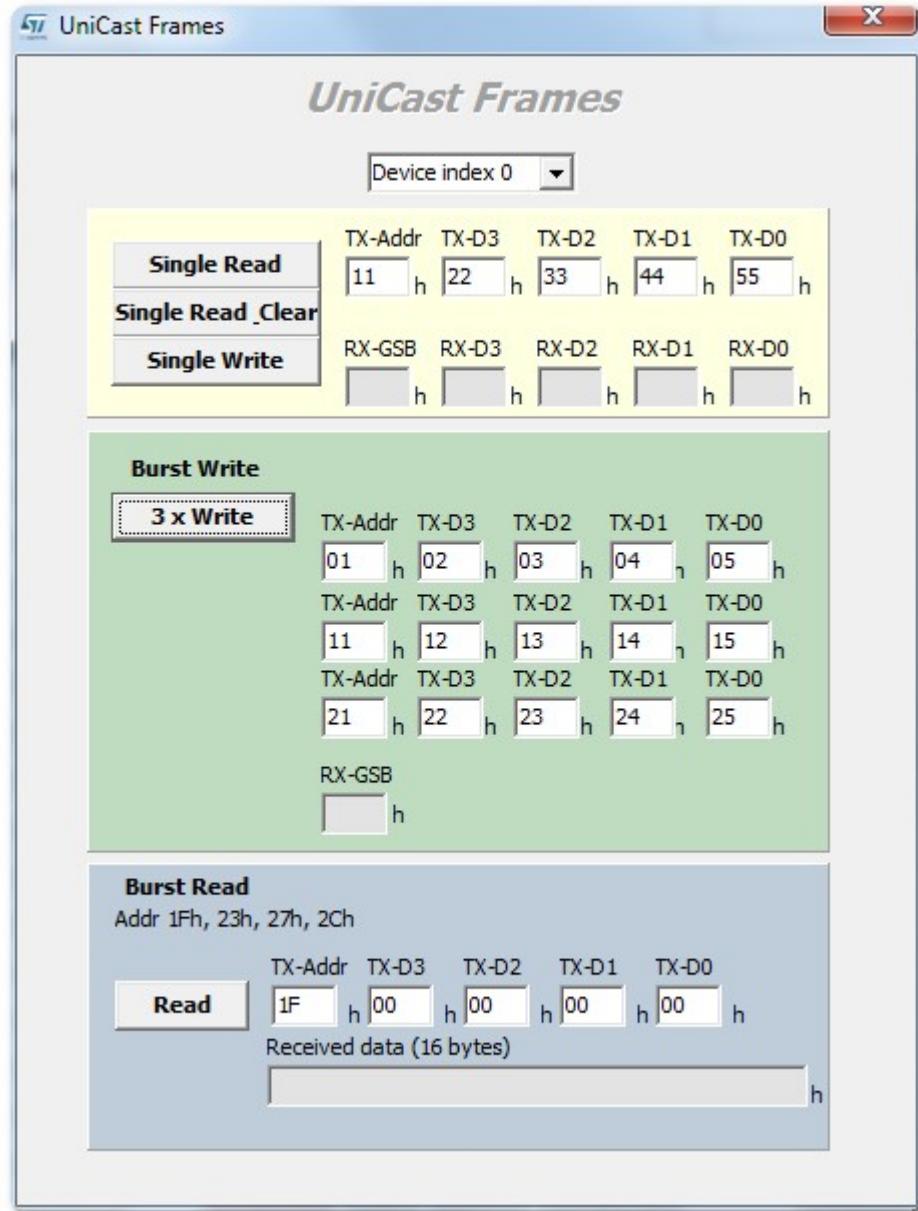
Figure 27. ROM memory map

DEVICE	
ROM Memory Map Dev0 — UR7H	
Adr: 0x3E	GSB Options
0 0 0 0 0 0 0 0	0x00
<input type="button" value="Refresh"/>	
Adr: 0x20	SPI CPHS test
0 1 0 1 0 1 0 1	0x55
Adr: 0x16	WD bit pos. 4
0 0 0 0 0 0 0 0	0x00
Adr: 0x15	WD bit pos. 3
0 0 0 0 0 0 0 0	0x00
Adr: 0x14	WD bit pos. 2
1 1 0 0 0 0 0 0	0xC0
Adr: 0x13	WD bit pos. 1
0 1 1 0 0 1 0 1	0x65
Adr: 0x12	WD Type 2
0 0 0 0 0 0 0 0	0x00
Adr: 0x11	WD Type 1
0 1 0 0 1 0 1 0	0x4A
Adr: 0x10	SPI mode
0 1 0 0 0 0 0 0	0x40
Adr: 0x0A	Silicon Ver.
0 0 0 0 0 0 1 0	0x02
Adr: 0x05	Device No. 4
0 1 0 0 1 0 0 0	0x48
Adr: 0x04	Device No. 3
0 0 0 0 0 1 1 1	0xD7
Adr: 0x03	Device No. 2
0 1 0 1 0 0 1 0	0x52
Adr: 0x02	Device No. 1
0 1 0 1 0 1 0 1	0x55
Adr: 0x01	Device Family
0 0 0 0 0 0 1 0	0x02
Adr: 0x00	Company Code
0 0 0 0 0 0 0 0	0x00

3.9 BroadCast

The user can send a broadcast CAN frame to devices connected to the same chain setting current or duty cycle through the below dialog box.

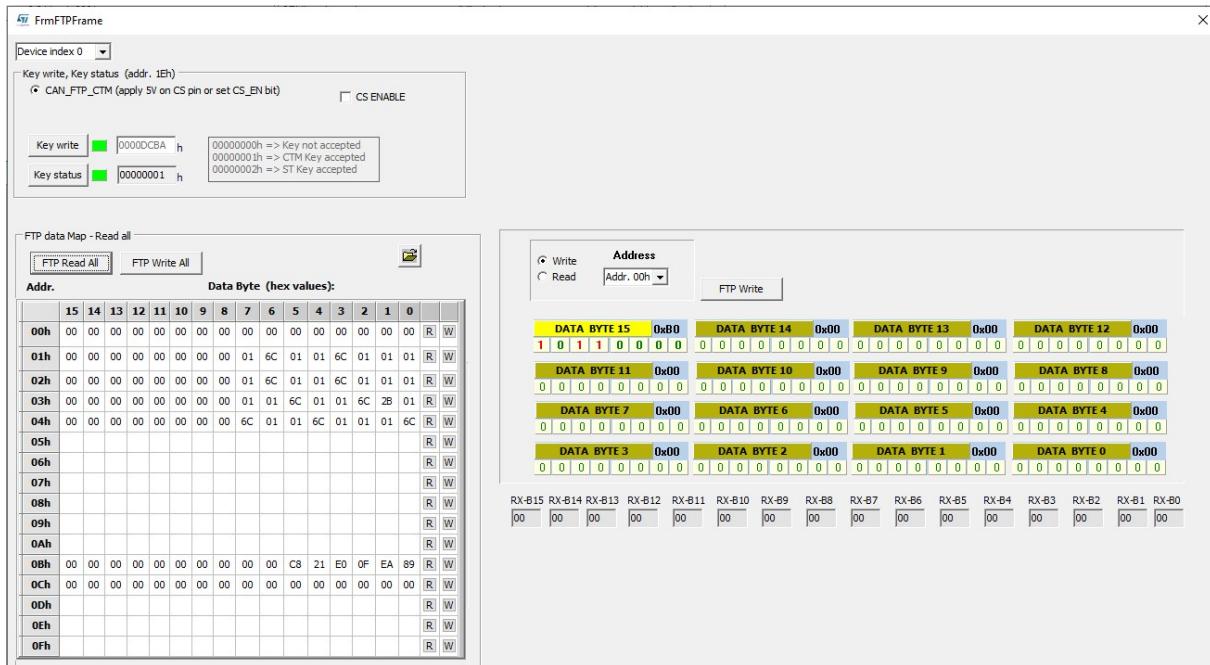
Figure 28. BroadCast CAN frame



3.10 FTP programming dialog

The user can access the Non-volatile Memory (NVM) section of the selected device through the below dialog box. The user can read or write one or more memory sectors modifying single or multiple bytes.

Figure 29. FTP programming dialog



Revision history

Table 1. Document revision history

Date	Revision	Changes
16-Sep-2022	1	Initial release.
25-Jun-2024	2	Updated Figure 1. STSW-EVLDLH32GEN graphical user interface, Figure 10. Tabs for device control, Section 3.1: Main menu, Section 3.3: Device diagnostic/communication, Figure 17. Standard control and Figure 25. Control register page.

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