MIPI A-PHY EOS protection in automotive applications

Introduction

MIPI A-PHY is a single or differential lane, point-to-point, serial interface designed for a wide range of long reach links. It is specifically used in automotive applications.

This physical layer carries multiple protocols from the MIPI alliance such as CSI-2 for image sensors, DSI, and DSI-2 for displays, with the help of an adaptation layer.

Non-MIPI protocols are also supported using a generic “Data link layer interface.”

MIPI A-PHY is designed to simplify the integration of cameras, sensors, and displays. It is also incorporating functional safety and security in automotive.

This application note presents the context of the various electrical and electromagnetic constraints in the automotive environment. It also gives an overview of the MIPI A-PHY electrical features, and electrical test specifications.

Finally, ST’s offer in ESD protection and filtering for MIPI A-PHY is presented.

1 Electrical hazards in the automotive environment

The automotive environment is the source of many electrical hazards: electromagnetic interferences or electrostatic discharges. Ignition, relay contacts, alternator, injectors, and others accessories generate these hazards, and other electrical disturbances.

These hazards can occur:

- Directly in the wiring harness in case of conducted disturbances
- Indirectly to the electronic modules by radiation.

These generated hazards can impact electronics in two ways depending on the environment:

- On the data lines
- On the supply rail wires.

In the rest of this section, we are only considering the impacts on the data lines.

For impacts on supply lines, more information can be found in AN2689.

Related links

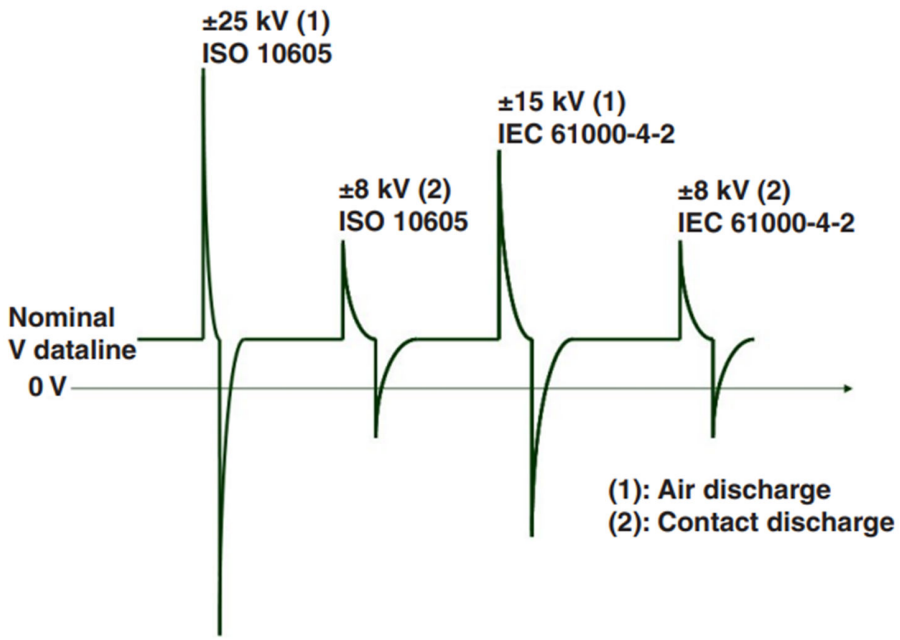
See AN2689 for more information.

1.1 Propagation of electrical hazards on data lines

Transients that are generated on data lines are mainly ESD surges. They feature a low energy but feature a very high dv/dt. It can then generate a strong electromagnetic field. The ISO 10605 and IEC 61000-4-2 standards define the ESD surges. The data lines concerned are communication lines: media transfer lines, video links, data buses, sensor data lines and so on.

Figure below shows the surge forms of hazards that can be found on data lines.

Figure 1. Kind of surge on data lines



ESD surge test is applied to a complete system. This is simulating the ESD occurring on an electronic module due to a human body contact or connector plugin, for example.

1.2 Standards for the protection of automotive electronics

Several standards bodies such as the society of automobile engineers (SAE), the automotive electronic council (AEC), and the international standard organization (ISO) describe the hazards indicated above.

The ISO 10605 and the ISO 7637 are the most important automotive standards regarding electrical hazards.

Regarding the MIPI A-PHY standard, a high level of electromagnetic immunity is specified for RF ingress (ISO 11452-2), BCI (ISO 11452-4), and fast transient (ISO 7637-2/3) stress.

2 MIPI A-PHY: How does it work?

2.1 Overview of architecture

Figure 2. Data and power structure

MIPI A-PHY link is composed of one coaxial line, or one differential lane: it is bidirectional and can carry power supply.

The main unidirectional data stream is transmitted through a high-speed **downlink**, which supports multiple 4K cameras, image sensors and displays. Command and control data are provided by the **uplink**, which is composed by a bidirectional low throughput up to 200 Mbps.

Finally, peripheral units can be powered over a data line, which is an optional feature.

A-PHY support two profiles:

- The profile 1 targets lower downlink speeds and lower complexity implementations. It uses channel attributes and design characteristics that enable lower cost implementations. Profile 1 is based on NRZ 8B/10B technology.
- The profile 2 targets solutions requiring superior noise immunity and higher downlink speeds. It also has a better bandwidth utilization (that is net data rate per gear). Profile 2 is based on pulse amplitude modulation (PAM) technology.

Table 1. NRZ 8B/10B versus PAM technology

Profile 1 (P1): NRZ 8B/10B technology	Profile 2 (P2): PAM technology
Easier to implement technology	Higher EMC immunity
Lower cost technology	Higher downlink speeds
Lower downlink speeds	More expensive and complex technology to implement

MIPI A-PHY is composed by multiple speed gears ranging from 2 Gbps up to 16 Gbps per lane.

The Table 2 and Table 3 shows five gear configurations with data rates and profile used by each one. Devices must be compatible with the Table 2 and optionally with the Table 3.

Table 2. MIPI A-PHY gears per profiles (mandatory)

Gear rate	Modulation	Symbole rate (GBaud)	Max net app data rate (Gbps)
G1 2 Gbps	NRZ-8B/10B	2	1.5
G2 4 Gbps	NRZ-8B/10B	4	3
G3 8 Gbps	PAM4	4	7.2
G4 12 Gbps	PAM8	4	10.8
G5 16 Gbps	PAM16	4	14.4

Table 3. MIPI A-PHY gears per profiles (optional)

Gear rate	Modulation	Symbole rate (GBaud)	Max net app data rate (Gbps)
G1 2 Gbps	PAM4	1	1.8
G2 4 Gbps	PAM4	2	3.6
G3 8 Gbps	NRZ-8B/10B	8	6

In the Table 4, we have the nominal amplitude levels for downlink and uplink per gear.

Table 4. Nominal T_X amplitude over coax, per gear, per direction

Gear	Nominal downlink amplitude (mV_{PP})	Nominal uplink amplitude (mV_{PP})
1	250	500
2	350	500
3	250	500
4	500	250
5	500	250
Exception case for optional mode G3, 8 Gbps, 8B/10B NRZ:		
3	500	500

2.2 Interconnect specifications

The interconnect between an A-PHY source and an A-PHY sink carries the high-speed uni-directional data stream. The low-speed bidirectional command and control data and optionally the power supply to an end unit.

A-PHY is defined for three different cable topologies as shown below:

- Unbalanced coax cables:

Figure 3. Coaxial cable

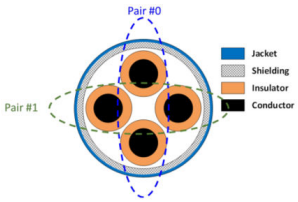
- Balanced cables like a shielded differential pair (SDP):

Figure 4. SDP

- Star quad Cable (STQ):

Star quad cable is composed of four conductors arranged as two differential pairs as shown below.

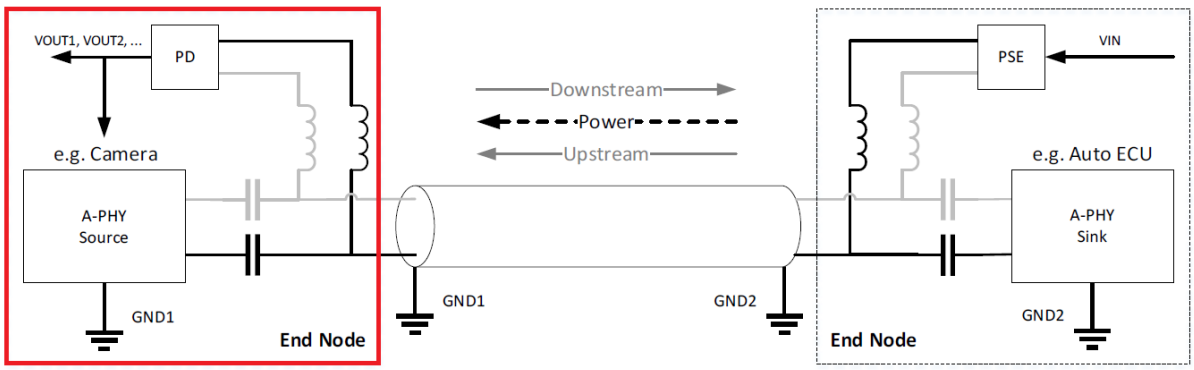
Figure 5. Four conductors arranged as two differential pairs



The complete physical connection of a lane consists of two end nodes with a transmission-line interconnect-structure (TLIS) in between.

An end node (framed in red below) comprises an A-PHY transceiver and an end-node interconnect-structure (ENIS). The TLIS between end nodes may be formed by cable segments (cable TLIS).

Figure 6. A-PHY interconnect



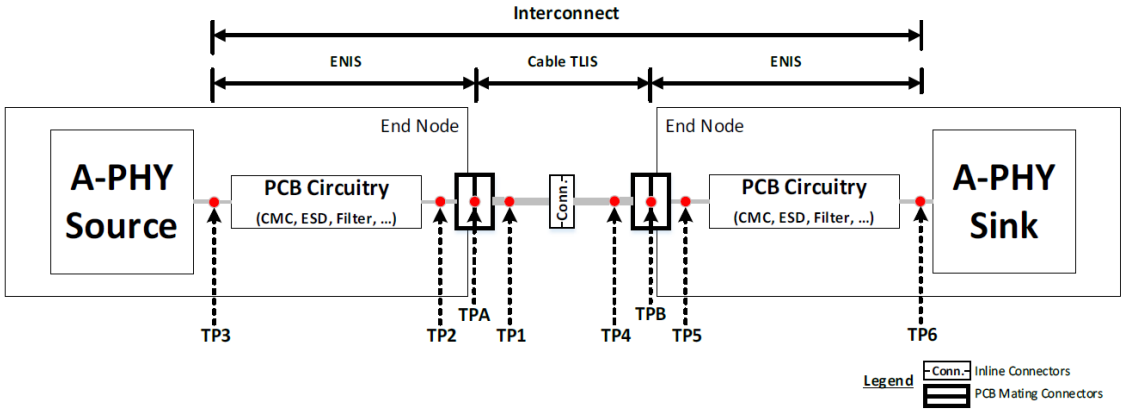
A capacitive coupling is present to ensure that the power supply does not go into the source or the sink. Finally, inductors prevent data from going into the power supply.

2.3 ENIS and S-parameters

The end-node-interconnect-structure (ENIS) is composed of:

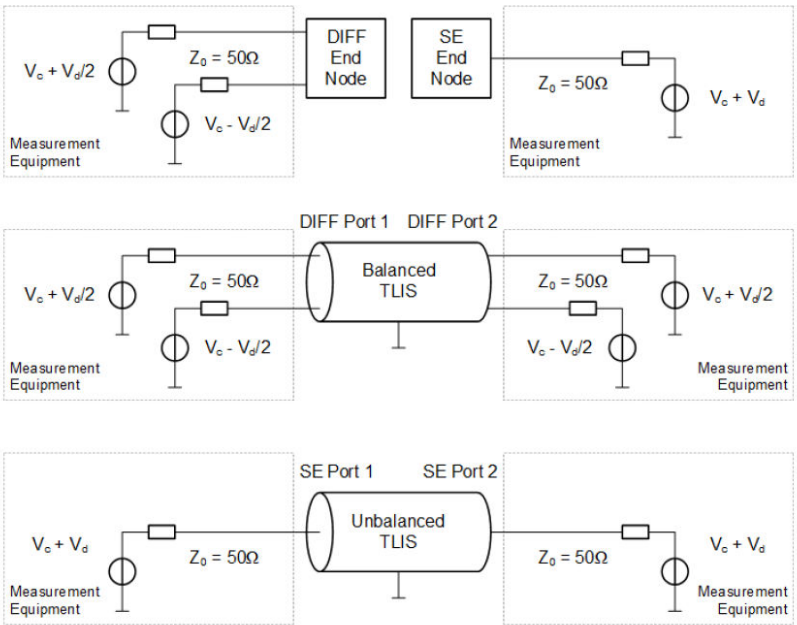
- PCB traces as well as any related vias
- Supporting circuitry for ESD protection
- Power feed
- Diplexer including AC caps
- Other signal conditioning functions.

Figure 7. Interconnect test points definition



All S-parameters for ENIS are measured at TPA and/or TPB point.

Figure 8. Set-up for S-parameter characterization



The nominal characteristic impedance of coax cable is 50 Ω and the nominal differential characteristic impedance of SDP/STQ cable is 100 Ω.

A-PHY links may include an optional power feed established between a PSE and PD using the same cable TLIS as the data and control streams.

3 MIPI A-PHY insertion losses, return losses, and eye-diagrams specifications

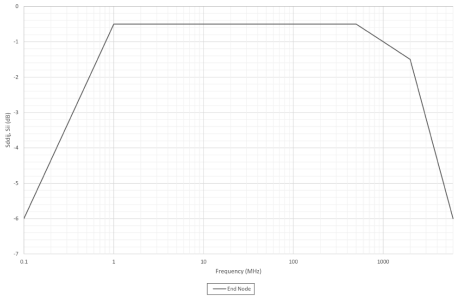
Eye-diagrams, insertion losses, and return losses are defined for the end-node-interconnect-structure in a MIPI A-PHY standard. These parameters are important to ensure a good signal integrity.

All these requirements are applied to both coaxial and differential pairs. The S-parameter limits are defined up to a maximum frequency of 6 GHz.

3.1 Insertion losses and return loss

A-PHY implementation must respect below ENIS insertion losses, for all gears.

Figure 9. End node insertion loss limit



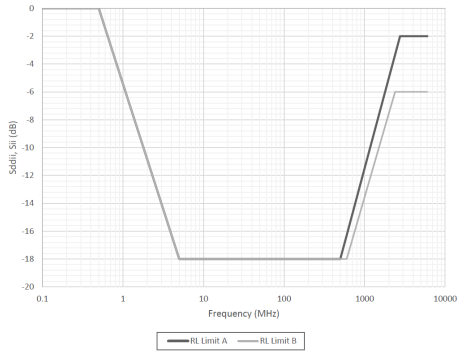
S_{DD21} or S_{21} insertion loss limits:

- -6 dB DC
- -0.5 dB from 1 to 500MHz
- -1 dB at 1 GHz
- -1.5 dB at 2 GHz
- -3 dB at 2.9 GHz
- -6 dB at 6 GHz

A-PHY implementation must respect below return losses.

The return loss limit B concerns Gear 3 in NRZ8B10B mode, and all other modes must comply with R_L limit A.

Figure 10. End node return loss limits



S_{DD11} and S_{DD22} or S_{11} and S_{22} return loss limits:

- -18 dB from 5 to 500 MHz
- Around -12 or -14 dB at 1GHz

3.2 Eye diagrams

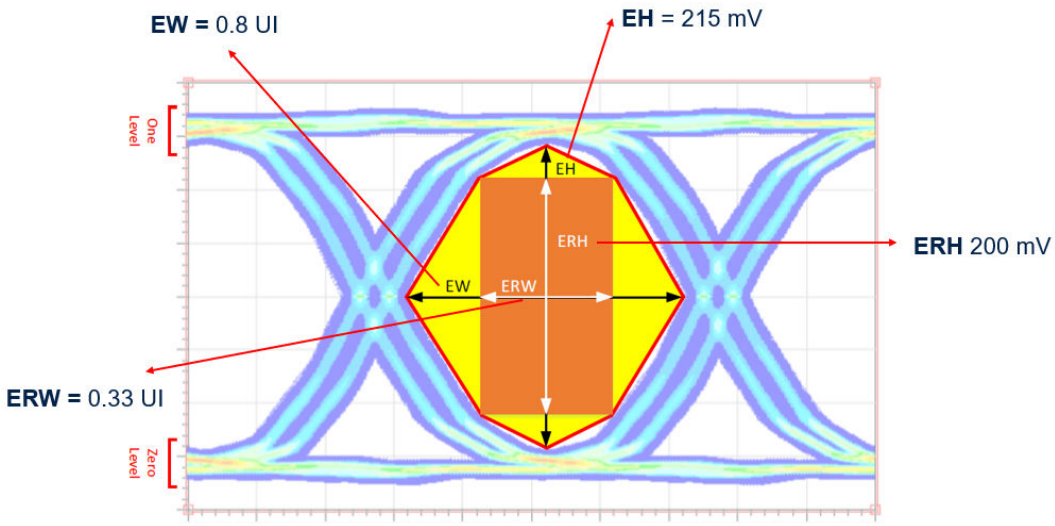
The signal quality transmission is evaluated through eye diagram measurement. MIPI A-PHY standard defines the eye diagram mask function of Gear data rate for NRZ-8B/10B technology. Eye diagrams are measured at TPA and/or TPB points.

Table 5. NRZ downlink eye mask parameters

NRZ downlink	EW (UI)	EH (mV)	ERW (UI)	ERH (mV)
Gear 1	0.80	215	0.33	200
Gear 2	0.80	280	0.40	220
Gear 3 (optional)	0.65	290	0.42	200

An example of eye diagram mask levels and timings is shown below: it is for gear 1 with a nominal downlink amplitude of 250 mV peak to peak.

Figure 11. NRZ downlink transmitter eye diagram



As ESD protection and common mode filter are part of ENIS, these components must be compliant with the above specifications.

4 ST offering for ESD protection

In ST's product offer, you can find some ESD protections devices compatible with the MIPI A-PHY standard.

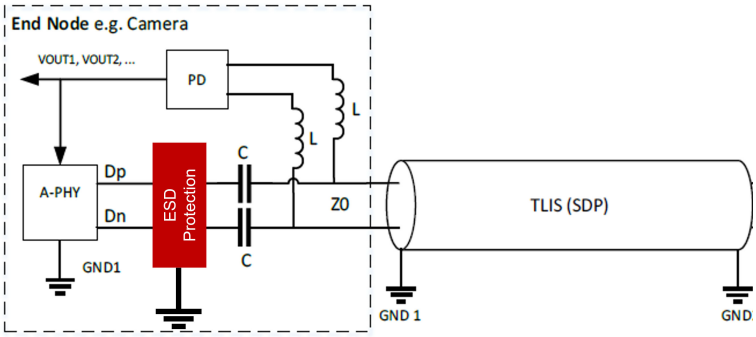
For ESD protections, the placement at the connector should always be preferred. As the DC bias voltage is canceled by an AC capacitor, only the data signal levels need to be considered.

The tracks between the ESD protection device and the line to be protected must be also as short as possible to minimize the inductor effect on clamping voltage value. The same rule applies between the protection device and the ground plane.

Indeed, the track parasitic inductor adds an extra voltage to the clamping voltage of the ESD protection device.

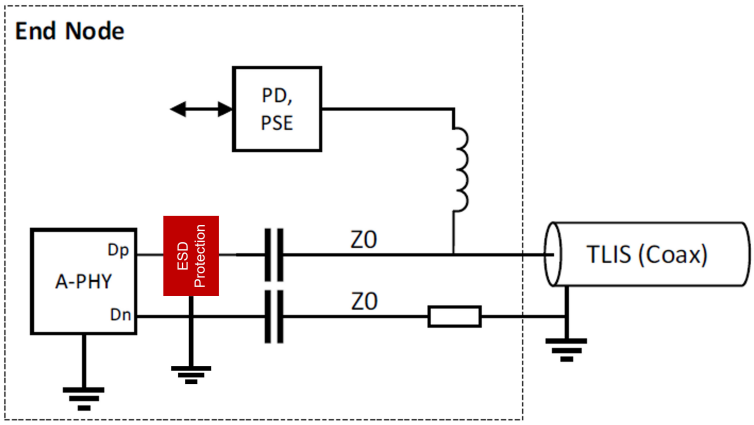
For more details, see AN5686. (PCB layout tips to maximize ESD protection efficiency).

Figure 12. ESD protection implementation on a differential system



Our ESD protections devices can be used on differential lines as well as on coaxial lines.

Figure 13. ESD protection implementation on a single-ended system



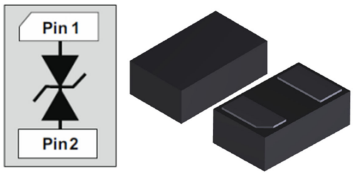
According to MIPI A-PHY characteristics, shown above, ESD protection requirements are:

- Unidirectional/Bidirectional devices are suitable.
- The capacitance of the product needs to be lower than 0.8 pF to be compliant with eye-diagrams and insertion losses specifications
- $V_{RM} \geq 1$ V
- ESD robustness versus ISO 10605 and IEC 61000-4-2 standards.

4.1 ESDAXLC6-1BT2Y

ESDAXLC6-1BT2Y is a single line ESD device designed for high-speed lines protection.

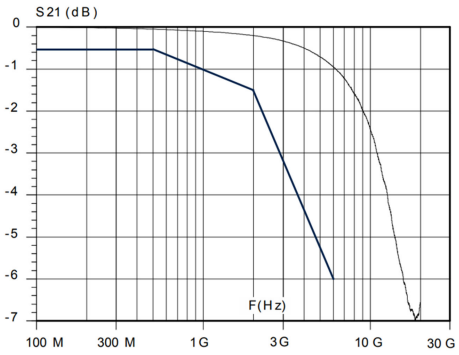
Figure 14. ESDAXLC6-1BT2Y functional schematic and package (0402)



With a capacitance lower than 0.5 pF and a high robustness against ESD stress, this product can fully meet the MIPI A-PHY standard.

The blue curve shows the MIPI A-PHY insertion losses requirements S21, and the dark curve shows the ESDAXLC6-1BT2Y S21 measurement.

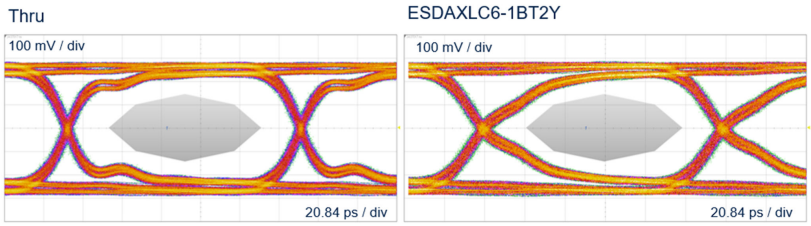
Figure 15. ESDAXLC6-1BT2Y insertion loss versus MIPI A-PHY requirements



As specified in the standard, it must be compliant with three eye-diagrams masks (gear 1, gear 2, and gear 3 for NRZ 8B/10B signals.)

Below eye diagrams show the compliancy of the ESDAXLC6-1BT2Y with gear 3, at 8 Gbps template. The figure on the left is performed on a thru (that is without component) and on the right the signal injected with an ESDAXLC6-1BT2Y.

Figure 16. ESDAXLC-1BT2Y MIPI A-PHY eye-diagram for gear 3 at 8 Gbps



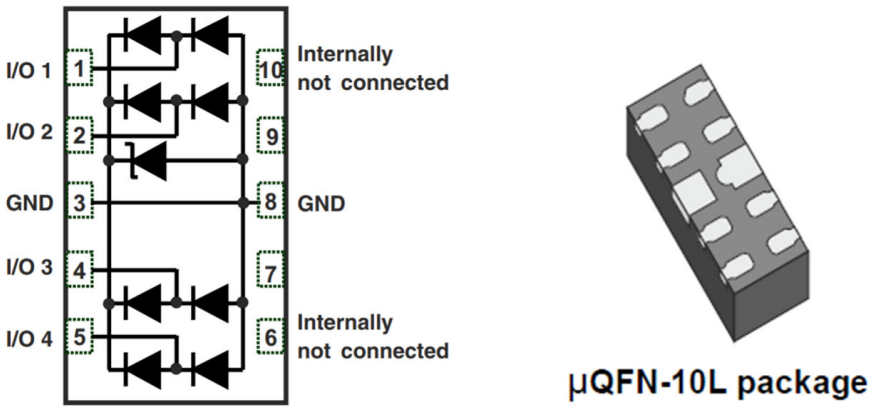
Related links

See ESDAXLC6-1BT2Y.

4.2 HSP061-4M10Y

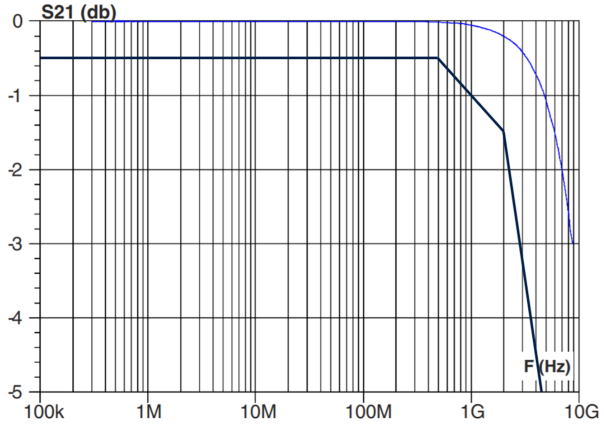
HSP061-4M10Y is a four-line ESD device designed for high-speed lines protection.

Figure 17. HSP061-4M10Y functional schematic and package



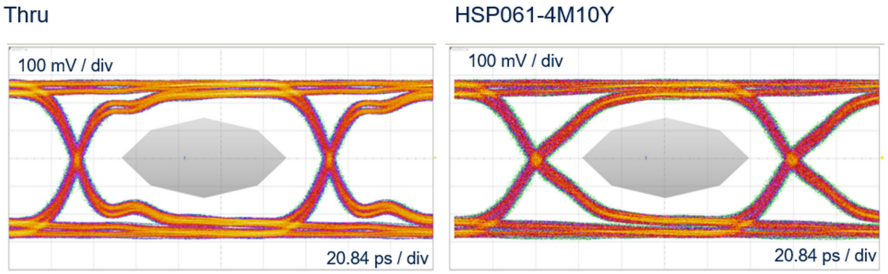
As shown below, HSP061-4M10Y S21 are compliant with MIPI A-PHY ENIS insertion losses.

Figure 18. HSP061-4M10Y insertion loss vs MIPI A-PHY requirements



Below eye-diagrams show the compliancy of HSP061-4M10Y with gear 3, at 8 Gbps template.

Figure 19. HSP061-4M10Y MIPI A-PHY eye-diagram for gear 3 at 8 Gbps



Related links

See HSP061-4M10Y.

5 ST offering for filtering and protection (ECMF)

An ECMF is a common-mode filter, which integrates an ESD protection die.

First of all, why do we need to use a common filter?

There are more high-speed lines and antennas in the automotive environment. These high-speed transmission lines generate frequencies harmonics.

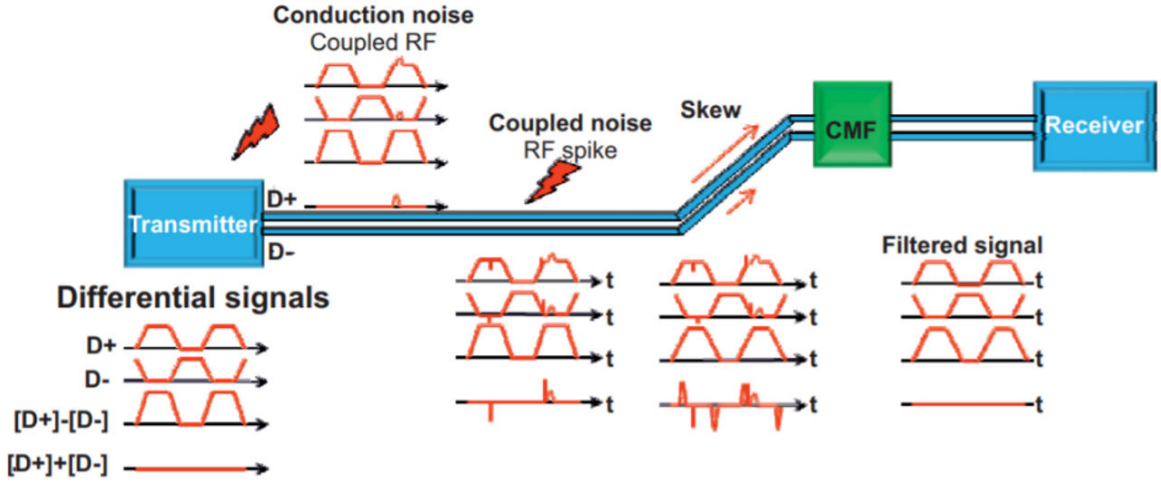
If the transmission generates parasitic frequencies or harmonics similar to the frequency the antenna is receiving, the useful signal will be mixed by coupling to the disturbing signal.

If the disturbing signal amplitude is too high in comparison to the useful signal, the receiver will not be able to get the useful signal.

On this case, we have the antenna desense phenomenon and we must filter the parasitic signal to ensure that the wanted signal is received correctly (for more details, see AN4356, antenna desense on handheld equipment). Filtering a differential high-speed line avoids its radiation, so avoid the antenna desense phenomenon.

In an embedded system, there is a multitude of high-speed digital clocks and skews, which can create some disturbances on the data signals (disturbances created by fast switching of clocks, phase shift between positive and negative data created by skew for example): these are responsible of the differential line radiations.

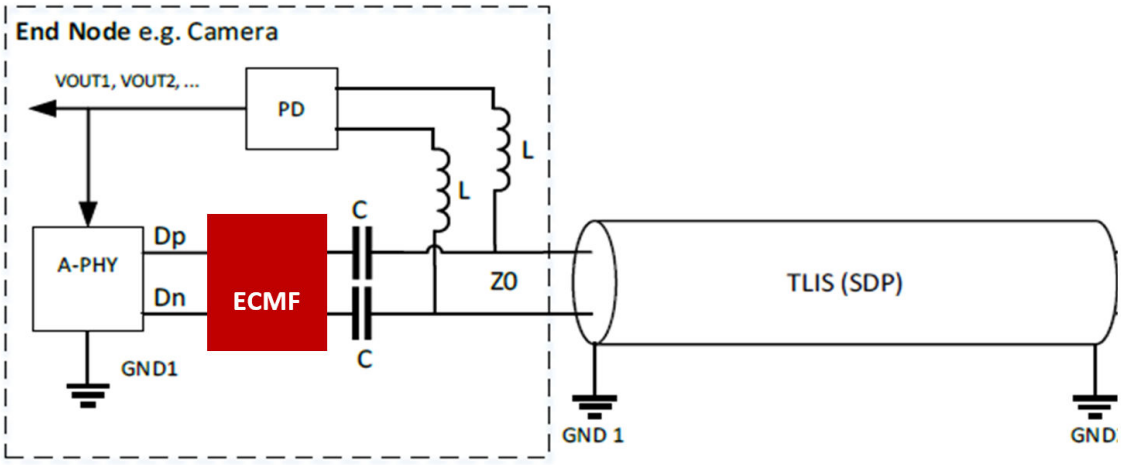
Figure 20. Common-mode filters and disturbances on a differential link



For more details on common-mode filters, see **AN4511**, common-mode filters.

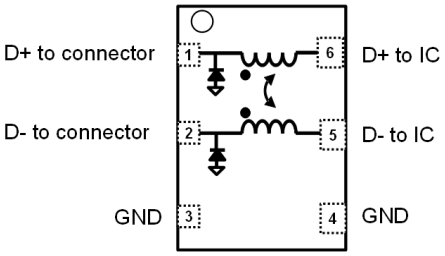
ECMF must be placed after the capacitor and as close as possible to the connector for the same ESD safety reasons explained before.

Figure 21. **ECMF implementation on a differential system**



To be compliant with the low frequency MIPI A-PHY ENIS insertion losses specification, ECMF R_{DC} needs to be lower than 5 Ω to comply with low frequencies. The differential bandwidth need to be higher than 8 GHz, and the device must be compliant with eye-diagram requirements.

Figure 22. **ECMF2-40A100M6Y functional diagrams**



The dark blue curve shows the MIPI A-PHY insertion losses requirements (S_{DD21}) and the red curve show the ECMF S_{DD21} measurement in dB.

Figure 23. **ECMF2-40A100M6Y insertion losses versus MIPI A-PHY requirements**

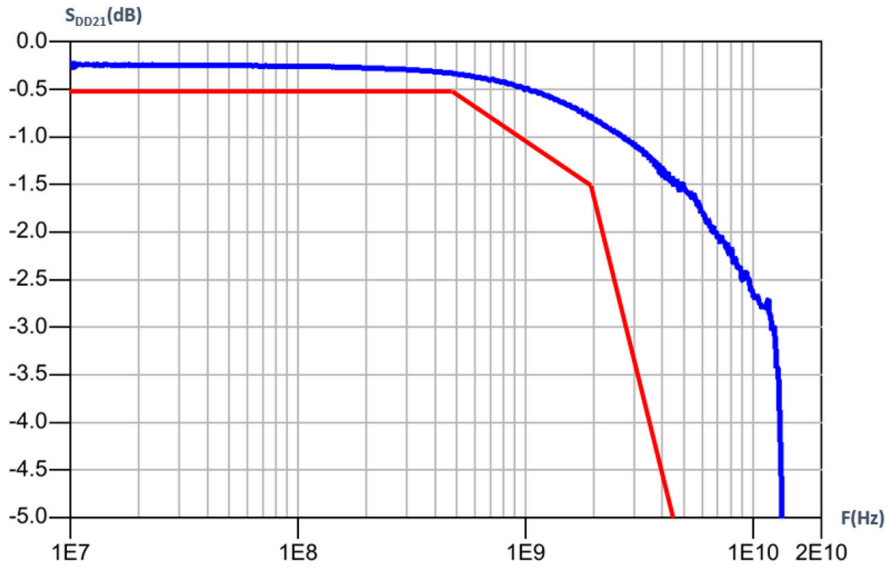
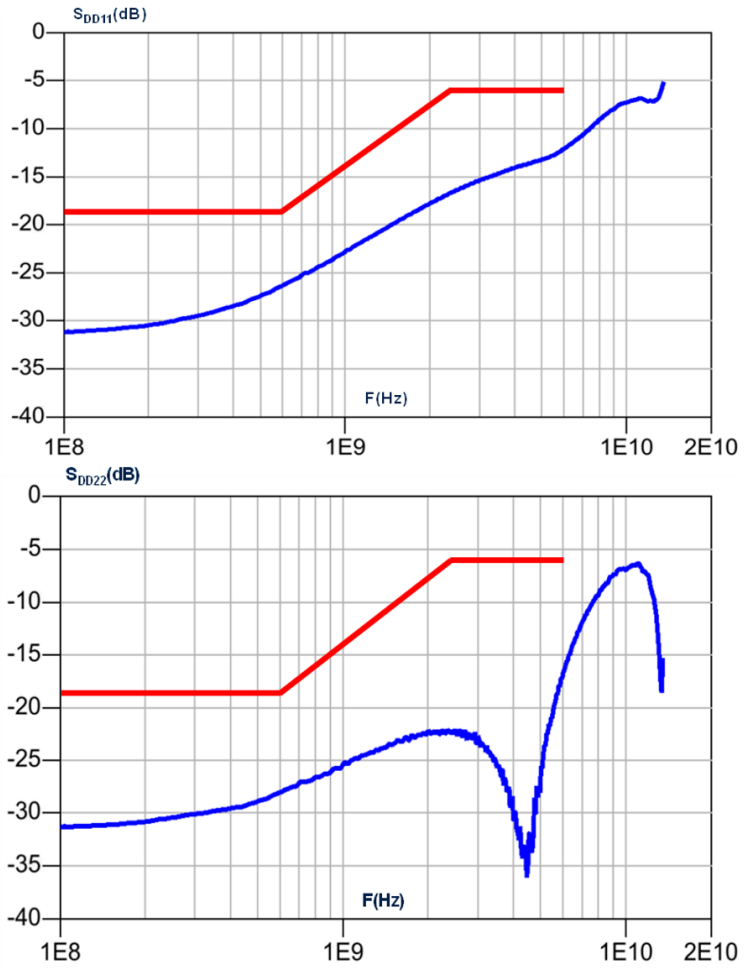


Figure 24. ECMF2-40A100M6Y return losses versus MIPI A-PHY requirements



Finally, the signal integrity is maintained with the presence of the product as shown below.

Figure 25. ECMF2 and ECMF4 MIPI A-PHY eye-diagram for gear 2 at 4 Gbps

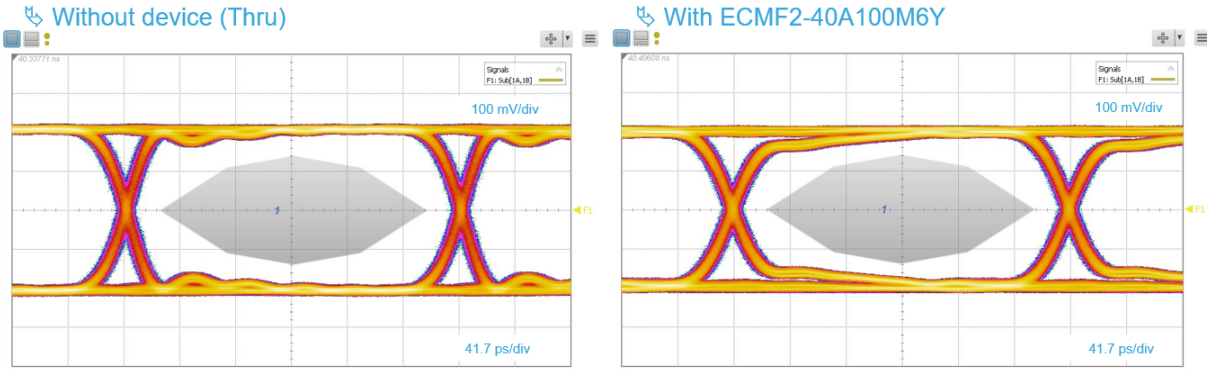
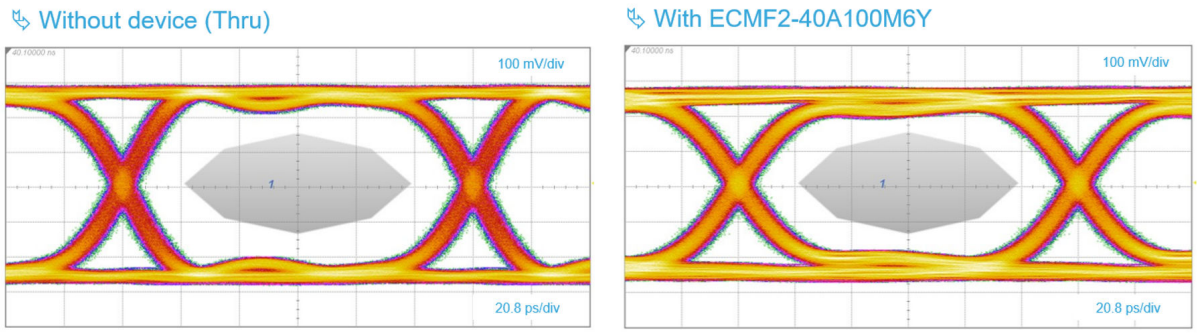


Figure 26. ECMF2 and ECMF4 MIPI A-PHY eye-diagram for gear 3 at 8 Gbps



6 Conclusion

This application note helps the user to understand the EMC issues encountered in the automotive industry.

The different principles and electrical specifications of the MIPI-A-PHY standard were presented. We also explained the parameters to be respected regarding the end-node-interconnect-structure.

Finally, to protect systems against ESD surges and to avoid radiations, ST offers ESD protections and ECMF that are compatible with the MIPI A-PHY standard specifications. The high frequency bandwidth of our products ensures a low impact on signal integrity.

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
11-Jan-2023	1	Initial release.
08-Jan-2024	2	Added *Section 5: ST offering for filtering and protection (ECMF)* and updated *Section 6: Conclusion*.
27-May-2024	3	Updated Figure 25.

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