# AN1262
# APPLICATION NOTE

# OFFLINE FLYBACK CONVERTERS DESIGN METHODOLOGY WITH THE L6590 FAMILY

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*The design of flyback converters is quite a demanding task that requires SMPS engineers to cope with several problem areas such as magnetics, control loop analysis, power devices, as well as regulations concerning safety, EMC and the emerging standby consumption requirements. Lots of variable are involved and complex tradeoffs are necessary to meet the goal.*

*In this scenario, the high-voltage monolithic switchers of the L6590 family greatly simplify the task and, at the same time, allow to build robust and cost-effective low-power systems.*

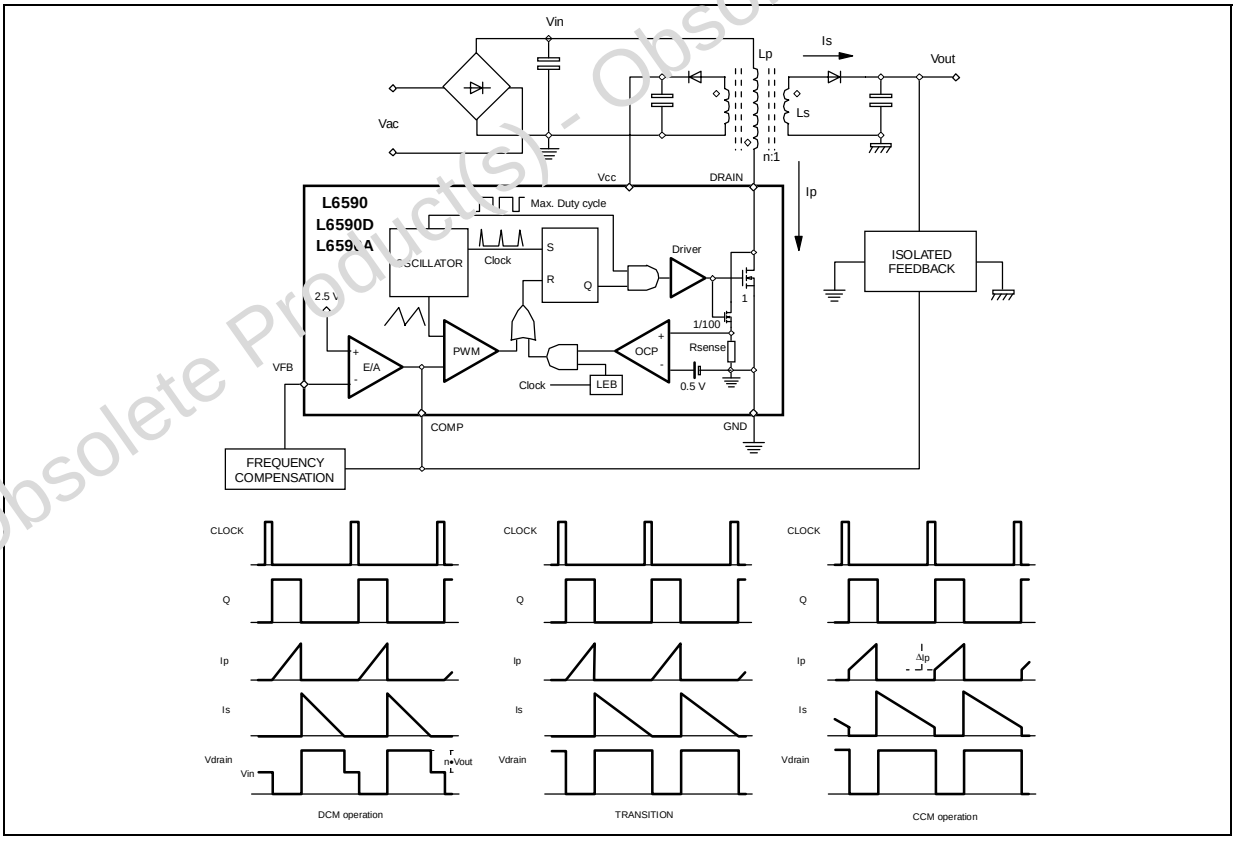
*In this application note, after a review of flyback topology, a step-by-step design procedure of an offline single-output flyback converter will be outlined. As an example, the design of the test board will be carried out in details.*



## 1 FLYBACK BASICS

Flyback operation will be illustrated with reference to the basic circuit and the waveforms of fig. 1. It is a two-step process. During the ON-time of the switch, energy is taken from the input and stored in the primary winding of the flyback transformer (actually, two coupled inductors). At the secondary side, the catch diode is reverse-biased, thus the load is being supplied by the energy stored in the output bulk capacitor.

**Figure 1. Flyback Topology and associated waveforms.**



When the switch turns off, the primary circuit is open and the energy stored in the primary is transferred to the secondary by magnetic coupling. The catch diode is forward-biased, and the stored energy is delivered to the output capacitor and the load. The output voltage $V_{out}$ is reflected back to the primary through the turns ratio n ($V_R$, reflected voltage) and adds up to the input voltage $V_{in}$, giving origin to a much higher voltage on the drain of the MOSFET.

Flyback is operated in DCM (Discontinuous Conduction Mode) when the input -or primary - current starts from zero at the beginning of each switching cycle. This happens because the secondary of the transformer has discharged all the energy stored in the previous period. If this energy transfer is not complete, the primary current will start from a value greater than zero at the beginning of each cycle. Then flyback is said to be operated in CCM (Continuous Conduction Mode). DCM is characterized by currents shaped in a triangular fashion, whereas CCM features trapezoidal currents.

The boundary between these two types of operation depends on several parameters. For a given converter, that is, as the switching frequency, inductance of the primary winding, transformer turns ratio and regulated output voltage are defined, it depends on the input voltage and the output load.

At design time, whether the converter will be operated in CCM or in DCM and where the boundary will be located is up to the designer. Usually CCM is selected with the objective of maximizing converter's power capability or minimizing primary RMS current. However, in CCM operation the system's dynamic behavior is considerably worse.

Usually, the converters based on the L6590 family devices are able to deliver the desired output power even with DCM operation, thus CCM will not be considered.

**Table 1. Converter specification data and pre-design choices**

| | |
|---|---|
| **Converter Electrical Specification** | |
| $V_{ACmin}$ | Minimum mains voltage |
| $V_{ACmax}$ | Maximum mains voltage |
| $f_L$ | Mains frequency (@ min. mains) |
| $N_H$ | Number of holdup cycles |
| $V_{out}$ | Regulated output voltage |
| $\Delta V_{out\%}$ | Percent output voltage tolerance (±) |
| $V_{r\%}$ | Percent output voltage ripple |
| $P_{outmax}$ | Maximum output power |
| $\eta$ | Expected converter efficiency |
| $T_{amb}$ | Maximum ambient temperature |
| **Pre-design Choices** | |
| $V_R$ | Reflected voltage |
| $\eta_T$ | Transformer efficiency |
| $V_{spike}$ | Leakage inductance overvoltage |
| $V_{cc}$ | IC supply voltage |
| $V_F$ | Secondary diode forward drop |
| $V_{BF}$ | Bridge Rectifier + EMI filter voltage drop |

## 2 CONVERTER ELECTRICAL SPECIFICATION

The starting point of the design procedure is the properties of the converter as a black-box, that is the set of data listed in the electrical specification table (table 1). Additional requirements, such as efficiency at zero load or line/load regulation or maximum junction temperature, etc., can be added to that list and their impact will be considered where appropriate.

- *Mains Voltage: Range and Frequency.* There are basically the three possible options listed in table 2, where a variation of ± 20% is assumed, according to common practice. There are exceptions like some distribution lines rated at 277 $V_{AC}$, where a ± 10% spread can be considered, or other special cases for specific applications. Table 2 shows also the line frequency to be considered in the standard cases at the minimum specified mains voltages. An additional specification may require the converter to be shut down if the mains voltage falls below a "brownout level". This additional specification will be used for setting up the brownout protection on the types where it is available.

**Table 2. Mains voltage specifications**

| Input ($V_{AC}$) | $V_{ACmin}$ ($V_{AC}$) | $V_{ACmax}$ ($V_{AC}$) | $f_L$ (Hz) |
|---|---|---|---|
| 110 | 88 | 132 | 60 |
| 220 | 176 | 264 | 50 |
| WRM (Wide Range Mains) | 88 | 264 | 60 |

- *Number of holdup cycles.* The holdup requirement is the ability of the converter to keep the output voltage in regulation even in case of mains interruption (missing cycles). This is usually specified in terms of number of mains cycles $N_H$. This feature is not always demanded (in which case, $N_H = 0$), otherwise the typical requirement is 1 mains cycle, that is $N_H = 1$. It impacts on the input bulk capacitor selection.
- *Output voltage tolerance.* It can be expressed either in absolute value or as a percentage of the nominal voltage. This requirement, as well as the ones on line and load regulation, if specified, will affect the choice of the feedback technique (primary or secondary).
- *Output voltage ripple.* The ripple superimposed on top of the DC output voltage is specified as the peak-to-peak amplitude and includes both low frequency (at $2 \cdot f_L$) and high frequency ($f_{sw}$) component. Switching noise due to parasitics of the printed circuit board and random noise are beyond the scope of this procedure. This requirement, if tight, may require the use of an additional filtering cell at the output.
- *Converter Efficiency.* The efficiency is, by definition, the ratio of the output power to the input power. This figure is strongly dependent on the output voltage, because of the losses on the secondary diode. It should be set based on experience, using numbers of similar converters as a reference. As a rule of thumb, 75% ($\eta = 0.75$) can be used for a low voltage output (3.3 V or 5 V) and 80% ($\eta = 0.8$) for higher output voltages (12 V and above).

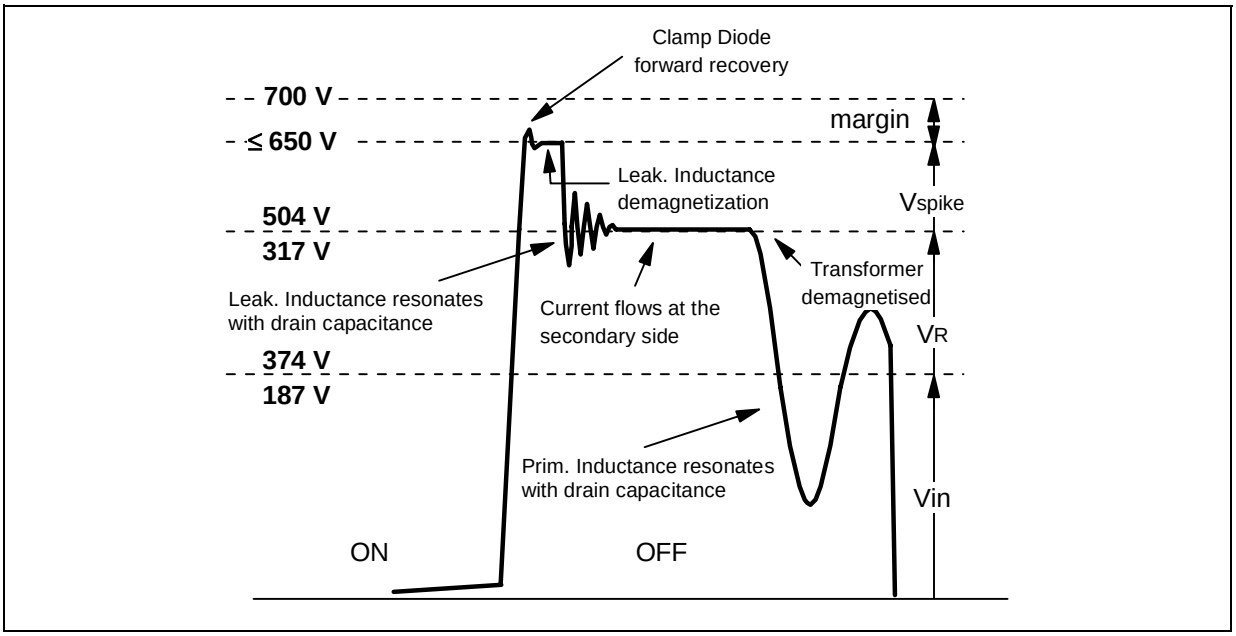
## 3 PRE-DESIGN CHOICES

Before starting the design calculations of the various parts of the converter, some parameters not defined at the "black-box level" need to be fixed. There is some degree of freedom in the selection of these parameters, provided some constraints are taken into account.

- *Reflected Voltage.* In principle, the reflected voltage should be as high as possible. In fact this leads to a greater duty cycle, which minimizes the RMS current through the IC's MOSFET for a given power throughput. There are two possible limitations to the maximum reflected voltage. One is the maximum duty cycle $D_{max}$ allowed by the devices (67% min.); some margin should be considered for load transients, thus the reflected voltage should be such that the maximum duty cycle (at minimum input voltage

and maximum output power) does not exceed 62-64%. The other limitation is that the sum of the maximum input voltage, reflected voltage and overvoltage spike - due to the leakage inductance - must be below the breakdown of the internal MOSFET (700 V min.). Some margin needs also to be considered: at least 50V is recommended to take the forward recovery of the diode of the clamp circuit and parameter spread into account. Figure 2 illustrates schematically how the drain voltage is apportioned. The suggested value of $V_R$ is 130 V: it leads to a maximum drain voltage slightly exceeding 500 V in 220$V_{AC}$ or WRM applications, and about 320 V in 110 $V_{AC}$ application, thus leaving enough room for an efficient leakage inductance demagnetization (see below). The maximum duty cycle will be about 60% in 110$V_{AC}$ and WRM applications, and close to 36% in 220 $V_{AC}$ applications.

**Figure 2. Drain voltage composition.**




- *Leakage inductance overvoltage.* The energy stored in the mutual inductance of the transformer at the primary side is not completely transferred to the secondary, after MOSFET turn-off, until the leakage inductance is demagnetized. This delays and makes inefficient the energy transfer from primary to secondary. To minimize this noxious effect the voltage across the leakage inductance (the leakage inductance spike) that resets the inductance itself should be as high as possible. Obviously, this is limited by the maximum allowable drain voltage. With the reflected voltage selected as previously discussed, it is possible to allow about 140 V extra voltage in 220 $V_{AC}$ or WRM applications and much more in 110 $V_{AC}$ applications (see fig. 2). This will affect the design of the clamp circuit.
- *Transformer efficiency.* By definition, it is the ratio of the power delivered by the secondary winding to the power entering the primary. The secondary power includes the converter output power and the one dissipated in the secondary rectifier. Besides the secondary one, the primary power includes the one dissipated inside the transformer and that not transferred to the secondary side and dissipated on the leakage inductance. For typical transformers used in converters based on the L6590 family IC's, typical values of efficiency ranges between 88% and 95%, depending on the power level and on the construction technique. Efficiency increases with the power level and by using winding interleaving construction technique. For consistency, check that the input power of the transformer be less than the converter input power.
- *Device supply voltage.* The supply voltage range of the IC spans from 7 to 16.5 V. Such a wide range is envisaged to accommodate the variation that the voltage generated by the self-supply winding may

experience in converters with opto-isolated feedback. This variation is a result of the poor magnetic coupling with the secondary winding. It is then recommended to design the turns ratio of the self-supply winding so as to get a voltage approximately in the middle of this range (e.g. 11-12 V). This will give allowance for increasing at heavy load and dropping at zero load.

- *Secondary diode forward drop*. The type of secondary diode will be selected basically depending on the output voltage. In fact this determines the maximum reverse voltage applied to the diode while the MOSFET is switched on. For low output voltages ≤15 V) a Schottky diode can be used and a typical forward drop of 0.5V can be considered; for higher output voltages an ultrafast PN diode will be used, with a typical forward drop of 0.8 V.
- *Bridge Rectifier + EMI filter voltage drop.* This drop is subtracted to the peak of the input AC voltage and affects the peak voltage of the ripple superimposed on top of the DC voltage across the input bulk capacitor. A typical value can be 3 V.

## 4 PRELIMINARY CALCULATIONS (STEP 1)

There are a few quantities that need to be calculated before starting the individual design of each functional block of the converter. They are summarized in table 3.

**Table 3. Preliminary calculations (step 1).**

| Symbol | Parameter | Definition |
|---|---|---|
| $P_{in}$ | Converter Input Power | $P_{in} = \frac{P_{outmax}}{\eta}$ |
| $I_{out}$ | DC Output Current | $I_{out} = \frac{P_{outmax}}{V_{out}}$ |
| $V_{PKmin}$ | Minimum Peak Input Voltage | $V_{PKmin} = V_{ACmin} \cdot \sqrt{2} - V_{BF}$ |
| $V_{PKmax}$ | Maximum Peak Input Voltage | $V_{PKmax} = V_{ACmax} \cdot \sqrt{2}$ |

## 5 BRIDGE RECTIFIER SELECTION

Due to the limited power range that the device is able to handle, no special considerations are needed to select the diodes of the bridge rectifier. Any 1A rated standard diodes with 400/600 V reverse voltage are suitable. Some manufacturers make integrated bridge rectifiers housed in small packages. See table 4 for some suggested parts.

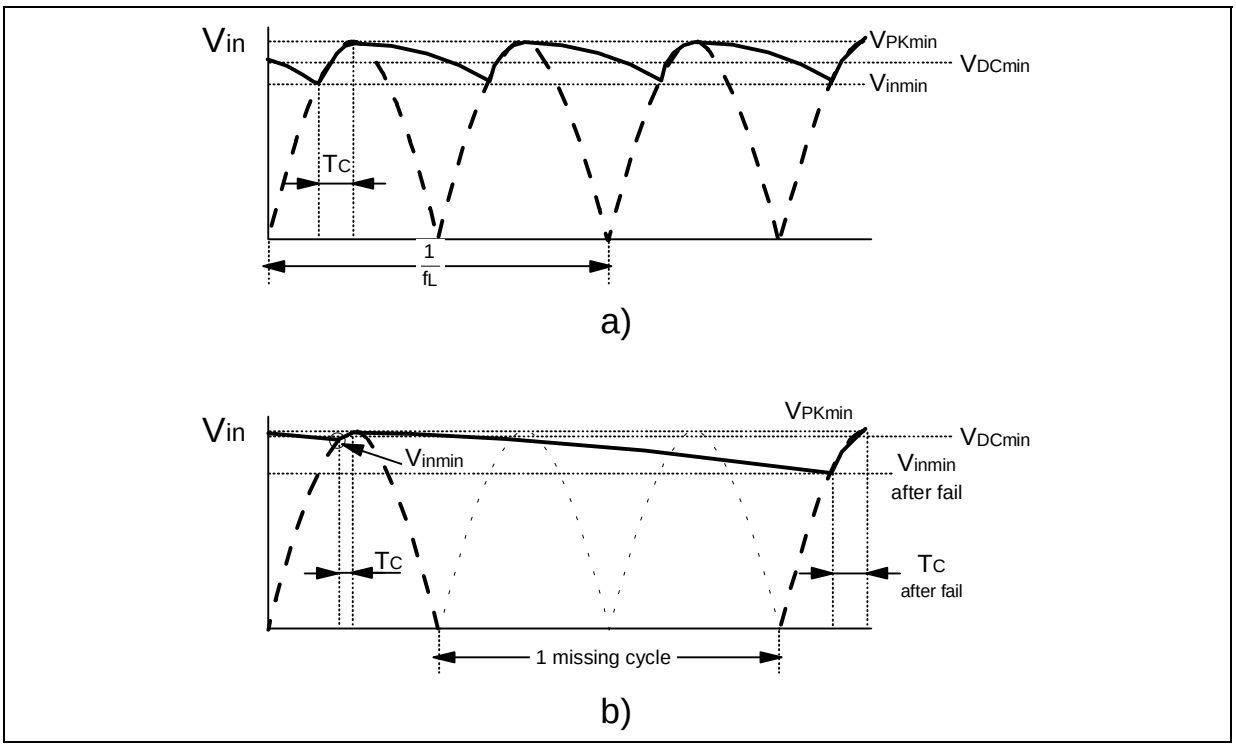
**Table 4. 1A standard silicon rectifier and bridge selection**

| Type | Part Number | Rated Voltage | Package | Manufacturer(s) |
|---|---|---|---|---|
| Diode | 1N4004 | 400 | DO41 | GI, GS, FAGOR, HTA, ON, TSC |
| Diode | 1N4005 | 600 | DO41 | GI, GS, FAGOR, HTA, ON, TSC |
| Bridge | DF04M | 400 | DIL4 | GI,TSC |
| Bridge | DF06M | 600 | DIL4 | GI,TSC |
| Bridge | KBP104G | 400 | SIL4 | TSC |
| Bridge | KBP105G | 600 | SIL4 | TSC |
| Bridge | DFS04M | 400 | DIL4 (SMD) | HTA |
| Bridge | DFS06M | 600 | DIL4 (SMD) | HTA |

## 6 INPUT BULK CAPACITOR SELECTION

The input bulk capacitor $C_{in}$, along with the bridge rectifier, converts the AC mains voltage to an unregulated DC bus, $V_{in}$, which is the input voltage for the downstream flyback converter. $C_{in}$ must be large enough to have a relatively low ripple superimposed on top of the DC level, as shown in fig. 3. At minimum specified mains voltage, the value of $C_{in}$ determines the absolute minimum, $V_{inmin}$, of the DC input voltage of the converter. The maximum duty cycle and the maximum peak current allowed by the IC must not be exceeded at this voltage. However, as to thermal consideration, the bus DC voltage ($V_{DCmin}$ @ $V_{ACmin}$) should be considered.

**Figure 3. Input voltage waveforms:**
**a) without holdup capability;**
**b) with holdup capability.**




Large values of $C_{in}$ result in higher $V_{DCmin}$ and $V_{inmin}$, lower peak and RMS current through the power MOSFET (i.e. less power dissipation in the device) and less duty cycle range to achieve regulation but, on the other hand, also in bigger capacitor size, higher peak and RMS current drawn from the mains (i.e. more power dissipation in the bridge rectifier). Small values of $C_{in}$ give origin to the opposite situation.

Experience shows that a good compromise between these contrasting requirements is a $C_{in}$ value that causes the peak-to-peak ripple amplitude to be 25-30% of the peak mains voltage (@ $V_{ACmin}$), which means that $V_{inmin}$ will be 70-75% of the peak value. Anyway, if holdup capability is required, a much larger capacitance values will be needed: the voltage ripple across $C_{in}$ is expected to be 25-30% of the peak value, after 1 mains cycle missing, which means that in normal operation the ripple will be much less.

Table 5 summarizes the required capacitance per watt of input power for a given value of $V_{inmin}$, with and without holdup requirement, and shows the resulting values of $V_{DCmin}$. This allows to calculate the minimum capacitance needed, by multiplying the value taken from the table times $P_{in}$. Then a standard value will be selected, taking also the tolerance into account.

**Table 5. Cin values for 1W input power**

| | 110 VAC or WRM | | 220 VAC | |
|---|---|---|---|---|
| $N_H$=0 | 2.0 µF/W | 3.0 µF/W | 0.55 µF/W | 0.8 µF/W |
| | $V_{inmin}$ = 90V<br>$V_{DCmin}$ = 105V | $V_{inmin}$ = 100V<br>$V_{DCmin}$ = 110V | $V_{inmin}$ = 180V<br>$V_{DCmin}$ = 210V | $V_{inmin}$ = 200V<br>$V_{DCmin}$ =220V |
| $N_H$=1 | 7.2 µF/W | 10.4 µF/W | 1.8 µF/W | 2.8 µF/W |
| | $V_{inmin}$ = 90V<br>$V_{DCmin}$ = 116V | $V_{inmin}$ = 100V<br>$V_{DCmin}$ = 117V | $V_{inmin}$ = 180V<br>$V_{DCmin}$ = 236V | $V_{inmin}$ = 200V<br>$V_{DCmin}$ =239V |

The actual values of $V_{inmin}$ and $V_{DCmin}$ need to be recalculated with the actual capacitance value. Since the evaluation of $V_{inmin}$ involves an equation having no closed form solution, an iterative cycle needs to be established:

$$V_{inmin} = \sqrt{V_{PKmin}^2 - \frac{P_{in}}{C_{in}} \cdot \left(\frac{1 + 2 \cdot N_H}{f_L} - 2 \cdot T_c\right)}; \quad T_c = \frac{\arccos\left(\frac{V_{inmin}}{V_{PKmin}}\right)}{2 \cdot \pi \cdot f_L} \qquad (1)$$

where $T_C$ is the recharging time of $C_{in}$, that is the time while the bridge diodes are conducting, which can be initially assumed equal to zero. After few iterations both $V_{inmin}$ and $T_C$ will converge to their respective values.

In case of holdup requirement the cycle should be executed twice. The first time with $N_H$ = 1 to find $V_{inmin}$ after one mains cycle missing (which will be used to check for maximum duty cycle and maximum peak current) the second one with $N_H$ = 0 to find $V_{inmin}$ in normal operation (to be used for steady state and thermal calculations).

$V_{DCmin}$ will be simply the average of $V_{inmin}$ (calculated with $N_H$ = 0 anyway) and $V_{PKmin}$:

$$V_{DCmin} = \frac{1}{2} \cdot (V_{PKmin} + V_{inmin}) \qquad (2)$$

The voltage rating of $C_{in}$ is selected depending on $V_{PKmax}$: it is usually 200 V for 110 $V_{AC}$ applications and 400V for 220 $V_{AC}$ or WRM applications.

## 7 PRELIMINARY CALCULATIONS (STEP 2)

The next step is to check for not exceeding the limits imposed by the IC. Prior to this, the power processed by the transformer ($P_{inT}$) and the average voltage drop across the ON-resistance of the internal MOSFET ($V_{DS(on)x}$) will be evaluated. $V_{DS(on)x}$ is subtracted to $V_{inmin}$ and the resulting value is the voltage actually applied to the primary winding of the transformer. The $R_{DS(on)}$ used must take temperature into account. Use the maximum value defined at 125°C.

The first limit to be checked is the maximum duty cycle $D_X$. If it exceeds 62-64%, either the reflected voltage $V_R$ should be lowered or the minimum input DC voltage $V_{inmin}$ should be increased by selecting a larger input capacitance.

The second limit to be checked is the maximum drain voltage during the OFF-state of the MOSFET. At least 50V margin should be ensured. The overvoltage spike can be reduced to allow more reflected voltage if necessary, keeping in mind that it cannot be much lower than $V_R$ not to hurt the primary-to-secondary energy transfer.

The last check concerns the peak primary current that must not exceed the minimum guaranteed OCP threshold (0.55A). If this is exceeded, a higher maximum duty cycle $D_X$ should be used, if possible. Also a higher $V_{inmin}$ is beneficial. Some iterations, involving a recheck of the first two points, may be necessary to find the optimum compromise. If no solution can be found, either CCM operation should be considered or the power handled by the converter should be derated.

All of the above mentioned calculation steps are summarized in table 6.

**Table 6. Preliminary Calculations (step 2)**

| Symbol | Parameter | Definition |
|---|---|---|
| $P_{inT}$ | Transformer Input Power | $P_{inT} = \frac{(V_{out} + V_F) \cdot I_{out}}{\eta_T}$ |
| $V_{DS(on)x}$ | Max. average drop on $R_{DS(on)}$ in ON-state | $V_{DS(on)} \approx \frac{V_{inmin} + V_R}{1 + \frac{V_{inmin} \cdot V_R}{P_{in} \cdot R_{DS(on)}}}$ |
| $D_x$ | Maximum Duty Cycle | $D_X = \frac{V_R}{(V_{inmin} - V_{DS(on)x}) + V_R}$ |
| $V_{DSmax}$ | Maximum drain Voltage in OFF-state | $V_{DSmax} = V_{PKmax} + V_R + V_{spike}$ |
| $Ip_{pkx}$ | Max. Peak Primary Current | $Ip_{pkx} = \frac{P_{inT}}{V_{inmin} - V_{DS(on)x}} \cdot \frac{2}{D_X}$ |

## 8 OPERATING CONDITIONS @ $V_{IN} = V_{DCMIN}$

From the thermal point of view the heaviest operating conditions for the IC, and for most of the other parts of the converter as well, are usually encountered at minimum input voltage.

That is why the operating conditions @ $V_{in} = V_{DCmin}$ need being evaluated. This will be done with the aid of the relationships in table 7.

**Table 7. Relationship useful for calculating converter's operating conditions @ $V_{in} = V_{DCmin}$**

| Symbol | Description | Definition |
|---|---|---|
| D | Duty Cycle (switch ON-time to switching period ratio) | $D = \frac{V_{inmin} - V_{DS(on)x}}{V_{DCmin} - V_{DS(on)x}} \cdot D_X$ |
| $Ip_{pk}$ | Peak Primary Current | $Ip_{pk} = Ip_{pkx}$ |
| $Ip_{DC}$ | DC Primary Current | $Ip_{DC} = \frac{D \cdot Ip_{pk}}{2}$ |
| $Ip_{RMS}$ | Total RMS Primary Current | $Ip_{RMS} = Ip_{pk} \cdot \sqrt{\frac{D}{3}}$ |
| $Ip_{AC}$ | RMS Primary Current (AC component only) | $Ip_{AC} = \sqrt{Ip_{RMS}^2 - Ip_{DC}^2}$ |
| D‘ | Secondary diode conduction time to switching period ratio | $D' = \frac{V_{DCmin} - V_{DS(on)x}}{V_R} \cdot D$ |
| $Is_{pk}$ | Peak Secondary Current | $Is_{pk} = \frac{2 \cdot I_{out}}{D'}$ |
| $Is_{DC}$ | DC Secondary Current | $Is_{DC} = I_{out}$ |

**Table 7. (continued)**

| Symbol | Description | Definition |
|---|---|---|
| $Is_{RMS}$ | Total RMS Secondary Current | $Is_{RMS} = Is_{pk} \cdot \sqrt{\frac{D'}{3}}$ |
| $Is_{AC}$ | RMS Secondary Current (AC component only) | $Is_{AC} = \sqrt{Is_{RMS}^2 - Is_{DC}^2}$ |

Once this information has been found, it is possible to evaluate the power dissipation of the IC and check for thermal limitations. Table 8 summarizes the relationships that can be used for this evaluation. In those formulae:

- $T_c$ is the crossover time of the voltage and current waveforms at MOSFET's turn off;

- $C_{drain}$ is the total capacitance of the drain, composed of the $C_{oss}$ of the MOSFET, the parasitic capacitance of the primary winding and, in case, some external capacitance.

As previously said, the worst-case operating conditions for the IC usually occur at $V_{in} = V_{DCmin}$, however it is worthwhile checking the losses also at maximum input voltage, that is at $V_{in} = V_{PKmax}$, especially if an external capacitor is added on the drain.

With the worst-case total losses in the IC it is possible to find the maximum junction-to-ambient thermal resistance allowed for safe operation at maximum ambient temperature.

The operating temperature range of the devices extends to 150 °C, however designing for such high temperature is not recommended. A reasonable target can be to design for 125 °C maximum die temperature:

$$R_{thmax} = \frac{125 - T_{amb}}{P_Q + P_{cond} + P_{sw} + P_{cap}} \quad (3)$$

**Table 8. IC's power losses estimate**

| Symbol | Description | Definition |
|---|---|---|
| $P_{cond}$ | Conduction losses | $P_{cond} = Ip_{RMS}^2 \cdot R_{DS(on)max}$ |
| $P_{sw}$ | Switching losses | $P_{sw} \approx \frac{1}{3} \cdot (V_{in} + V_R) \cdot Ip_{pk} \cdot T_c \cdot f_{sw}$ |
| $P_{CAP}$ | Capacitive losses | $P_{CAP} \approx \frac{1}{2} \cdot C_{drain} \cdot (V_{in} + V_R)^2 \cdot f_{sw}$ |
| $P_Q$ | Quiescent losses | $P_Q = V_{CC} \cdot I_{op}$ |
| Assume:<br>$R_{DS(on)\ max}$ = 28 Ω (@ $T_j$ = 125 °C)<br>$T_c$ = 50ns<br>$f_{sw}$ = 65kHz<br>$C_{drain}$ = 100pF<br>$I_{op}$ = 7mA | | |

With the aid of the diagrams shown in fig. 20 it is possible to estimate whether the required thermal resistance is feasible or not and, in the positive case, how large the on-board copper area is supposed to be. Consider that copper areas larger than 4 $cm^2$ do not give significant reduction of thermal resistance and may cause PCB layouting to become a serious issue.

If the thermal check does not give positive results, a different heatsinking strategy may be considered, otherwise a higher maximum duty cycle $D_X$ should be used, if possible, to reduce the RMS current. Also a higher $V_{inmin}$

(that is a larger input capacitor) is of help. Some iterations, involving a recheck of the points mentioned in "Preliminary Calculations - step 2", may be necessary.

If no solution can be found, either some specification should be relaxed or the power handled by the converter should be derated.

## 9 FLYBACK TRANSFORMER DESIGN

To complete the set of data needed to design the flyback transformer, the primary inductance value ($L_p$) and the primary-to-secondary turns ratio (n) are still to be defined.

The primary inductance will be chosen so that the converter is operated on the boundary between DCM and CCM at $V_{in} = V_{inmin}$:

$$Lp = \frac{[(V_{inmin} - V_{DS(on)x)}) \cdot D_X]^2}{2 \cdot f_{sw} \cdot P_{inT}} \quad (4)$$

while the primary-to-secondary turns ratio is defined so as to get the desired reflected voltage $V_R$:

$$n = \frac{V_R}{V_{out} + V_F} \quad (5)$$

With the complete set of specification, the transformer design can start with the selection of the magnetic core material and geometry.

**Table 9. Ferrite Materials selection**

| Grade | Saturation flux density [T] | Specific Power Losses @100 °C [W/cm$^3$] | Manufacturer |
|---|---|---|---|
| B2 | 0.36 | $\overline{P}_{Fe} = 1.15 \cdot 10^{-5} \cdot \Delta B^{2.26} \cdot f_{sw}^{1.11}$ | THOMSON |
| 3C85 | 0.33 | $\overline{P}_{Fe} = 1.54 \cdot 10^{-7} \cdot \Delta B^{2.62} \cdot f_{sw}^{1.54}$ | PHILIPS |
| N67 | 0.38 | $\overline{P}_{Fe} = 8.53 \cdot 10^{-7} \cdot \Delta B^{2.54} \cdot f_{sw}^{1.36}$ | EPCOS (ex S+M) |
| PC30 | 0.39 | $\overline{P}_{Fe} = 1.59 \cdot 10^{-6} \cdot \Delta B^{2.58} \cdot f_{sw}^{1.32}$ | TDK |
| F44 | 0.4 | $\overline{P}_{Fe} = 2.39 \cdot 10^{-6} \cdot \Delta B^{2.23} \cdot f_{sw}^{1.26}$ | MMG |

As to the magnetic material, a standard soft ferrite for power applications (gapped core-set with bobbin) is the usual choice: the switching frequency is not so high thus special grades for high frequency operation are not required. Table 9 shows some suitable materials.

The geometry will be usually a popular E or E-derived type. Other configurations, such as RM or PQ cores, are not recommended because they are inherently high leakage geometries, since they result in narrower and thicker windings. Consider that minimizing leakage inductance is one of the major tasks in the design of a flyback transformer.

Among the various shapes and styles offered by manufacturers the most suitable one will be selected with technical and economic considerations. Table 10 shows some possible choices with the relevant data useful for the design.

The next quantity to be defined is the peak flux density $B_{max}$ which the transformer will be operated at. Being this a DCM design, $B_{max}$ will also equal the maximum flux density swing $\Delta B_{max}$.

Due to the moderate switching frequency, $B_{max}$ will be limited by core saturation and not by core losses. This means that transformer's power losses will be located mostly in the windings.

As shown in table 9, ferrites saturate above 0.3 T thus a value of $B_{max}$ equal to 0.28-0.30 T may be selected to maximize core utilization, or $B_{max}$ = 0.25 T can be chosen for a more conservative design.

This maximum peak flux density will occur when the peak primary current is maximum. However, it is not sufficient to consider the peak current $Ip_{pkx}$ resulting from table 6. To guarantee that the transformer does not saturate even under short circuit conditions, the maximum peak primary current to be considered is the maximum value of the OCP threshold ($I_{lim}$ = 0.7A, from the datasheet).
Now a step-by-step procedure for the design of the transformer will be given.

**Table 10. Core list and significant design data**

| Core | Ve [$cm^3$] | Ae [$cm^2$] | Aw [$cm^2$] | AP [$cm^4$] | K1 | K2 | Lt [cm] | WB [cm] | Rth [°C/W] |
|---|---|---|---|---|---|---|---|---|---|
| **THOMSON (B2)** | | | | | | | | | |
| EF1505A | 0.51 | 0.15 | 0.15 | 0.022 | 29.7 | -0.68 | 2.63 | 0.92 | 75 |
| EF2007A | 1.46 | 0.31 | 0.26 | 0.081 | 61.1 | -0.7 | 3.65 | 1.32 | 45 |
| EF2509A | 3.3 | 0.58 | 0.4 | 0.232 | 103 | -0.73 | 4.64 | 1.64 | 30 |
| E2006A | 1.5 | 0.32 | 0.35 | 0.112 | 62.2 | -0.7 | 3.9 | 1.18 | 46 |
| E2507A | 3.2 | 0.55 | 0.6 | 0.33 | 90 | -0.73 | 5.2 | 1.54 | 40 |
| **PHILIPS (3C85)** | | | | | | | | | |
| E16/8/5 | 0.75 | 0.201 | 0.216 | 0.043 | 42.2 | -0.7 | 3.3 | 0.94 | 65 |
| E20/10/6 | 1.49 | 0.32 | 0.35 | 0.112 | 62.2 | -0.69 | 3.9 | 1.18 | 46 |
| E25/13/7 | 2.99 | 0.52 | 0.56 | 0.291 | 90 | -0.73 | 4.9 | 1.56 | 40 |
| **EPCOS (ex S+M) (N67)** | | | | | | | | | |
| E16/8/5 | 0.76 | 0.2 | 0.22 | 0.044 | 42.2 | -0.7 | 3.4 | 1 | 65 |
| E20/10/6 | 1.49 | 0.32 | 0.34 | 0.109 | 62.2 | -0.69 | 4.12 | 1.25 | 46 |
| E25/13/7 | 3.02 | 0.52 | 0.61 | 0.317 | 90 | -0.73 | 5 | 1.56 | 40 |
| **TDK (PC30)** | | | | | | | | | |
| EI16-Z | 0.67 | 0.198 | 0.267 | 0.053 | 66 | -0.57 | 3.31 | 0.86 | 44 |
| EI22-Z | 1.63 | 0.42 | 0.2 | 0.084 | 85.4 | -0.71 | 3.86 | 0.845 | 33 |
| EI25-Z | 1.93 | 0.41 | 0.425 | 0.174 | 119 | -0.57 | 4.94 | 0.98 | 31 |
| **MMG - NEOSID (F44)** | | | | | | | | | |
| EF16 | 0.754 | 0.225 | 0.216 | 0.049 | 42.2 | -0.7 | 3.3 | 1 | 65 |
| EF20 | 1.5 | 0.314 | 0.348 | 0.109 | 62.2 | -0.69 | 3.9 | 1.2 | 46 |
| EF25 | 3.02 | 0.515 | 0.564 | 0.29 | 90 | -0.73 | 4.8 | 1.6 | 40 |

1) *Choose core size.* Transformer's core must be able to handle the power throughput $P_{InT}$ without saturating and with acceptable power losses, with the minimum size. Determining its optimum size is a trial-and-error process and a proper starting point may reduce considerably the number of iterations needed.

   A most common way of describing core size is the so-called Area Product (AP), which is the product of the effective cross-sectional area of the core times the window area available to accommodate the windings. It is possible to define the minimum AP required by a specific application.

   The following equation can be useful to estimate the minimum AP (in $cm^4$) required:

$$Ap_{min} = 10^3 \cdot \left( \frac{L_p \cdot Ip_{RMS}}{\Delta T^{\frac{1}{2}} \cdot K_u \cdot B_{max}} \right)^{1.316} \quad [cm^4] \qquad (6)$$

In this equation $\Delta T$ is the hot-spot temperature rise (located in the core center leg, where heat can be removed more difficultly), defined as $\Delta T = T_{max} - T_{amb}$. For reliability reasons $T_{max}$ is usually limited at 100°C where, by the way, ferrites usually feature minimum losses. $K_u$ is the window utilization factor, that is the portion of the total core window area occupied by the windings, which can be estimated equal to 0.4 for margin wound construction and to 0.7 for triple insulated wire construction.

The smallest core with an AP greater then $AP_{min}$ will be chosen from the catalog data (the core list of table 10 can be used as a reference). If there is a core with an $AP < AP_{min}$ but very close to, it might be worthwhile trying to design with this smaller core before trying the larger one.

2) *Calculate the required minimum number of primary turns of the primary winding.* It will be given by:

$$Np_{min} = \frac{Lp \cdot 0.7}{B_{max} \cdot A_e} \cdot 10^4$$

3) *Define primary and secondary windings' turns number.* In the case of single-output under consideration, the secondary winding turns number Ns will be simply:

$$N_s = \left[ \frac{Np}{n} + 1 \right],$$

that is, the result of the division will be rounded up to the next larger integer. The actual primary turns will then be calculated, rounding the result to the closest integer.

$$Np = [Ns \cdot n + 0.5].$$

It can be convenient to round to the next even number when interleaved winding technique is to be used for transformer construction, so as to split the primary in two equal halves.

4) *Calculate the air gap length.* The gap length ($l_g$) needed to get the desired inductance Lp will be calculated with the following empirical formula:

$$l_g = \left( \frac{Lp}{Np^2} \cdot \frac{10^9}{k1} \right)^{\frac{1}{k2}} \quad [mm] \qquad (7)$$

If the calculated value is not available as a standard part, if possible, the primary turns number can be adjusted a little bit to get an off-the-shelf part.

The air gap should be located on the core center leg only, to minimize radiated fields. In prototyping, center leg grinding to get nonstandard gap values can be avoided by keeping the two half-cores apart by about half the calculated value with spacers.

5) *Calculate transformer total losses.* The allowed total transformer losses ($P_{tot}$) can be calculated by dividing the hot-spot temperature rise $\Delta T$ by the thermal resistance of the wound core $R_{th(core)}$:

$$P_{tot} = \frac{\Delta T}{R_{th(core)}} \quad [W]$$

If the manufacturer does not provide thermal data, $R_{th(core)}$ can be estimated. It has been shown [1] that there is a good correlation between core's area product and thermal resistance, regardless of its shape:

$$R_{th(core)} \approx 23 \cdot AP^{-0.37} \quad [°C/W];$$

this best-fit equation refers to natural convection cooling.

6) *Calculate the actual flux swing,* the actual core losses and the allowed copper losses. The flux swing will be given by:

$$\Delta B = \frac{Lp \cdot Ip_{pk}}{Np \cdot A_e} \cdot 10^4 \quad [T] \tag{8}$$

and the corresponding core losses can be calculated with the formulae in table 9:

$$P_{Fe} = V_e \cdot k \cdot \Delta B^p \cdot f_{sw}^q \quad [W] \tag{9}$$

The allowed copper losses will obviously be:

$$P_{Cu} = P_{tot} - P_{Fe} \quad [W] \tag{10}$$

7) *Design windings.* The goal is to find the right wire size so that copper losses are within the limit stated by (10). At this moment, losses due to skin and proximity effect will not be accounted for. The construction technique of the transformer will be such that these effects will be minimized.

Copper losses will be equally apportioned to the primary and the secondary winding (the power handled by the auxiliary one is negligible). Therefore the maximum primary and secondary winding resistance will be respectively:

$$Rp = \frac{P_{Cu}}{2 \cdot Ip_{RMS}^2} \quad [\Omega] \; ; \quad Rs = \frac{P_{Cu}}{2 \cdot Is_{RMS}^2} \quad [\Omega] \tag{11}$$

The primary and secondary conductor copper cross-section area will be obtained considering the resistivity of copper at 100°C ($\rho_{100} = 2.303 \cdot 10^{-6}\ \Omega \cdot cm$) and the average length-per-turn (4) of the bobbin associated to the selected core:

$$Ap_{Cumin} = \frac{\rho_{100} \cdot Np \cdot L_t}{Rp} \quad [cm^2] \tag{12}$$

$$As_{Cumin} = \frac{\rho_{100} \cdot Ns \cdot L_t}{Rs} \quad [cm^2] \tag{13}$$

A wire table (like the sample one shown in table 11) will be looked up and a wire with a copper area ($Ap_{Cu}$, $As_{Cu}$) equal or greater than the minimum above calculated will be selected. Anyway, to minimize skin effect, the selected wire diameter should not exceed $2 \cdot \delta$, where $\delta$ is the skin depth of copper (about 0.3 mm at 65 kHz and 100°C). In practice, the maximum wire size for minimum skin effect is AWG23 (∅ 0.57 mm, $A_{Cu}$ = 0.2573 $mm^2$). If $Ap_{Cu}$ is larger, a number (Nwp, Nws) of such (or smaller) wires will be paralleled so as to achieve the desired total area:

$$Nwp = \frac{Ap_{Cumin}}{Ap_{Cu}}$$

$$Nws = \frac{As_{Cumin}}{As_{Cu}}$$

where the results will be rounded up to the next larger integer.

**Table 11. Wire Table (RS-214). Copper wire. Heavy insulation.**

| AWG | Diameter Copper [cm] | Diameter Insulated [cm] | Area Copper [$cm^2$] | Area Insulated [$cm^2$] |
|---|---|---|---|---|
| 22 | 0.064 | 0.071 | 0.003255 | 0.004013 |
| 23 | 0.057 | 0.064 | 0.002582 | 0.003221 |
| 24 | 0.051 | 0.057 | 0.002047 | 0.002586 |
| 25 | 0.045 | 0.051 | 0.001624 | 0.002078 |
| 26 | 0.040 | 0.046 | 0.001287 | 0.001671 |
| 27 | 0.036 | 0.041 | 0.001021 | 0.001344 |
| 28 | 0.032 | 0.037 | 0.000810 | 0.001083 |
| 29 | 0.029 | 0.033 | 0.000642 | 0.000872 |
| 30 | 0.025 | 0.030 | 0.000509 | 0.000704 |
| 31 | 0.023 | 0.027 | 0.000404 | 0.000568 |
| 32 | 0.020 | 0.024 | 0.000320 | 0.000459 |
| 33 | 0.018 | 0.022 | 0.000254 | 0.000371 |

Finally the total winding area must be checked to make sure they fit the bobbin window Aw:

$$Api \cdot Nwp \cdot Np + As_i \cdot Nws \cdot Ns \leq K_u \cdot Aw \quad (14)$$

where Api and Asi are the individual wire cross-section, primary and secondary respectively, including isolation. If the above inequality is not verified there are the following options:

a) if Np is quite larger than $Np_{min}$, try decreasing Np and go back to step 3;

b) choose a smaller wire, recalculate Nwp and Nws and recheck window fitting;

c) use fewer wires in a strand accepting a likely larger temperature rise;

d) use the next size core and restart from step 2.

Finally, the auxiliary winding will be defined. It has not been considered before because it handles a very low power, thus it will be made with a single thin wire (e.g. AWG32 or AWG33) which gives a negligible contribution to winding build and losses. Just the turns number needs to be defined:

$$N_{aux} = Ns \cdot \frac{V_{CC} + 0.7}{V_{out} + V_F} \quad (15)$$

where 0.7 V is the typical forward drop on the auxiliary (small signal) diode.

8) *Calculate actual power dissipation and hot-spot temperature rise.* The actual resistance of the primary and secondary windings has to be calculated first:

$$Rp = \rho_{100} \cdot \frac{Np \cdot L_t}{Nwp \cdot Ap_{Cu}}; \quad Rs = \rho_{100} \cdot \frac{Ns \cdot L_t}{Nws \cdot As_{Cu}},$$

then the total power dissipation and the hot spot temperature rise will be respectively:

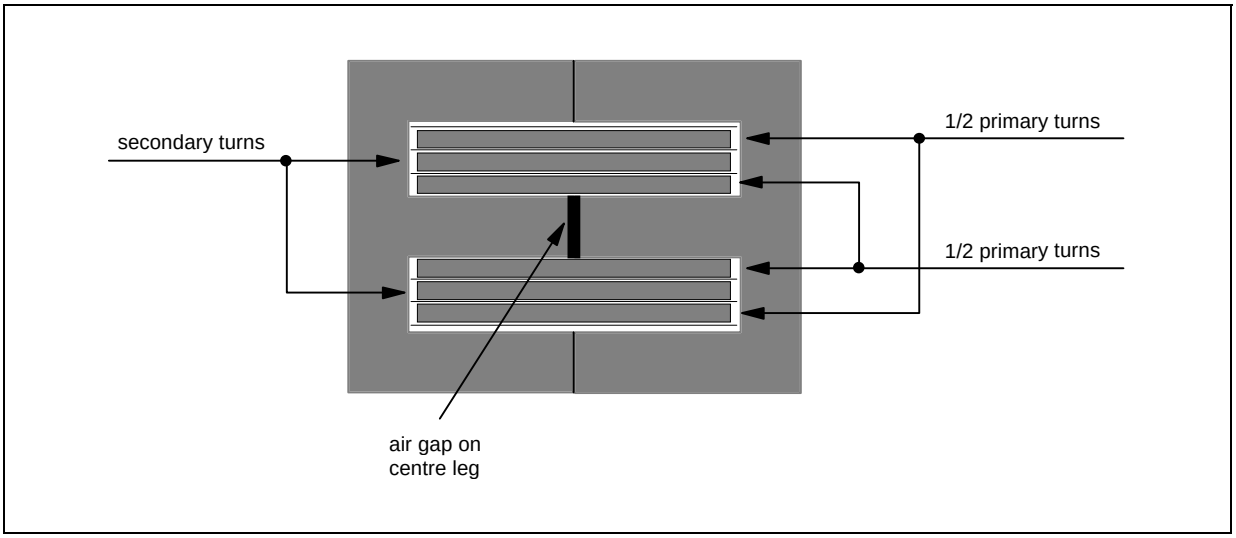
$$P_{tot} = P_{Fe} + Rp \cdot Ip_{RMS}^2 + Rs \cdot Is_{RMS}^2$$

$$\Delta T = P_{tot} \cdot R_{th}$$

Finally, some suggestions on the transformer construction techniques. When building a transformer, the general rule is to minimize parasitics, basically leakage inductance and winding capacitance.

In order for a transformer to meet isolation and safety norms, primary and secondary windings must be separated by isolation layers, thus their coupling cannot be intimate. Moreover, in a margin wound construction the entire window breadth cannot be used (2.5 to 3 mm margin on each side must be considered to achieve sufficient creepage distance) thus the winding becomes shorter and thicker, which hurts coupling. This is why triple insulation construction is recommended.

**Figure 4. Interleaved winding technique**




As a result, it is not possible to reduce leakage inductance below a certain extent. Practically, for a well assembled transformer, leakage inductance will be about 1 to 3% of the primary inductance.

Interleaved windings technique (putting on half the primary turns first, then the secondary and finally the other half of the primary, see fig. 4) may considerably reduce leakage inductance (theoretically almost four times). The two primary halves must be series connected, never paralleled. Other tricks, such as spacing windings evenly across a layer (when they do not completely fill it), or using multiple strands of wire, or keeping isolation between windings to a minimum are also effective. Besides, the use of split bobbins is not recommended.

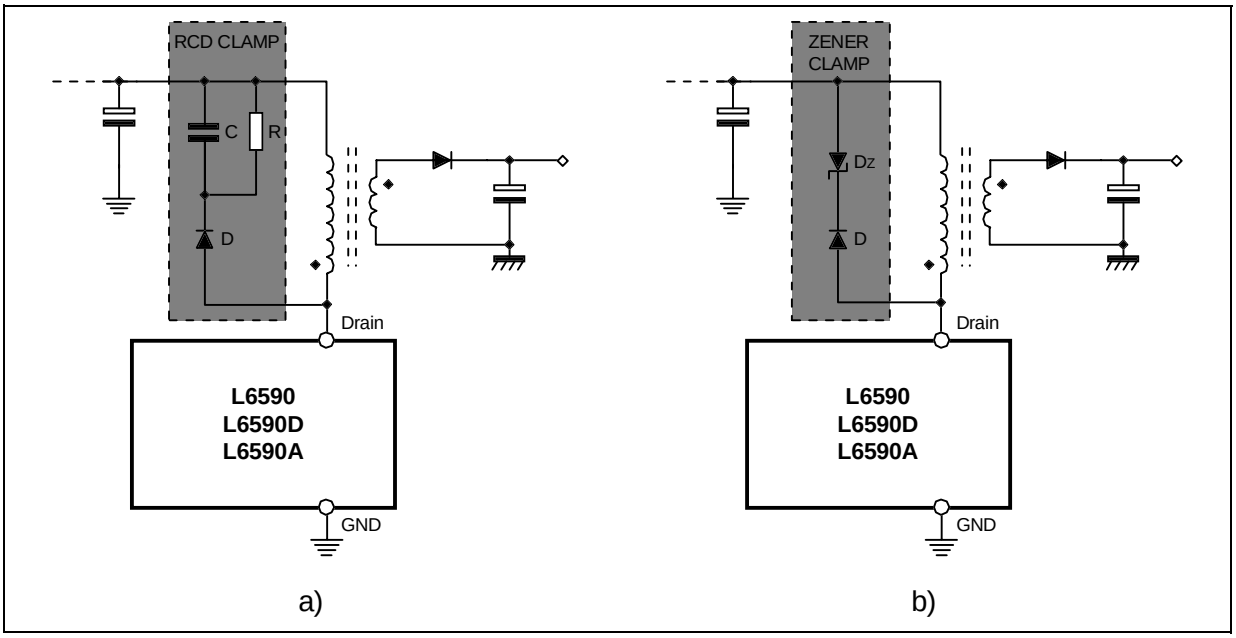
Primary winding capacitance is the major component of the $C_{drain}$ capacitance earlier mentioned. Besides contributing to internal MOSFET power losses, it causes ringing and noise problems that may force the use of additional damping networks to comply with EMC requirements.

To achieve a low capacitance, always wind first the primary winding and, in particular, the half whose end is to be connected to the drain of the MOSFET. In this way the second half primary has a shielding effect that reduces the capacitive coupling. In case of multiple layer windings, which exhibit higher capacitance, it is useful to embed one layer of isolation between two adjacent winding layers. This, however, tends to increase leakage inductance and therefore should be done with care.

## 10 CLAMP CIRCUIT DESIGN

The drain pin of the IC needs to be properly clamped to prevent the spike due to the transformer leakage inductance from exceeding the breakdown voltage (700V minimum). An RCD clamp (see fig. 5a) is a popular cheap solution, however it dissipates power even under no-load conditions: there is at least the reflected voltage $V_R$ across the clamp resistor at all times. If minimizing the light load losses is a must, the use of a zener or transil clamp (see fig. 5b) is recommended whenever possible. Such circuit gives also a better defined clamping level but dissipates more power at full load.

**Figure 5. Suggested clamp circuit topologies**




The clamp may not be necessary in a $110V_{AC}$ operated converter but, before giving up this circuit, it is important to check carefully the spike under overload and start-up conditions to make sure that the voltage rating of the MOSFET is never exceeded.

*RCD clamp*. The clamp capacitor is charged by the energy stored in the leakage inductance and must ensure that the maximum allowed overvoltage $V_{spike}$ is never exceeded, even under short circuit conditions (when the peak primary current is $I_{lim}$ = 0.7 A). Its minimum value will be then:

$$C_{min} = \frac{L_{LK} \cdot I_{lim}^2}{(V_R + V_{spike})^2 - V_R^2}$$

The capacitor must be low-loss type (with polypropylene or polystyrene film dielectric) to reduce power dissipation and prevent overheating due to the high peak currents it experiences.

The minimum value of the clamp resistance is:

$$R_{min} = \frac{1}{f_{sw} \cdot C_{min} \cdot \ln\left(1 + \frac{V_{spike}}{V_R}\right)},$$

and its power rating has to be:

$$P_R = \frac{V_R^2}{R_{min}} + \frac{1}{2} \cdot L_{LK} \cdot I_{lim}^2 \cdot f_{sw}$$

Usually the resistor value will be selected much higher than the minimum to reduce losses. The clamp capacitor will then be quite larger than the minimum as well.

The blocking diode must be not only very fast-recovery but also very fast-turn-on type to avoid additional drain overvoltage. A 1A rated diode with a breakdown voltage at least $V_{PKmax} + V_R$ is needed. Table 12 shows the suggested ST parts.

**Table 12. Recommended ST parts for blocking diode.**

| 110 $V_{AC}$ | | | 220 $V_{AC}$ or WRM | | |
|---|---|---|---|---|---|
| **Diode** | **$V_{RRM}$** | **Package** | **Diode** | **$V_{RRM}$** | **Package** |
| BYT01-400 | 400 | F126 | STTA106 | 600 | F126 |
| SMBYT01-400 | 400 | SMB | STTA106U | 600 | SMB |

*Zener clamp.* The Transil (or zener) clamp voltage should be equal to:

$$V_{CL} = V_R + V_{spike} \quad (16)$$

Usually Transils are rated by their stand-off Voltage $V_{RM}$ at 25°C temperature, which is defined at low current, whereas the desired clamp voltage is to be considered at operating junction temperature and $I_{lim}$ current.

To take this into consideration, as a rule of thumb the stand-off voltage can be selected as high as 70% of the desired clamp level. Please refer to [2] and [3] to see how these problems are handled.

The Transil or zener must have an adequate power handling capability in steady state operation:

$$P_Z = \frac{1}{2} \cdot \frac{V_{CL}}{V_{CL} - V_R} \cdot L_{LK} \cdot I_{lim}^2 \cdot f_{sw} .$$

Table 13 lists some recommended devices available from ST.

The same recommendations as in the RCD clamp case apply to the blocking diode in series to the Transil. Only the breakdown voltage could be derated to $V_{PKmax}$.

**Table 13. Recommended ST parts for clamping.**

| **VR** | **Pz ≤ 0.75 W** | **Pz = 1W** | **Pz = 1.5W** |
|---|---|---|---|
| ≤100 V | BZW04-154<br>BZW06-154<br>SMAJ154A-TR | BZW04-154<br>BZW06-154<br>SMBJ154A-TR | P6KE180A<br>1.5KE180A<br>SMCJ154A-TR |
| 130 V | BZW04-188<br>BZW06-188<br>SMAJ188A-TR | BZW04-188<br>BZW06-188<br>SMBJ188A-TR | P6KE200A<br>1.5KE200A<br>SMCJ188A-TR |

## 11 SECONDARY RECTIFIER SELECTION

Although the converter is operated in DCM, it is recommended to use an ultrafast p-n diode or, whenever allowed by the reverse voltage, a Schottky type. The latter, besides optimizing the reverse recovery, minimizes conduction losses as well.

The voltage rating will be higher than the maximum reverse voltage it experiences:

$$V_{REV} = V_{out} \cdot \left(1 + \frac{V_{PKmax}}{V_R}\right), \quad (17)$$

with a suitable safety margin (usually 20-25%). As to its current rating, it is a common design practice to choose a diode rated for 2-3 times the DC output current $I_{out}$. Table 14 lists some recommended devices available from ST assuming $V_R$ = 130 V. In each cell of the table there are two recommended devices, the first one is an axial or through-hole diode and the second one is in SMD package. The sale types in italic are p-n diodes, the others are Schottky type.

**Table 14. Recommended ST parts for secondary rectification.**

| | 110 $V_{AC}$ | | | 220 $V_{AC}$ or WRM | | |
|---|---|---|---|---|---|---|
| $V_{out}$ (V) | $P_{out}$≤5W | $P_{out}$=7.5W | $P_{out}$=10W | $P_{out}$≤5W | $P_{out}$=7.5W | $P_{out}$=10W |
| 3.3 | 1N5820<br>STPS5L25B | STPS5L25B-1<br>STPS5L25B | STPS10L25D<br>STPS10L25G | 1N58210<br>STPS3L25S | STPS5L25B-1<br>STPS5L25B | STPS10L25D<br>STPS10L25G |
| 5 | 1N5820<br>STPS5L25B | 1N5820<br>STPS5L25B | STPS10L25D<br>STPS10L25G | 1N5821<br>STPS340C | 1N5822<br>STPS340B | STPS640CT<br>STPS640CB |
| 9 | 1N5821<br>STPS2L30A | 1N5821<br>STPS340B | 1N5822<br>STPS340B | –<br>STPS160U | –<br>STPS3L60S | STPS5H100-1<br>STPS3L60S |
| 12 | 1N5819<br>STPS1L40A | 1N5822<br>STPS3L60S | –<br>STPS3L60S | –<br>STPS1H100U | –<br>STPS2H100U | STPS5H100B-1<br>STPS2H100U |
| 15 | BYV10-60<br>STPS160A | BYV10-60<br>STPS160A | –<br>STPS3L60S | –<br>STPS1H100U | –<br>STPS2H100U | STPS5H100B-1<br>STPS2H100U |
| 18 | BYV10-60<br>STPS160A | BYV10-60<br>STPS1H100U | *BYW98-100*<br>STPS2H100U | –<br>STPS1H100U | –<br>STPS2H100U | STPS5H100B-1<br>STPS2H100U |
| 24 | BAT49<br>STPS1H100A | –<br>STPS1H100U | –<br>STPS1H100U | *BYW100-200*<br>*STPR120A* | *BYW100-200*<br>*STPR120A* | *BYW100-200*<br>*SMBYW02-200* |

## 12 OUTPUT CAPACITOR SELECTION AND POST FILTER

Large, low-ESR electrolytic capacitors usually do the filtering work. The parameters to be considered for their selection are the working voltage, RMS ripple rating and ESR, the actual capacitance value is of secondary importance.

Obviously, the DC working voltage must be greater than $V_{out}$. A margin of 25% is recommended for the sake of reliability.

The AC current the output capacitor undergoes causes power dissipation on its ESR and a resulting temperature rise. This is the major responsible for capacitor degrading. Thus it is important not to operate the capacitor beyond its AC current ripple rating, otherwise its lifetime will be considerably shortened. This parameter is usually specified at 85°C or 105°C ambient temperature, depending on capacitor's quality. The value could be derated considering the actual maximum ambient temperature ($T_{amb}$) and the capacitor's target lifetime. For a conservative design no derating will be applied. The AC current capability must then be larger than $Is_{AC}$ and

may be achieved by using paralleled capacitors.

ESR, besides being responsible for capacitor heating, is what basically determines the switching frequency voltage ripple superimposed on top of the DC value. This is true as long as the capacitive contribution to the ripple is negligible, that is if:

$$C_{out} >> 100 \cdot \frac{I_{out} \cdot D_x}{V_{r\%} \cdot V_{out} \cdot f_{sw}} \quad (18)$$

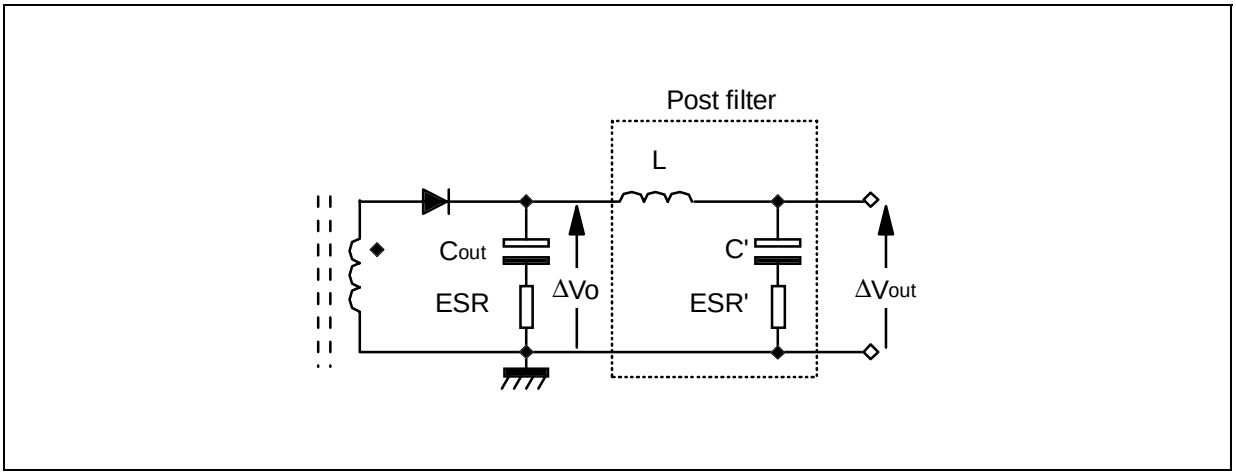
The specification on the maximum allowed output ripple is then translated into a requirement on the maximum ESR of the capacitor:

$$ESRx = \frac{V_{r\%}}{100} \cdot \frac{V_{out}}{Is_{pk}} \quad (19)$$

Anyway, once the specification on either the AC ripple current or the ESR is fulfilled, the resulting capacitance value definitely meets condition (18).

If the requirement on ESR is very tight, there is an alternative to using a large number of output capacitors: it is possible to tolerate a higher ripple on $C_{out}$ (provided the AC ripple requirement is met) and add an LC post filter, like the one shown in fig. 6, that attenuates the ripple to the desired level.

**Figure 6. Output post filter for ripple reduction**




The attenuation factor of such filter is approximately given by:

$$Ka = \frac{\Delta V_{out_{p-p}}}{\Delta V_{Op-p}} \approx D \cdot (1-D) \cdot \frac{ESR'}{f_{sw} \cdot L}$$

which is the same for complementary duty cycles and minimum for D=0.5. Thus, to get the desired attenuation factor the following design equations can be applied:

$$Ka = \frac{ESR'}{4 \cdot f_{sw} \cdot L} \quad \text{for } Dx > 0.5 \qquad Ka = Dx \cdot (1-Dx) \cdot \frac{ESR'}{f_{sw} \cdot L} \quad \text{for } Dx < 0.5$$

It is convenient to choose an off-the-shelf choke and then select a capacitor with an ESR low enough to get the desired attenuation level. For low output current (less than 1 A) ferrite beads may be used. At any rate, the DC current rating of the choke should be oversized to minimize DC voltage drop. In fact, the feedback should be connected upstream the post filter to avoid stability problems (see "Control loop compensation" section).

## 13 SELF-SUPPLY CIRCUIT DESIGN

To define the self-supply circuit it is necessary to select the bias rectifier and the supply capacitor (see fig. 7) since the turns number of the auxiliary winding has been defined already.

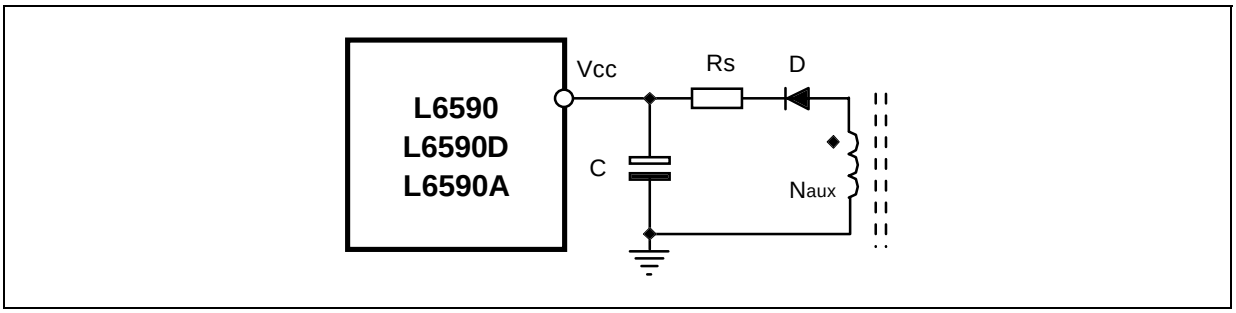
The bias rectifier has to withstand a reverse voltage equal to:

$$V_{REV} = V_{CC} \cdot \left(1 + \frac{V_{PKmax}}{V_R}\right)$$

with an appropriate safety margin of 20-25%. The current rating is of little concern since the diode has to carry few mA. A popular 1N4148 (75V rating) or an UF4003 (200V rating) may be suitable choices.

The supply capacitor has to be large enough to keep the device running during the time needed for the auxiliary winding to develop its correct voltage at start-up. A minimum value of 10 µF is recommended and any low cost electrolytic capacitor will do the job. The resistor Rs in series to D filters the voltage spike appearing on the positive-going edge of the voltage generated by the self-supply winding that causes the voltage Vcc to increase with the converter's output load. The optimum value depends on the transformer's stray parameters (mainly the coupling between the auxiliary and the secondary winding) and can be found empirically once the transformer spec and construction have been frozen. A small and inexpensive axial inductor in the range of 1 to 10µH may be used instead of $R_S$, with even better results.

**Figure 7. Self-supply circuit**




## 14 BROWNOUT PROTECTION DESIGN (L6590A AND L6590D ONLY)

With reference to the schematic of fig. 8, the following relationships can be established for the ON ($V_{inON}$) and OFF ($V_{inOFF}$) thresholds of the input voltage:

$$V_{inON} \cdot \frac{R2}{R1 + R2} = 2.5,$$

$$\frac{V_{inOFF} - 2.5}{R1} + 50 \cdot 10^{-6} = \frac{2.5}{R2}.$$

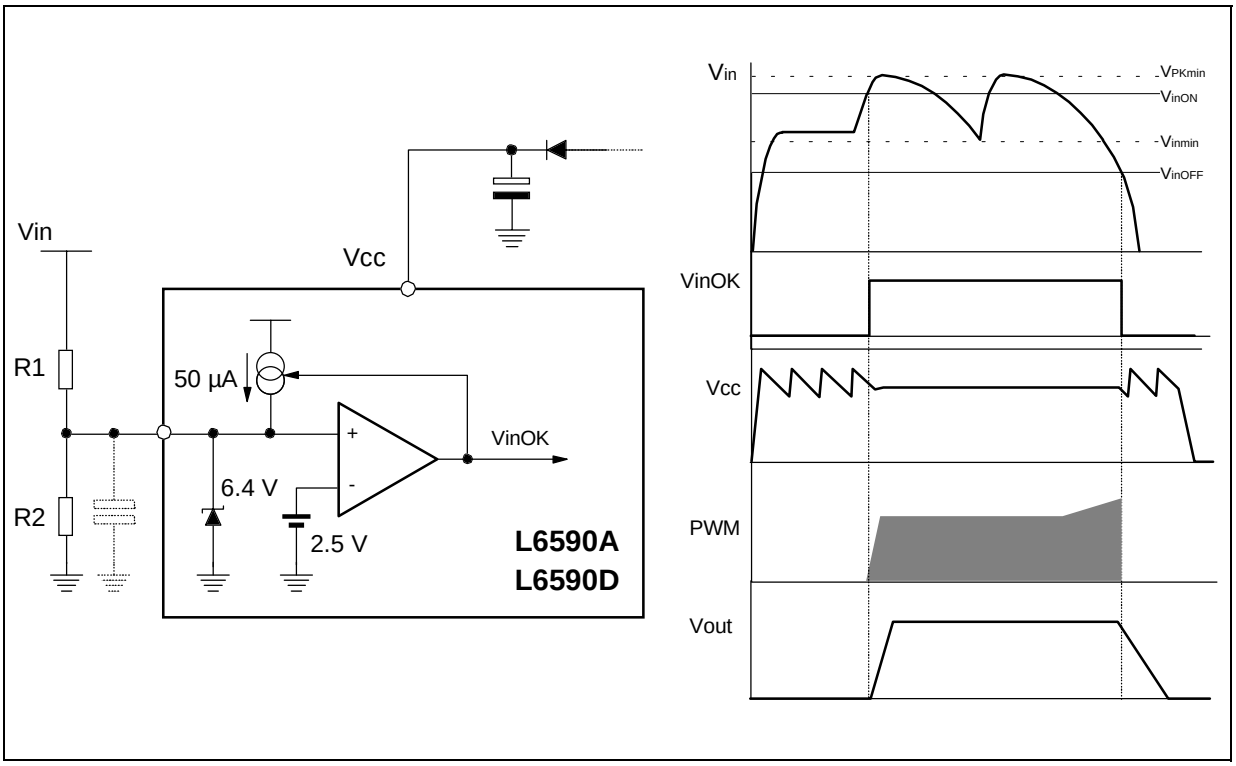
Solving for R1 and R2:

$$R1 = \frac{V_{inON} - V_{inOFF}}{50 \cdot 10^{-6}}$$

$$R2 = R1 \cdot \frac{2.5}{V_{inON} - 2.5}$$

For a proper operation of this function, $V_{inON}$ must be less than $V_{PKmin}$ and $V_{inOFF}$ less than $V_{inmin}$ (see the timing diagram of figure 8).

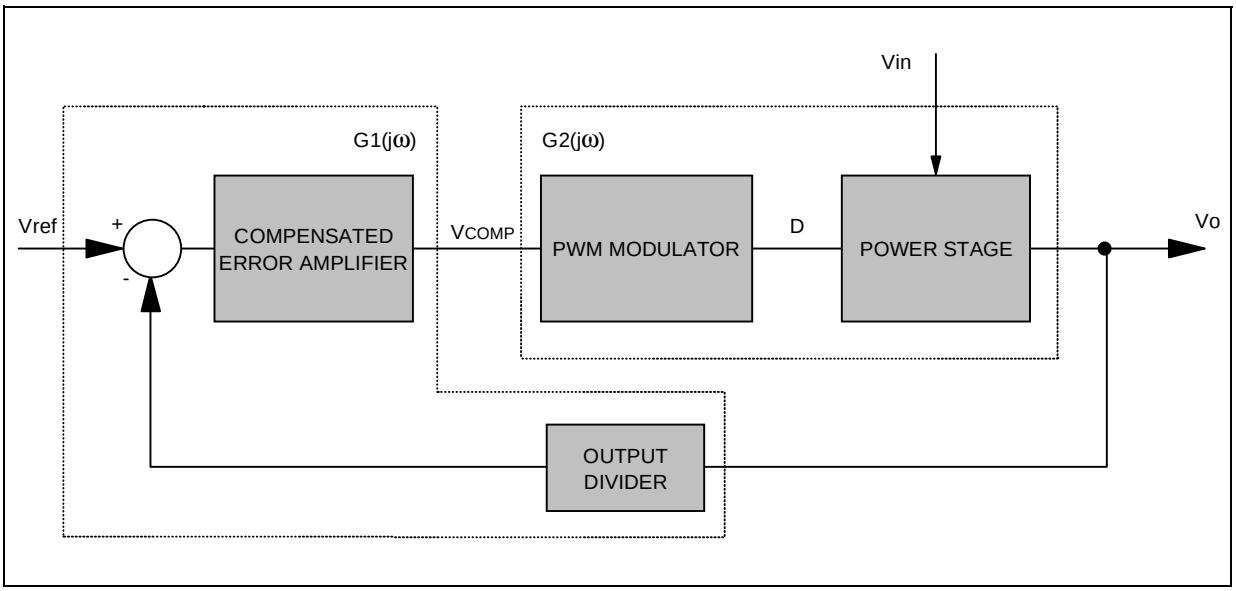
**Figure 8. Brownout protection circuit and timing diagram**




## 15 CONTROL LOOP DESIGN

The control loop can be summarized as shown in figure 9, where each block is described by its transfer function in the complex frequency domain represented by means of a Bode plot.

**Figure 9. Control loop Block Diagram**




The set PWM modulator + Power stage is what, in control theory terminology, is called the "plant", while the compensated error amplifier is the "controller".

The transfer function G2(jω) of the plant is defined by the control method (voltage mode), the topology of the converter (flyback) and its operating mode (DCM in the specific case). The task of the control loop design is then to determine the transfer function G1(jω) of the error amplifier and define the relevant frequency compensation network. The objective of the design is to ensure that the resulting closed-loop system will be stable and well performing in terms of dynamic response, line and load regulation.

The characteristics of the closed-loop system can be inferred from its open-loop properties. Provided the open-loop gain crosses the 0 dB axis only once at f= $f_c$ (crossover frequency), stability will be ensured if the gain phase shift (besides the 180° due to negative feedback) is less than 180° at f = $f_c$. This is the well-known Nyquist's stability criterion.

Anyway, adequate margin to this boundary condition must be provided to prevent instability due to parameter variations and to optimize the dynamic response that would be severely underdamped otherwise. Under worst case condition this "phase margin" $\Phi_m$ should never go below 20 or 30°. Typically, $\Phi_m$ = 45° in nominal conditions is used as a design guideline: this ensures fast transient response with very little ringing. Sometimes a higher margin (up to 60° or 75°) is required to account for very large spreads in line, load and temperature changes as well as manufacturing tolerances.

Although Nyquist's criterion allows the phase shift to be over 180° at a frequency below $f_c$, this is not recommended because it would result in a conditionally stable system. A reduction of the gain (which may temporarily happen during large load transients) would cause the system to oscillate, therefore the phase shift should not get close to 180° at any frequency below $f_c$.

Optimum dynamic performance requires a large gain bandwidth, that is the crossover frequency $f_c$ to be pushed as high as possible ($\leq f_{sw}/4$). When optimum dynamic performance is not a concern, $f_c$ will be typically chosen equal to $f_{sw}/10$.

Good load and line regulation implies a high DC gain, thus the open loop gain should have a pole at the origin. In this way the theoretical DC gain would tend to infinity, whereas the real-world one will be limited by the low-frequency gain of the Error Amplifier. Since voltage mode control has poor open-loop line regulation, the overall gain should be still high also at frequencies around 100-120 Hz to maximize rejection of the input voltage ripple. This is related to phase margin: a higher phase margin leads to a lower low-frequency gain.

Once the goal of the design has been established in terms of crossover frequency and phase margin, the next step is to determine the transfer function of the plant G2(jω) in order to select an appropriate structure for G1(jω).

The transfer function G2(jω) of the plant is described in Tab. 15, while its asymptotic Bode plot is illustrated in Fig.10.

In $G2_0$ definition the ratio $D_{max}/Vs$ is the PWM modulator gain, while $D_{max}$ = 0.7 is the maximum duty cycle and $V_s$ = (3.5-1.5) = 2 V is the oscillator peak-to-valley swing (see the relevant section). $R_{out} = V_{out}/I_{out}$ is the equivalent load resistor.

This kind of plant will be stabilized in closed-loop operation by what is commonly known as a Type 2 amplifier. Its transfer function G1(jω), which comprises a pole at the origin and a zero-pole pair, is defined as:

$$G1(j\omega) = \frac{G1_0}{j\omega} \cdot \frac{1 + \frac{j\omega}{\omega_Z}}{1 + \frac{j\omega}{\omega_P}}$$

Its asymptotic Bode plot is illustrated in Fig. 11.

The main task of this correction is to boost the phase of the overall loop (actually, to reduce the phase lag of G2(jω)) in the neighborhood of the crossover frequency.

**Figure 10. Plant transfer function G2(jω) of DCM Flyback (Bode Plots)**

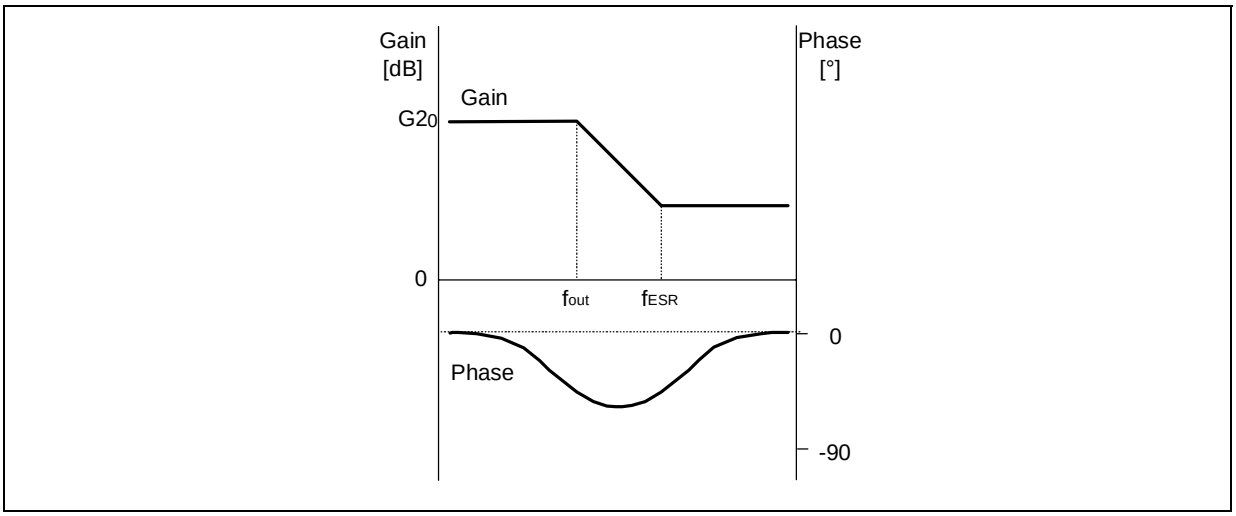
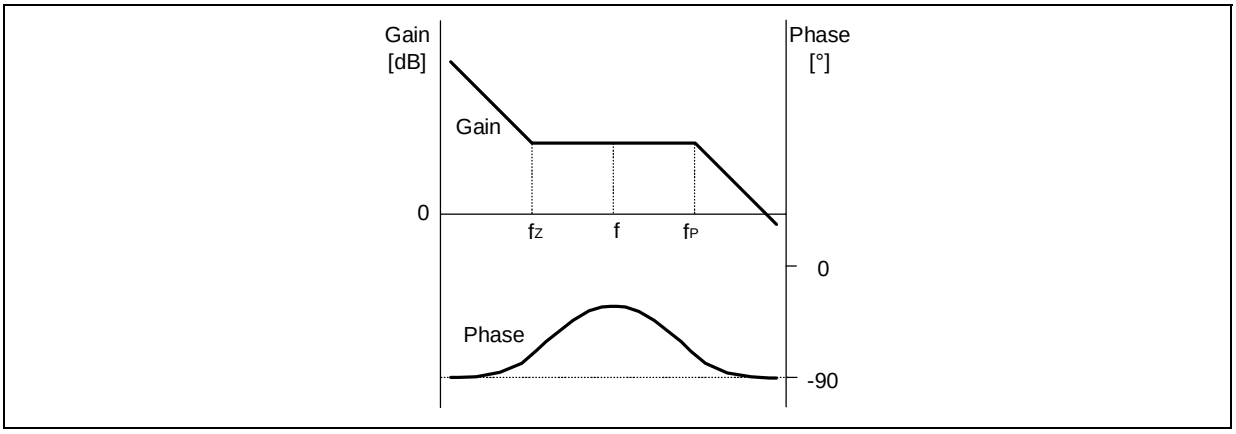



**Table 15. Plant Transfer Function and its Main Quantities**

| Symbol | Definition |
|---|---|
| G2(jω) | $G2(j\omega) = G2_0 \cdot \frac{1 + \frac{j\omega}{\omega_{ESR}}}{1 + \frac{j\omega}{\omega_{out}}}$ |
| $G2_0$ | $G2_0 = \frac{D_{max}}{V_s} \cdot V_{in} \cdot \sqrt{\frac{R_{out}}{2 \cdot Lp \cdot f_{sw}}}$ |
| $f_{ESR}$ | $f_{ESR} = \frac{\omega_{ESR}}{2 \cdot \pi} = \frac{1}{2 \cdot \pi \cdot ESR \cdot C_{out}}$ |
| $f_{out}$ | $f_{out} = \frac{\omega_{out}}{2 \cdot \pi} = \frac{1}{\pi \cdot R_{out} \cdot C_{out}}$ |

**Figure 11. Controller Transfer Function G1(jω) (Bode Plots)**



The synthesis of G1(jω) can be done by following the following step-by-step procedure:

a) Calculate gain and phase of G2(jω) at the desired crossover frequency ($f_c$). That is:

$$G2_c = \left|G2(2 \cdot \pi \cdot f_c)\right|$$

$$\Phi 2_c = \frac{180}{\pi} \cdot \arg[G2(2 \cdot \pi \cdot f_c)] ;$$

G2(jω) will be calculated at maximum input voltage and maximum load, where the gain-bandwidth product is maximum.

b) Calculate gain and phase of G1(jω) at $f = f_c$ in order for the overall open-loop gain to cross the 0 dB axis at $f = f_c$ with the phase margin $\Phi_m$:

$$G1_c = \left|G1(2 \cdot \pi \cdot f_c)\right| = \frac{1}{G2_c} ;$$

$$\Phi 1_c = \frac{180}{\pi} \cdot \arg[G1(2 \cdot \pi \cdot f_c)] = -180 + \Phi_m - \Phi 2_c ,$$

c) Cancel the pole of G2(jω) by placing the zero of G1(jω) in the neighborhood:

$$f_Z = \frac{\omega_Z}{2 \cdot \pi} = \alpha \cdot \frac{\omega_{out}}{2 \cdot \pi} \quad (\alpha = 1 \text{ to } 5)$$

d) Place the pole of G1(jω) so as to get the desired phase margin:

$$f_P = \frac{\omega_P}{2 \cdot \pi} \approx \frac{f_C}{\left|\tan\left(\frac{\pi}{180} \cdot \Phi 1_c\right)\right|} ,$$

e) Calculate the unity gain frequency $G1_0$:

$$G1_0 \approx 2 \cdot \pi \cdot G1_c \cdot \frac{f_c \cdot f_Z}{f_P}$$

The synthesis of G1(jω) is completed. The following step will concern the practical implementation of such function, that is the realization of a Type 2 amplifier. This will be done considering two cases, the secondary and the primary sensing feedback.

## 16 SECONDARY FEEDBACK IMPLEMENTATION

This kind of feedback, shown in fig. 12, uses a popular arrangement with a TL431 as secondary reference/error amplifier and an optocoupler to transfer the control signal to the primary side. The error amplifier of the IC is then used as a current source whose characteristic is shown in fig. 12 as well: the voltage $V_{COMP}$ is changed (and the duty cycle is controlled) by modulating the current Ic sunk from the pin. A change of Ic causes a change of $V_{COMP}$ corresponding to a resistance $R_{COMP}$ = 9 kΩ. The resulting transfer function is:

$$G1(j\omega) = \frac{\Delta V_{COMP}}{\Delta V_{out}} = \frac{\Delta V_{COMP}}{\Delta I_C} \cdot \frac{\Delta I_C}{\Delta I_F} \cdot \frac{\Delta I_F}{\Delta V_K} \cdot \frac{\Delta V_K}{\Delta V_{out}} = \frac{CTR_{max} \cdot R_{COMP}}{R_B \cdot R_H \cdot C_F} \cdot \frac{1}{j\omega} \cdot \frac{1 + j\omega \cdot (R_H + R_F) \cdot C_F}{1 + j\omega \cdot R_{COMP} \cdot C_{COMP}}$$

and table 16 shows how its quantities are defined

**Figure 12. Secondary feedback: TL431 + optocoupler circuit (I)**

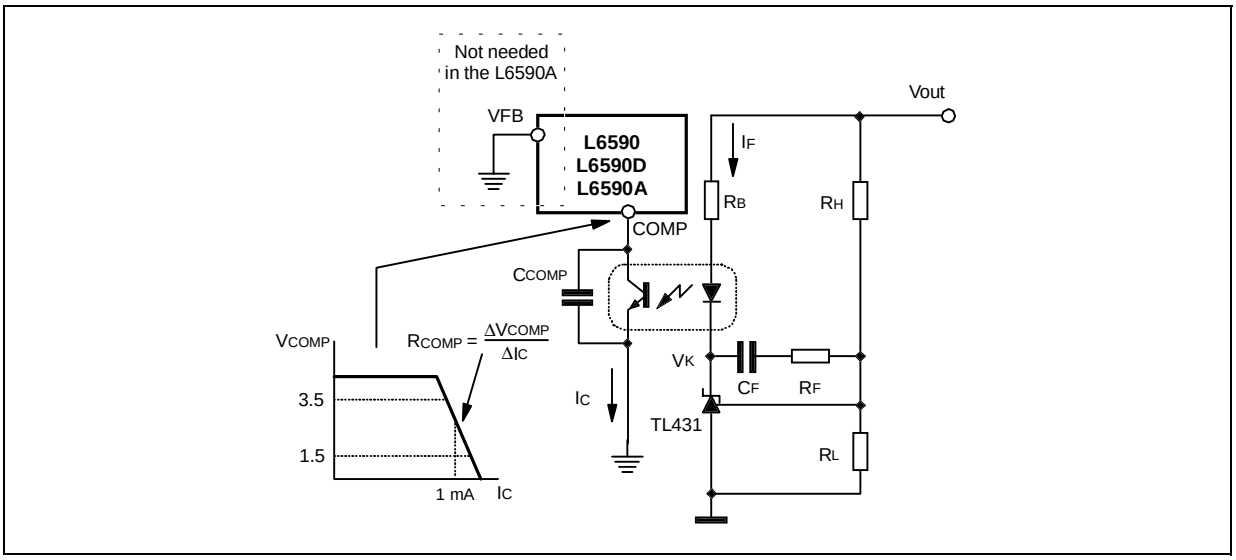



**Table 16. G1(jω) Implementation: secondary feedback (I)**

| Symbol | Definition |
|---|---|
| $R_L$ | $R_L \approx 0.27$ to $2.7$ [kΩ] |
| $R_H$ | $R_H = \frac{V_{out} - 2.5}{2.5} \cdot R_L$ |
| $R_B$ | $R_B < CTR_{min} \cdot \frac{V_{out} - 3.5}{I_{Cmax}}$ |
| $C_F$ | $C_F = \frac{CTR_{max} \cdot R_{COMP}}{R_B \cdot R_H \cdot G1_0}$ |
| $R_F$ | $R_F = \frac{1}{2 \cdot \pi \cdot f_Z \cdot C_F} - R_H$ |
| $C_{COMP}$ | $C_{COMP} = \frac{1}{2 \cdot \pi \cdot f_P \cdot R_{COMP}}$ |

This technique provides very good regulation of the output voltage and galvanic isolation from the primary side at the same time.

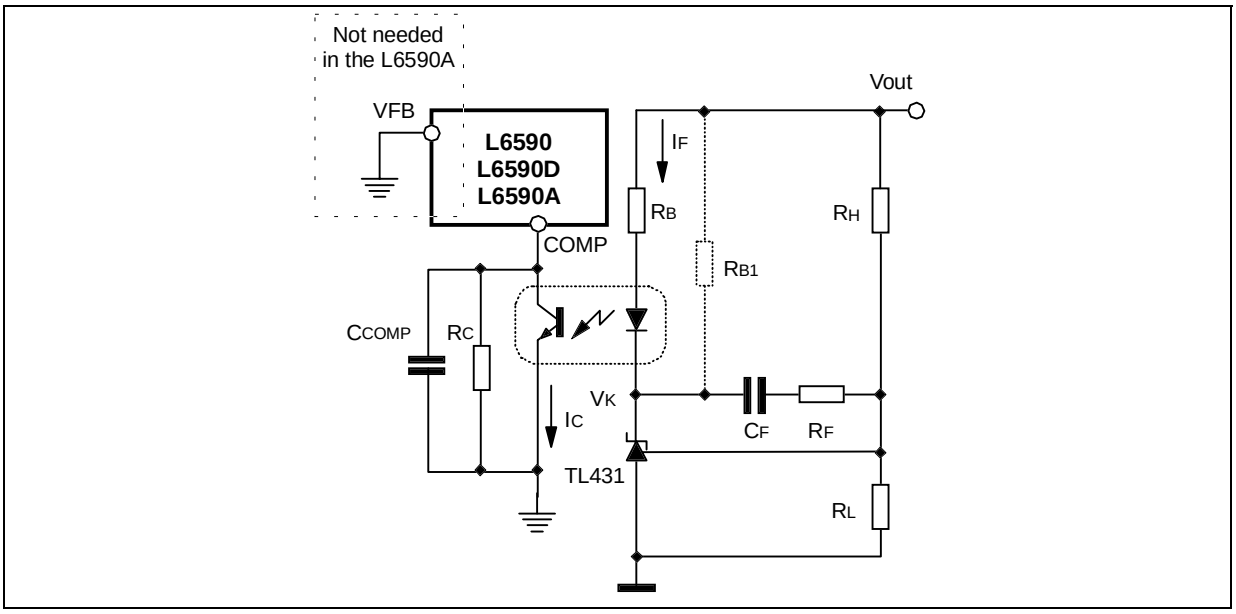
In Table 16 it is possible to find the design relationships useful to derive the part values. Icmax is specified in the Datasheet (2.5mA).

The following condition should be met:

$$\frac{CTR_{max}}{CTR_{min}} \leq G1_c \cdot \frac{\left|\tan\left(\frac{\pi}{180} \cdot \Phi 1_c\right)\right|}{R_{COMP}} \cdot \frac{V_{out} - 3.5}{I_{Cmax}}, \quad (20)$$

otherwise t will not be possible to find a positive value for $R_F$. If the condition (20) is not met, an optocoupler with a narrower $CTR_{min}$ - $CTR_{max}$ spread should be selected. If that is not possible, either a higher $f_c$ or a lower $\Phi_m$ should be selected and the calculations from step a) to step e) redone.

**Figure 13. PWM gain reduction by $R_C$ (secondary feedback II).**




A resistor $R_C$ in parallel to $C_{COMP}$, as shown in fig. 13, is useful to reduce the PWM gain $\Delta V_{COMP}/\Delta I_C$. In fact, the resistor comes dynamically in parallel to $R_{COMP}$, thus reducing the equivalent value appearing at the numerator of the gain. Moreover, since it diverts part of the current sourced by the pin COMP, the opto's transistor carries less current and a slightly higher bias resistor $R_B$ can be used, thus giving some extra gain reduction. An additional resistor, $R_{B1}$, of some kΩ could be needed to guarantee sufficient bias to the TL431.

To be able to exploit the full dynamics of the error amplifier under worst case conditions, $R_C$ must not be lower than 7 kΩ, which reduces the gain by a 1/0.35 ≅ 2.86 factor. $R_C$ values lower than 7 kΩ will reduce the gain further on but will reduce also the maximum duty cycle allowed (worst case). Depending on the maximum duty cycle specified for a given application, this can be acceptable.
Table 17 summarizes the situation for different values of $R_C$.

**Table 17. PWM gain reduction for different $R_C$ values**

| $R_C$ (kΩ) | $R_C$ // $R_{COMP}$ (kΩ) | $D_{max}$ | PWM Gain Reduction | $K_B$ ($R_B$ multiplier) | Total Gain Reduction |
|---|---|---|---|---|---|
| 7.5 | 4.09 | 0.7 | 2.2 | 1.24 | 2.73 |
| 7 | 3.94 | 0.7 | 2.29 | 1.25 | 2.86 |
| 6.8 | 3.87 | 0.68 | 2.32 | 1.25 | 2.91 |
| 6.2 | 3.67 | 0.62 | 2.45 | 1.27 | 3.11 |
| 5.6 | 3.45 | 0.55 | 2.61 | 1.28 | 3.34 |
| 5.1 | 3.26 | 0.49 | 2.76 | 1.29 | 3.58 |
| 4.7 | 3.09 | 0.44 | 2.91 | 1.31 | 3.8 |
| 4.3 | 2.91 | 0.38 | 3.09 | 1.32 | 4.07 |
| 3.9 | 2.72 | 0.32 | 3.31 | 1.33 | 4.4 |
| 3.6 | 2.57 | 0.28 | 3.5 | 1.34 | 4.69 |

In this case the design procedure outlined in table 16 should be slightly modified as shown in table 18.

**Table 18. G1(jω) Implementation: secondary feedback (II)**

| Symbol | Definition |
|---|---|
| $R_L$ | $R_L \approx 0.27$ to $2.7$ [kΩ] |
| $R_H$ | $R_H = \frac{V_{out} - 2.5}{2.5} \cdot R_L$ |
| $R_C$, $K_B$ | Select from table 17 |
| $R_B$ | $R_B < CTR_{min} \cdot \frac{V_{out} - 3.5}{I_{Cmax}} \cdot K_B$ |
| $C_F$ | $C_F = \frac{CTR_{max} \cdot (R_{COMP} // R_C)}{R_B \cdot R_H \cdot G1_0}$ |
| $R_F$ | $R_F = \frac{1}{2 \cdot \pi \cdot f_Z \cdot C_F} - R_H$ |
| $C_{COMP}$ | $C_{COMP} = \frac{1}{2 \cdot \pi \cdot f_P \cdot (R_{COMP} // R_C)}$ |

More flexibility is given by the network illustrated in figure 14, applicable with the L6590 and L6590D which have the error amplifier on board.
For this circuit, to be able to find a positive value for $R_F$, the condition is:

$$\frac{CTR_{max}}{CTR_{min}} \leq G1_c \cdot \frac{\left|\tan\left(\frac{\pi}{180} \cdot \Phi 1_c\right)\right|}{R_{F2}} \cdot \left(1 + \frac{R_C}{R_E}\right) \cdot \frac{V_{out} - 3.5}{I_{Cmax}},$$

which is less stringent than (20). The resulting function is:

$$G1(j\omega) = \frac{\Delta V_{COMP}}{\Delta V_{out}} = \frac{\Delta V_{COMP}}{\Delta V_E} \cdot \frac{\Delta V_E}{\Delta I_C} \cdot \frac{\Delta I_C}{\Delta I_F} \cdot \frac{\Delta I_F}{\Delta V_K} \cdot \frac{\Delta V_K}{\Delta V_{out}} = \frac{CTR_{max} \cdot R_E \cdot R_{F2}}{(R_E + R_C) \cdot R_B \cdot R_H \cdot C_{F1}} \cdot \frac{1}{j\omega} \cdot \frac{1 + j\omega \cdot (R_H + R_{F1}) \cdot C_{F1}}{1 + j\omega \cdot R_{F2} \cdot C_{F2}},$$

and Table 19 shows how its quantities are defined.

**Figure 14. Secondary feedback: TL431 + optocoupler circuit (III)**

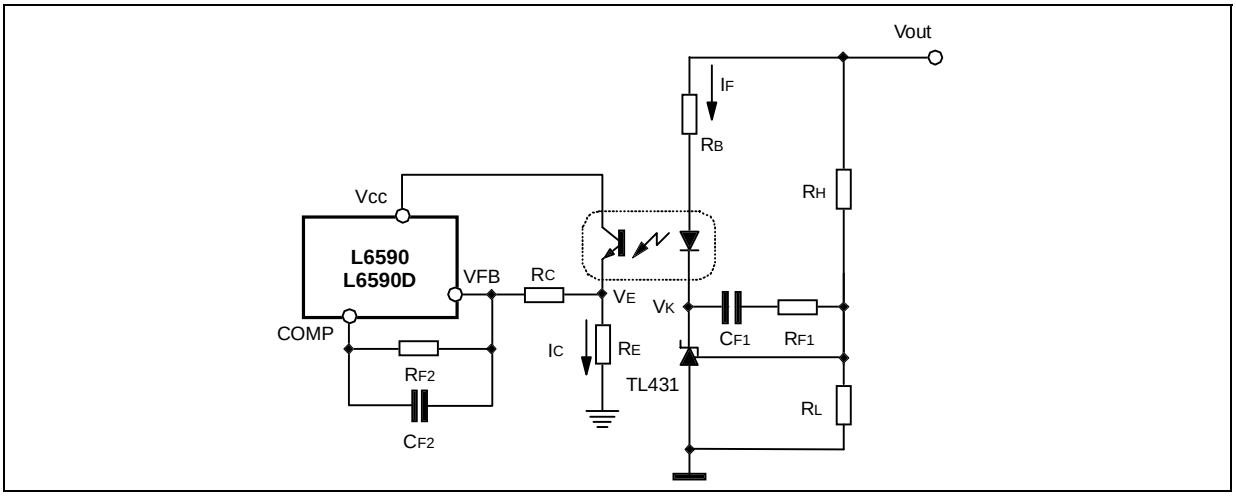


**Table 19. G1(jω) Implementation: secondary feedback (III)**

| Symbol | Definition |
|---|---|
| $R_{F2}$; $R_C$ | $R_{F2} > 2k\Omega \quad ; \quad R_C < 2.5 \cdot R_{F2}$ |
| $R_E$ | $R_E > 1k\Omega$ |
| $R_L$ | $R_L \approx 0.27$ to $2.7$ [kΩ] |
| $R_H$ | $R_H = \frac{V_{out} - 2.5}{2.5} \cdot R_L$ |
| $R_B$ | $R_B < CTR_{min} \cdot \frac{V_{out} - 3.5}{2.5} \cdot R_E$ |
| $C_{F1}$ | $C_{F1} = \frac{CTR_{max} \cdot R_E \cdot R_{F2}}{(R_E + R_C) \cdot R_B \cdot R_H \cdot G1_0}$ |
| $R_{F1}$ | $R_{F1} = \frac{1}{2 \cdot \pi \cdot f_Z \cdot C_{F1}} - R_H$ |
| $C_{F2}$ | $C_{F2} = \frac{1}{2 \cdot \pi \cdot f_P \cdot R_{F2}}$ |

Figure 15 shows a special configuration, with the optocoupler connected in series to the supply pin of the IC that provides the following benefits:

a) a large range of the voltage generated by the auxiliary winding can be allowed since the changes are "damped" by the phototransistor and Vcc is stabilized by the error amplifier; this is useful with a poor quality transformer or when the output voltage (tracked by the auxiliary voltage) may decrease because of constant current regulation (e.g. battery chargers, see fig.40 on L6590's datasheet).

b) during overload and short circuit the power throughput is automatically reduced because the operation of the device becomes intermittent. In fact, the phototransistor carries the quiescent current $I_Q$ of the IC and, if the output voltage is too low, there will not be enough current through the photodiode at the secondary side to maintain $I_Q$. The device will be switched off as it goes into UVLO.

c) despite the IC's OVP protection is bypassed by such configuration, the system is still protected against optocoupler's failures: if that happens, the phototransistor will no longer be able to supply the IC, which will go into UVLO just like in case of overload or short circuit.

The transfer function of the schematic of Fig. 15 is:

$$G1(j\omega) = \frac{\Delta V_{COMP}}{\Delta V_{out}} = \frac{\Delta V_{COMP}}{\Delta V_{CC}} \cdot \frac{\Delta V_{CC}}{\Delta I_C} \cdot \frac{\Delta I_C}{\Delta I_F} \cdot \frac{\Delta I_F}{\Delta V_K} \cdot \frac{\Delta V_K}{\Delta V_{out}} =$$

$$= CTR_{max} \cdot \frac{R_{F2}}{R_B} \cdot \frac{1}{j\omega \cdot R_{H1} \cdot C_{F1}} \cdot \frac{(1 + j\omega \cdot R_c \cdot C_s) \cdot [1 + j\omega \cdot (R_{H1} + R_{F1}) \cdot C_{F1}]}{[1 + j\omega \cdot (R_{H2} + R_c) \cdot C_s] \cdot (1 + j\omega \cdot R_{F2} \cdot C_{F2})}.$$

The $V_{CC}$ capacitor has a significant effect on the frequency characteristic of this circuit: in particular, it introduces a low-frequency pole that causes a phase lag noxious for the phase margin. This pole needs to be compensated by a zero, which requires an additional resistor ($R_C$) in series to the capacitor.

The zero $(R_{H1} + R_{F1}) \cdot C_{F1}$ will be placed close to the pole due to the $V_{CC}$ capacitor, $(R_{H2}+R_C) \cdot C_S$ so as to compensate it. The pole at the origin and the other zero-pole pair realize a type 2 amplifier (see Table 20 to see how

**Figure 15. Secondary feedback: TL431 + optocoupler circuit (IV)**

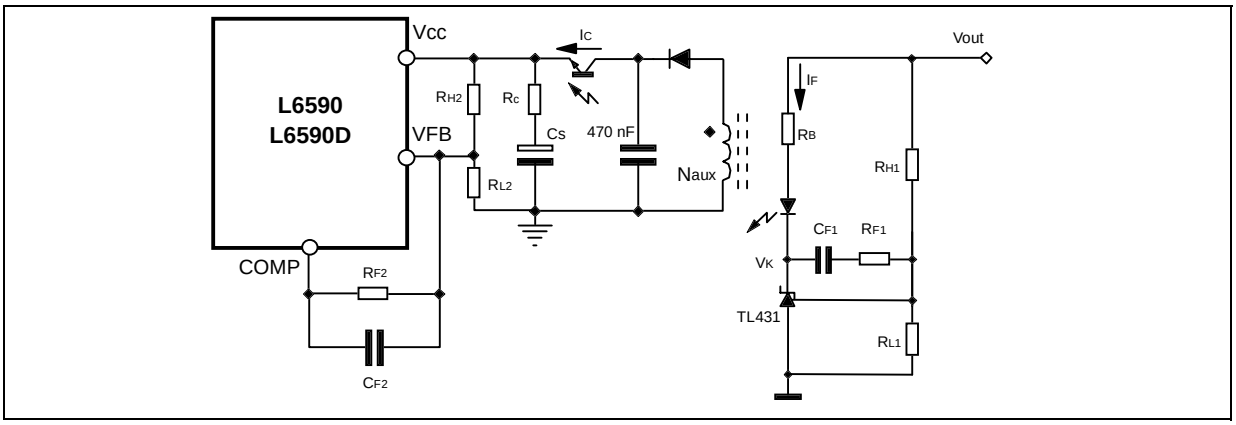



**Table 20. G1(jω) Implementation: secondary feedback (IV)**

| Symbol | Definition |
|---|---|
| $R_{L2}$; $R_{H2}$ | $R_{L2} > \frac{15V}{V_{CC}}$ [kΩ] ; $R_{H2} = \frac{V_{CC} - 2.5}{2.5} \cdot R_{L2}$ |
| $R_{F2}$ | $R_{F2} > 0.4 \cdot R_{H2}$ |
| $R_{L1}$ | $R_{L1} \approx 0.27$ to 2.7 [kΩ]; $R_{H1} = \frac{V_{out} - 2.5}{2.5} \cdot R_{L1}$ |
| $R_B$ | $R_B < CTR_{min} \cdot \frac{V_{out} - 3.5}{I_Q + \frac{2.5}{R_{L2}}}$ |
| $R_C$ | $R_C = \frac{1}{2 \cdot \pi \cdot f_Z \cdot C_S}$ |
| $C_{F1}$ | $C_{F1} = \frac{CTR_{max} \cdot R_{F2}}{R_B \cdot R_{H1} \cdot G_{10}}$ |
| $R_{F1}$ | $R_{F1} = \frac{(R_{H2} + R_C) \cdot C_S}{C_{F1}} - R_{H1}$ |
| $C_{F2}$ | $C_{F2} = \frac{1}{2 \cdot \pi \cdot R_{F2} \cdot f_P}$ |

this network can be designed). The bias resistor of the photodiode will be selected so as to sustain the quiescent current of the L6590 and the current through the divider $R_{H2}$+$R_{L2}$. Please note that the steady state supply voltage Vcc (used in table 20 to choose $R_{L2}$ and $R_{H2}$) has to be sufficiently higher than the UVLO threshold (say 3-4 V, depending on $C_S$). In fact, the PWM starts only when the Vcc voltage has decayed from the start-up threshold to the neighborhood of the steady state value. During this time the PWM is inhibited by the error amplifier, saturated low because the voltage at the pin $V_{FB}$ is higher than 2.5V.

The turn number of the auxiliary winding will be such that the $V_{CE}$ across the phototransistor never falls below 1-2 V, to let it work in its active region. In case of constant current regulation, the variation of the output voltage

must be accounted for as well (the minimum specified value will be considered) and the turn number may result quite high.

## 17 PRIMARY FEEDBACK IMPLEMENTATION

In this approach, which will be considered with regards to the L6590 and the L6590D only, the voltage generated by the self-supply winding is sensed and regulated. This solution, shown in fig. 16, is cheap because no opto-coupler is needed, but provides poor regulation, especially as a result of load changes.

Ideally, the voltage generated by the self supply winding and the output voltage should be related by the $N_{aux}$/Ns turn ratio only. Actually, numerous non-idealities, mainly transformer's parasitics, cause the actual ratio to deviate from the ideal one. Line regulation is quite good, in the range of ± 2%, whereas load regulation is about ±5%. Output voltage tolerance is instead in the range of ±10%. The resulting transfer function is:

$$G1(j\omega) = \frac{\Delta V_{COMP}}{\Delta V_{out}} = \frac{N_{aux}}{N_S} \cdot \frac{\Delta V_{COMP}}{\Delta V_{CC}} = \frac{N_{aux}}{N_S} \cdot \frac{1}{R_H \cdot (C_{Fs} + C_{Fp})} \cdot \frac{1}{j\omega} \cdot \frac{1 + j\omega \cdot R_F \cdot C_{Fs}}{1 + j\omega \cdot R_F \cdot \frac{C_{Fs} \cdot C_{Fp}}{C_{Fs} + C_{Fp}}}.$$

Table 21 shows how its quantities are defined. As to the selection of Vcc, the same considerations concerning the circuit of fig. 15 apply to the circuit in fig. 16a. Such limitation is not in the circuit of fig. 16b.

**Figure 16. Primary feedback: circuits**

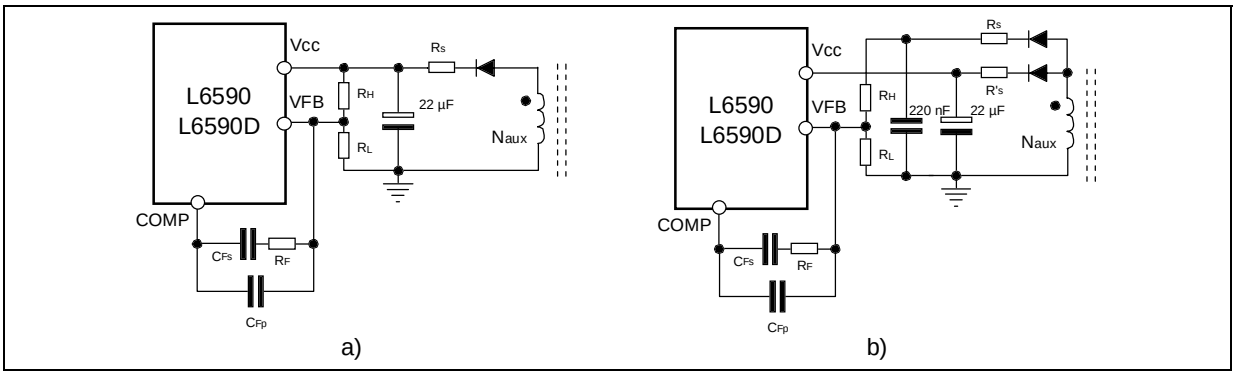


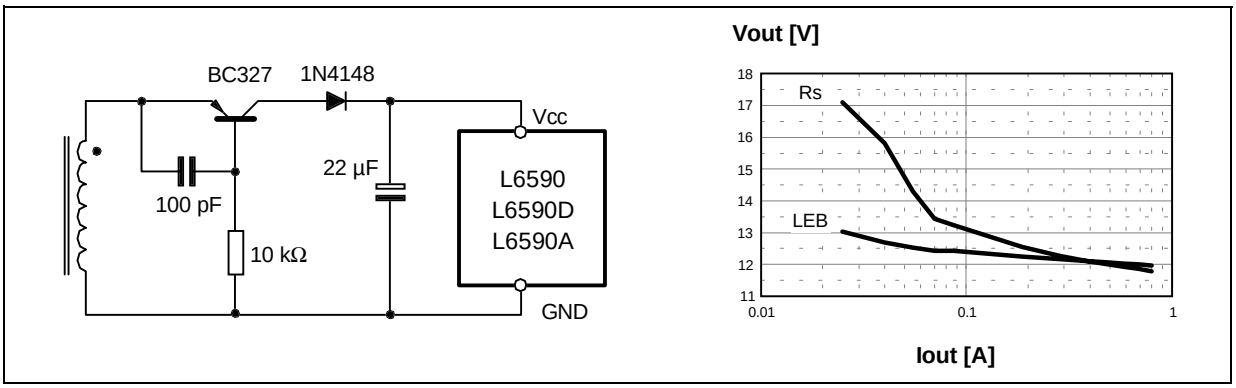

**Table 21. G1(jω) Implementation: Primary Feedback**

| Symbol | Definition |
|---|---|
| $R_L$ | $R_L > \frac{15V}{V_{CC}} \quad [k\Omega]$ |
| $R_H$ | $R_H = \frac{V_{CC} - 2.5}{2.5} \cdot R_L$ |
| $C_{Fp}$ | $C_{Fp} = \frac{N_{aux}}{N_S} \cdot \frac{f_Z}{f_P} \cdot \frac{1}{G1_0 \cdot R_H}$ |
| $C_{Fs}$ | $C_{Fs} = C_{Fp} \cdot \left(\frac{f_P}{f_Z} - 1\right)$ |
| $R_F$ | $R_F = \frac{1}{2 \cdot \pi \cdot f_Z \cdot C_{Fs}}$ |

The value of the resistor Rs (R's for the circuit of fig. 16b) in series to the bias diode will be selected to achieve minimum load regulation and its value may range from few units to some hundred ohm.

The optimum value will be found empirically once the transformer construction has been frozen. Also the divider $R_H$, $R_L$ that sets the $V_{CC}$ voltage (and as a consequence, the output voltage) is likely to need adjustment after bench verification. Some improvement in terms of load regulation can be achieved by using an inductor (typically, between 1 and 10µH) instead of a resistor. Any inexpensive axial inductor able to carry few mA will serve the purpose.

**Figure 17. Leading Edge Blanking (LEB) circuit for leakage inductance spikes filtering**

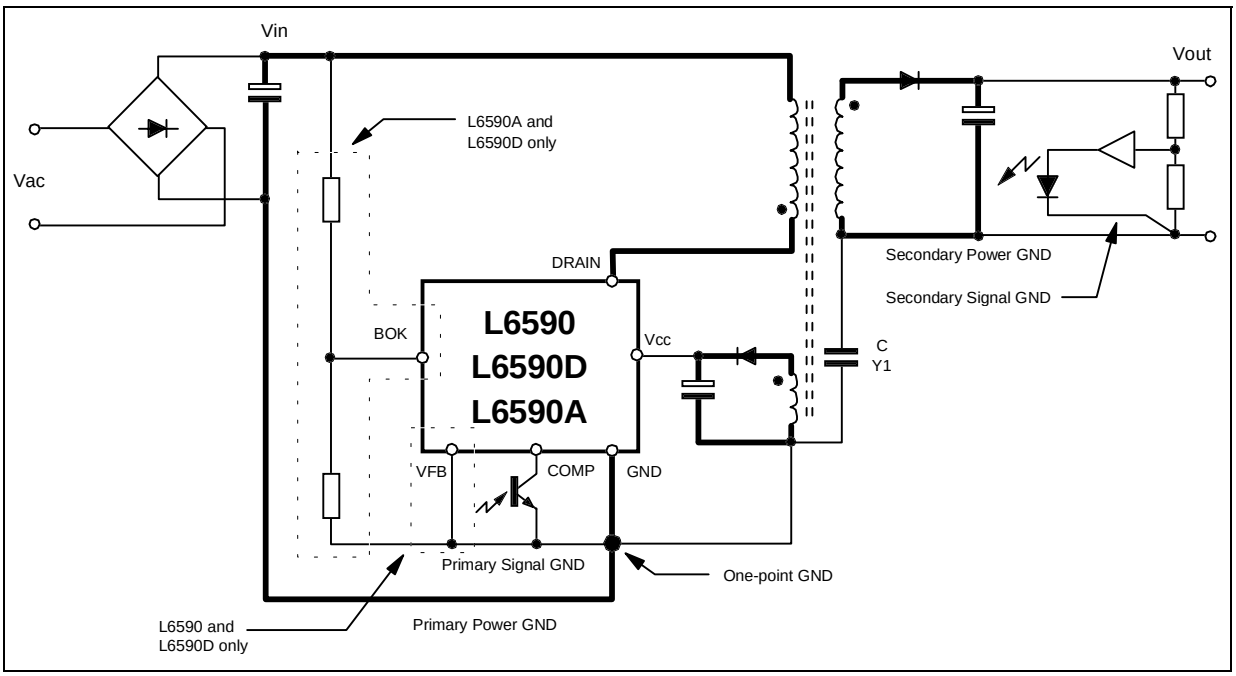



However, the most effective way to improve regulation is to use the circuit shown in figure 17, which blanks the spike appearing at the leading edges of the voltage generated by the self-supply winding. This spike, due to the transformer's leakage inductance, is the major responsible for the poor load regulation.

## 18 LAYOUT RECOMMENDATIONS

A proper printed circuit board (PCB) layout is essential for correct operation of any switch-mode converter and this is true for the devices of the L6590 family as well. Careful component placing, correct traces routing, appropriate traces widths and compliance with isolation distances are the major issues.

**Figure 18. Suggested ground routing for converters with secondary feedback.**

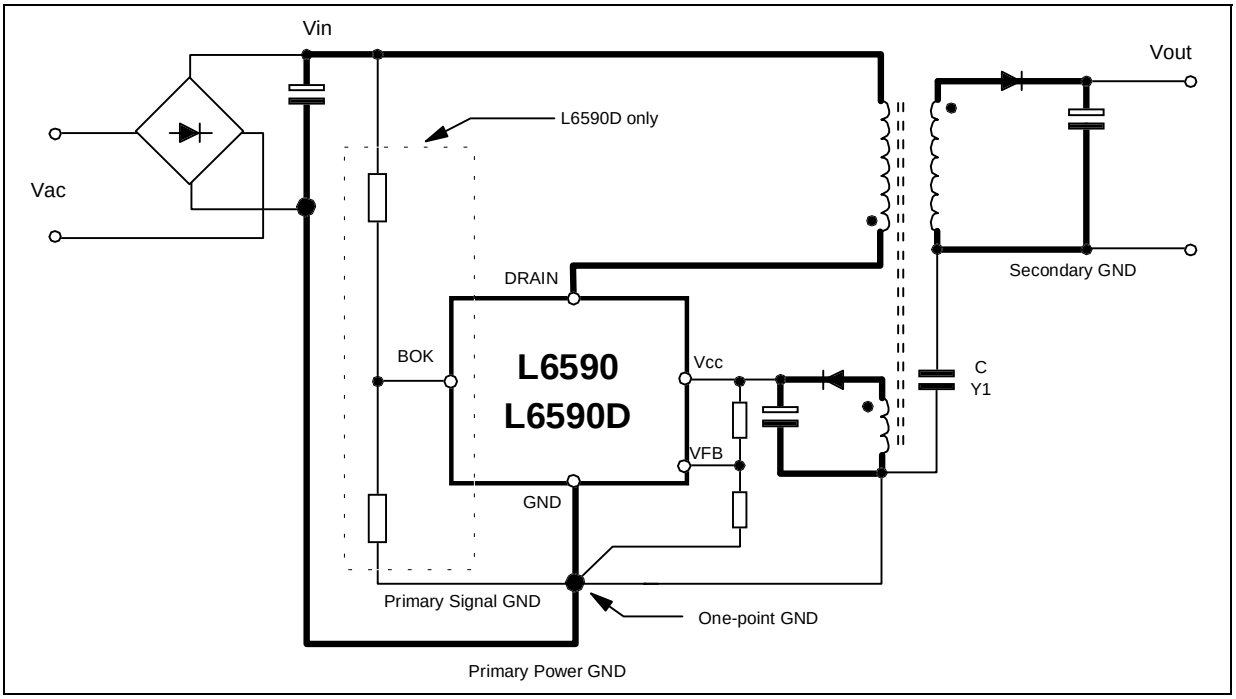


Some fundamental rules will be given to enable the designer to successfully produce a good layout.

All of traces carrying high currents, especially if pulsed (the bold ones in figures 18 and 19), should be as short and fat as possible. This will keep both resistive and inductive effects to a minimum, in favor of efficiency as well as radiated RFI. If a two layer PCB is used, some of these traces could be routed parallel on both sides.

Noise coupling and radiation will also be reduced by minimizing the area circumscribed by current loops where high pulsed currents flow, that is the bolded ones in figures 18 and 19. The most critical loop is that including the input bulk capacitor, the transformer and the L6590, thus these components should be next to one other. In figure 20 an example of possible component placement is given.

**Figure 19. Suggested ground routing for converters with primary feedback**




Current returns (or ground) routing is also very important. All of them (signal ground, power ground, shielding, etc.) should be routed separately and should be connected only at a single ground point, as suggested in figures 18 and 19.

Generally, traces carrying signal currents should run far from others carrying pulsed currents or with quickly swinging voltages like the bolded ones of figures 18 and 19. From this viewpoint, particular care should be taken of the feedback path. In case of two layer PCB, it is a good practice to route signal traces on one PCB side and power traces on the other side.

Some crucial points of the circuit need or may need filtering, such as the $V_{CC}$ pin or the BOK pin. In case, high-frequency filter capacitors (with plastic film or ceramic dielectric) should be placed between these pins and the "signal ground" route, as close to the IC as possible.

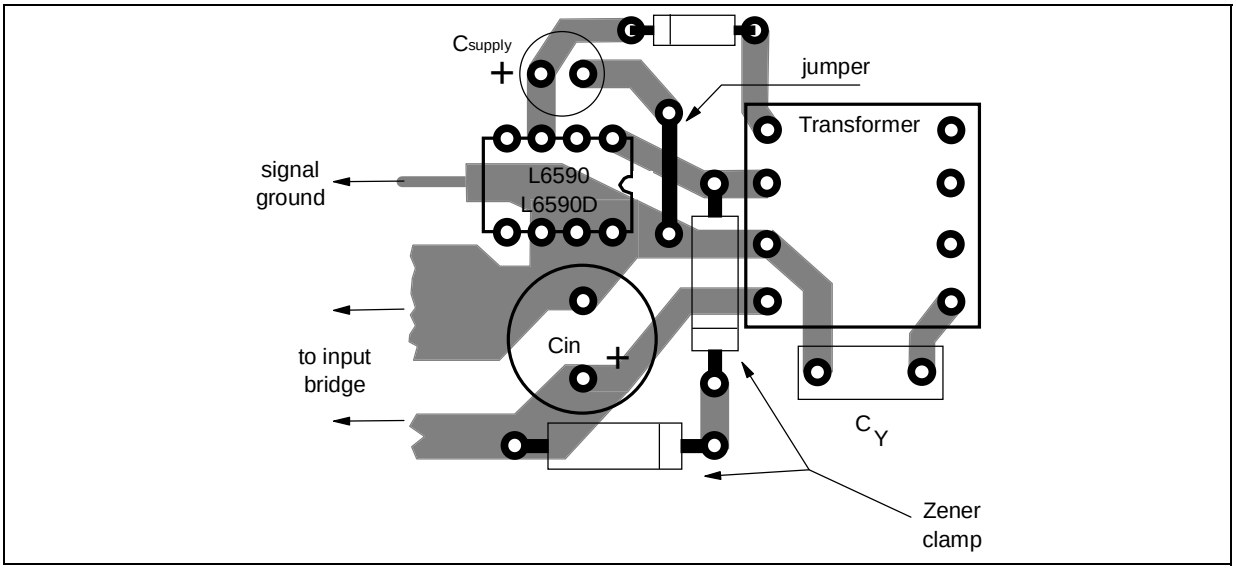
Reduction of common mode emissions requires a Y1 class capacitor (or two series connected Y2 class ones) connected between the primary and secondary ground. This decoupling capacitor should be connected as close to the transformer as possible.

Another important point is related to creepage distance: this must be observed between primary and secondary ground (8mm), between the phases of the input voltage (4 mm) and the opposite ends of the primary winding of the transformer (4mm). Concerning the primary-to-secondary ground separation, no component or traces

must be placed in this region, except the above mentioned common mode suppression capacitor and any optocoupler for secondary feedback.

Filling any unused space in the PCB with a ground plane helps reduce noise emission, but does not exempt from using the above mentioned care in component placing and traces routing. For instance, if a signal ground is connected to a ground plane along a pulsed current path between two components, (it is usually the most direct one) noise will be injected into the signal circuitry.

**Figure 20. Possible component placement.**




## 19 TEST BOARD: DESIGN AND EVALUATION

In order to show how to proceed with the design of an application based on the L6590 family, the design of the test board, used to evaluate the device's performance, will be illustrated in details. Finally, the resulting electrical schematic and a bench evaluation of the test board will be presented. The electrical specifications of the test board and some preliminary choices are listed in table 22. Table 23a) shows the results of some preliminary calculations needed to go further with the design steps.

**Table 22. Test board's electrical specification and pre-design choices**

| Electrical Specification | | |
|---|---|---|
| $V_{ACmin}$ | 88 V | Minimum mains voltage |
| $V_{ACmax}$ | 264 V | Maximum mains voltage |
| $f_L$ | 60 Hz | Mains frequency (@ min. mains) |
| $N_H$ | 0 | Number of holdup cycles |
| $V_{out}$ | 5 V | Regulated output voltage |
| $\Delta V_{out\%}$ | 2 % | Percent output voltage tolerance (±) |
| $V_{r\%}$ | 1 % | Percent output voltage ripple |
| $P_{outmax}$ | 10 W | Maximum output power |
| $\eta$ | 0,75 | Expected converter efficiency |
| $T_{amb}$ | 40 ° | Maximum ambient temperature |

**Table 22.** (continued)

| Pre-design Choices | | |
|---|---|---|
| $V_R$ | 120 V | Reflected voltage |
| $\eta_T$ | 0,9 | Transformer efficiency |
| $V_{spike}$ | 80 V | Leakage inductance overvoltage |
| $V_{CC}$ | 12 V | L6590 supply voltage |
| $V_F$ | 0.6 V | Secondary diode forward drop |
| $V_{BF}$ | 3 V | Bridge Rectifier + EMI filter voltage drop |

**Bridge rectifier selection.**

An integrated bridge (DF06M, 4x1A/600V, GI) has been selected.

**Input Bulk Capacitor.**

From table 5, in order for the valley voltage on the input cap to be around 90 V, a minimum capacitance of about 27 µF should be used. A standard 22 µF/400V electrolytic capacitor will be chosen. After few iterations, the (1) cycle converges at $V_{inmin}$ = 84.9V, $T_c$ = 2.11 ms. From eqn. 2, $V_{DCmin}$ = 103.2 V.

Table 23b) shows the results of a second step of calculations, aimed at checking that no limit of the device is violated. The result is OK.

**Operating conditions @ $V_{in} = V_{DCmin}$ and thermal check.**

The results are listed in table 23c). With these data the power dissipated by the L6590 is calculated and the result is shown in table 23d).

From eqn. 3, the maximum junction-to-ambient thermal resistance needed for reaching thermal balance at Tj = 125 °C is 51.2 °C/W. From the diagrams of fig. 21 it is possible to see that this can be obtained with about 1 $cm^2$ copper area on the PCB.

**Figure 21. L6590 Family Packages Junction-to-Ambient Thermal Resistance**

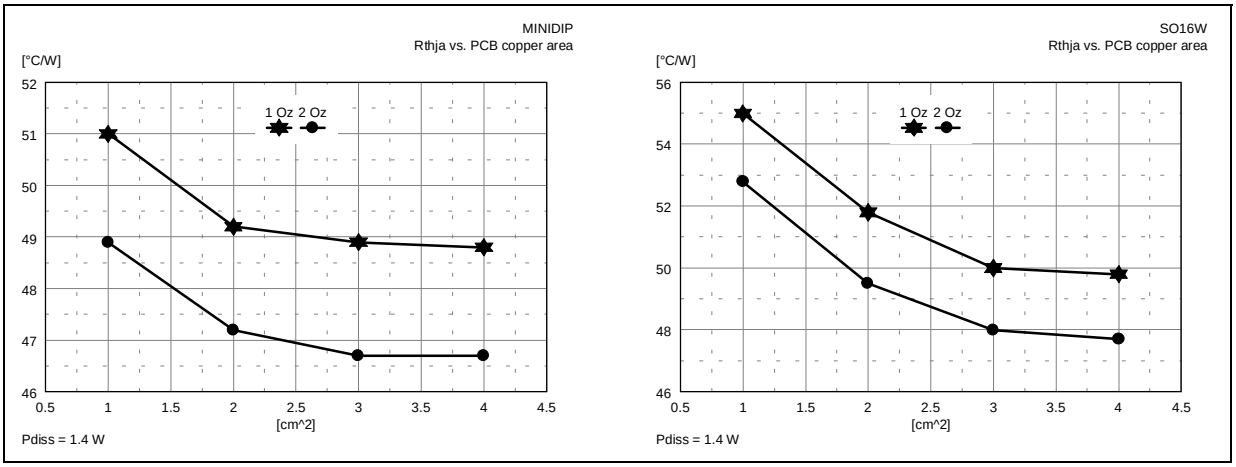


**Table 23. Test Board design calculations results.**

| a) Preliminary Calculations results (step 1) | | |
|---|---|---|
| **Symbol** | **Parameter** | **Value** |
| $P_{in}$ | Converter Input Power | 13.33 W |
| $I_{out}$ | DC Output Current | 2 A |
| $V_{PKmin}$ | Minimum Peak Input Voltage | 121.5 V |
| $V_{PKmax}$ | Maximum Peak Input Voltage | 373.4 V |
| **b) Preliminary Calculations results (step 2)** | | |
| $V_{inmin}$ | Absolute minimum Input DC Voltage | 84.9 V |
| $V_{DCmin}$ | Minimum Input DC bus Voltage | 103.2 V |
| $P_{inT}$ | Transformer Input Power | 12.44 W |
| $V_{DS(on)x}$ | Max. average drop on $R_{DS(on)}$ in ON-state | 7.24 V |
| $D_x$ | Maximum Duty Cycle | 0.607 |
| $V_{DSmax}$ | Maximum drain Voltage in OFF-state | 573.4 V |
| $I_{ppkx}$ | Max. Peak Primary Current | 0.528 A |
| **c) Operating Conditions @ Vin = $V_{DCmin}$** | | |
| $V_{DS(on)}$ | Average drop on $R_{DS(on)}$ in ON-state | 7.24 V |
| D | Duty Cycle (switch ON-time to switching period ratio) | 0.496 |
| $Ip_{pk}$ | Peak Primary Current | 0.528 A |
| $Ip_{DC}$ | DC Primary Current | 0.131 A |
| $Ip_{RMS}$ | Total RMS Primary Current | 0.215 A |
| $Ip_{AC}$ | RMS Primary Current (AC component only) | 0.170 A |
| D’ | Secondary diode conduction time to switching period ratio | 0.397 |
| $Is_{pk}$ | Peak Secondary Current | 10.08 A |
| $Is_{DC}$ | DC Secondary Current | 2 A |
| $Is_{RMS}$ | Total RMS Secondary Current | 3.67 A |
| $Is_{AC}$ | RMS Secondary Current (AC component only) | 3.08 A |
| **d) Device power dissipation @ Vin = $V_{DCmin}$** | | |
| $P_{cond}$ | Conduction losses | 1.29 W |
| $P_{sw}$ | Switching losses | 0.13 W |
| $P_{cap}$ | Capacitive losses | 0.16 W |
| $P_q$ | Quiescent losses | 0.08 W |
| $P_{tot}$ | Total losses | 1.66 W |
| $R_{thj\text{-}amb}$ | Maximum junction-ambient thermal resistance | 51.2 °C/W |

### Flyback transformer design

Eqn. 4 gives the primary inductance (Lp = 1.37 mH, rounded up to 1.4 mH), while eqn. (5) gives the primary-to-secondary turns ratio (n = 21.4). The design will be done considering Philip's E-cores in 3C85 ferrite and assuming a maximum peak flux of 0.25T, a temperature rise of 40 °C and 40% window utilization factor. Going step-by-step:

1) Eqn. 6 provides a minimum AP of 0.042 $cm^4$. Table 10 shows that an E20/10/6 core could fit the design.
2) The primary turns number will be $Np_{min}$ = 122.5.
3) The resulting secondary turn number will be 122.5/21.4=5.7 which will rounded up to 6. The primary turns number will then become 6·21.4=128.4. Finally, the choice will be Np=128 turns and Ns=6 turns, which yields an actual turns ratio of 128/6 = 21.33, very close to the target.
4) From eqn. 7, the air gap needed to get the desired value of Lp will be 0.63 mm.
5) Table 10 shows that the thermal resistance of the finished core is 46 °C/W, thus the maximum power dissipation inside the transformer shall not exceed 40/46 = 0.87 W.
6) Equations 8, 9 and 10 will provide the actual flux swing (which will be lower than 0.25 T because Np>Npmin), the actual core losses and the allowed copper losses respectively. The resulting flux swing is $\Delta B$=180 mT: the relevant core losses amount at 66 mW, thus it is possible to dissipate up to 0.8 W in the windings.
7) The required primary and secondary winding resistance will be 8.65 Ω and 30 mΩ respectively (resulting from eqns. 11). The resulting primary resistance is quite high and the drop across it reduces significantly the actual voltage applied at the primary inductance. The target primary resistance is then reduced at 4Ω and the secondary will be increased at 46mΩ to maintain the same total copper losses.

   The required primary and secondary copper area will be $2.87 \cdot 10^{-4}$ $cm^2$ and $1.2 \cdot 10^{-3}$ $cm^2$ respectively (eqns. 12, 13). Table 11 shows that this can be done with one AWG32 wire at the primary and four paralleled (twisted) AWG32 wires at the secondary. This will both minimize high frequency effects and simplify the BOM. The total occupied area will be 7 $mm^2$ (eqn. 14), 20% of the total available area, thus the windings will fit.

   On top of the primary and secondary winding, 14 turns of AWG32 wire will be wound to make the auxiliary winding (eqn. 15).
8) The actual resistance of the primary and secondary windings will be 3.6 Ω and 42 mΩ respectively, for total copper losses of 0.73 W. The total losses will be about 0.8 W and the resulting temperature rise 36.8 °C.

### Zener clamp

To optimize losses at light load a zener clamp will be used. The clamp voltage should be around 200 V (eqn. 16), thus a BZW06-154 is first selected.

Assuming a leakage inductance of 30 µH (about 2% of the primary inductance), power dissipation will be about 0.6 W in normal operation and about 1.1 W in overcurrent limitation. The relevant clamping voltages would be 196 V and 209 V respectively. The initial choice will then be confirmed.

An STTA106 (1A / 600V turboswitch diode) will be used as the blocking diode.

### Secondary rectifier

According to eqn. 17, and considering 25% margin, the blocking voltage of the diode should exceed 28 V, while its current rating should be in excess of 4 A. Although table 14 suggests a bigger device, an 1N5822 (3A/40V) Schottky diode is selected for this test board.

### Output Capacitor

Capacitor's ripple current rating should exceed 3 A. The minimum capacitance value should be 373 µF (eqn. 18) and the maximum ESR should be less than 5 mΩ. For long-time reliability the capacitor(s) should also be able to withstand at least 3.08 A current ripple. Three Rubycon's ZL series 470 µF/16V paralleled capacitors were selected, for a total ripple capability of nearly 3 A and a total ESR of about 20 mΩ. To meet the requirement on the output voltage ripple an LC post filter is needed that attenuates ripple at least four times. Choosing a standard value of L = 4.7 µH, the maximum ESR of the additional capacitor should not exceed 300mΩ.
An additional 220 µF/10V ZL capacitor has been added.

### Self-supply circuit

The self supply circuit will include an 1N4148 diode and a 22 µF supply capacitor. A 10 Ω resistor will be added in series to the diode to reduce Vcc voltage variations with the load current. This value is likely to be adjusted after bench verification.

### Control loop design

The crossover frequency will be selected as high as 10 kHz, worst case. The objective will be to get 70° phase margin.

The plant transfer function is:

$$G2(j\omega) = G2_0 \cdot \frac{1 + \frac{j\omega}{\omega_{ESR}}}{1 + \frac{j\omega}{\omega_{out}}}$$

with G2o = 11.5, $f_{ESR}$ = 5464 Hz, $f_{out}$ = 90.3 Hz (@ max. load and max. $V_{in}$). A type 2 amplifier will be used for G1(jω).

Going step-by-step:

a) The gain and phase of G2 at f=10 kHz are 0.281 and -29° respectively;

b) In order for the overall open-loop gain to cross the 0 dB axis at f=10 kHz with 70° phase margin, the gain and phase of G1(jω) will be 3.56 and -81° respectively;

c) the compensating zero will be placed at 360 Hz (α = 4, to maximize 100Hz gain);

d) the compensating pole will be placed at 2270 Hz;

e) the unity gain factor is $35.4 \cdot 10^4$ s/rad.

Since a tight tolerance on the output voltage is required, an optoisolated feedback will be used and G1(jω) will be realized with the schematic of figure 13. The TL431 and an optocoupler PC817A from Sharp will be used. The CTR is specified between 0.8 and 1.6.

Using a 6.8kΩ resistor as $R_C$, the resulting part values are:

$$R_L = R_H = 2.43\ k\Omega;\ R_B = 560\ \Omega;\ R_F = 2k\Omega;\ C_F = 100\ nF;\ C_{COMP} = 22\ nF.$$

### Electrical Schematic, BOM and evaluation results

In fig. 22 the electrical schematic of the test board is illustrated and table 24 lists the relevant BOM. The diagrams of figure 23 show the evaluation results of the board, figure 24 shows some typical waveforms and figure 25 the effect of the frequency change on the output voltage transient.

**Figure 22. Test board electrical schematic**

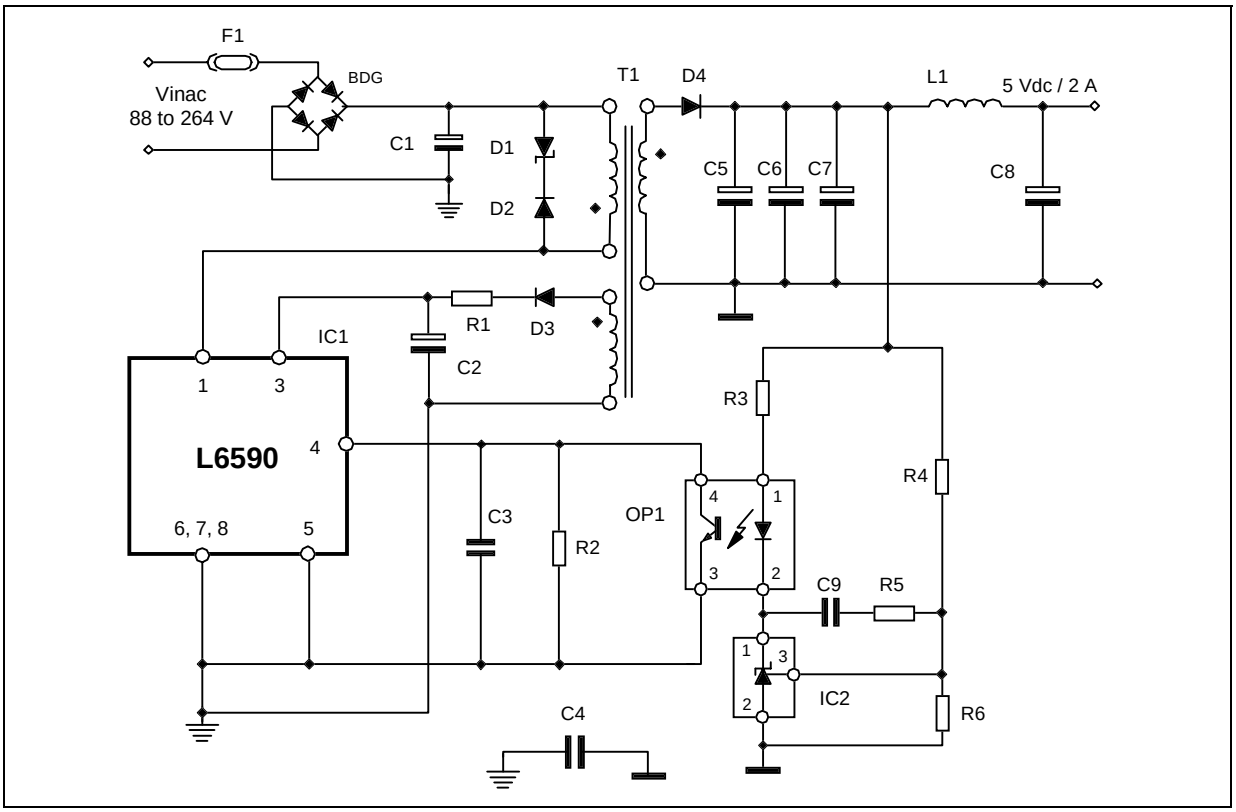



**Table 24. Test board Bill Of Material**

| Symbol | Value | Notes |
|---|---|---|
| R1 | 10 Ω | ¼ W, 5% |
| R2 | 6.8kΩ | ¼ W, 1% |
| R3 | 560Ω | ¼ W, 1% |
| R4, R6 | 2.43kΩ | ¼ W, 1% |
| R5 | 2kΩ | ¼ W, 1% |
| C1 | 22 µF | 400 V, electrolytic, ELNA RE3 or equivalent |
| C2 | 22 µF | 25 V, electrolytic |
| C3 | 22 nF | plastic film |
| C4 | 2.2 nF | 250V Y class |
| C5, C6, C7 | 470 µF | 16 V, electrolytic, RUBYCON ZL or equivalent |
| C8 | 220 µF | 10 V, electrolytic, RUBYCON ZL or equivalent |
| C9 | 100 nF | 10V electrolytic |
| L1 | 4.7 µH | UK ltd., ELC8D4R7E |
| D1 | BZW06-154 | 154V / 600W peak Transil, ST |

**Table 24. (continued)**

| Symbol | Value | Notes |
|---|---|---|
| D2 | STTA106 | 1A / 600V Turboswitch, ST |
| D3 | 1N4148 | |
| D4 | 1N5822 | 3A / 40V Schottky, ST |
| IC1 | L6590 | Monolithic HV Switcher, ST |
| OP1 | PC817A | Optocoupler, Sharp |
| BD1 | DF06M | GI, or equivalent 1A, 600 V |
| T1 | --- | Core E20/10/6, 3C85 ferrite, Philips or equivalent<br>≈ 0.6 mm air gap for a primary inductance of 1.4 mH ($L_{LK}$ <30 µH)<br>Pri: 64T+64T, series conneceted, AWG32 (∅ 0.22 mm)<br>Sec: 6T, 4xAWG32 (∅ 0.22 mm)<br>Aux: 14T, AWG32 (∅ 0.22 mm) |
| F1 | T2A250V | 2A, 250V ELU |

**Figure 23. Test board evaluation results**

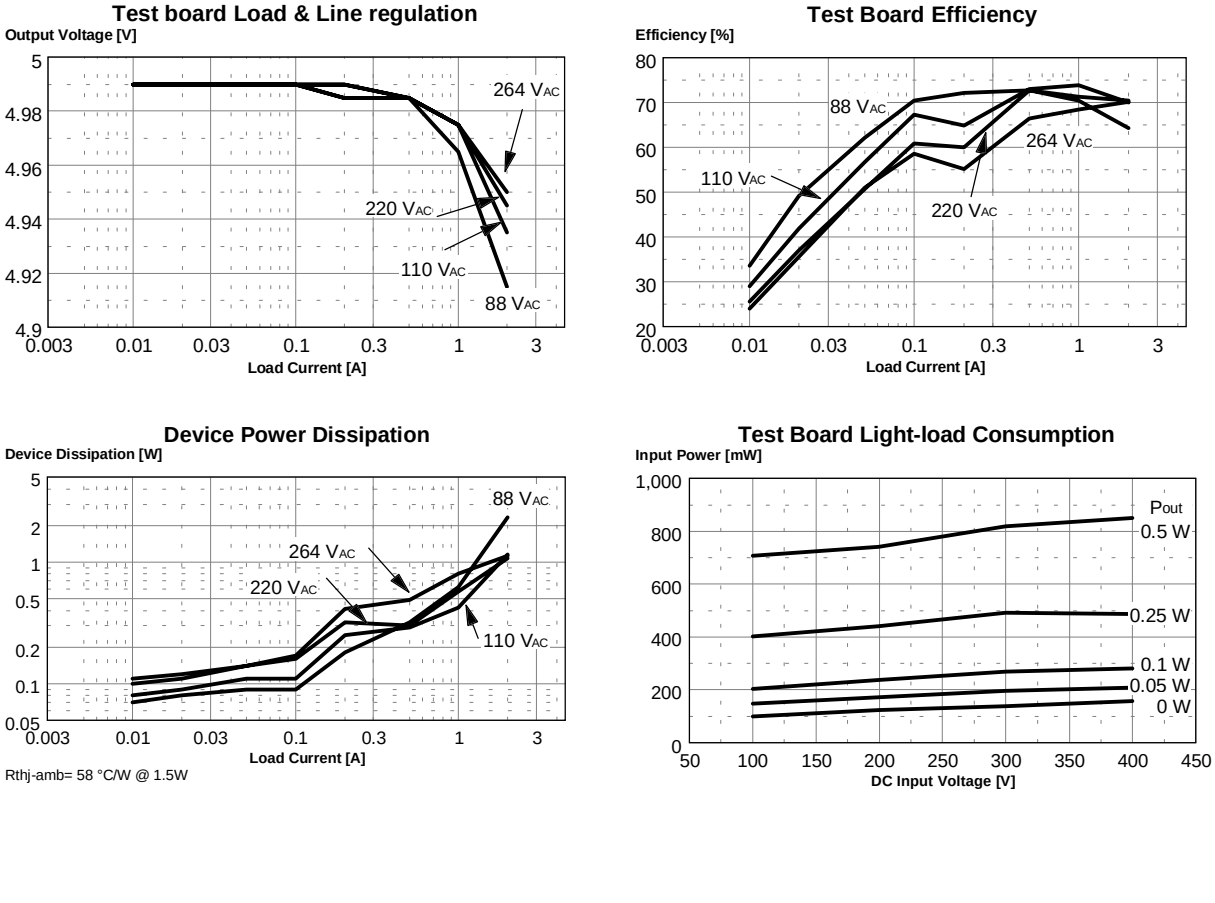


**Figure 24. Test board main waveforms under different operating conditions**

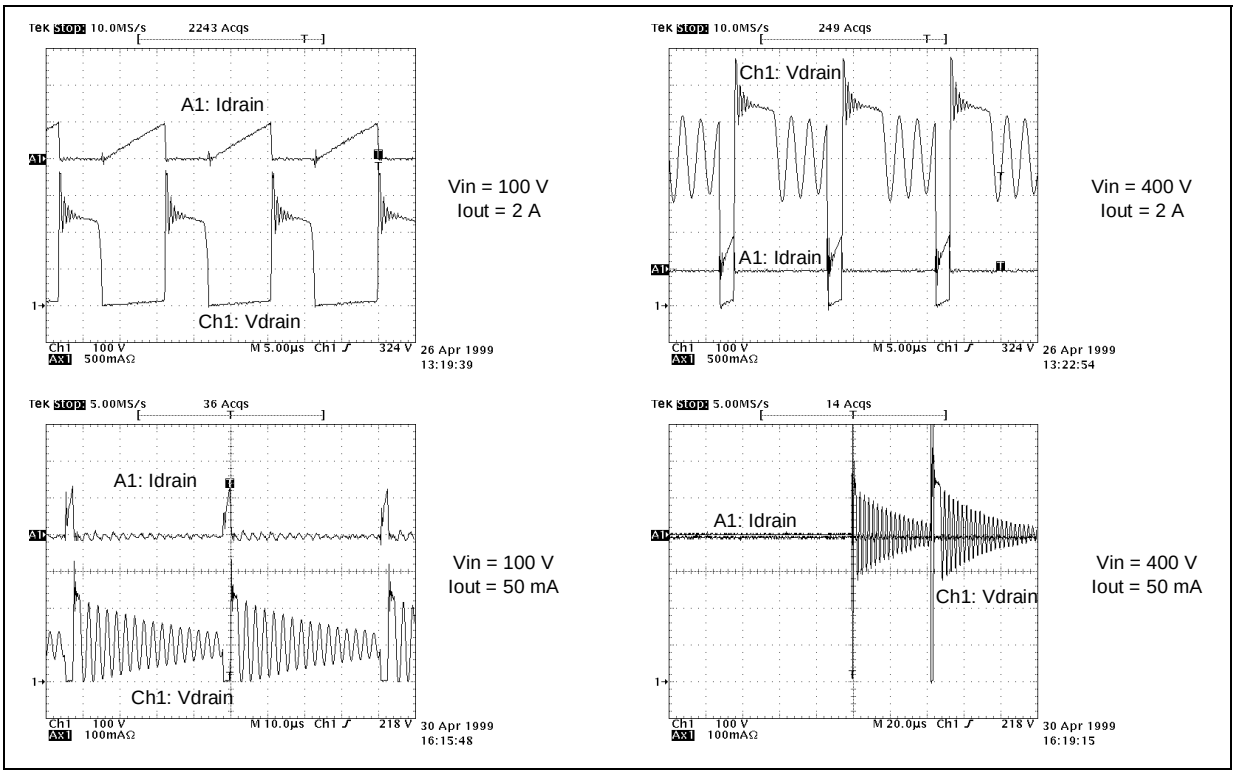
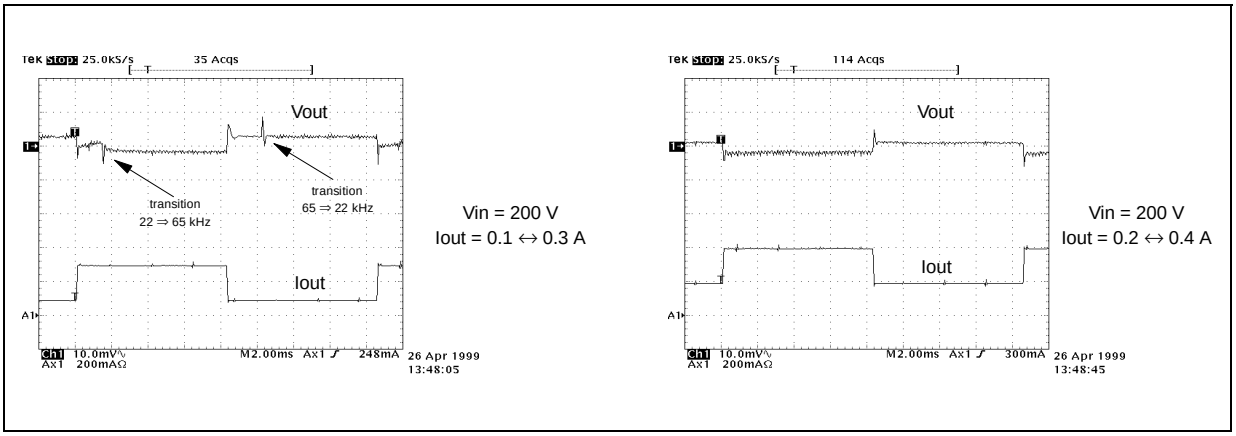



**Figure 25. Test board load transient response; effect of frequency change (left).**




## 20 REFERENCES

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[2]"Calculation of Transil Apparent Dynamic Resistence" (AN575)

[3]"Transistor Protection by Transil" (AN587)

[4]"Getting Familiar with the L6590 Family High-voltage Fully Integrated Power Supply" (AN1261)

## SUMMARY