AN2480
Application note

STA333BW demo board application note

Introduction

The purpose in this document is:

- to describe how to connect the AN2480 demo board,
- how to evaluate the demo board performance with electrical curve data,
- how to avoid critical board and layout issues.

Application note can be configured for either:

- 2.0 channels (2 x 20 W), with headphone output,
- 2.1 channels (2 x 10 W + 20 W) without headphone function.

The AN2480 demo board is combined with DDx® power amplifier and an operation amplifier for headphones. It is a total solution for digital audio power amplifier TV and portable applications.

Note: All the test items and graph data in this document are measured by Audio Precision equipment.

Contents

1 Test condition and connection of demo board

1.1 Test condition

1.1.1 Power supply and interface connections

1. Connect positive voltage of 12 V DC power supply to +Vcc pin and negative to GND.
2. Connect positive voltage of 3.3 V DC power supply to +3.3 V pin and negative to GND.
3. Connect GUI LPT interface board to the J1 connector of AN2480 demo board.
4. Connect the S/PDIF signal cable to the RCA jack on the interface board, the other side connecting to the signal source such as Audio precision or DVD player.
5. The voltage range of the DC power supply for Vcc is from 5 V to 18 V.

1.1.2 Output configuration

STA333BW demo board can be configured in the ternary state for 2.0 channels.

1.2 Equipment requirement

- Audio Precision (System 2700) by AP Co., USA
- DC power supply (5 V to 18 V)
- Digital oscilloscope (TDS3034B) by Tektronix
- PC (with AN2480 GUI control software installed)

1.3 Connection method

Top view of demo board.

Figure 1. Block diagram

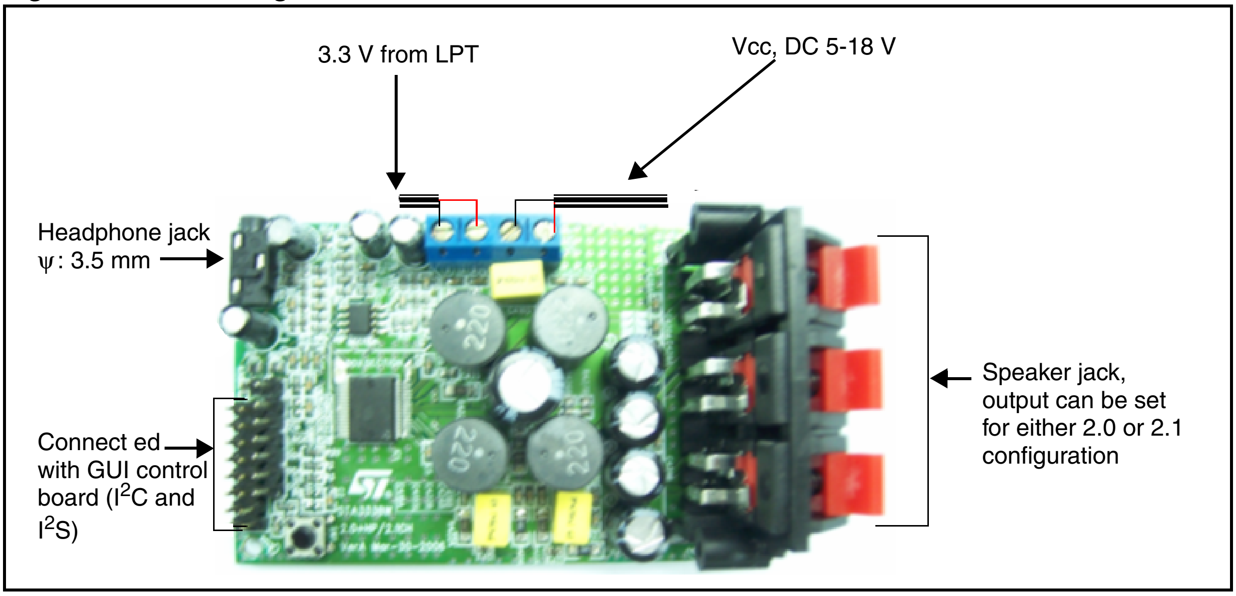


Figure 2. 2.0 speaker jack configuration

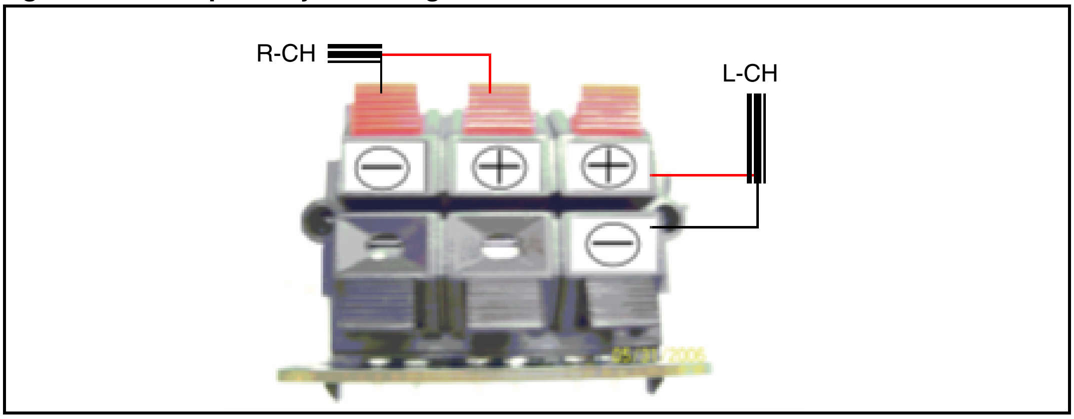
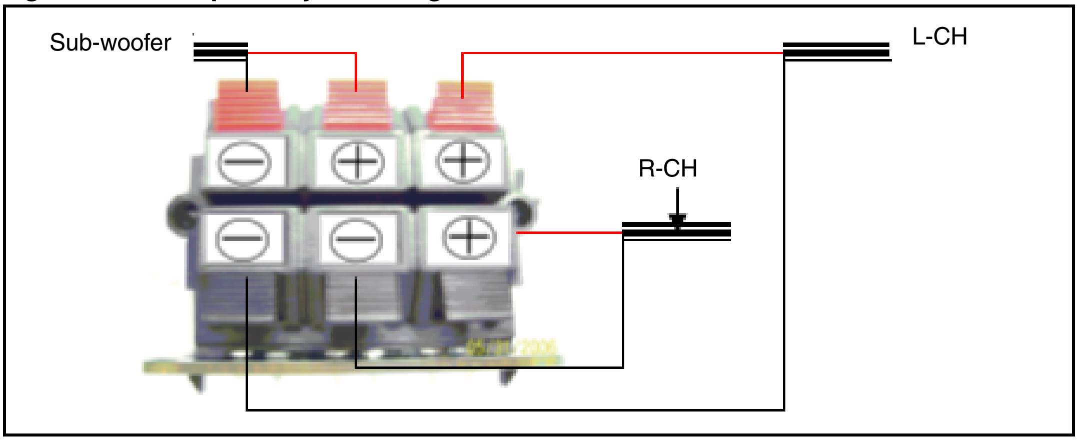


Figure 3. 2.1 speaker jack configuration



1.3.1 Schematic

Figure 4. DDx schematic diagram

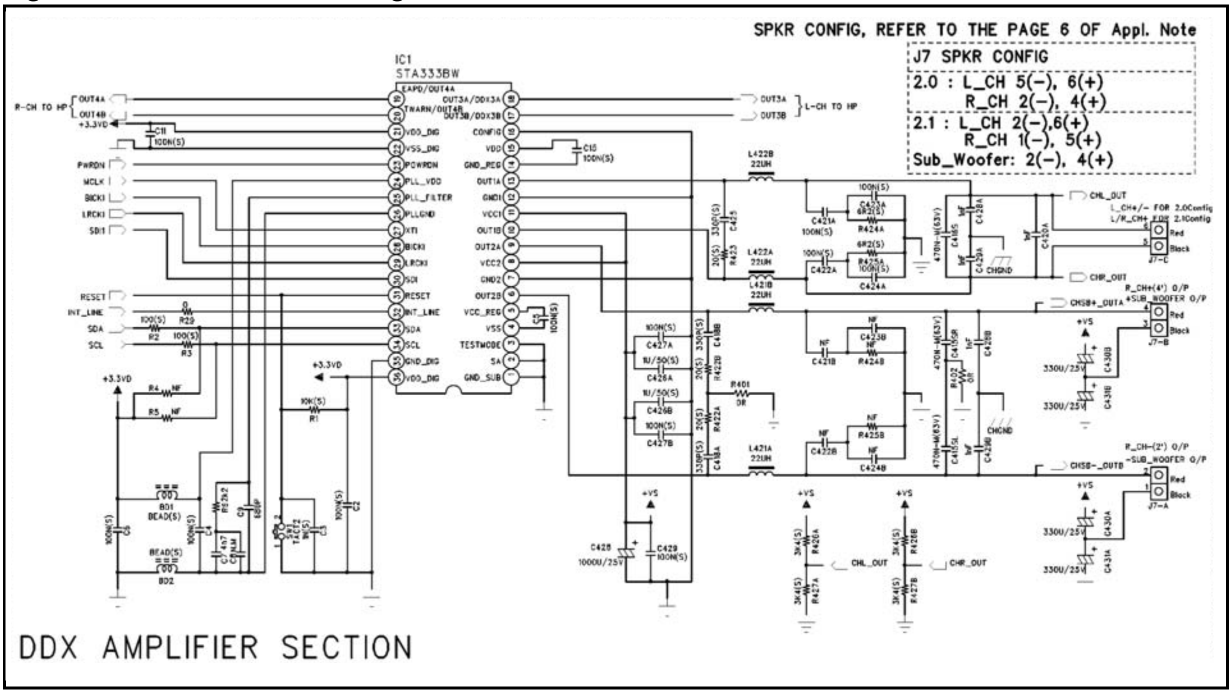
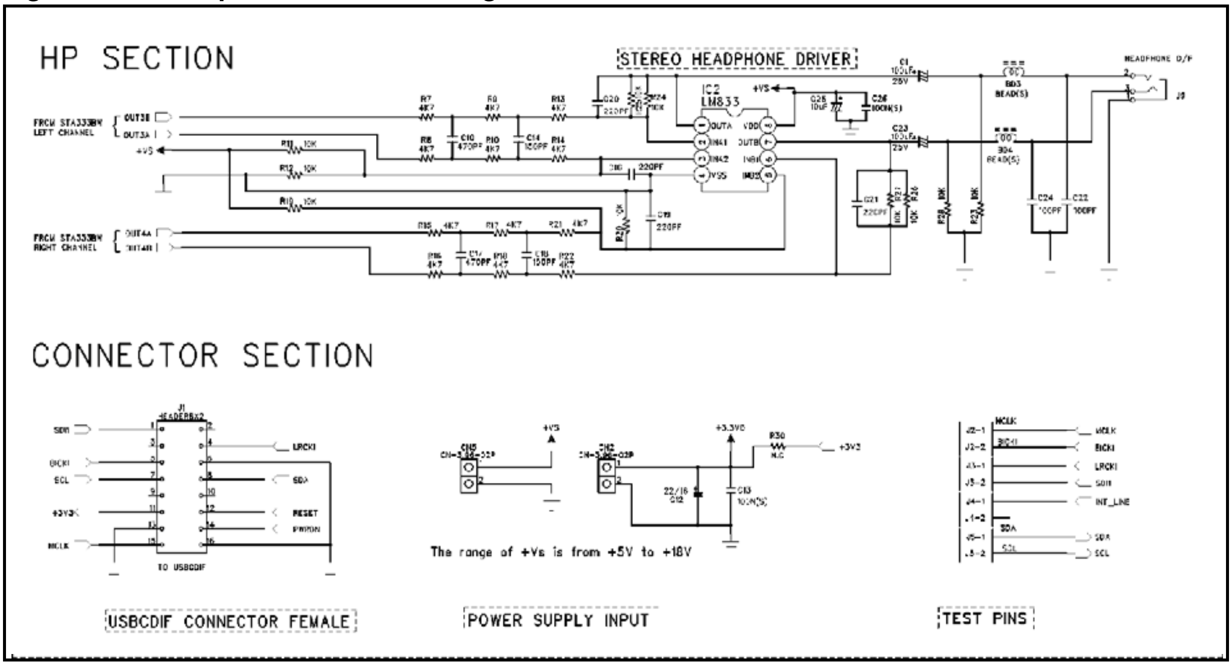


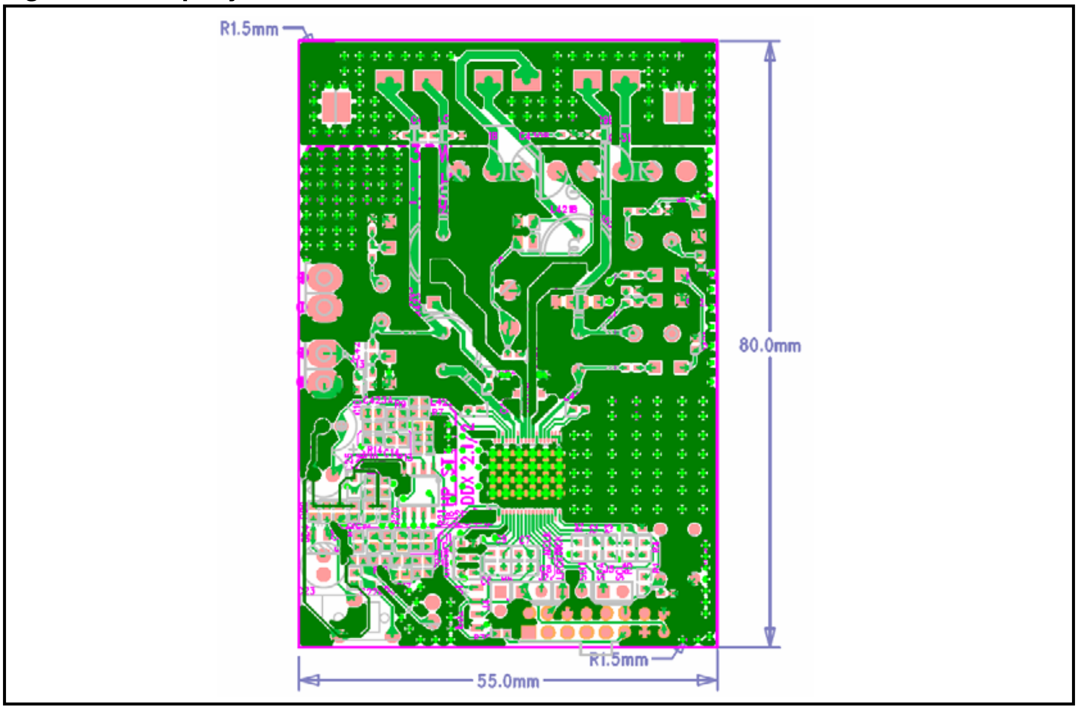
Figure 5. Headphone schematic diagram



1.4 PCB Layout

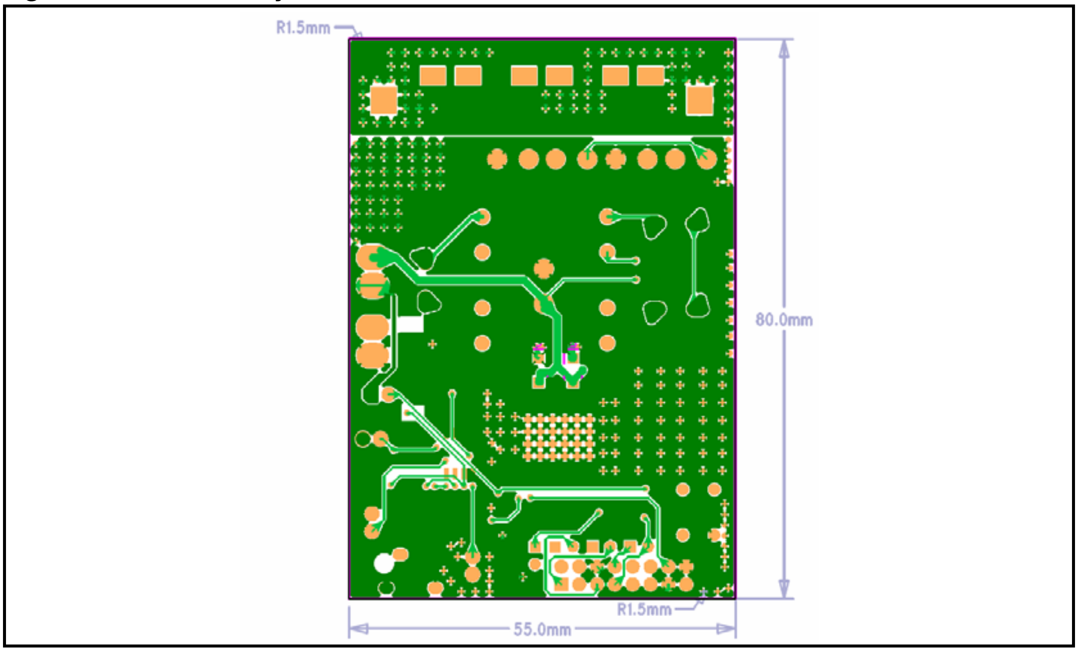
1.4.1 Top view of PCB layout

Figure 6. Top layout



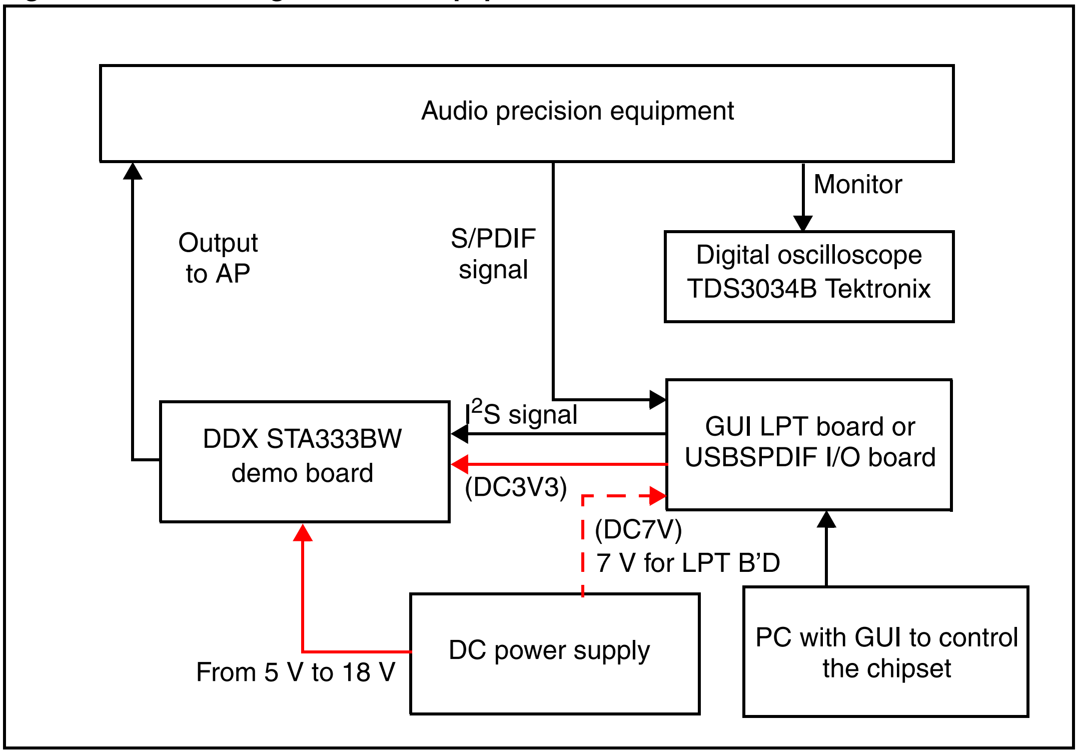
1.4.2 Bottom view of PCB layout

Figure 7. Bottom layout



1.4.3 Test connection

Figure 8. Block diagram of test equipment



2 Electrical characteristics

Table 1. Electrical characteristics(1)

Parameter	Configuration	Test condition	Unit
PSRR (50 Hz - 120 Hz)	BTL configuration	Please refer to measurements section	65 dB
Min SNR	BTL configuration	1 W output, -20 dBFs input, 1 KHz	100 dB
Max modulation index	DDX modulation mode		98.5%
Vcc current (18 V)	BTL configuration	Operating Quiescent Standby/sleep	40 mA 30 mA 0 mA

1. Refer to the STA333BW demo board circuit. Vs= +18 V, Tamb = 25.5 ^{o}C, f = 1 KHz, Ref = 1 W unless otherwise specified.

Note: THD works better with high impedance loading (based on a fixed value of R_{dsON}).

2.1 BOM list

Table 2. BOM

Item no.	Type	Package	Description	Qty	Reference code	Manufacturer
1	CCAP	CCAP0603	50 V NPO 100pF +/- 10 %	2	C22, C24	Murata
2	CCAP	CCAP0603	50 V NPO 150pF +/- 10 %	2	C14, C18	Murata
3	CCAP	CCAP0603	50 V NPO 220pF +/- 10 %	4	C16, C19, C20, C21	Murata
4	CCAP	CCAP0603	50 V NPO 330pF +/- 10 %	3	C418A, C418B, C425	Murata
5	CCAP	CCAP0603	50 V NPO 470pF +/- 10 %	2	C10, C17	Murata
6	CCAP	CCAP0603	50 V NPO 680pF +/- 5 %	1	C9	Murata
7	CCAP	CCAP0603	50 V 1 nF +/- 10 %	2	C3	Murata
8	CCAP	CCAP0603	50 V 4.7 nF +/- 10 %	1	C7	Murata
9	CCAP	CCAP0603	50 V 100 nF +/- 10 %	24	C2, C4, C5, C6, C11, C13, C15, C26, C429, C420A, C421A, C421B, C423A, C422A, C422B, C423B, C424A, C424B, C427A, C427B, C428A, C428B, C429A, C429B	Murata
10	CCAP	CAP1206	50 V, 1U +/- 10 %	2	C426A, c426B	Rubycon
11	BEAD	L0805	600 ohm @ 100 MHz	2	BD1, BD2	Murata
12	RES	R1206	6.2 +/- 10 % 1/8 W	4	R423, R422A, R425A, R425B	Murata
13	RES	R1206	20 +/- 10 % 1/8 W	3	R423, R422A, R422B	Murata

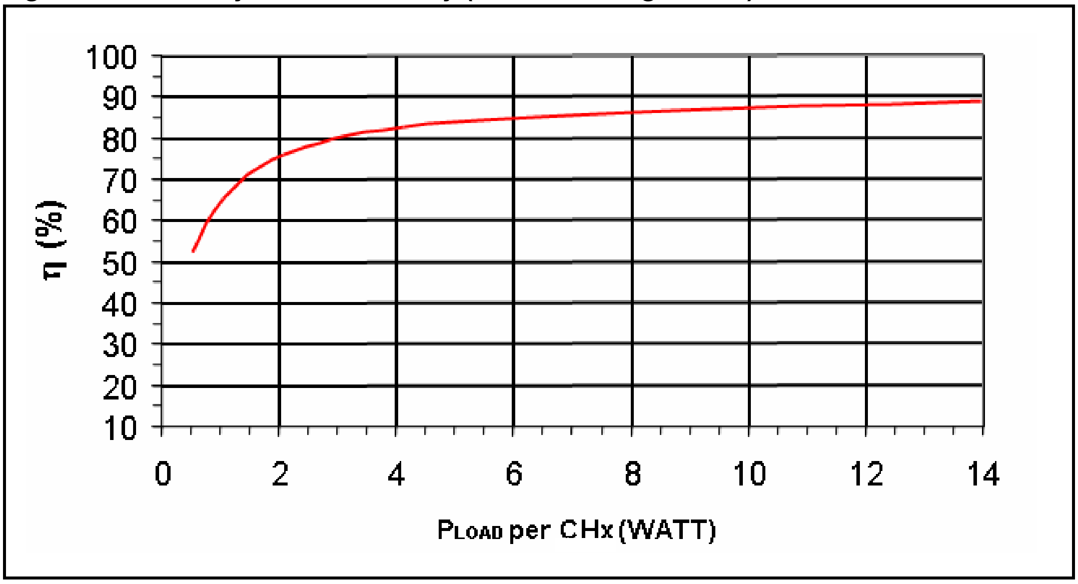
Table 2. BOM

Item no.	Type	Package	Description	Qty	Reference code	Manufacturer
14	RES	R0603	0 ohm 1/16 W	4	R29, R30, R401, R402	Murata
15	RES	R0603	100 +/- 10 % 1/16 W	2	R2, R3	Murata
16	RES	R0603	2.2 K +/- 10 % 1/16 W	1	R6	Murata
17	RES	R0805	33 ohm +/- 10 % 1/10 W	2	BD3, BD4	Murata
18	RES	R0805	3.4 K +/- 10 % 1/10 W	4	R426A, R426B, R427A, R427B	Murata
19	RES	R0603	4.7 K +/- 10 % 1/16 W	12	R7, R8, R9, R10, R13, R14, R15, R16, R17, R18, R21, R22	Murata
20	RES	R0603	10 K +/- 10 % 1/16 W	13	R1, R4, R5, R11, R12, R19, R20, R23, R24, R25, R26, R27, R28	Murata
21	ECAP	ECAP25X5	100 µ/25 V	4	C1, C12, C23, C25	Rubycon/ Panasonic
22	ECAP	ECAP25X5	N.M.			
23	ECAP	ECAP25X8	330 µ/25 V	4	C430A, C430B, C431A, C431B	Rubycon/ Panasonic
24	ECAP	ECAP25X10	100 µF/25 V	1	C4	Rubycon/ Panasonic
25	IC	STA333BW	STA333BW(SS036)	1	IC1	ST
26	IC	LM833	LM833(SO8)	1	IC2	ST
27	Coil	L22n_1015	22 nH choke coil	4	L421A, L421B, L422A, L422B	Kwangsung
28	Jack	SPKR_JACK	6P speaker jack	1	J7	Any source
29	MCAP	470N-M (63 V)	470NF-M963 V) capacitor	3	C415SL, C415SR, C416S	Any source
30	Terminal	CNN_ Terminal	2P pitch: 5 mm connector terminal	2	CN2, CN5	Any source
31	SW	TACT SW	4P tact switch	1	SW1	Any source
32	Jack	3.5 mm phone jack	3P 2 CH 3.5 MM phone jack	1	J9	Any source
33	CNN	16P-CNN	16P (8 x 2 row) 2.5 mm male CNN	1	J1	Any source
34	JW	2P-2.5 mm JW	Not mounting	4	J2, J3, J4, J5	Any source

3 Test curve report

3.1 Ternary mode

Figure 9. Ternary mode efficiency (2.0 BTL configuration)



Condition: R_{LOAD} =8 ohm; VCC=18 V

3.2 BTL configuration

Figure 10. Output power versus supply voltage

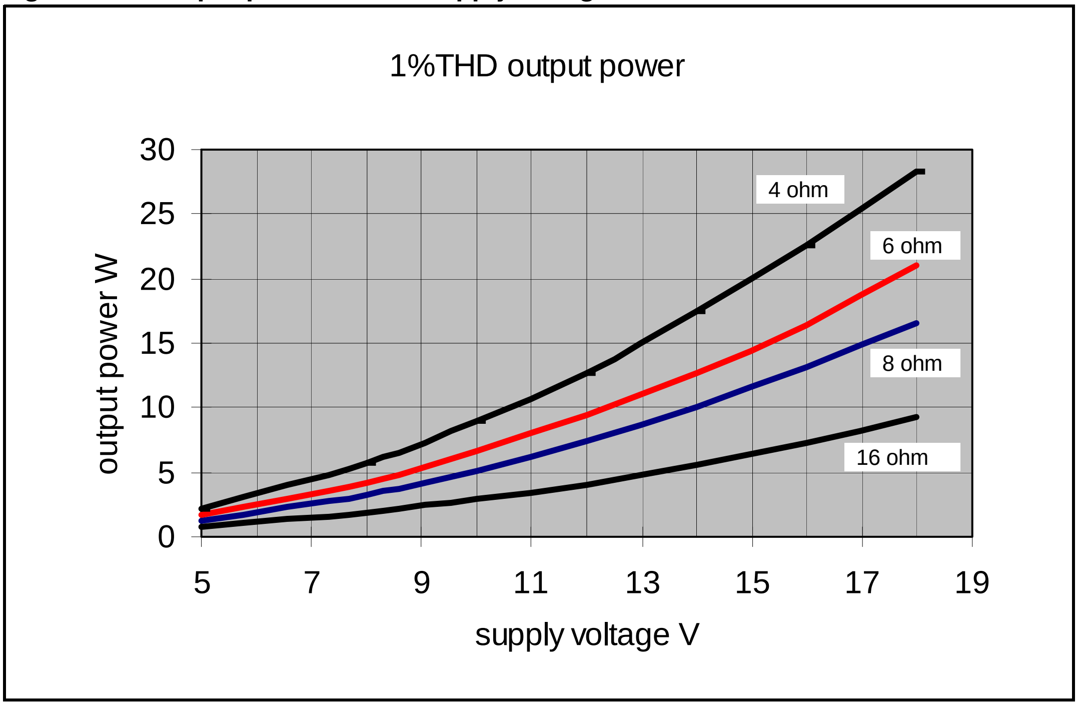


Figure 11. Channel separation 5 V 1 W 4 ohm

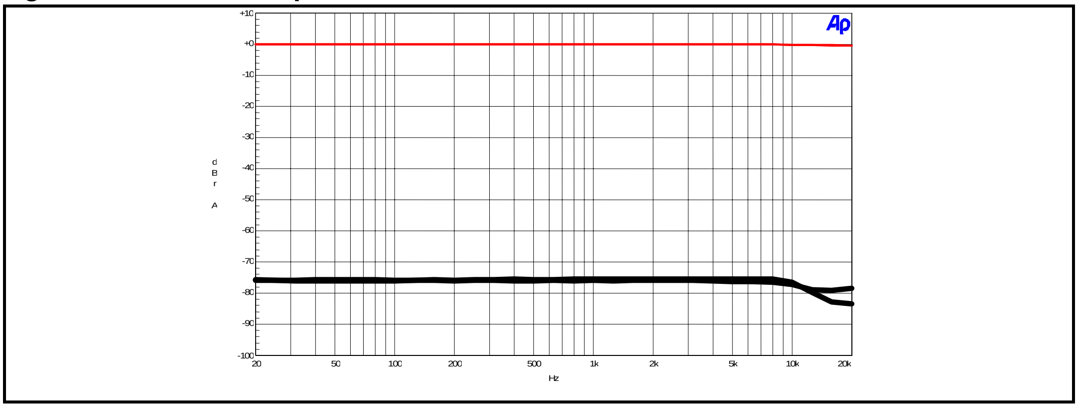


Figure 12. Channel separation 5 V 1 W 8 ohm

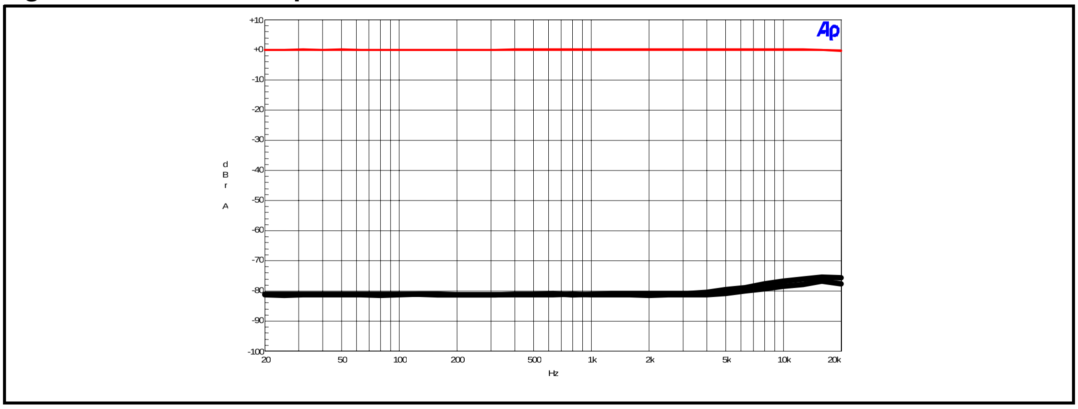


Figure 13. FFT 0 dBFs 1 KHz 5 V 4 ohm

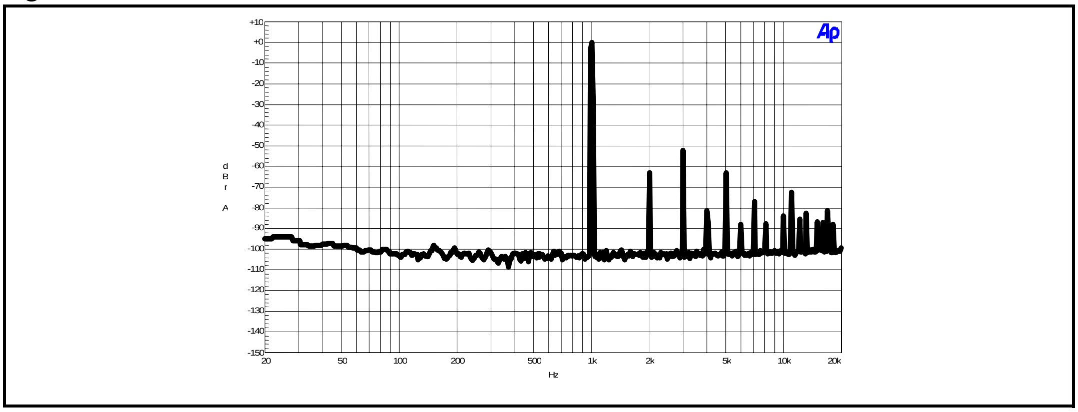


Figure 14. FFT -60 dBFs 1 KHz 5 V 4 ohm

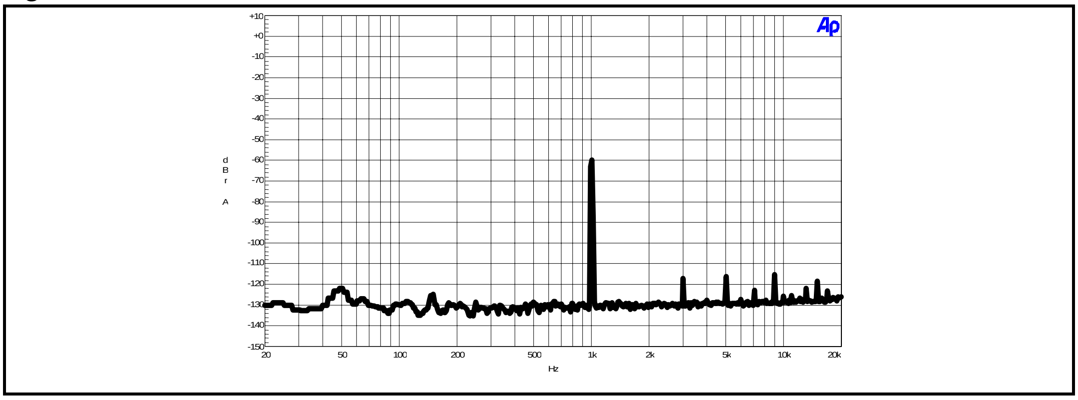


Figure 15. FFT 0 dBFs 1 KHz 5 V 6 ohm

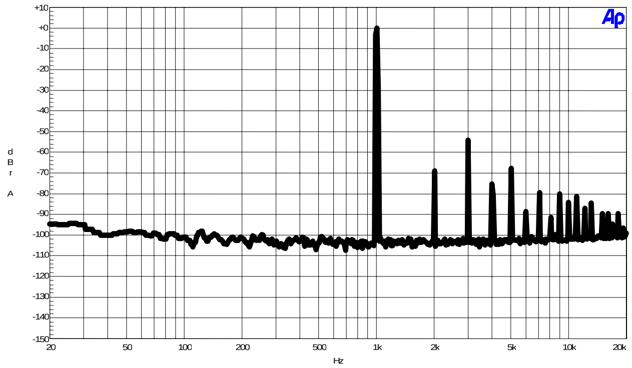


Figure 16. FFT -60 dBFs 1 KHz 5 V 6 ohm

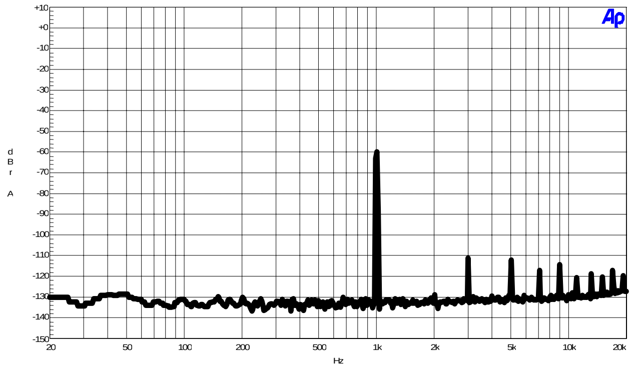


Figure 17. FFT 0 dBFs 1 KHz 5 V 8 ohm

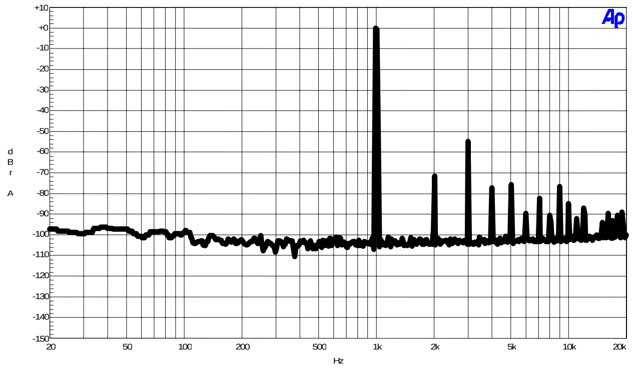


Figure 18. FFT -60 dBFs 1 KHz 5 V 8 ohm

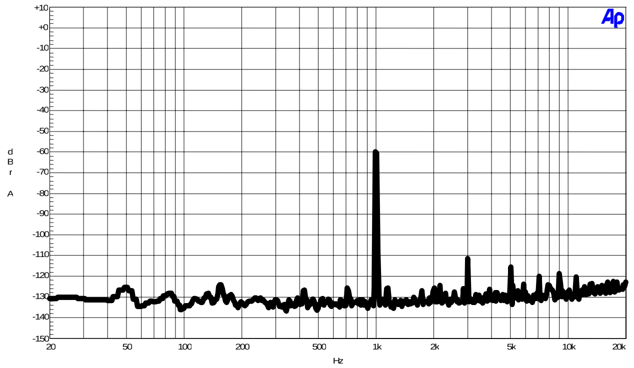


Figure 19. THD versus Freq. 5 V Vcc 1 W output

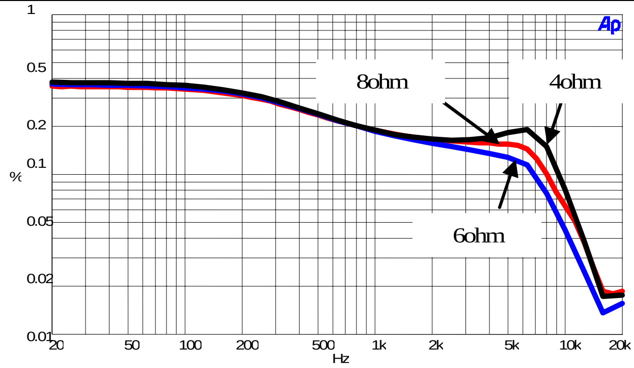


Figure 20. PSSR 5 V 1 W

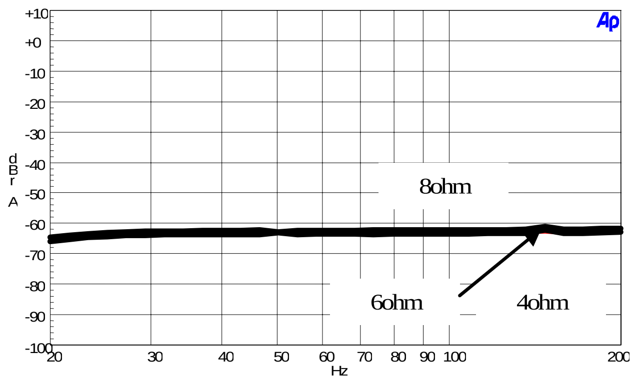


Figure 21. Channel separation 12 V 1 W 4 ohm

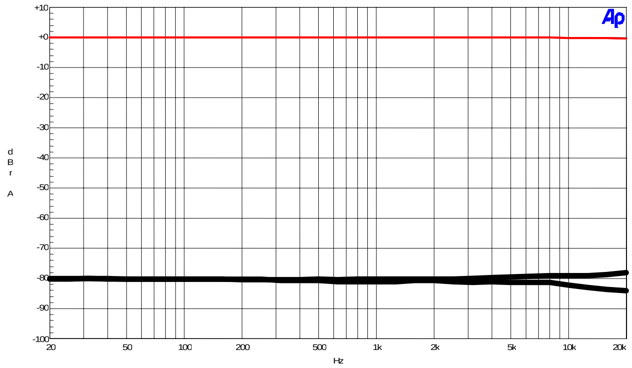


Figure 22. Channel separation 12 V 1 W 8 ohm)

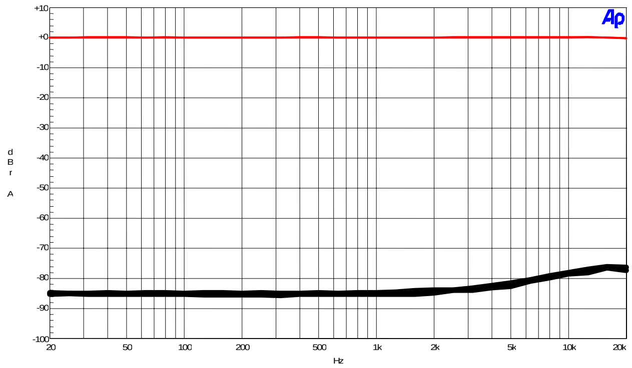


Figure 23. FFT 0 dBFs 1 KHz 12 V 4 ohm

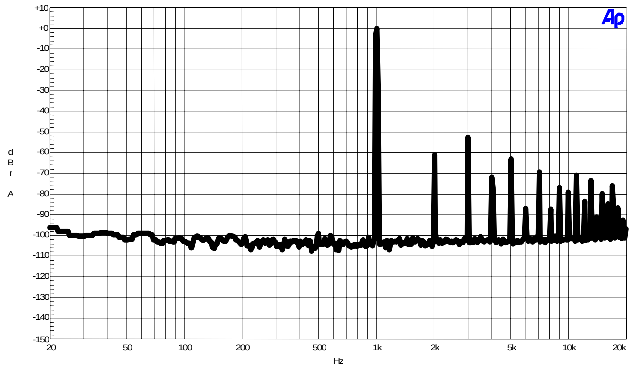


Figure 24. FFT -60 dBFs 1 KHz 12 V 4 ohm

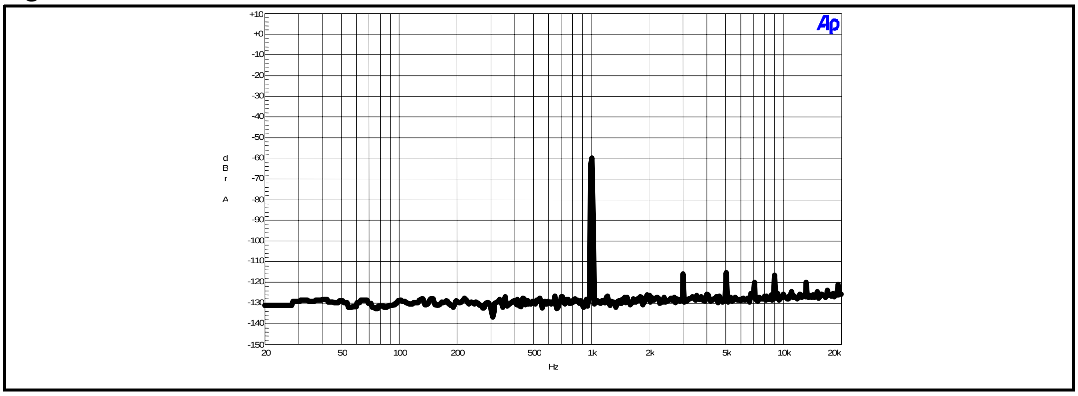


Figure 25. FFT 0 dBFs 1 KHz 12 V 6 ohm

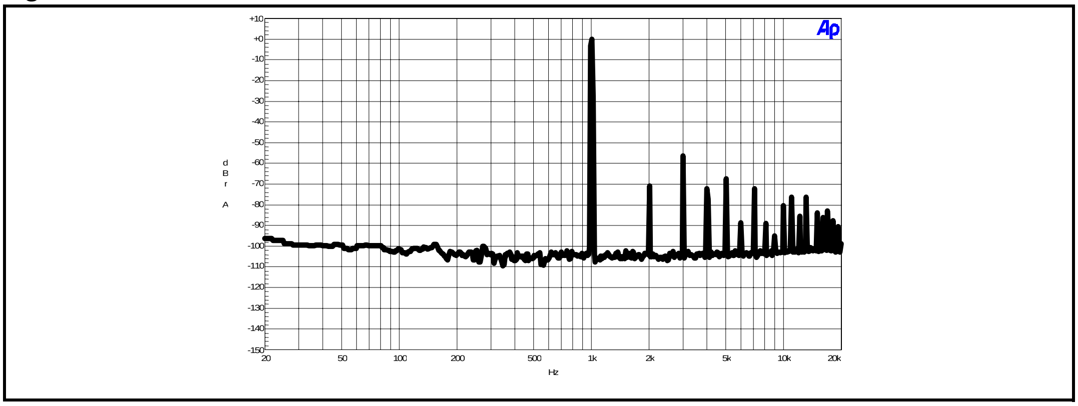


Figure 26. FFT -60 dBFs 1 KHz 12 V 6 ohm

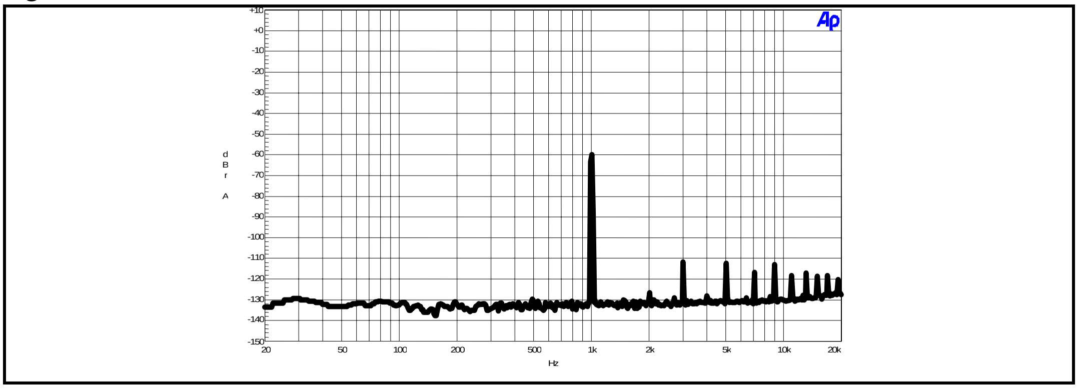


Figure 27. FFT 0 dBFs 1 KHz 12 V 8 ohm

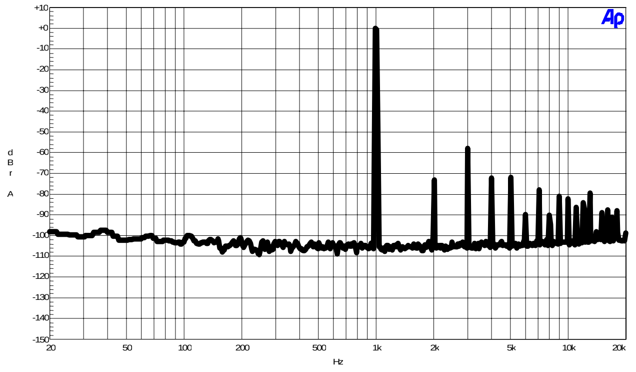


Figure 28. FFT -60 dBFs 1 KHz 12 V 8 ohm

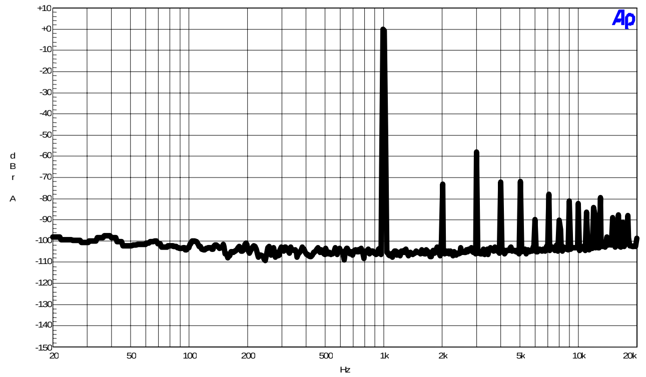


Figure 29. THD versus Freq 12 V Vcc 1 W output

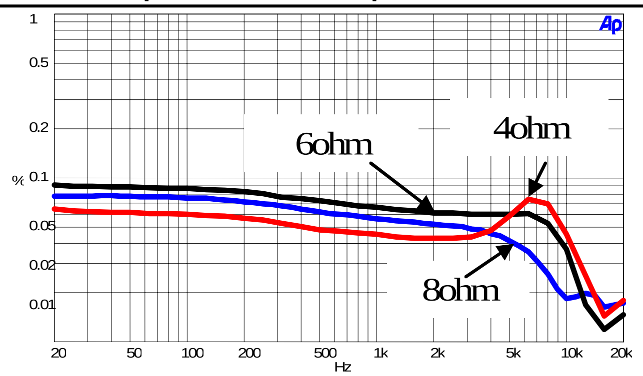


Figure 30. PSSR 12 V 1 W

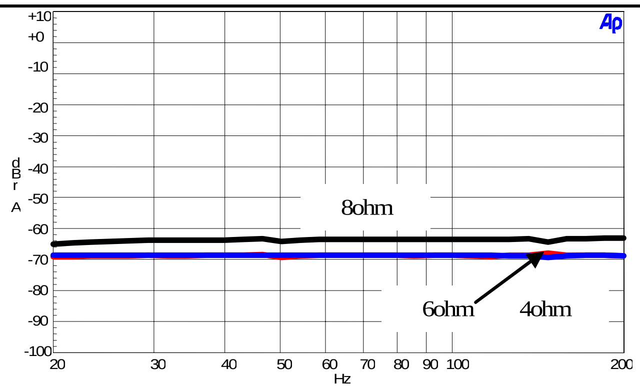


Figure 31. Channel separation 18 V 1 W 4 ohm

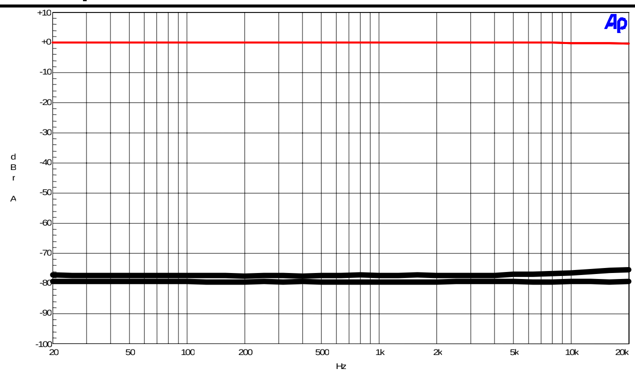


Figure 32. Channel separation 18 V 1 W 6 ohm

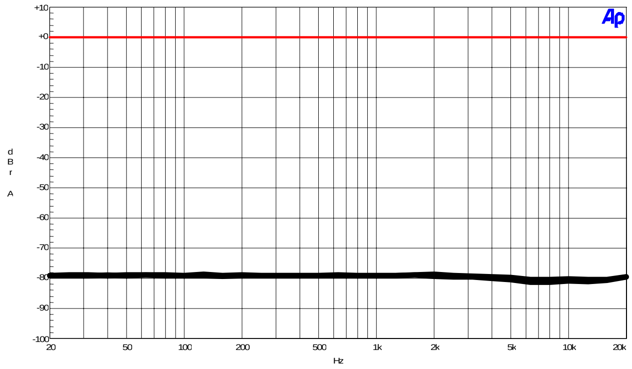


Figure 33. FFT 0 dBFs 1 KHz 18 V 4 ohm

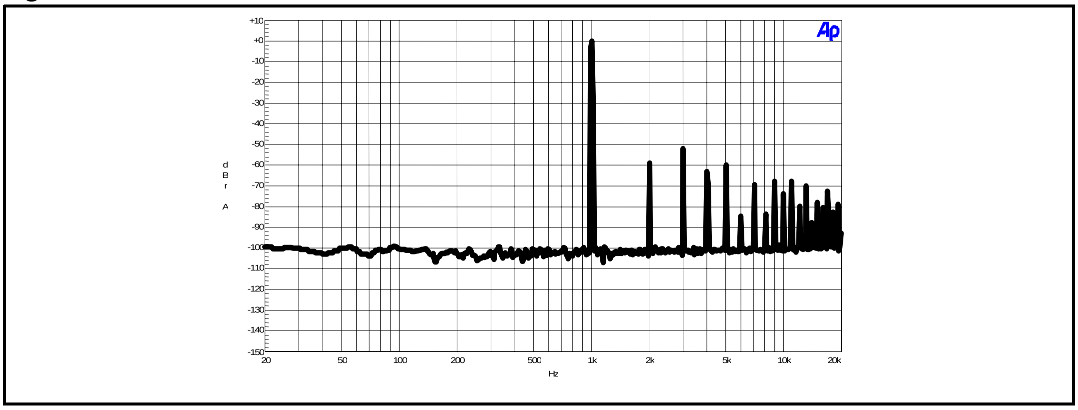


Figure 34. FFT -60 dBFs 1 KHz 18 V 4 ohm

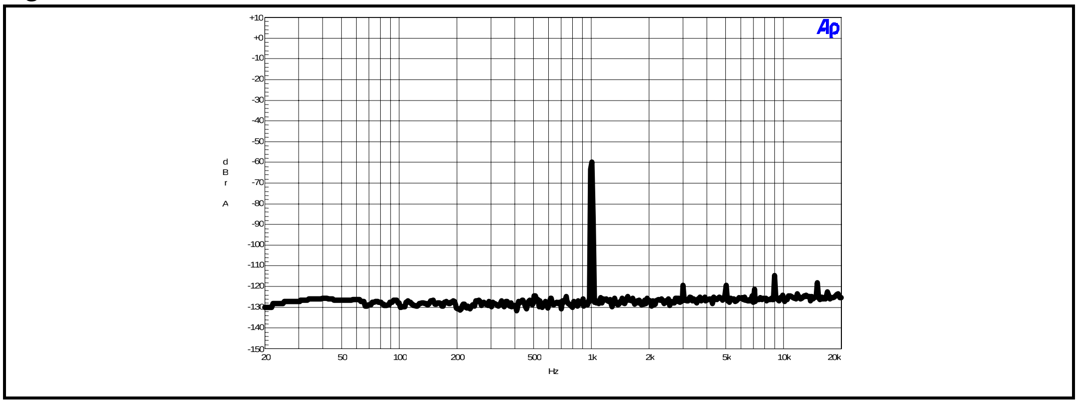


Figure 35. FFT 0 dBFs 1 KHz 18 V 6 ohm

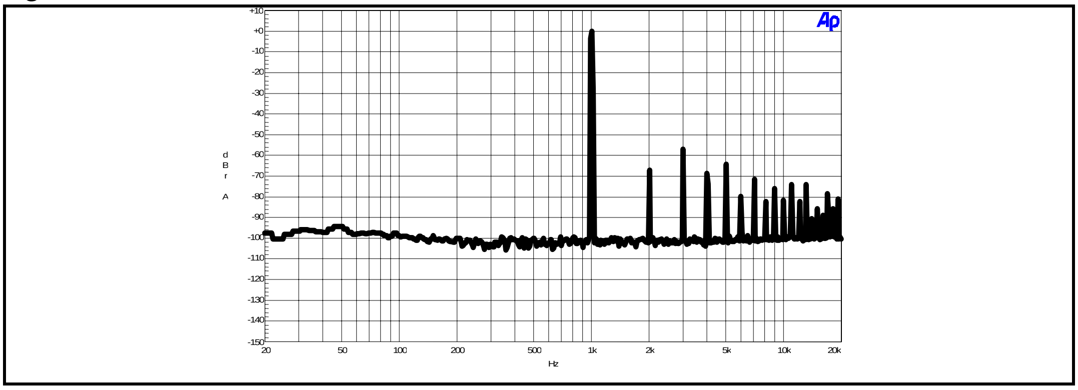


Figure 36. FFT -60 dBFs 1 KHz 18 V 6 ohm

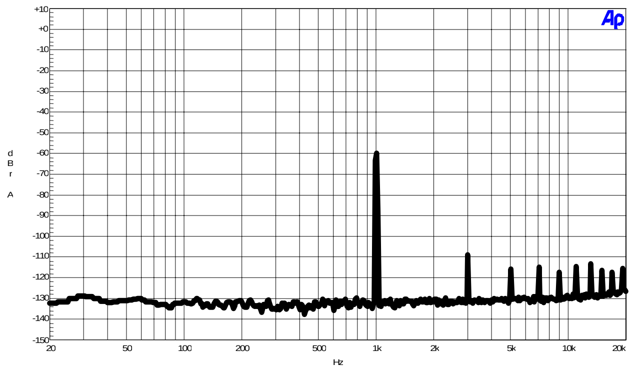


Figure 37. FFT 0 dBFs 1 KHz 18 V 8 ohm

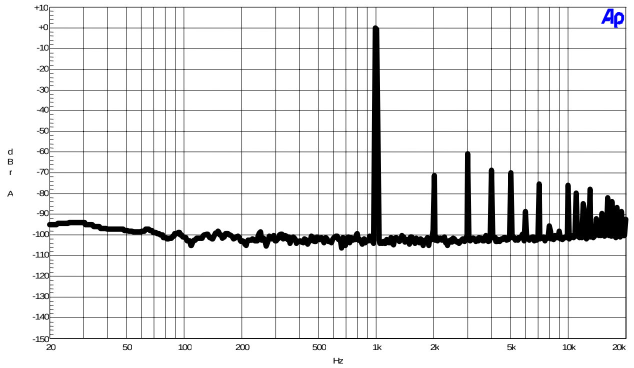


Figure 38. FFT -60 dBFs 1 KHz 18 V 8 ohm

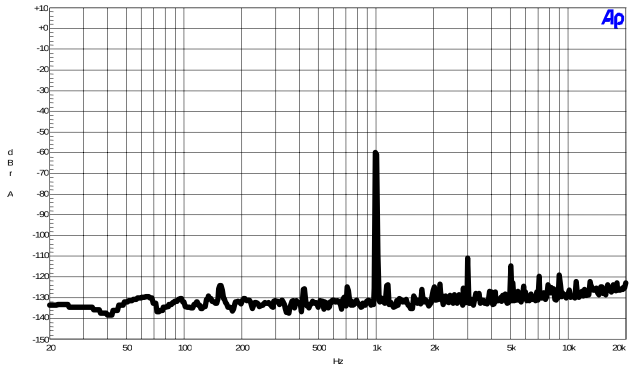


Figure 39. THD versus Freq. 18 V Vcc 1 W

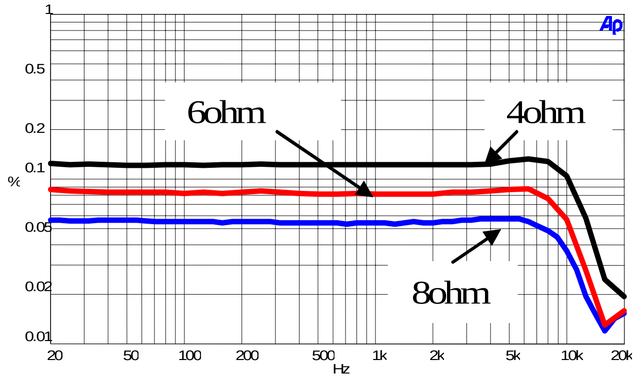


Figure 40. PSSR 18 V 1 W

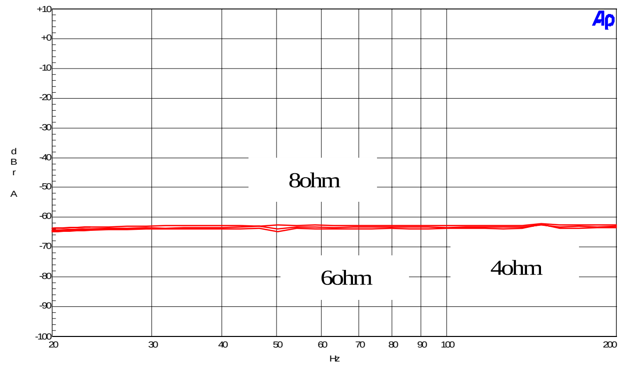


Figure 41. Frequency response 18 V Vcc 1 W

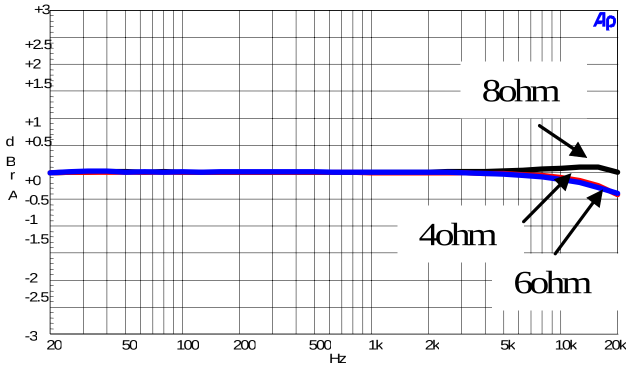


Figure 42. THD versus Freq 18 V Vcc 16 W output

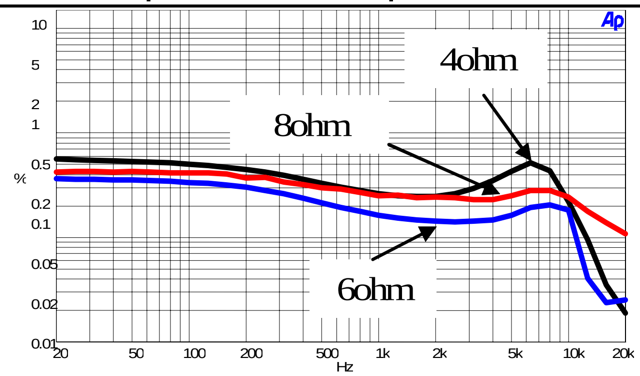


Figure 43. THD versus PWR 4 ohm load

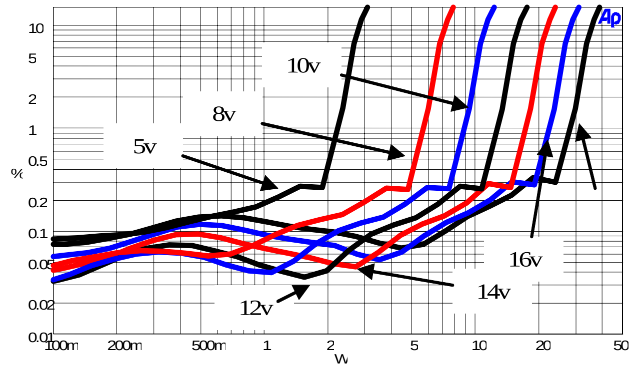


Figure 44. THD versus PWR 6 ohm load

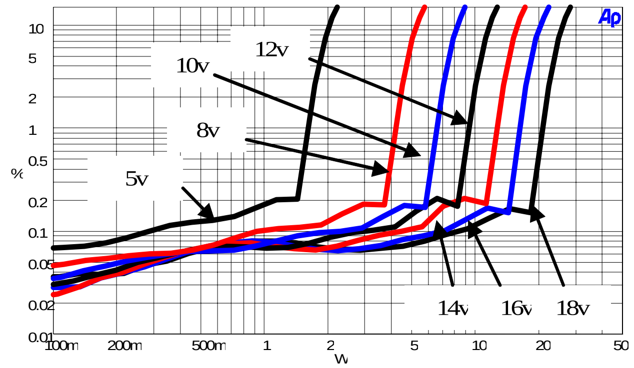


Figure 45. THD versus PWR 8 ohm load

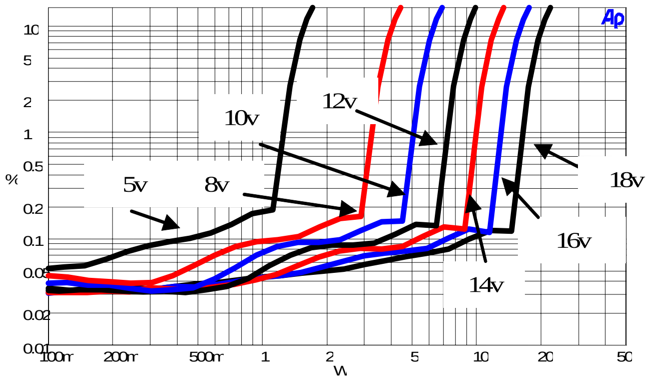
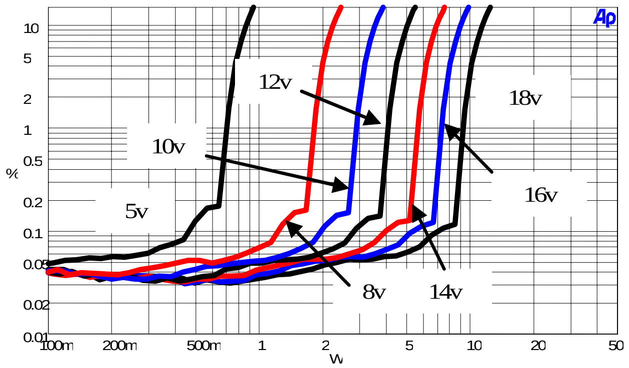
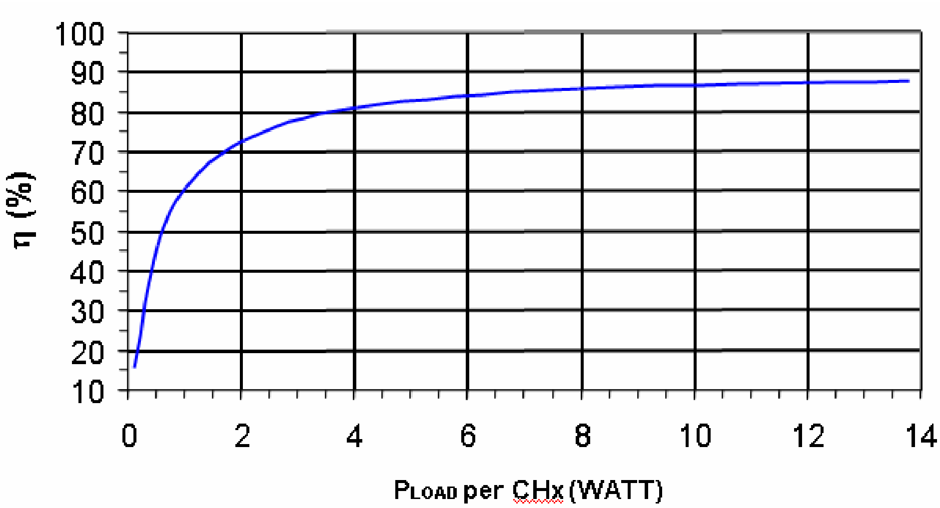


Figure 46. THD versus PWR 16 ohm load



3.3 Binary mode

Figure 47. Binary mode efficiency (2.1 single end configuration)



Condition: R_{LOAD} =8 ohm; VCC=18 V

3.4 Single end configuration

Figure 48. Output power versus supply voltage

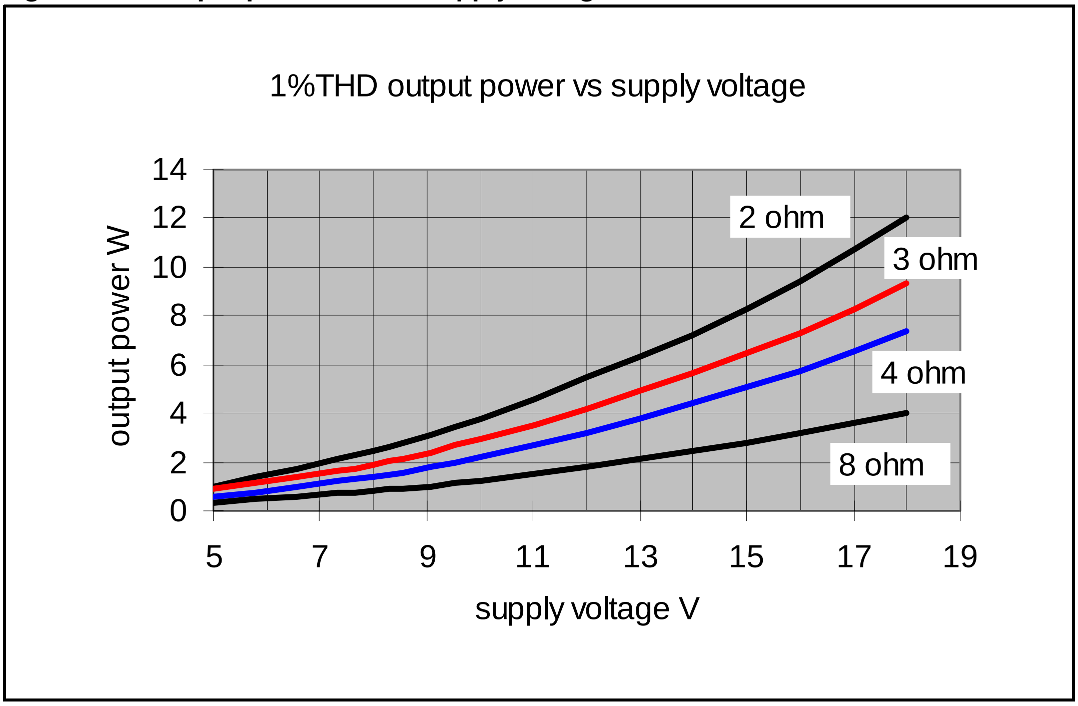


Figure 49. Channel separation 5 V 1 W 2 ohm single end

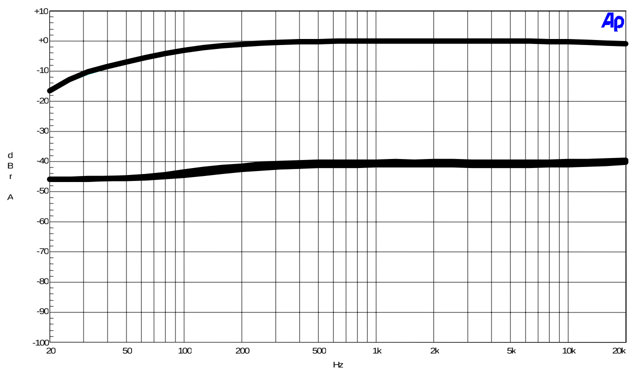


Figure 50. Channel separation 5 V 1 W 3 ohm single end

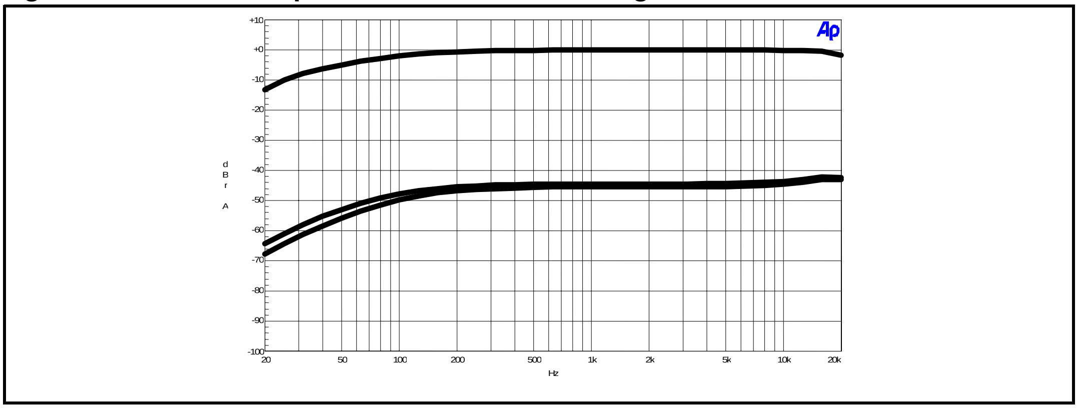


Figure 51. Channel separation 5 V 1 W 4 ohm single end

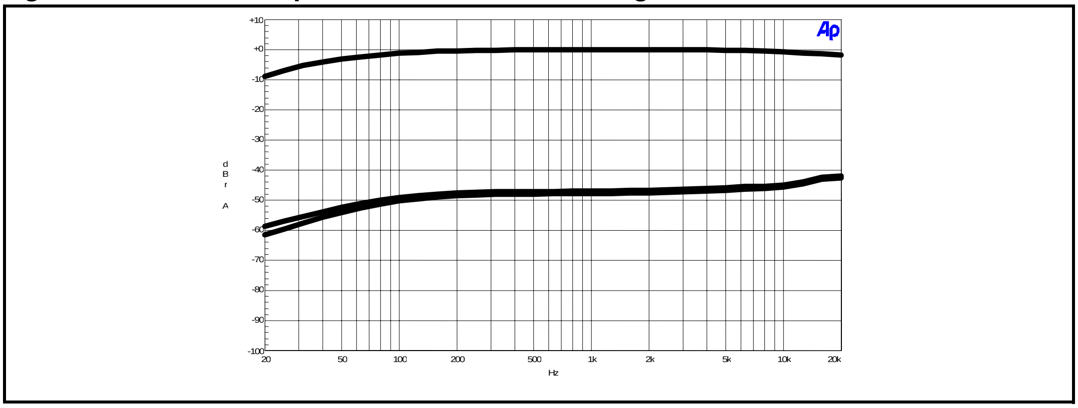


Figure 52. FFT 0 dBFs 1 KHz 5 V 2 ohm single end

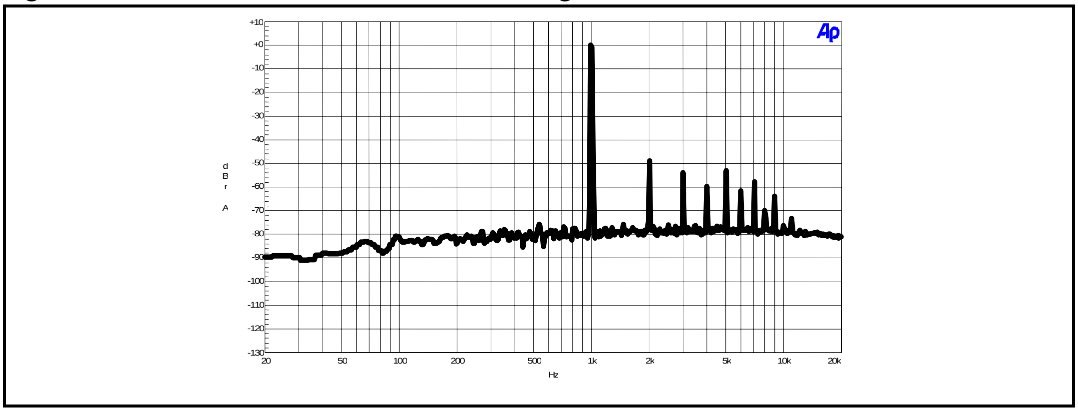


Figure 53. FFT -60 dBFs 1 KHz 5 V 2 ohm single end

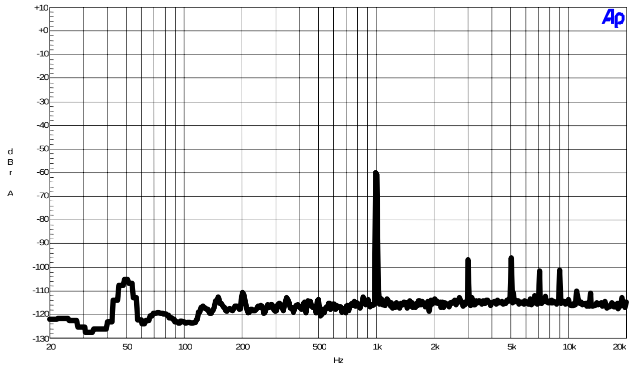


Figure 54. FFT 0 dBFs 1 KHz 12 V 3 ohm single end

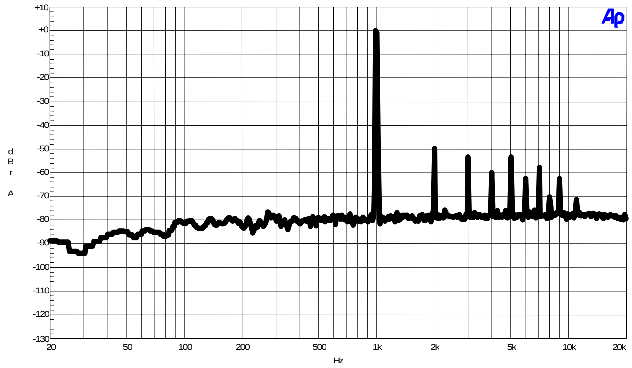


Figure 55. FFT -60 dBFs 1 KHz 5 V 3 ohm single end

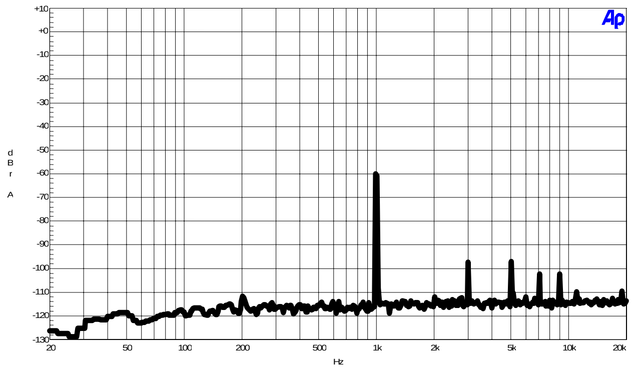


Figure 56. FFT 0 dBFs 1 KHz 5 V 4 ohm single end

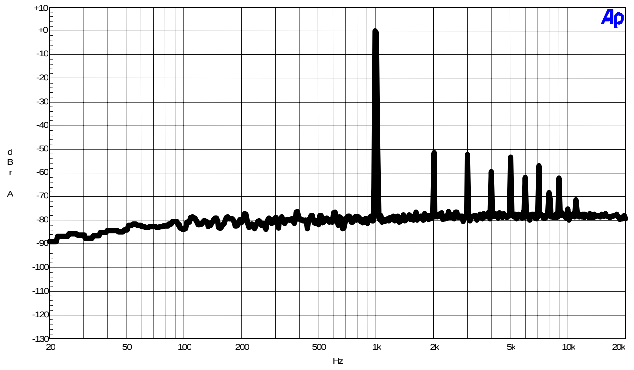


Figure 57. FFT -60 dBFs 1 KHz 5 V 4 ohm

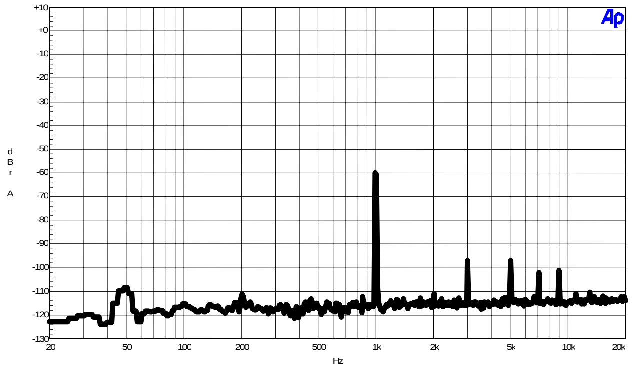


Figure 58. PSSR 5 V 1 W

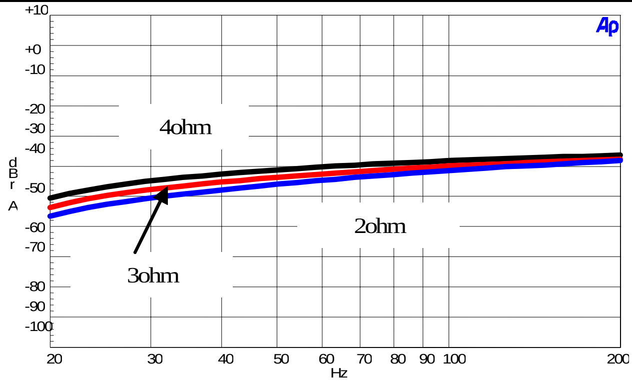


Figure 59. Channel separation 12 V 1 W 2 ohm single end

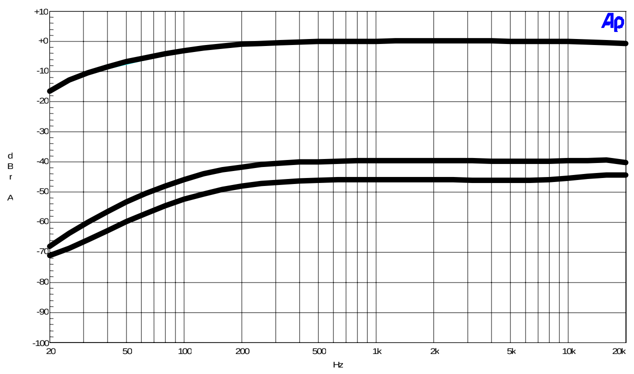


Figure 60. Channel separation 12 V 1 W 3 ohm single end

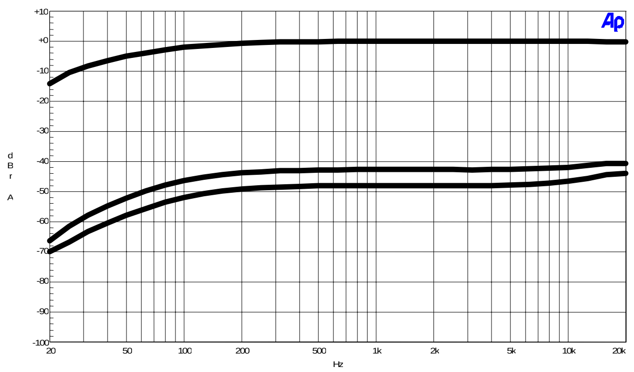


Figure 61. Channel separation 12 V 1 W 4 ohm single end

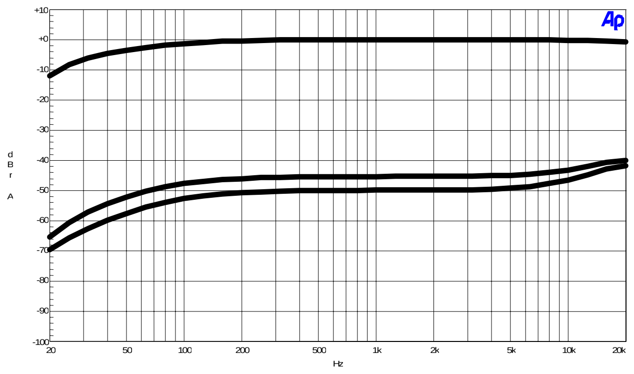


Figure 62. FFT 0 dBFs 1 KHz 12 V 2 ohm single end

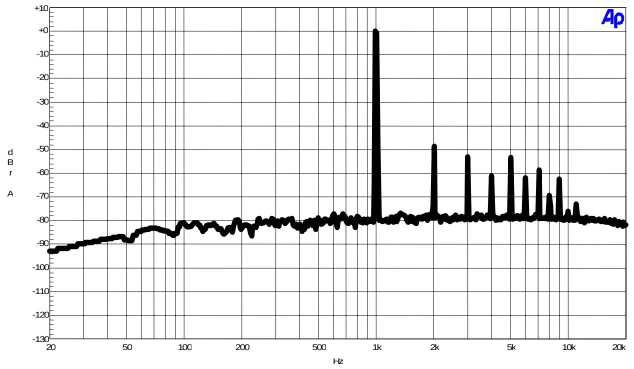


Figure 63. FFT -60 dBFs 1 KHz 12 V 2 ohm single end

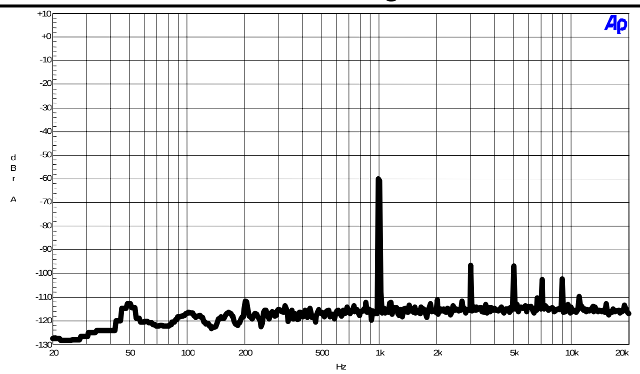


Figure 64. FFT 0 dBFs 1 KHz 12 V 3 ohm single end

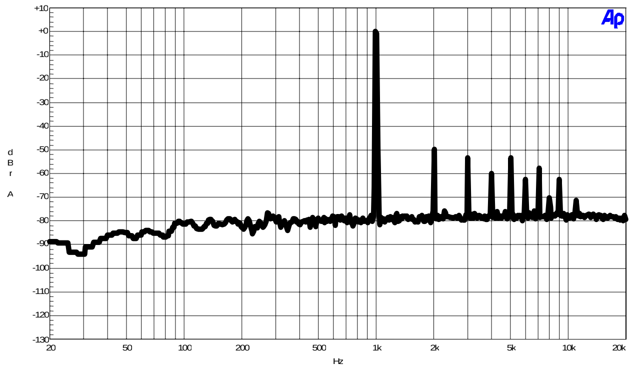


Figure 65. FFT -60 dBFs 1 KHz 12 V 3 ohm single end

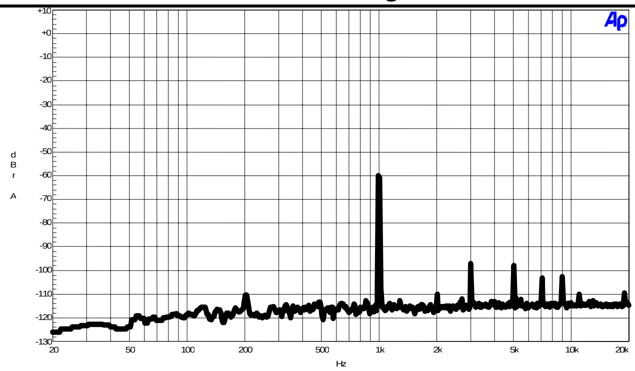


Figure 66. FFT 0 dBFs 1 KHz 12 V 4 ohm single end

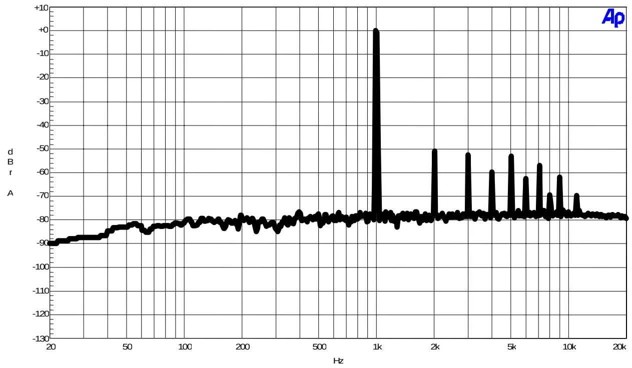


Figure 67. FFT -60 dBFs 1 KHz 12 V 4 ohm single end

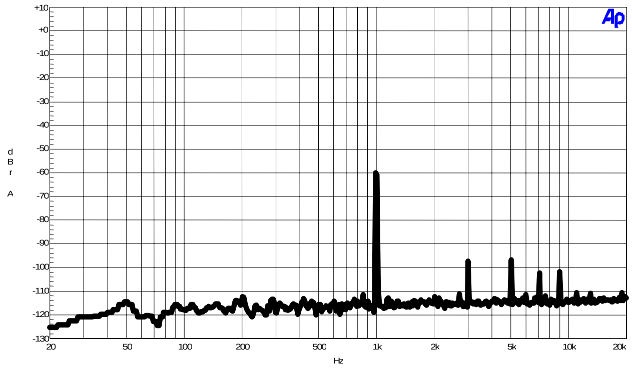


Figure 68. PSSR 12 V 1 W

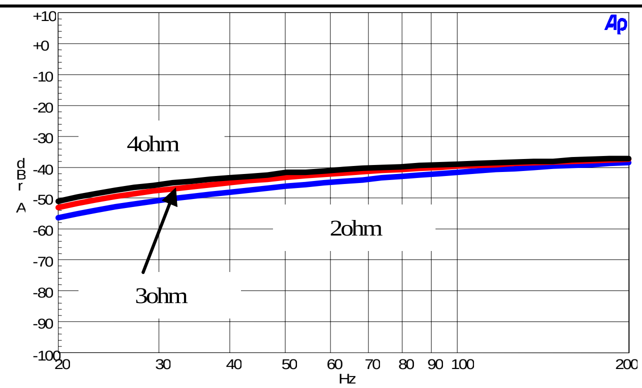


Figure 69. THD versus Freq 12 V Vcc 1 W output single end

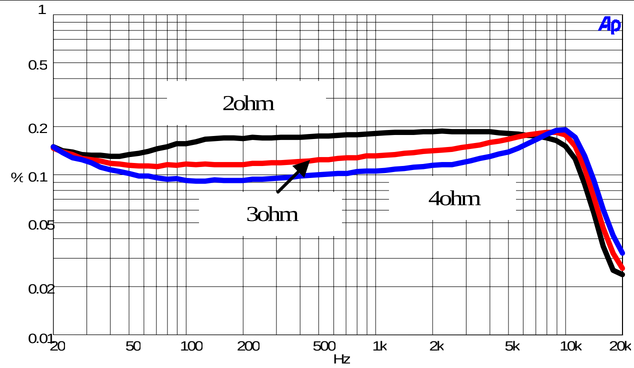


Figure 70. Channel separation 18 V 1 W 2 ohm single end

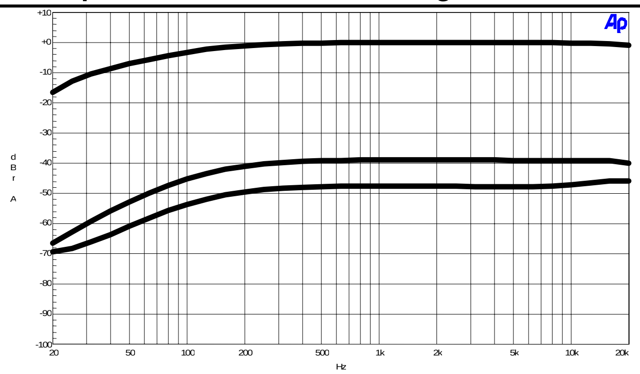


Figure 71. Channel separation 18 V 1 W 3 ohm single end

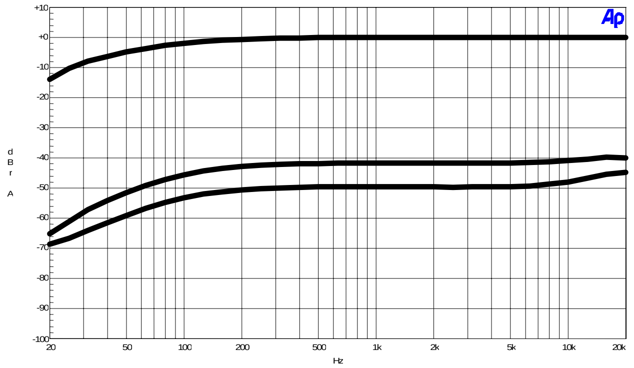


Figure 72. Channel separation 18 V 1 W 4 ohm single end

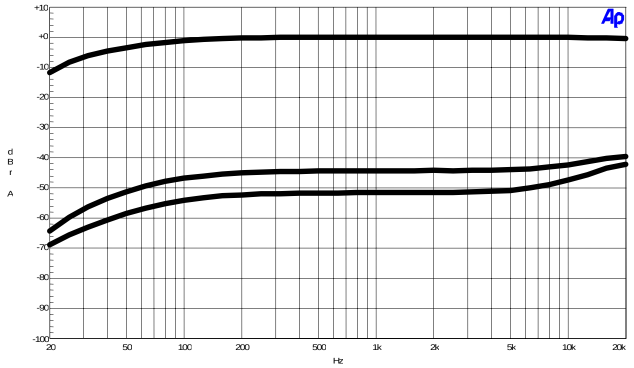


Figure 73. FFT 0 dBFs 1 KHz 18 V 2 ohm single end

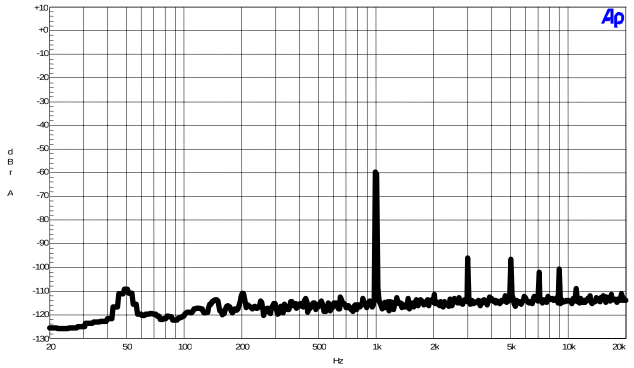


Figure 74. FFT -60 dBFs 1 KHz 18 V 2 ohm single end

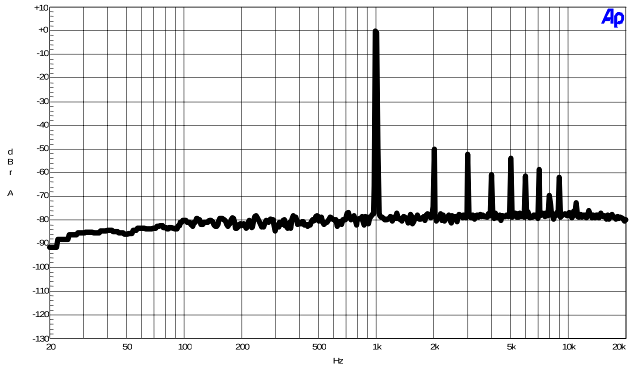


Figure 75. FFT 0 dBFs 1 KHz 18 V 3 ohm single end

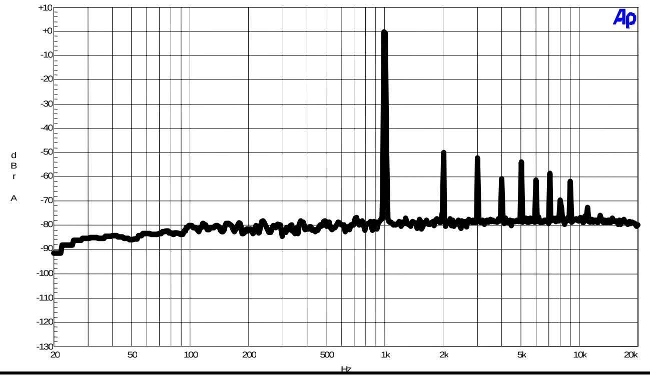


Figure 76. FFT -60 dBFs 1 KHz 18 V 3 ohm single end

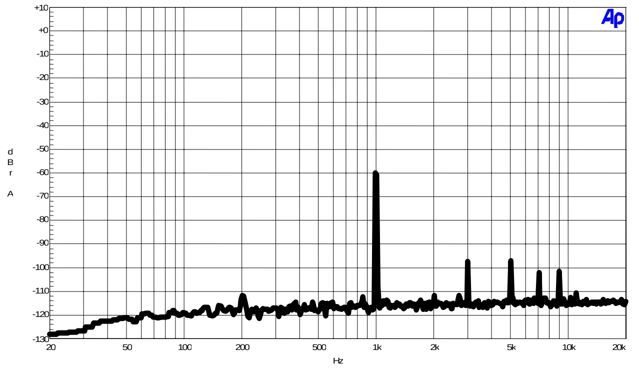


Figure 77. FFT 0 dBFs 1 KHz 18 V 4 ohm single end

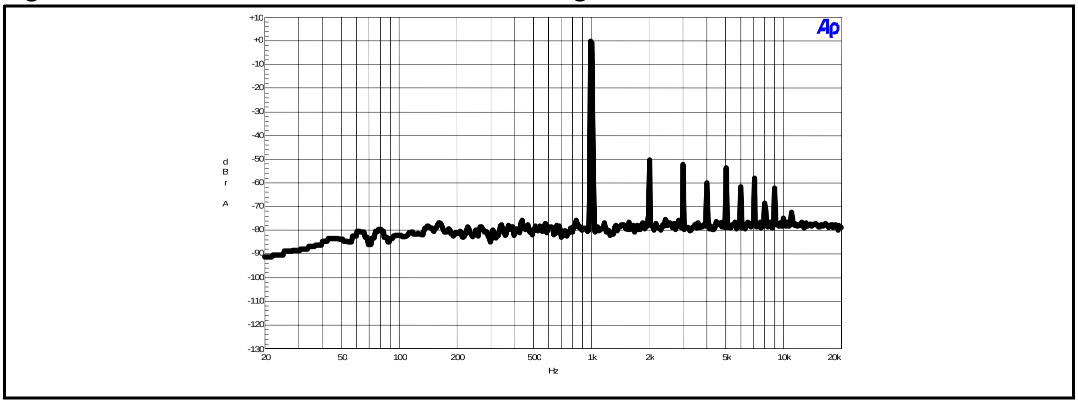


Figure 78. FFT -60 dBFs 1 KHz 18 V 4 ohm single end

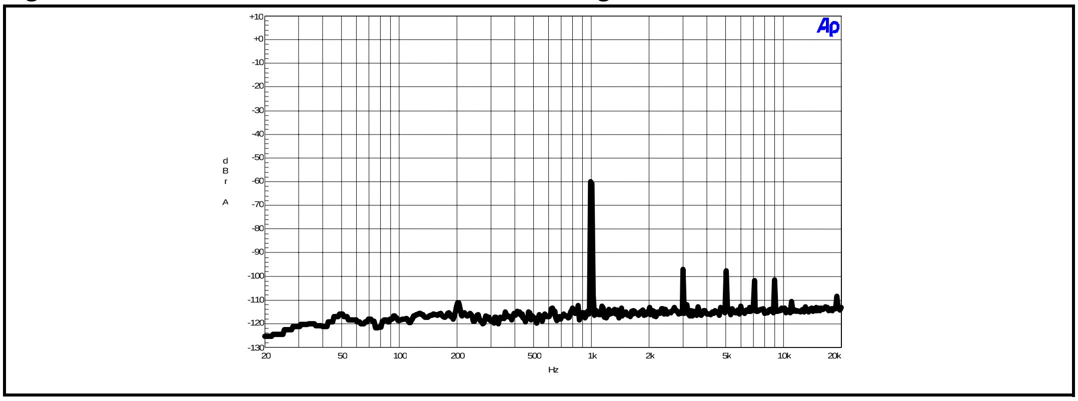


Figure 79. PSSR 18 V 1 W

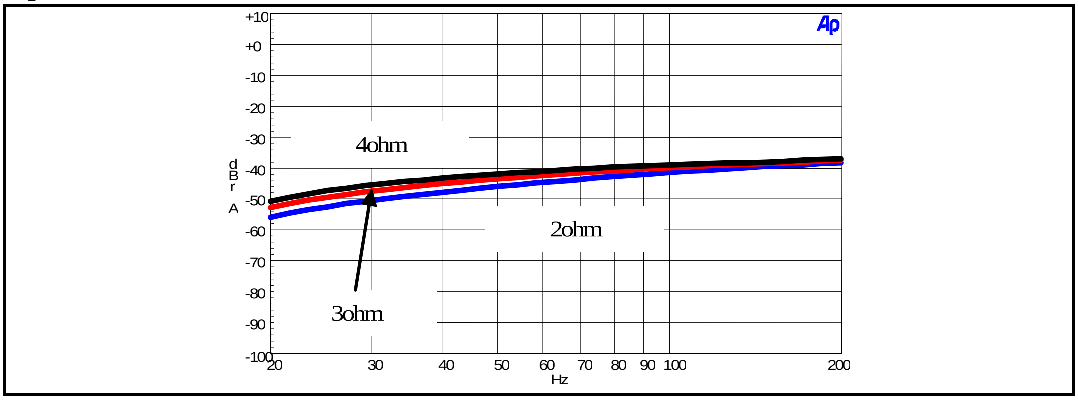


Figure 80. THD versus Freq 18 V Vcc 1 W output single end

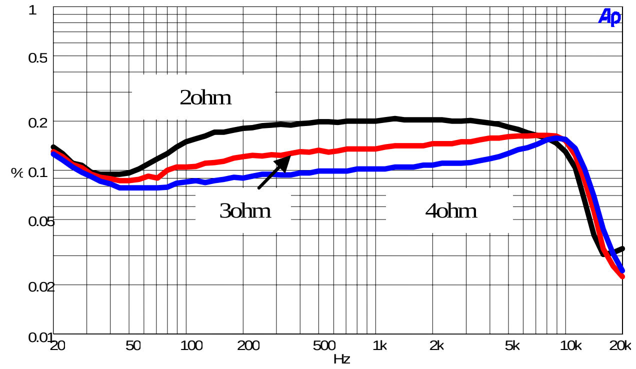


Figure 81. THD versus PWR 2 ohm load single end

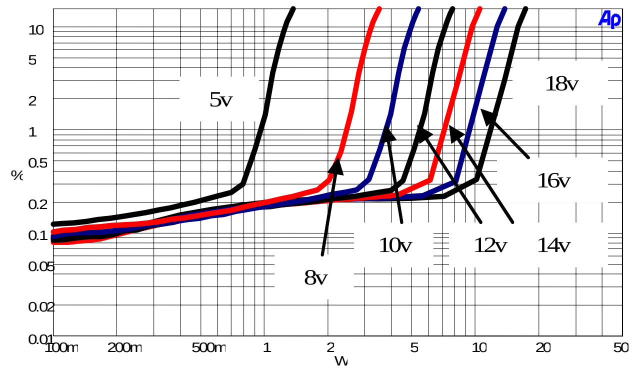


Figure 82. THD versus PWR 3 ohm load single end

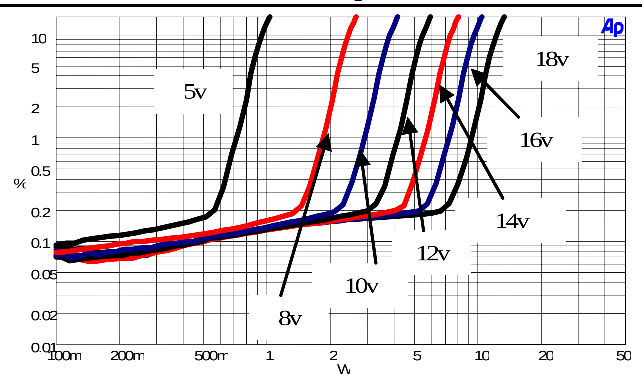


Figure 83. THD versus PWR 4 ohm load single end

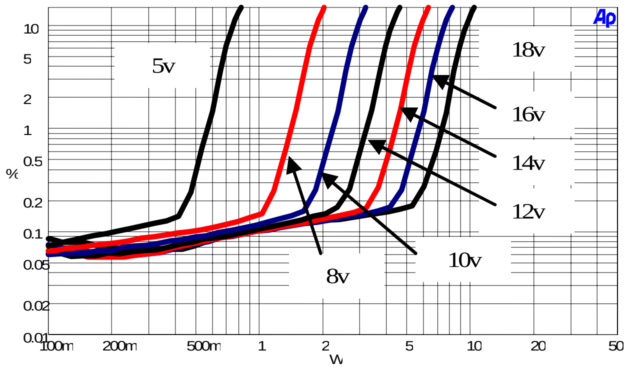
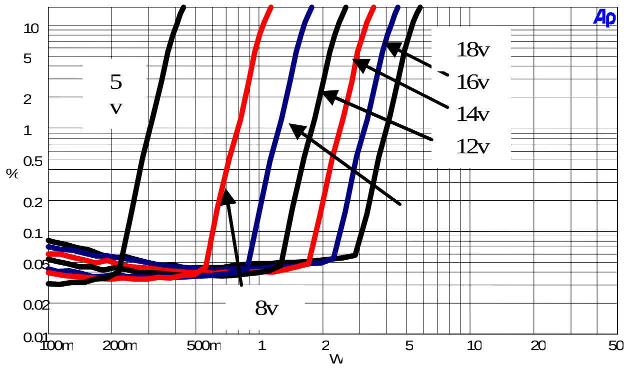


Figure 84. THD versus PWR 8 ohm load single end



3.5 Headphone performance

Figure 85. Channel separation 5 V 1 mW 16 ohm

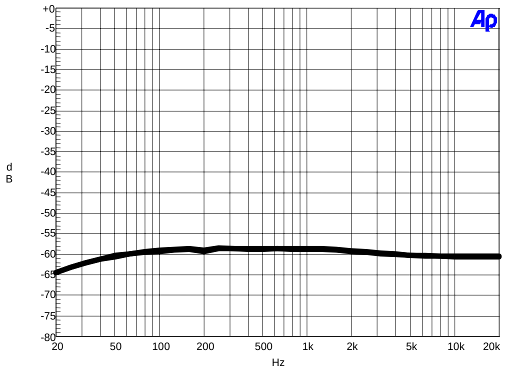


Figure 86. Channel separation 5 V 1 nW 32 ohm

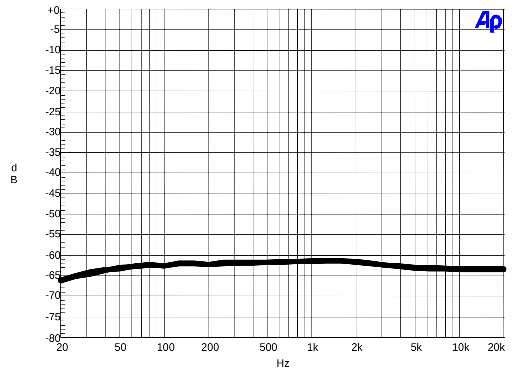


Figure 87. Channel separation 12 V 1 mW 16 ohm

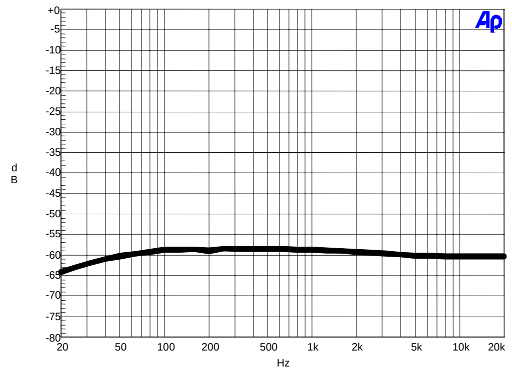


Figure 88. Channel separation 12 V 1 mW 32 ohm

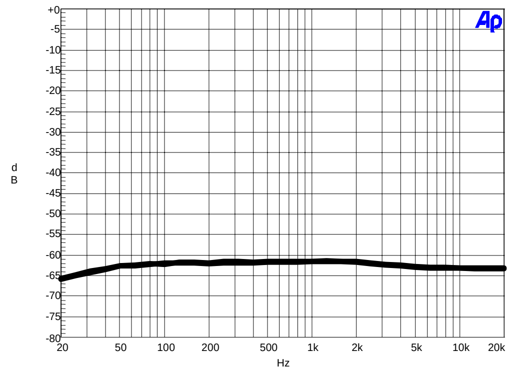


Figure 89. Channel separation 18 V 1 nW 16 ohm

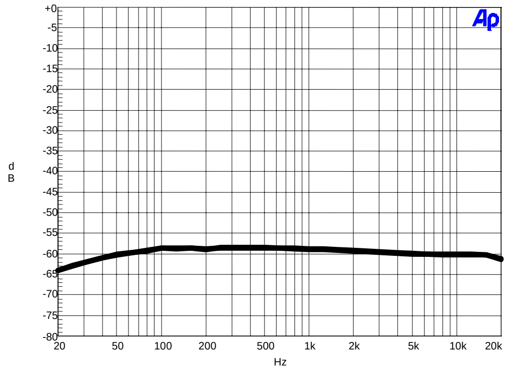


Figure 90. Channel separation 12 V 1 mW 32 ohm

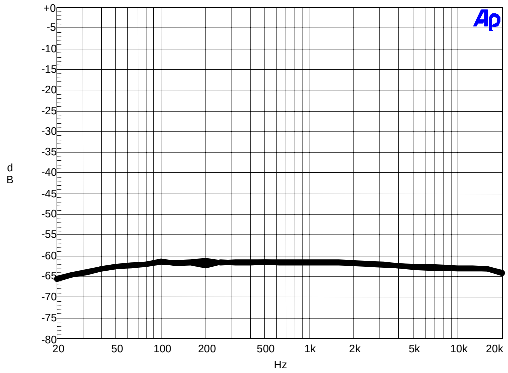


Figure 91. Noise floor 5 V 16 ohm

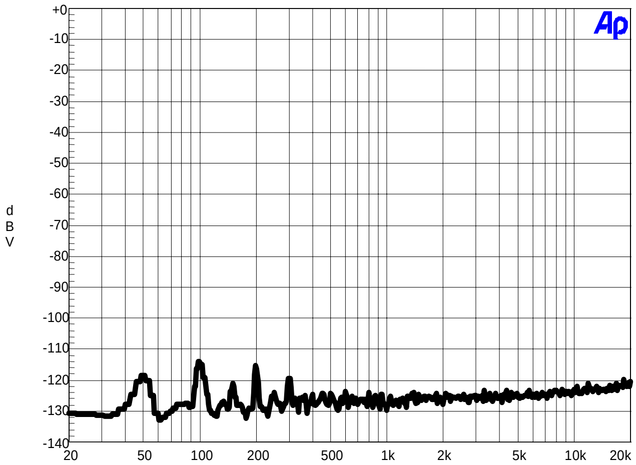


Figure 92. FFT 0 dBFs 1 KHz 5 V 16 ohm

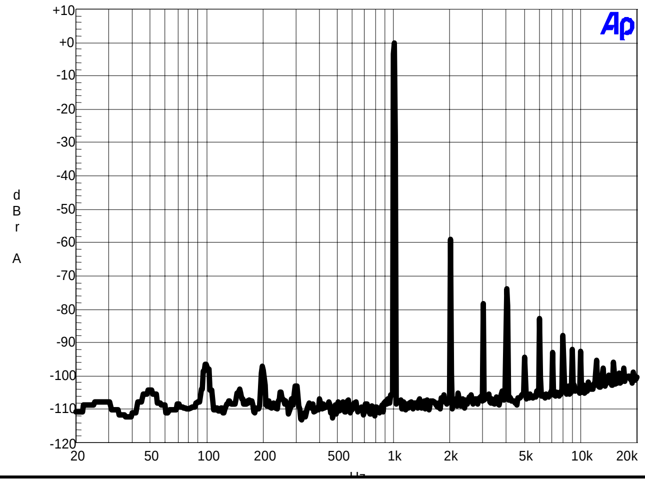


Figure 93. FFT -60 dBFs 1 KHz 5 V 16 ohm

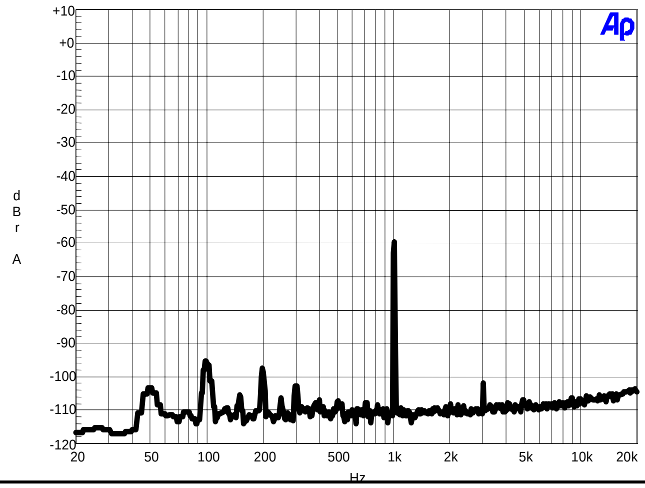


Figure 94. Noise floor 5 V 32 ohm

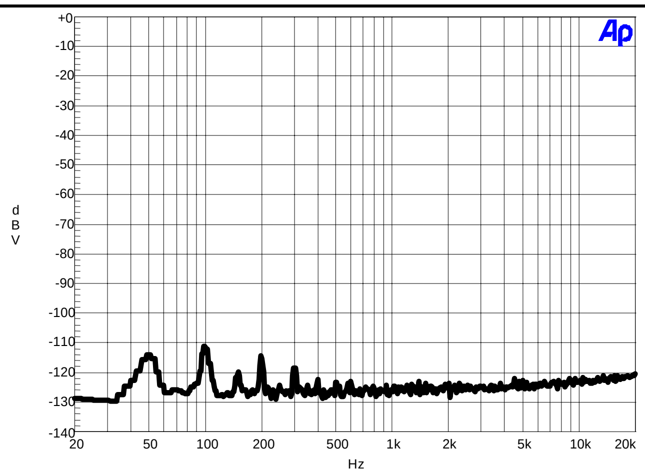


Figure 95. FFT 0 dBFs 1 KHz 5 V 32 ohm

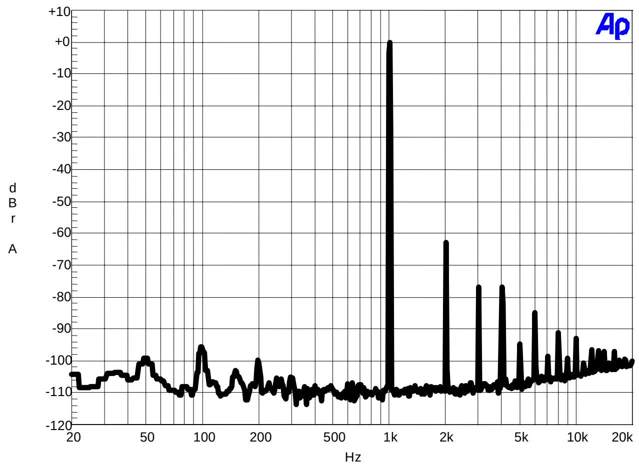


Figure 96. FFT -60 dBFs 1 KHz 5 V 32 ohm

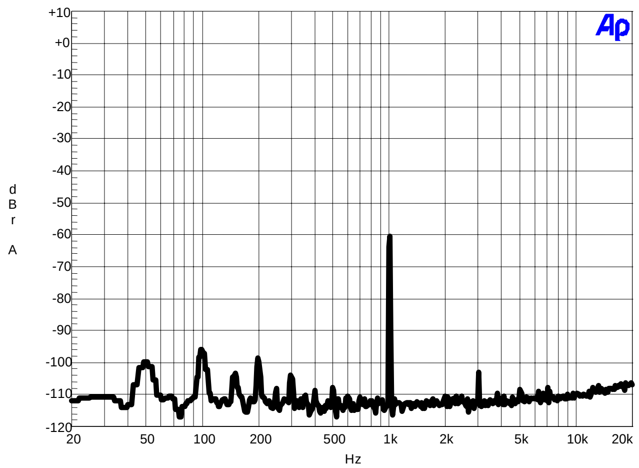


Figure 97. Noise floor 12 V 16 ohm

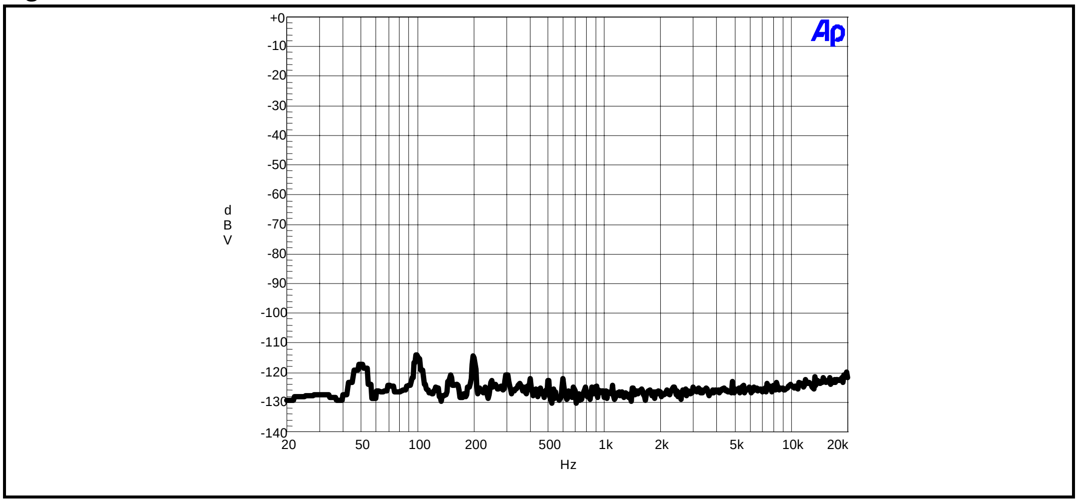


Figure 98. FFT 0 dBFs 1 KHz 12 V 16 ohm

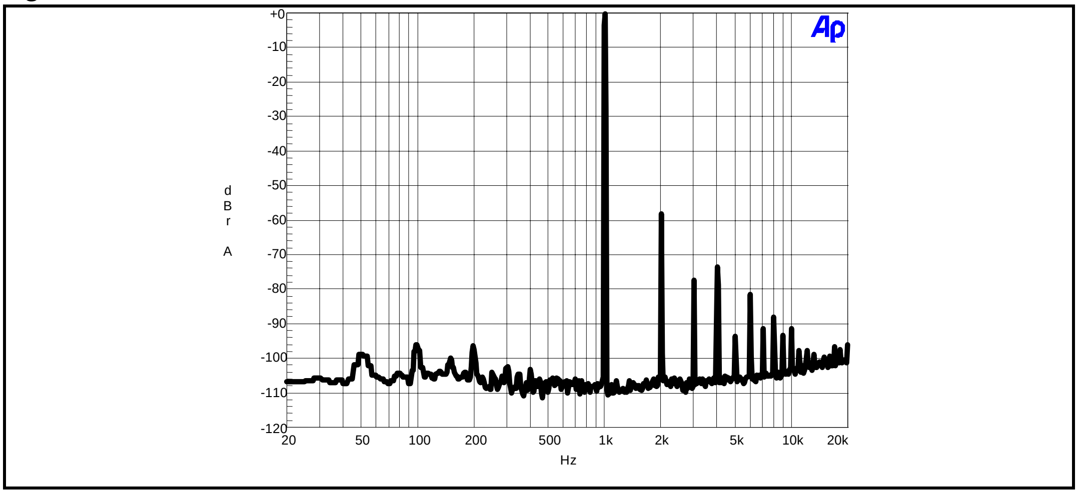


Figure 99. FFT -60 dBFs 1 KHz 12 V 16 ohm

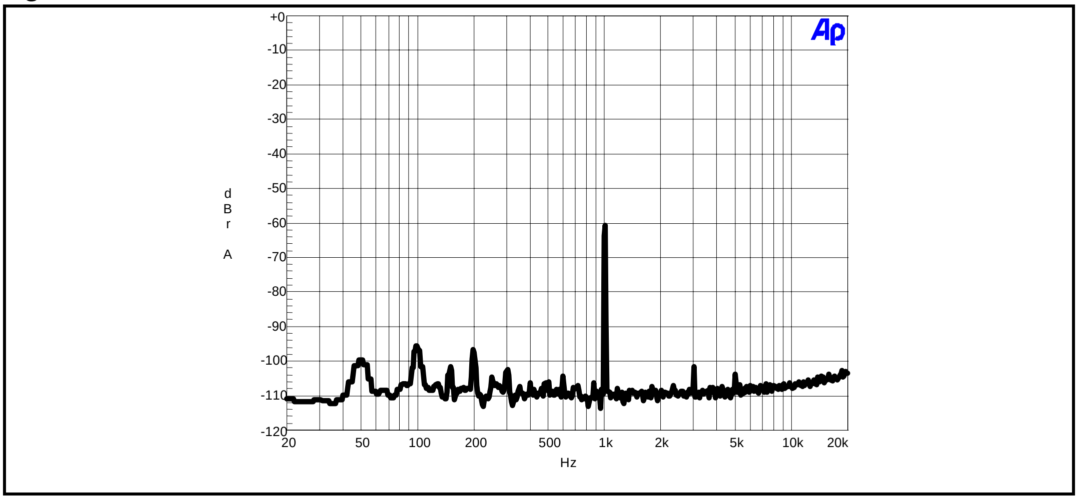


Figure 100. Noise floor 12 V 32 ohm

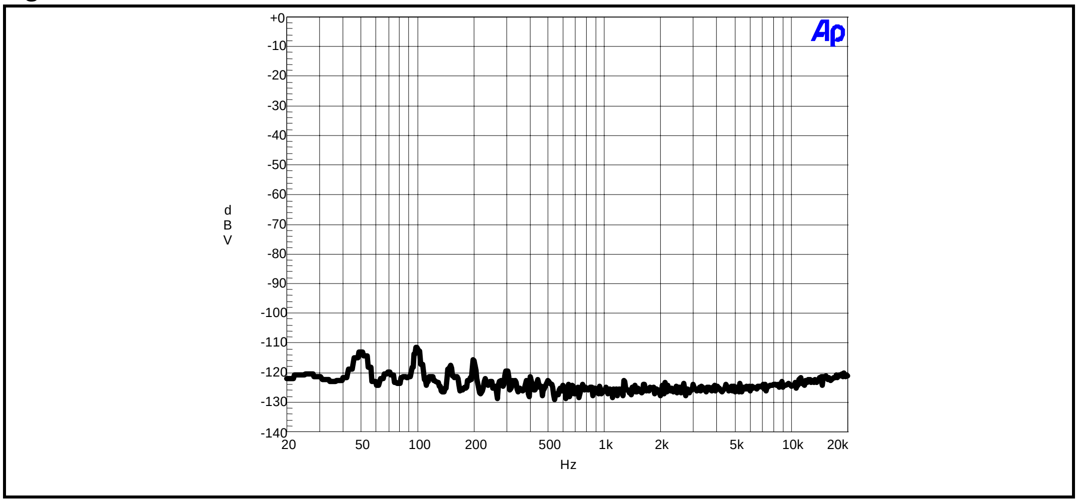


Figure 101. FFT 0 dBFs 1 KHz 12 V 32 ohm

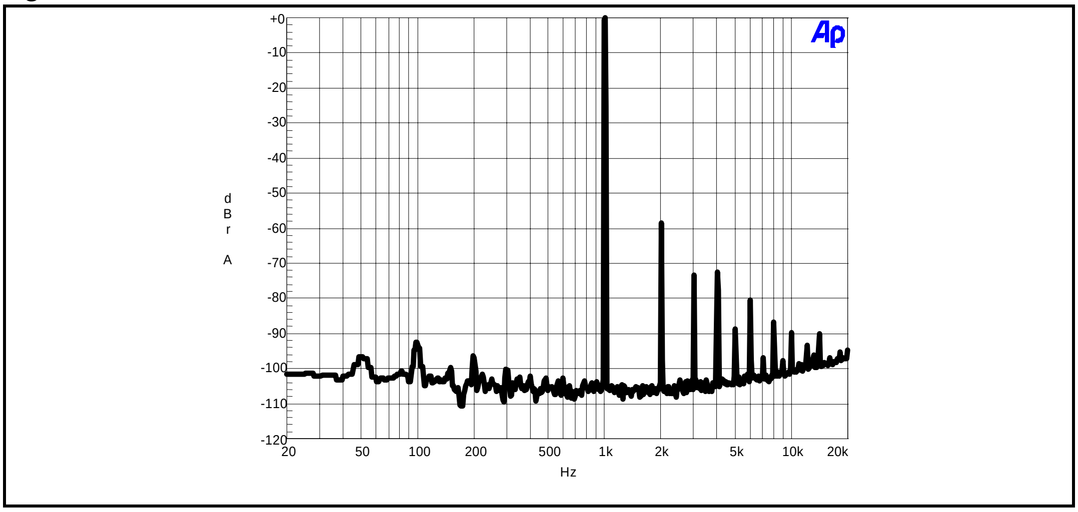


Figure 102. FFT -60 dBFs 1 KHz 12 V 32 ohm

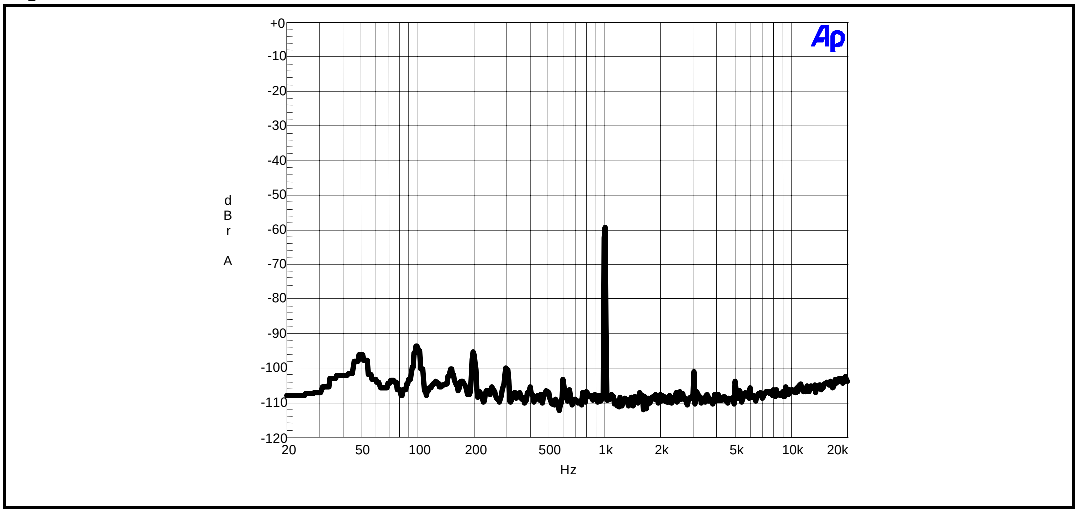


Figure 103. Noise floor 18 V 16 ohm

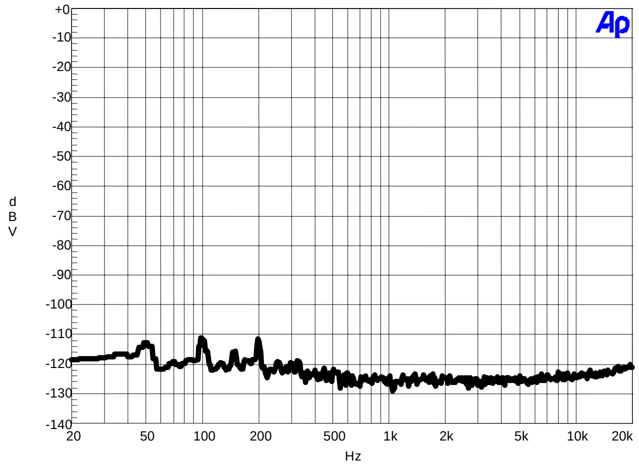


Figure 104. FFT 0 dBFs 1 KHz 18 V 16 ohm

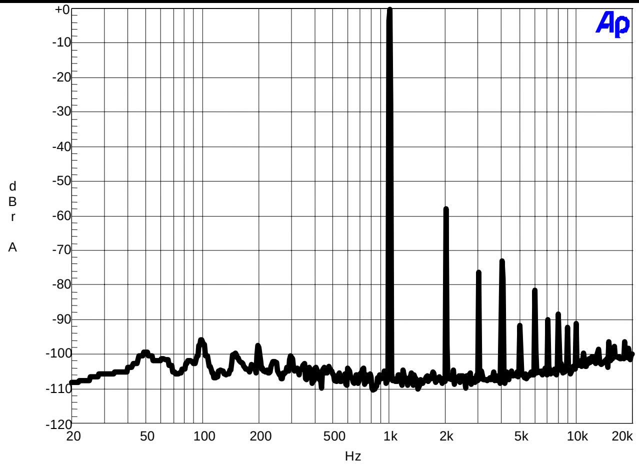


Figure 105. FFT -60 dBFs 1 KHz 18 V 16 ohm

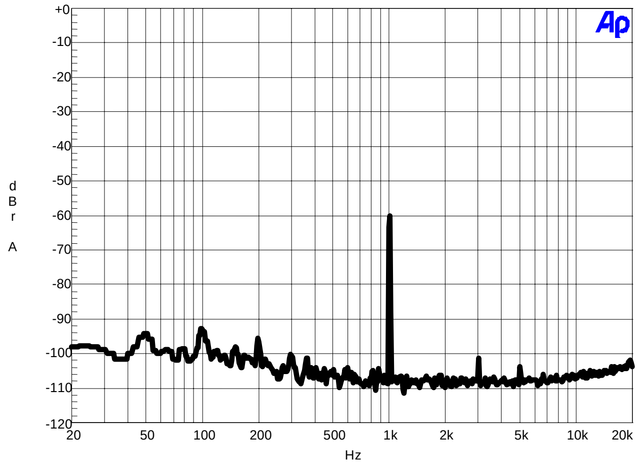


Figure 106. Noise floor 18 V 32 ohm

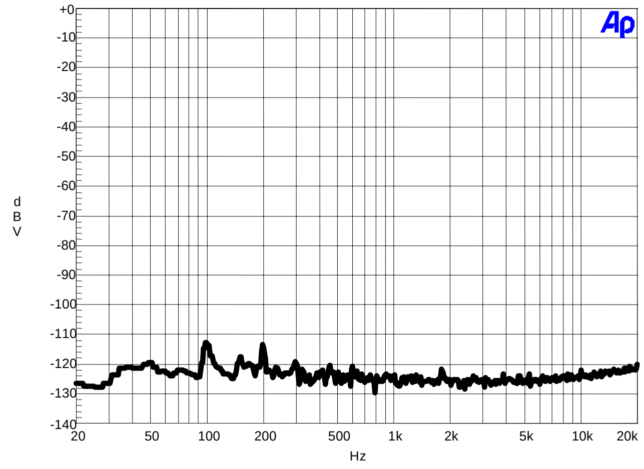


Figure 107. FFT 0 dBFs 1 KHz 18 V 32 ohm

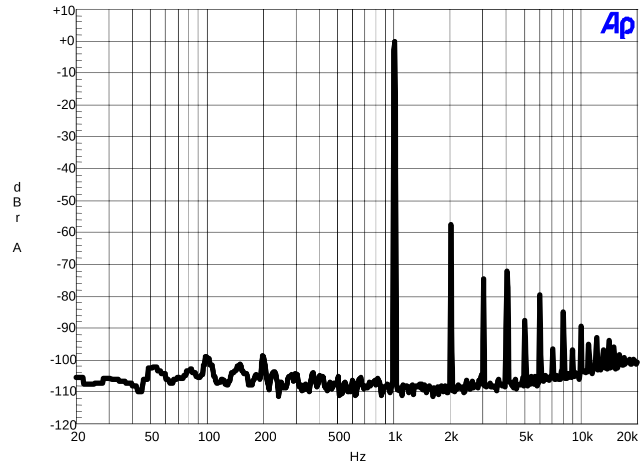


Figure 108. FFT -60 dBFs 1 KHz 18 V 32 ohm

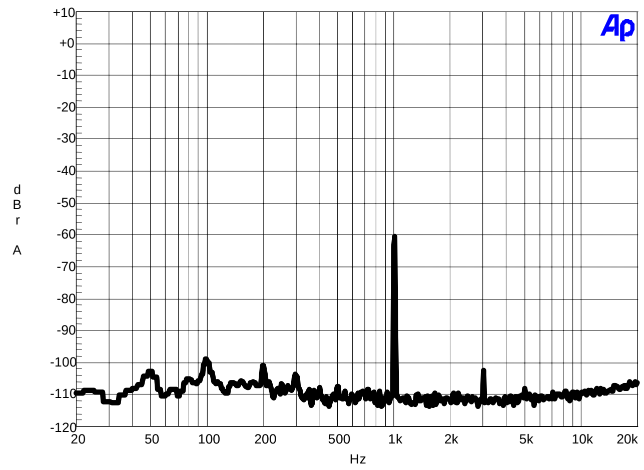


Figure 109. THD versus Freq 5 V 1 mW 16 ohm

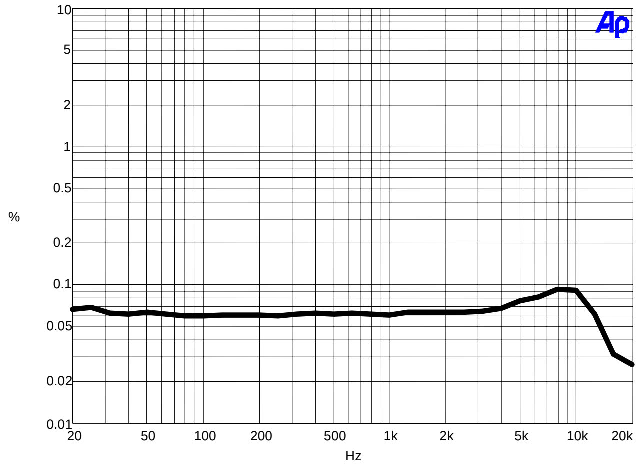


Figure 110. THD versus Freq 5 V 1 mW 32 ohm

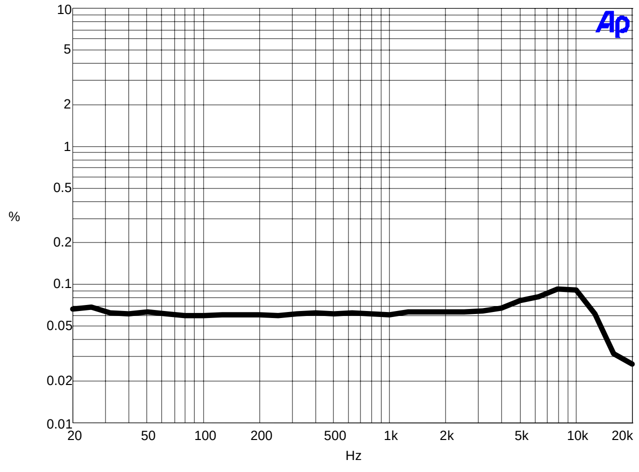


Figure 111. THD versus Freq 12 V 1 mW 16 ohm

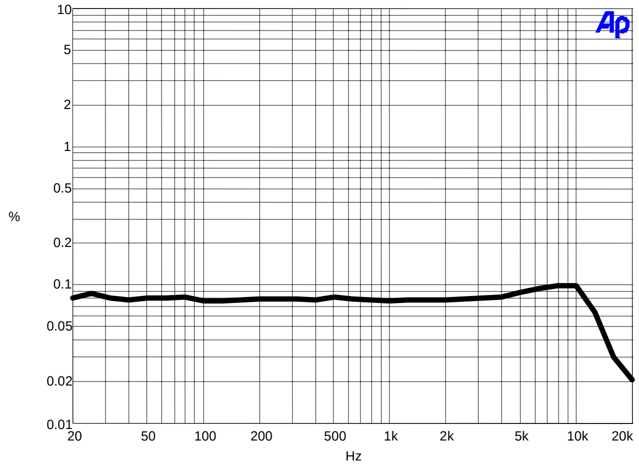


Figure 112. THD versus Freq 12 V 1 mW 32 ohm

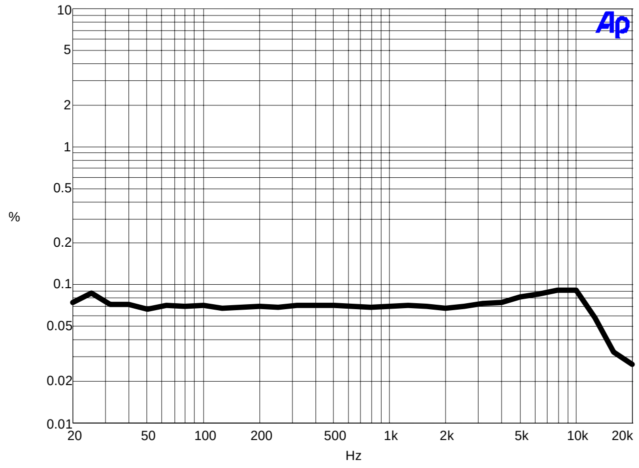


Figure 113. THD versus Freq 18 V 1 mW 16 ohm

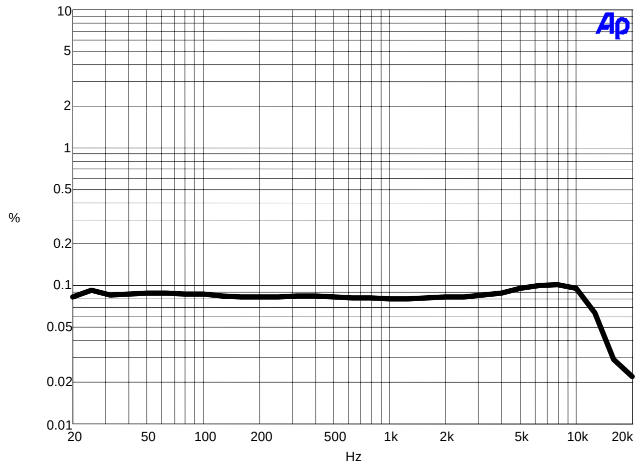


Figure 114. THD versus Freq18 V 1 mW 32 ohm

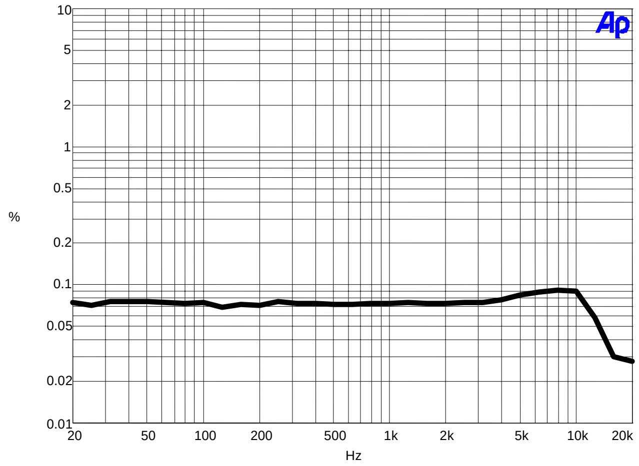


Figure 115. THD versus PWR 16 ohm

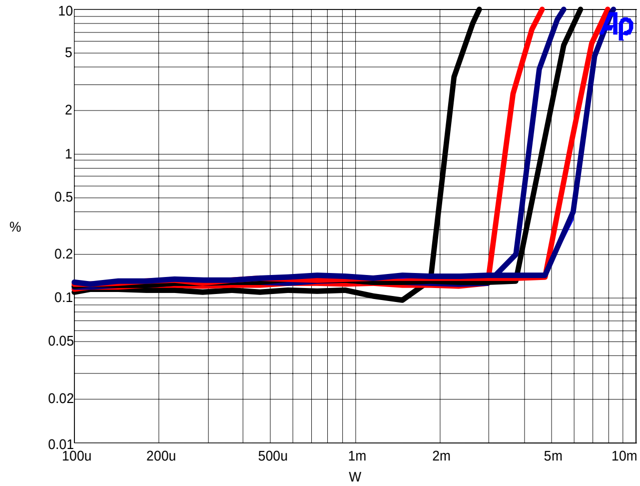
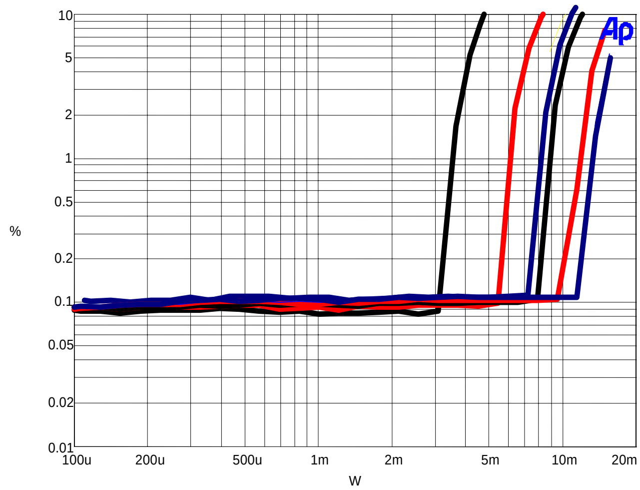


Figure 116. THD versus PWR 32 ohm



4 Design guideline for PCB schematic and layout

4.1 Schematic

4.1.1 Main driver for components selection

- Absolute maximum rate: 20 V.
- Bypass capacitor 100 nF in parallel to 1 µF for each power Vcc branch. Preferable dielectric is X7R.
- Vdd and ground for PLL filter separate of the power supply.
- Coil saturation current compatible with the peak current of the application.

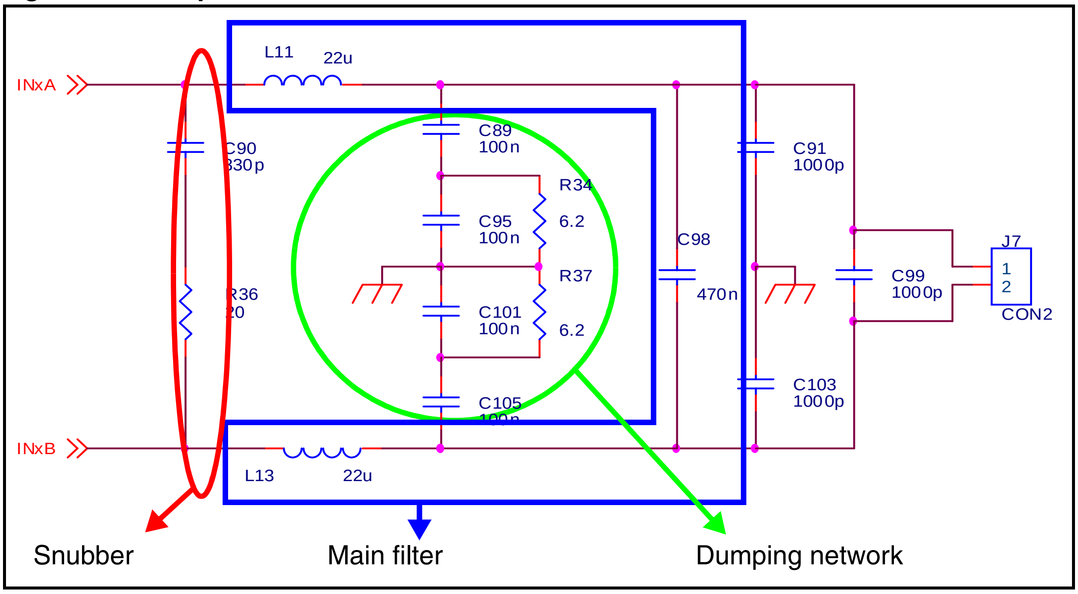
4.2 Decoupling capacitors

There are two different ways to use the decoupling capacitors:

- shared among the channels: the best practise layout route must be used for the board,
- one decoupling system per channel: it is mandatory that the decoupling capacitor must be as close as possible to the IC pins.

4.2.1 Output filter

Figure 117. Output filter

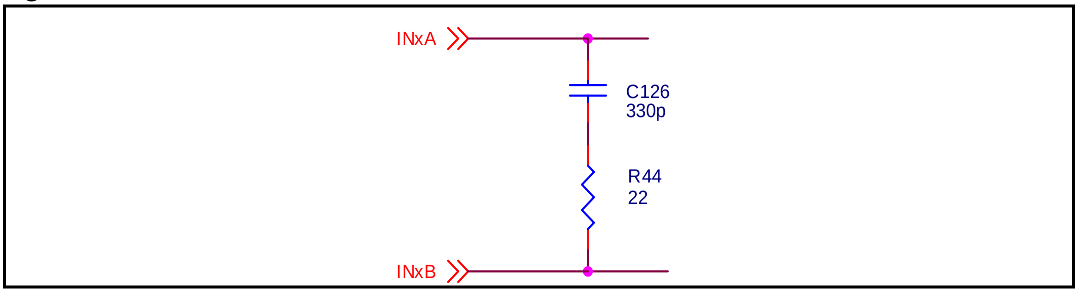


- The key function of a snubber network is to absorb energy from the reactance in the power circuit. The purpose of the snubber RC network is in order to avoid the high pulse energy (such as spikes) in the power circuit which can be dangerous to the system. When using the snubber network, the energy is be transferred to and from the snubber network, ensuring the system can work safely.

- The purpose of the main filter is to remove frequency higher than audible range of 20 KHz. The main filter uses the Butterworth formula to define the cut off frequency, which must be higher than 20 KHz, otherwise the frequency response is affected.
- The purpose of the dumping network is to avoid high frequency oscillation on the output circuit. After using the dumping network the THD can be improved, and can also avoid the inductive copper on the PCB route when the system is working in high frequency with PWM or PCM.

Snubber filter

Figure 118. Snubber filter

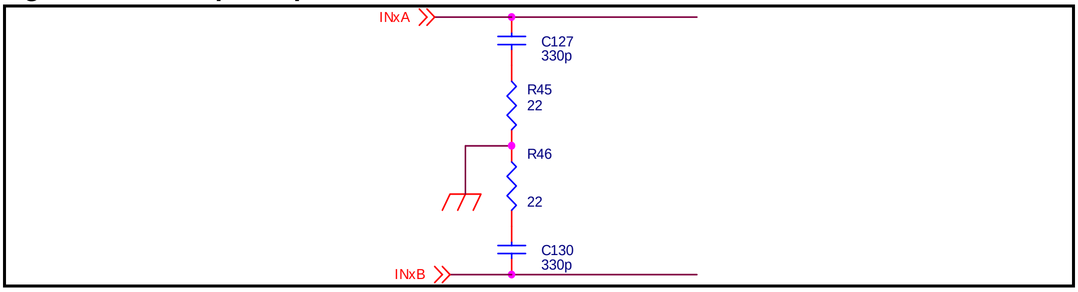


The snubber circuit must be optimized for the application. Starting values are 330 pF in series to 22 ohm. The power can be defined by the following formula which considers the power supply, frequency and capacitor value:

P=C*f*(2*V)^2

This power is dissipated in series resistance.

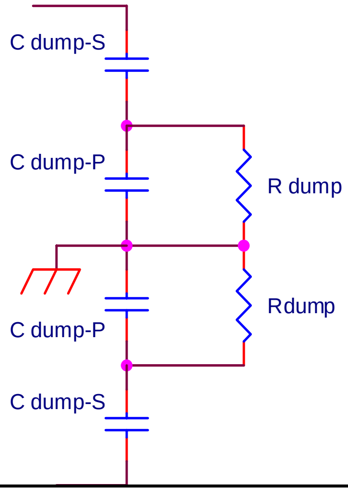
Figure 119. Dissipated power



Dumping network

The C-R-C is a dumping network. It is mainly intended for high inductive loads.

Figure 120. Dumping filter



Main filter

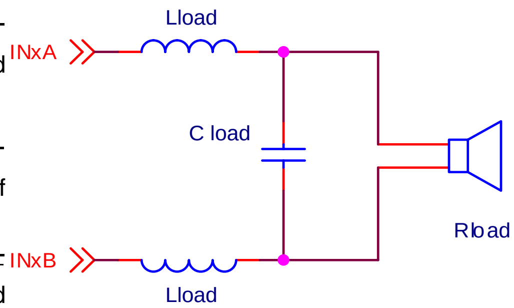
The main filter is an L and C based Butterworth filter. The cut-off frequency must be chosen between the upper limit of the audio band (20 KHz) and the carrier frequency (384 KHz).

Figure 121. Main filter

$$C_{load} = \frac{1}{2\sqrt{2} \times \Pi \times f_{cutoff} \times R_{load}}$$

$$L_{load} = \frac{R_{load}}{2 \times \Pi \times \sqrt{2} \times f_{cutoff}}$$

$$F_{cutoff} = \frac{1}{2 \times \Pi \times \sqrt{2 \times C_{load} \times L_{load}}}$$

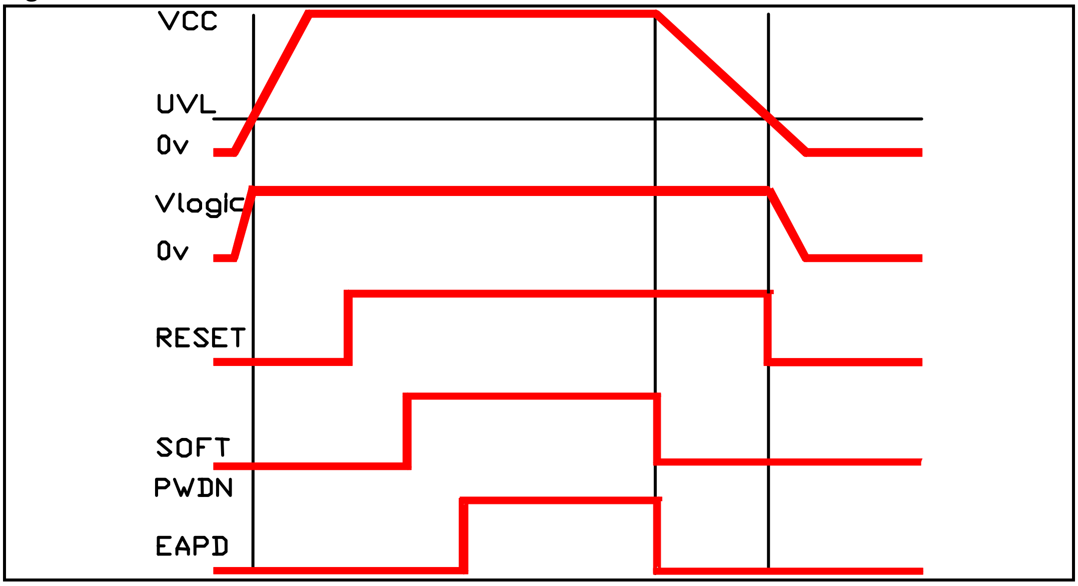


Recommended values

Rload	8 ohm	4 ohm
Lload	22 µH	10 µH
Cload	470 nF	1 µH
C dump-S	100 nF	220 nF
C dump-P	220 nF	220 nF
R dump	6.2	2.7

Recommended power up and power down sequence

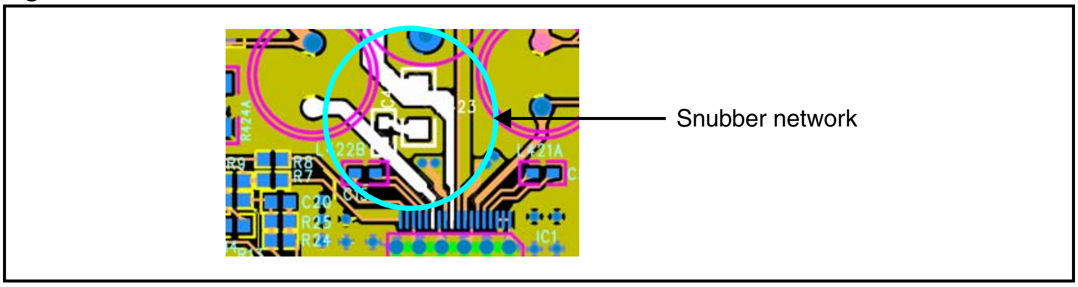
Figure 122. Main filter



4.3 Layout

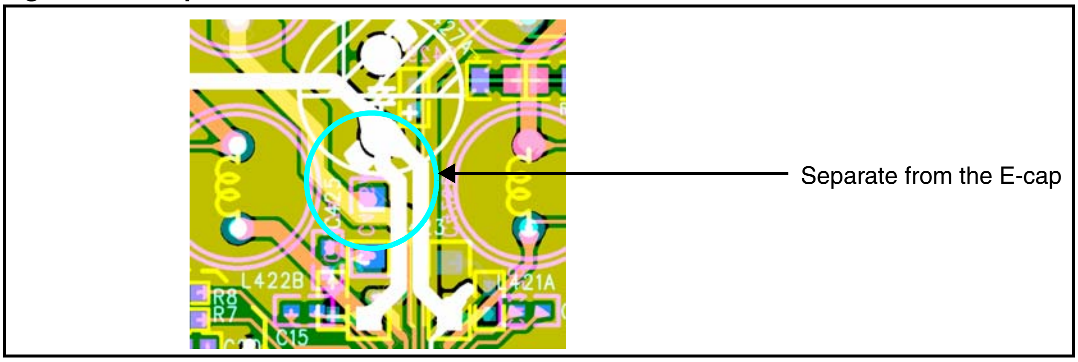
1. Solder snubber network as close as possible to the IC related pin.

Figure 123. Snubber network



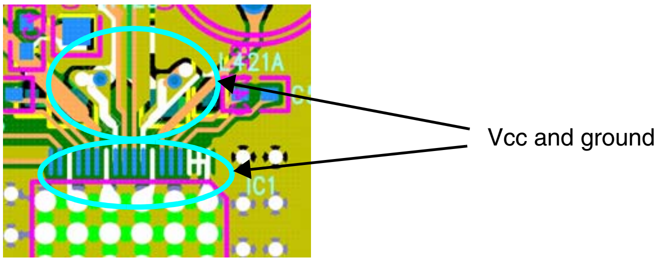
2. Use electrolytic capacitor first to separate the Vcc branches.

Figure 124. Separate the Vcc branches



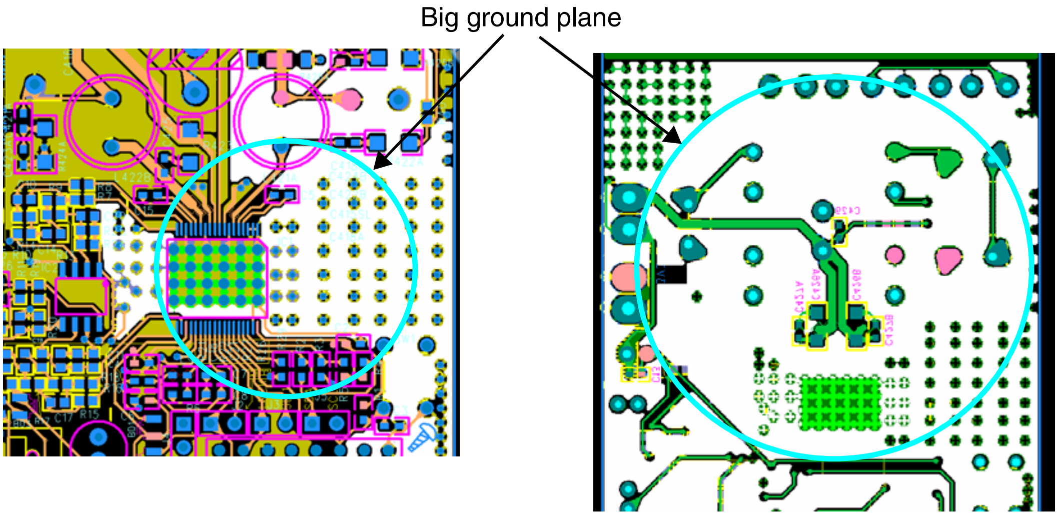
3. Minimize the path between Vcc pins and ground pin in order to avoid inductive paths.

Figure 125. Minimized paths between Vcc and GND



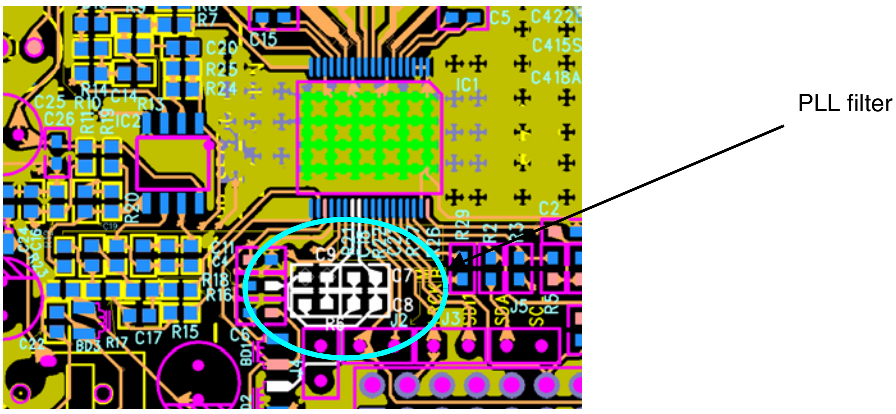
4. To dissipate the thermal with a ground plane.

Figure 126. Dissipate thermal



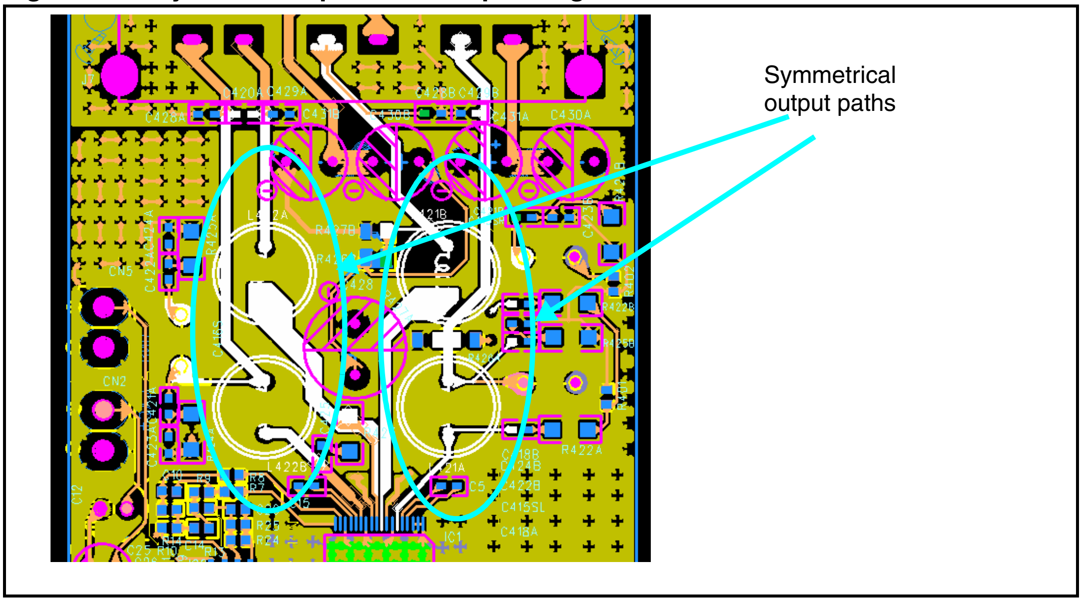
5. Solder PLL filter as close as possible to the FILT pin.

Figure 127. PLL filter



6. For differential application create symmetrical paths for the output stage.

Figure 128. Symmetrical paths for output stage



7. Separate the coil and the neighboring coil are vertical to avoid crosstalk.

Figure 129. Avoiding crosstalk

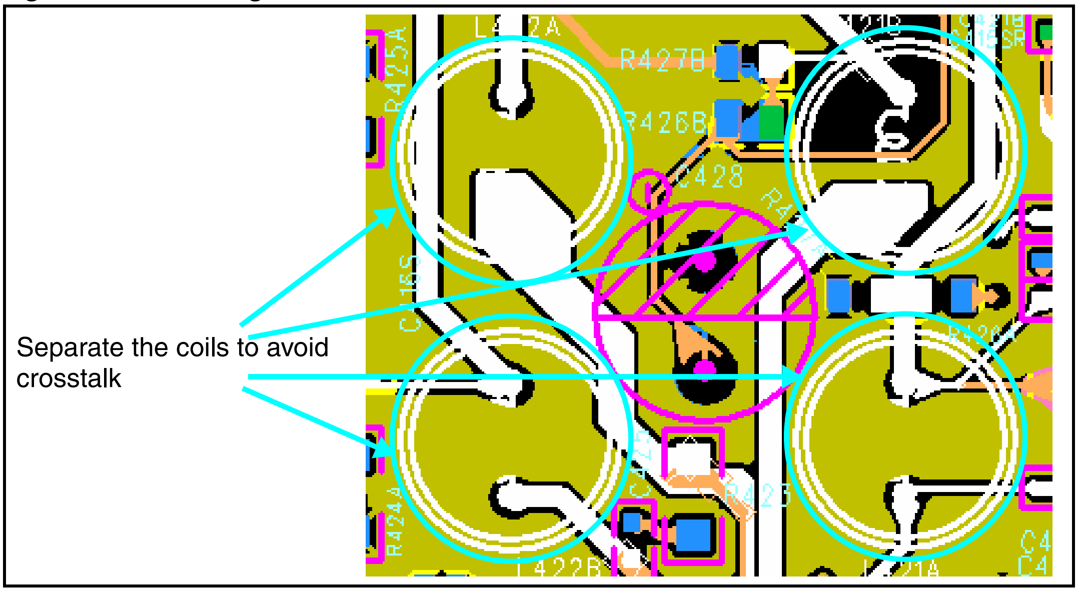
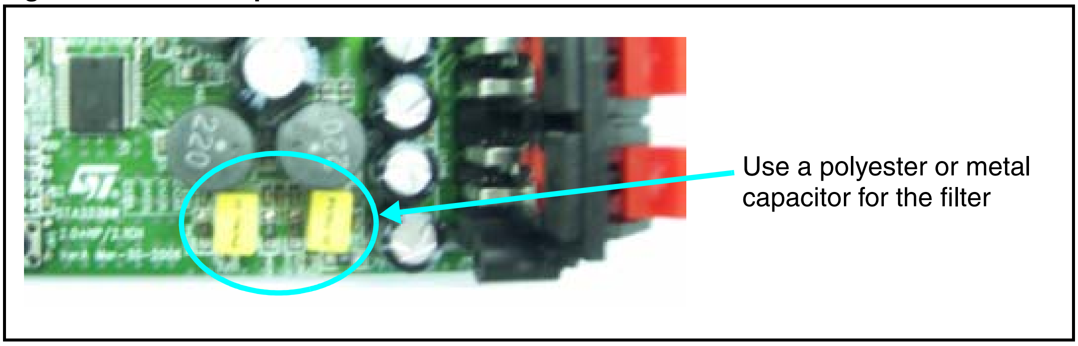
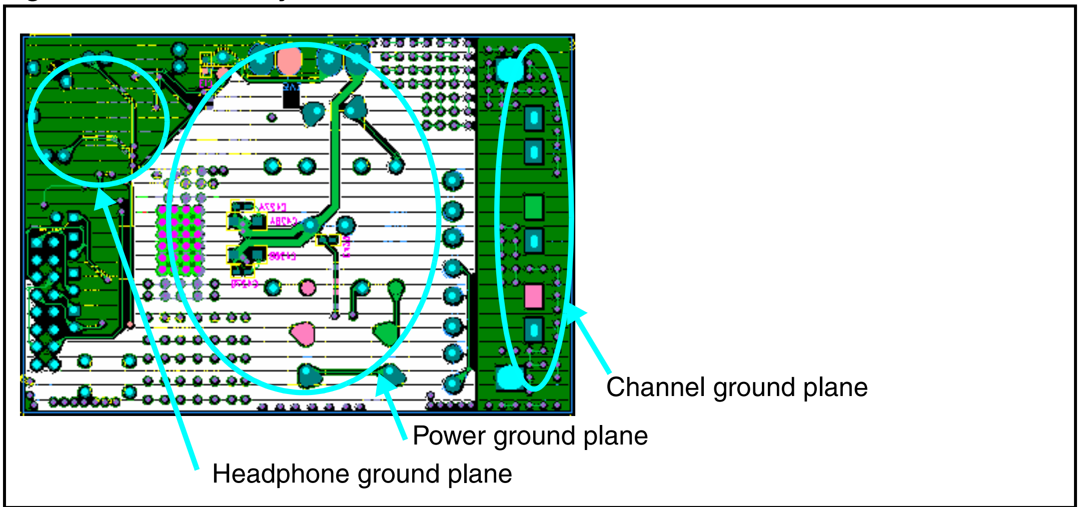


Figure 130. Filter capacitor



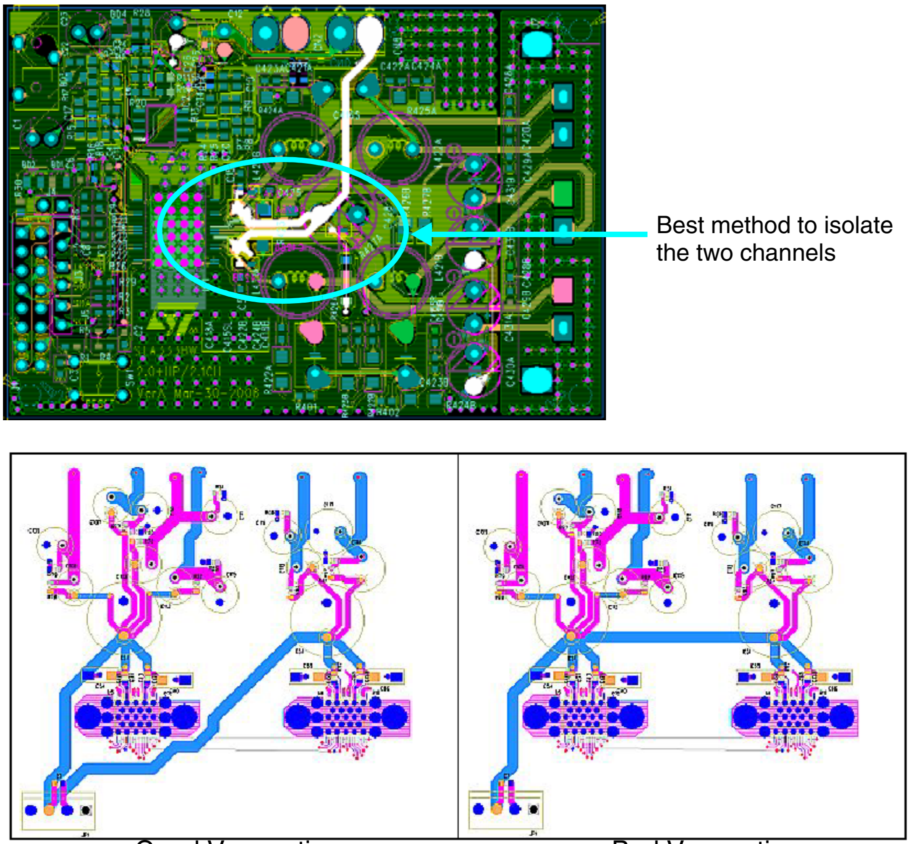
8. Consider ground layout. To avoid interference between ground power and small signal ground, it is necessary to divide the grounding as shown in *Figure 131*.

Figure 131. Ground layout



9. VCC routing.
   The best route for the Vcc supply is one which avoids interference between different signals (for example, part A is idle whilst part B is working at full load).

Figure 132. Vcc routing

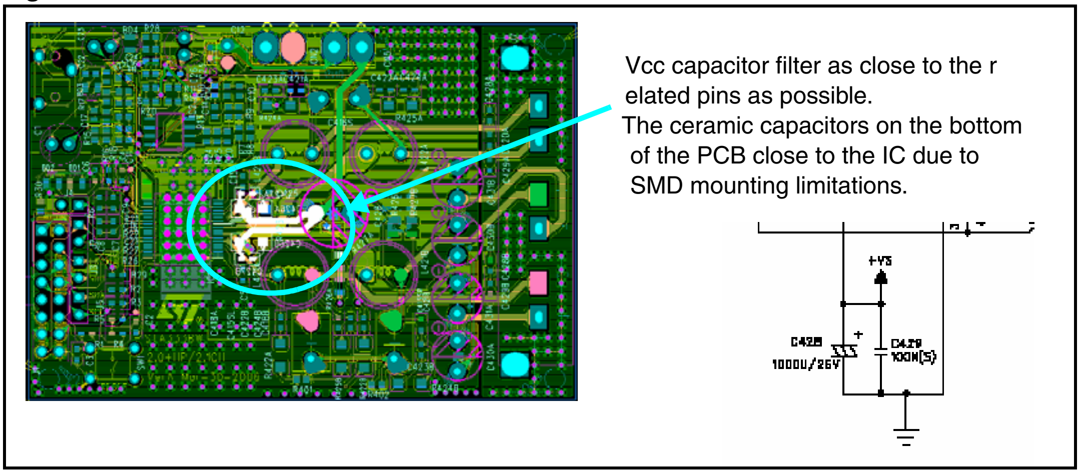


Good Vcc routing
amplifiers are isolated from each other

Bad Vcc routing
two amplifiers are daisy chained

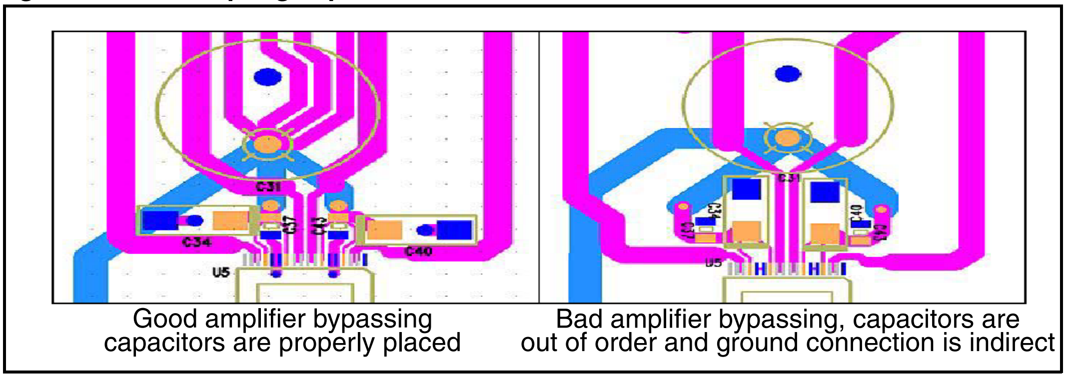
10. Vcc filter for high frequency.
    The PWM system works with a fast switch (frequency of 340 KHz approximately) which means the copper wire works as a coil. In order to avoid this, a ceramic capacitor should be used to balance resistance. It is a mandatory requirement that ceramic capacitors are placed as close as possible to the related pins. The distance between the capacitor and their respective pins should be less then 5 mm in order to minimize inductive coil effect generated by the copper wire.

Figure 133. Vcc filter



11. Decoupling capacitors.
    Solder decoupling capacitors as close as possible to their respective IC pin. This reduces the inductive coil effect.

Figure 134. Decoupling capacitors



12. Snubber filters for high frequency spike protection on the PWM.

Figure 135. Snubber filter placement

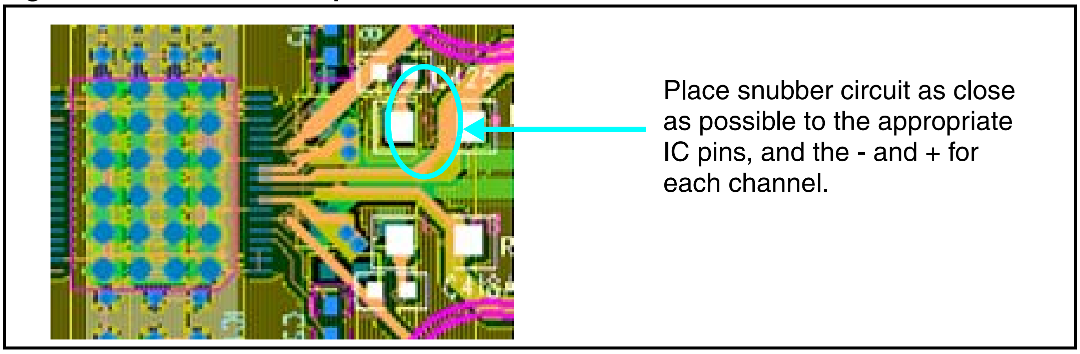
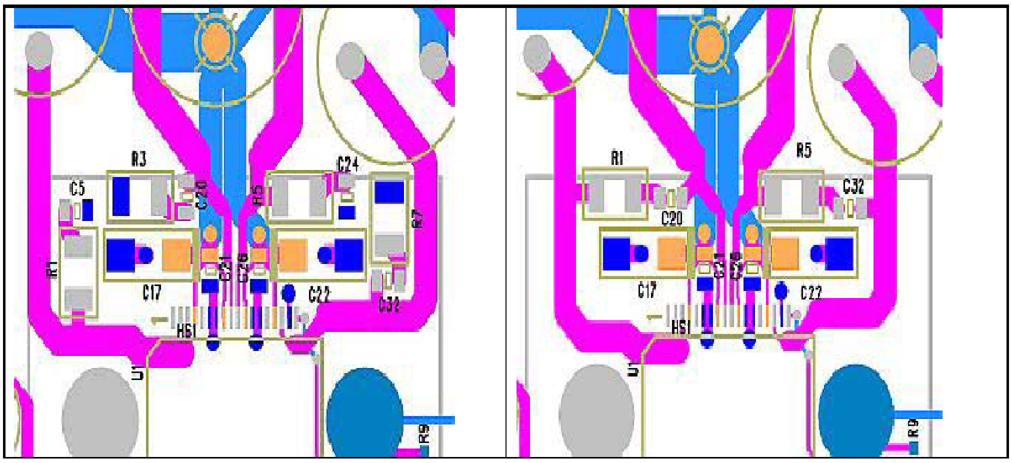


Figure 136. Examples of snubber filter placement

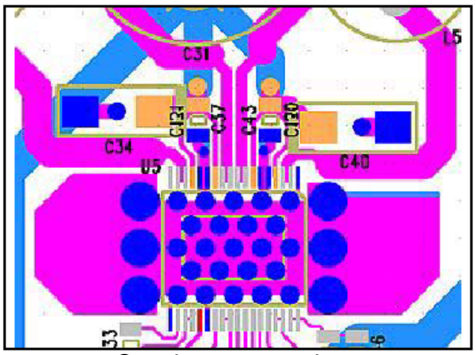


Good common mode snubber placement | Good differential snubber placement

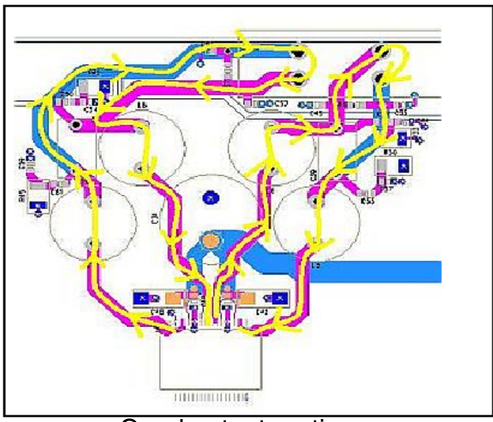
Caution: A spike can occur if there > 3 mm distance between the snubber network and the pins. This can cause damage to the IC. Therefore the distance must be kept below 3 mm.

13. Output routing

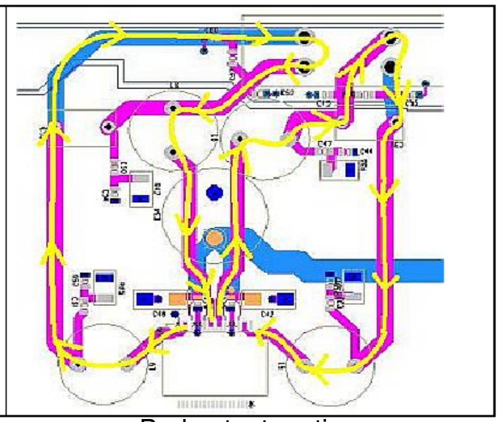
Figure 137. Output routing



Good output routing
traces grow wider as space allows



Good output routing
area between outputs is small



Bad output routing
area between outputs is large

14. Thermal layout bit big ground

Note: *The thermal pad must be connected to ground in order to properly set the IC references. It is necessary to allow the heat to flow freely to all sides of the board including top and bottom. For optimum heat dissipation it is recommended that the PCB has some solder via holes.*

Figure 138. Thermal layout (1 of 3 top and bottom layers)

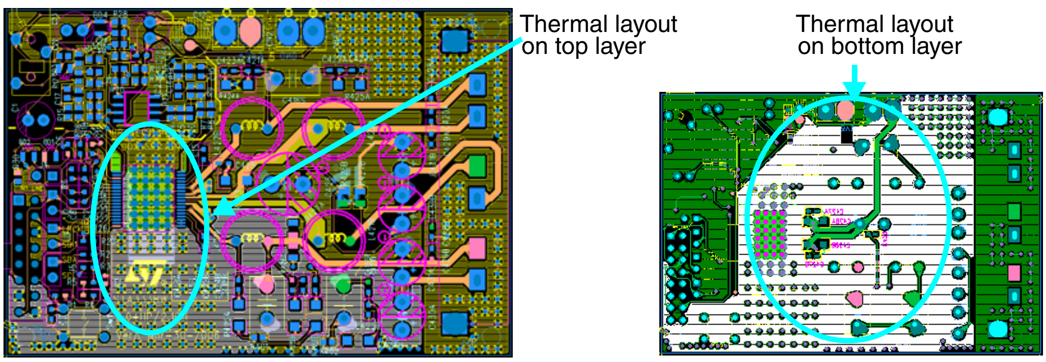
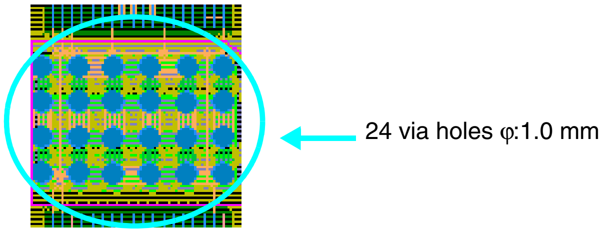
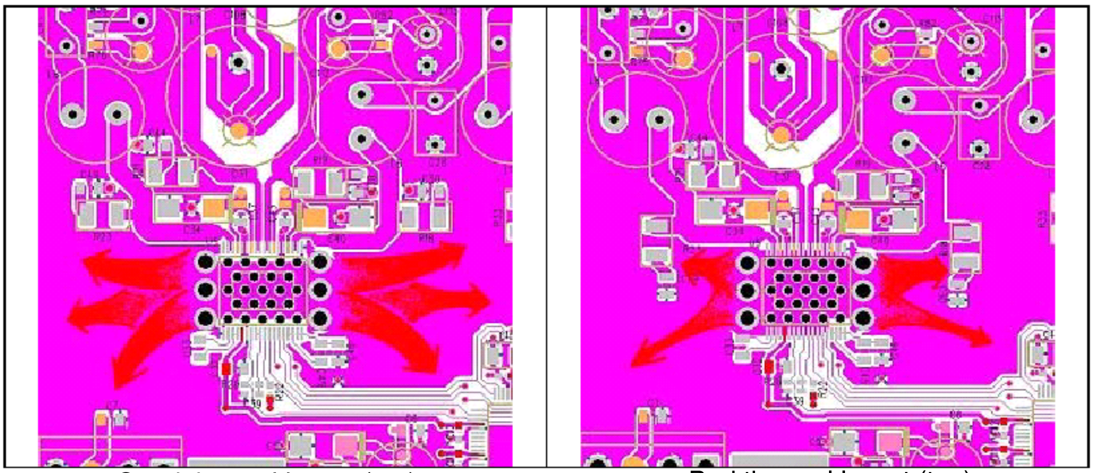


Figure 139. Thermal layout (2 of 3 thermal and soldering holes)



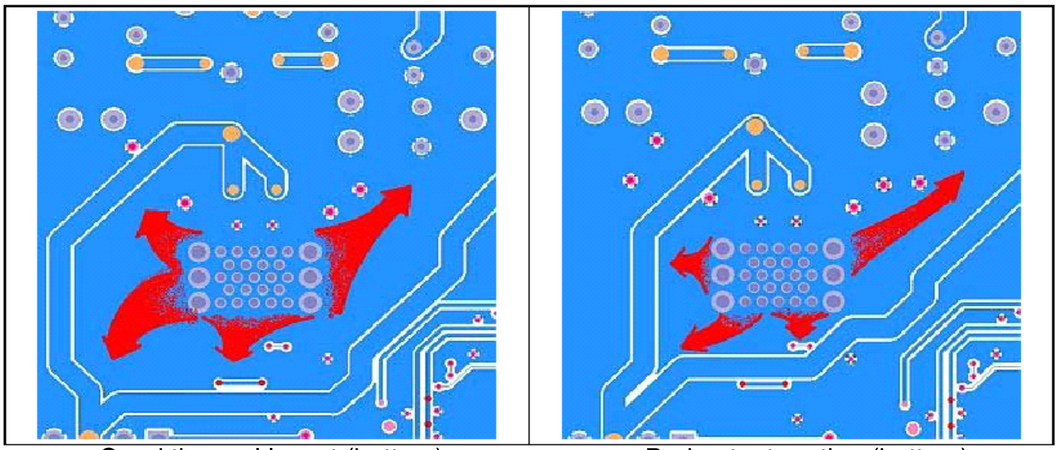
The thermal resistance junction at the bottom of the STA333BW to the ambient obtainable with a ground copper area of 4 x 4 cm and with 24 via holes (see *Figure 139*)

Figure 140. Thermal layout (3/3 heat flow direction)



Good thermal layout (top)
heat can flow freely to the sides

Bad thermal layout (top)
heat flow cut off by the snubbers



Good thermal layout (bottom)
plenty of copper area

Bad output routing (bottom)
little copper area on 3 sides

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
12-Dec-2006	1.0	Initial release.