AN3275
Application note

Improving the performance of smartcard interfaces using the ST8024L

Introduction

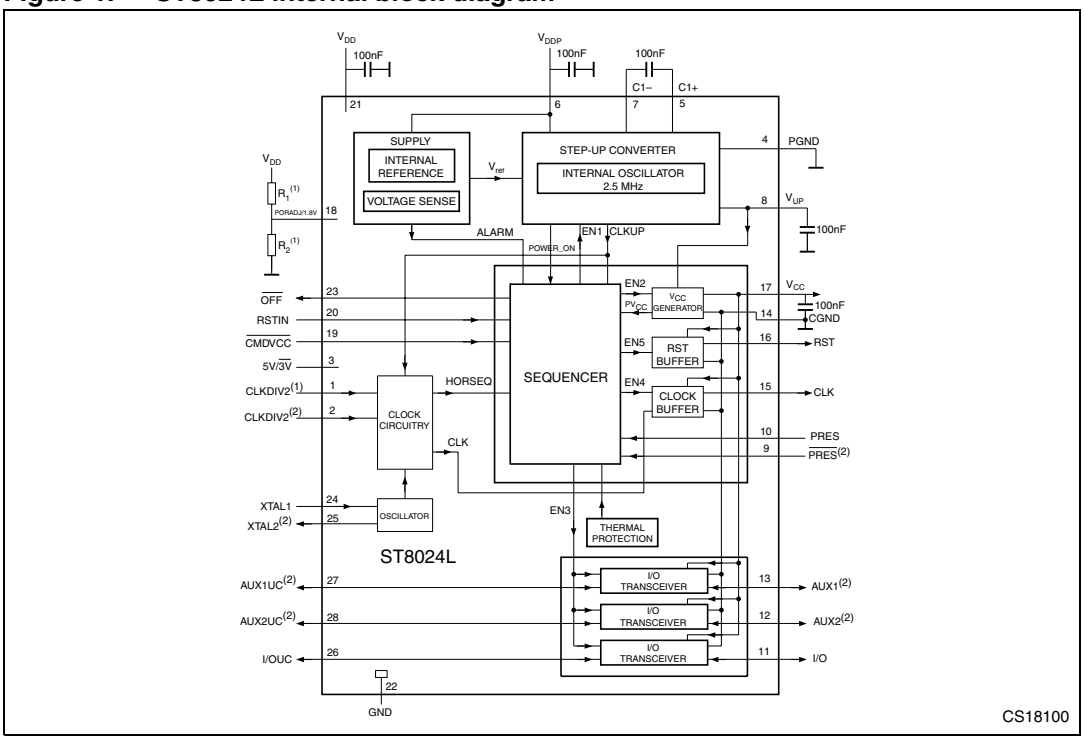
The ST8024L is a smartcard interface offered as a drop-in replacement for the ST8024 device. Enhancements and changes to the ST8024L device include:

- Improved performance by reducing the noise sensitivity in the charge pump
- Incorporated 1.8 V V_{CC} output
- Lower V_{TH} threshold voltage

This application note provides information and suggestions for the optimal use and performance of the ST8024L smartcard interface, including PCB layout, external component placement, and connections (see *ST8024L application hardware guidelines on page 18*). The implementation of all the blocks and procedures for card activation and deactivation (see *Figure 1*) of the smartcard are also explained.

The ST8024L is a smartcard interface designed to minimize microprocessor hardware and software complexity in all applications that require a smartcard (e.g., set-top box, electronic payment, pay TV, and identification cards). The electrical characteristics of the ST8024L are in accordance with New Digital Systems (NDS) and compliant with ISO7816-3, GSM11.11, and EMV 4.0. Two devices (ST8024LCDR and ST8024LCTR) in the ST8024L family have been certified by NDS.

Figure 1. ST8024L internal block diagram



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1 Activation/deactivation sequence

The core of the ST8024L is the sequencer (shown in *Figure 1 on page 1*) that must coordinate the Enable signals for the activation and deactivation sequence as well as check for possible fault conditions. The smart card is basically a microcontroller and needs to be activated/deactivated by a correct sequence as required by the ISO/IEC7816 standard. The ST8024L activation and deactivation sequences are shown in *Figure 2* and *Figure 3 on page 6*, respectively. Please refer to the ST8024L datasheet for details.

Figure 2 shows the activation sequence (the card is active) and $\overline{\text{CMDVcc}}$ taken from high to low. The activation sequence starts and the first block to be enabled is the step-up converter (V_{UP}), linked to En1 (see *Figure 1*), while the last enabled signal is RST that allows the card software to start.

Figure 3 shows the deactivation sequence (when $\overline{\text{CMDVcc}}$ goes high). The circuit executes an automatic deactivation sequence, finishing in the inactive state after t_{de} (deactivation time).

Figure 2. ST8024L activation sequence

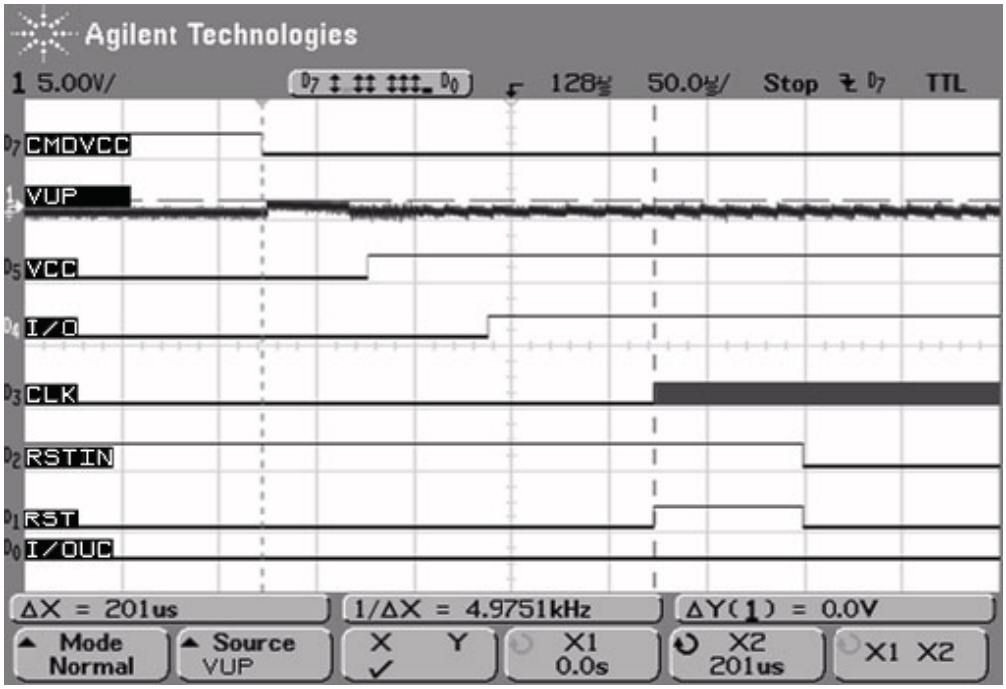


Figure 3. Deactivation sequence

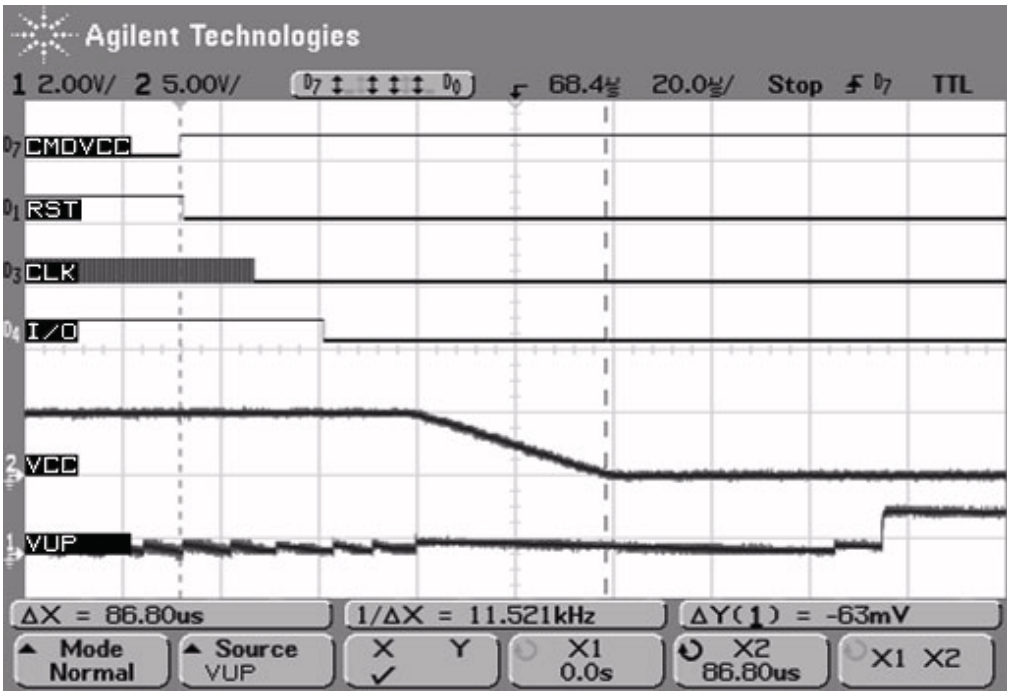
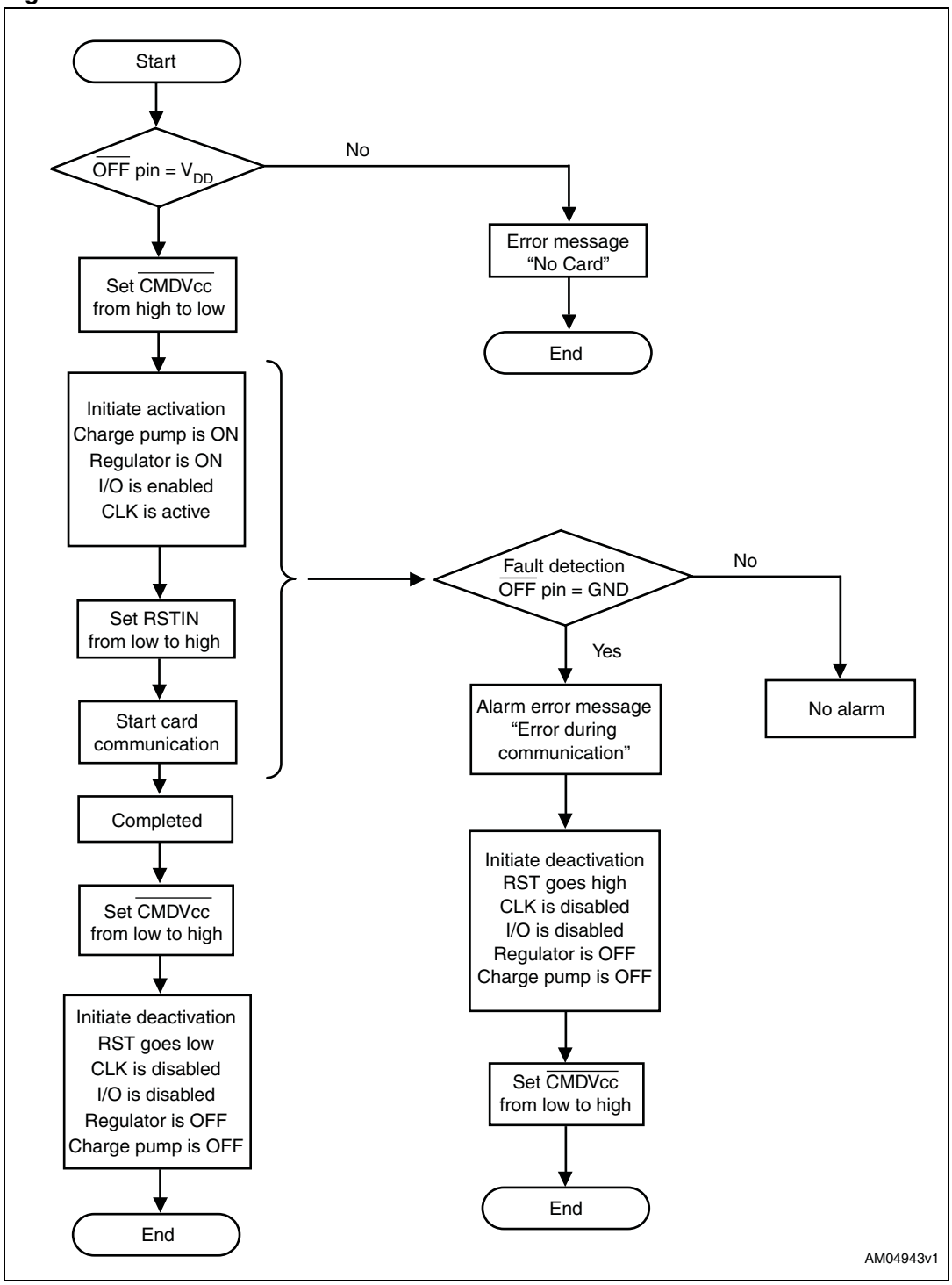


Figure 4. Card activation/deactivation flowchart



2 Card clock

The card clock signal (CLK) is present on the CLK pin when the ST8024L is activated. It is linked to the internal En4 signal (see *Figure 1 on page 1*) and its frequency is obtained according to the settings in *Table 1*.

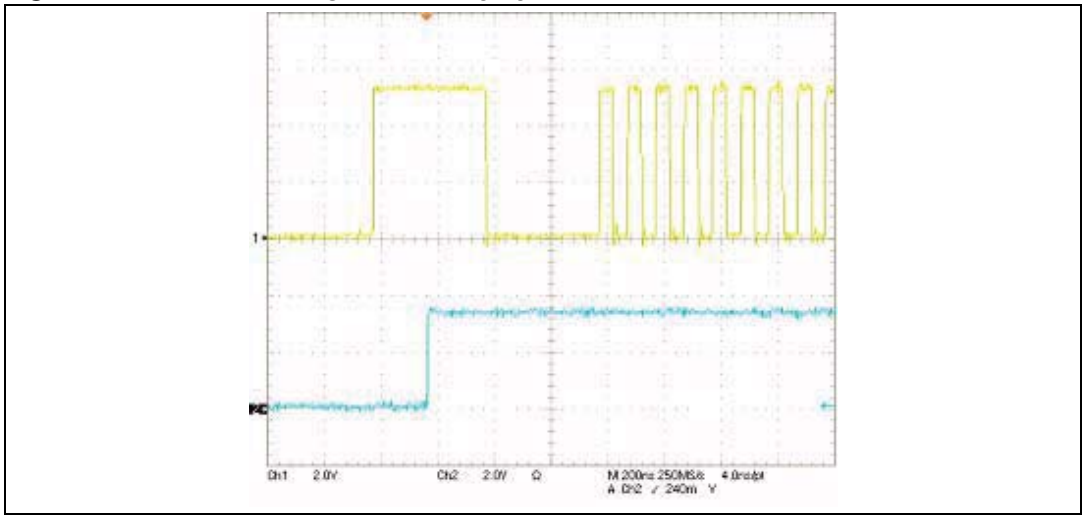
According to the ISO/IEC7816 specifications, the CLK duty cycle must be guaranteed between 45% and 55%, even when the status of CLKDIV1 or CLKDIV2 changes. *Figure 5* shows how the ST8024L ensures duty cycle accuracy by waiting for completion of a whole clock cycle before changing the frequency (CLKDIV1 change, rising edge of CH2). The output duty cycle is 50% ±5%, even if the clock division changes.

The card clock signal (CLK) can be established by connecting a crystal (“XTAL”) between the XTAL1 and XTAL2 pins, or by an external signal applied to the XTAL1 pin. In this case, the XTAL2 pin **must** be left floating. The external signal voltage level must be limited between GND and V_{DD} voltage.

Table 1. CLK division factor

CLKDIV1	CLKDIV2	f_{clk}
0	0	1/8 f_{XTAL}
0	1	1/4 f_{XTAL}
1	1	1/2 f_{XTAL}
1	0	f_{XTAL}

Figure 5. CLKDIV change clock duty cycle



CH1 = output CLK waveform

CH2 = CLKDIV1 pin

Conditions: V_{DD} = 3.3 V; V_{DDP} = 5 V; 5/3V = H

Mode: ACTIVE

f_{XTAL} = 10 MHz; CLKDIV2 = 0 V

3 Emergency deactivation/fault detection

ST8024L is equipped with a fault detection circuitry which monitors the following conditions (see *Figure 1 on page 1*):

- V_{DD} undervoltage
- Fault on card removal
- V_{CC} short-circuit
- V_{DDP} drop, and
- Overtemperature

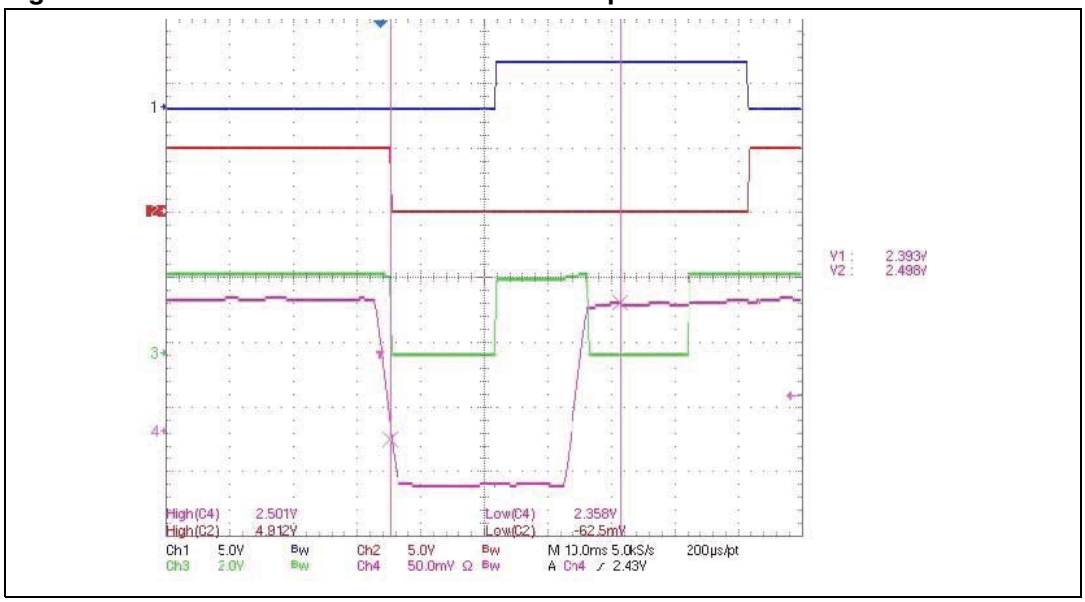
3.1 PORADJ V_{DD} undervoltage without external resistor bridge

The PORADJ pin can be used to provide early detection of power failure on V_{DD}. The ST8024L logic circuitry is supplied by V_{DD}. In order to avoid voltage spikes that could cause damage or malfunction of the device and/or card, a voltage supervisor block is embedded (see *Figure 1*). This block monitors V_{DD} and when it gets lower than V_{TH2} (falling threshold voltage on V_{DD}, 2.45 V, typ), the supervisor immediately starts the deactivation sequence and V_{CC} goes low.

As V_{DD} goes higher than $V_{TH2} + V_{HYS2}$, (V_{HYS2} is the hysteresis of threshold voltage, 100 mV, typ), after a certain amount of time ($t_w + t_{debounce}$, where t_w is the internal power-on reset pulse width, 8 ms typ, see *Figure 6 on page 10*), $\overline{\text{CMDVcc}}$ goes low. The activation sequence starts and V_{CC} goes high. The PORADJ pin can be left floating, but connecting it to GND to avoid capturing noise is recommended.

Note: See Fault on card removal on page 14 for $t_{debounce}$ feature details.

Figure 6. ST8024L automatic deactivation sequence



CH1 = $\overline{\text{CMDVcc}}$

CH2 = V_{CC}

CH3 = $\overline{\text{OFF}}$

CH4 = V_{DD}

Conditions: V_{DD} = 3.3 V; V_{DDP} = 5 V; 5/3V = H

Mode: ACTIVE

f_{XTAL} = 10 MHz; CLKDIV2 = 0 V

Note: Deactivation: $V_{TH2} \approx 2.393$ V.
Activation: As $V_{DD} \geq V_{TH2} + V_{HYS2}$ (≈2.498 V) and $\overline{\text{CMDVcc}}$ goes low, V_{CC} goes high.

3.2 PORADJ V_{DD} undervoltage with external divider

In this case, a resistor bridge is applied to the PORADJ pin (see *Figure 7*). $V_{TH(ext)\ rise}$ and $V_{TH(ext)\ fall}$ are the external rising threshold voltage and the external falling threshold voltage on V_{DD}, respectively. They are the voltages on pin PORADJ that switch the device on and off. By knowing these values and using the formula:

$$V_{PORADJ} = (R_2/R_1 + R_2) \times V_{DD}$$

it is possible to set R_1 and R_2 such that the device powers on and off at the values of V_{DD} desired by the user ($R_1 + R_2$ = 100 kΩ typ).

In particular, R_1 and R_2 have to be set so that, when V_{DD} is getting low, before turning the microcontroller off, the smartcard has to be switched off properly as well. The same is true for the microcontroller startup in that the smartcard has to be turned on after the microcontroller. *Figure 8* and *Figure 9 on page 13* show the $V_{TH(ext)\ rise}$ and $V_{TH(ext)\ fall}$ on the PORADJ pin (1.196 V and 1.155 V, respectively).

The $V_{TH(ext)fall}$ threshold of the ST8024L is slightly lower (80 mV typ.) than the ST8024 device. If for example, the microcontroller is shut down at 2.5 V, appropriate resistor values must be chosen to ensure proper deactivation of the ST8024L device.

Table 2 shows an example of the resistor values between the ST8024 and ST8024L devices if the microcontroller is shut down at 2.5 V.

Table 2. Resistor values for $V_{TH(ext)fall}$ trip point

	ST8024	ST8024L
R1	50 kΩ	55.5 kΩ
R2	50 kΩ	44.5 kΩ
$V_{TH(ext)fall}$	1.25 V	1.14 V

Table 3. V_{PORADJ} trip point

V_{DD}	V_{PORADJ}	
	ST8024	ST8024L
5.0	2.500	2.275
4.5	2.250	2.048
4.0	2.000	1.820
3.5	1.750	1.593
3.0	1.500	1.365
2.5	1.250	1.138
2.0	1.000	0.910

As long as V_{DD} gets the proper startup value (so that $V_{TH(ext)\ rise}$ = 1.196 V), $\overline{OFF}$ goes low for $t_w + t_{debounce}$ ($t_w \approx$16 ms, in this case). During this time, the device cannot be turned on by $\overline{CMDVcc}$. To turn the device on, $\overline{CMDVcc}$ must go low for at least approximately 16 ms (while $\overline{OFF}$ is high).

Figure 7. External resistor bridge applied to PORADJ

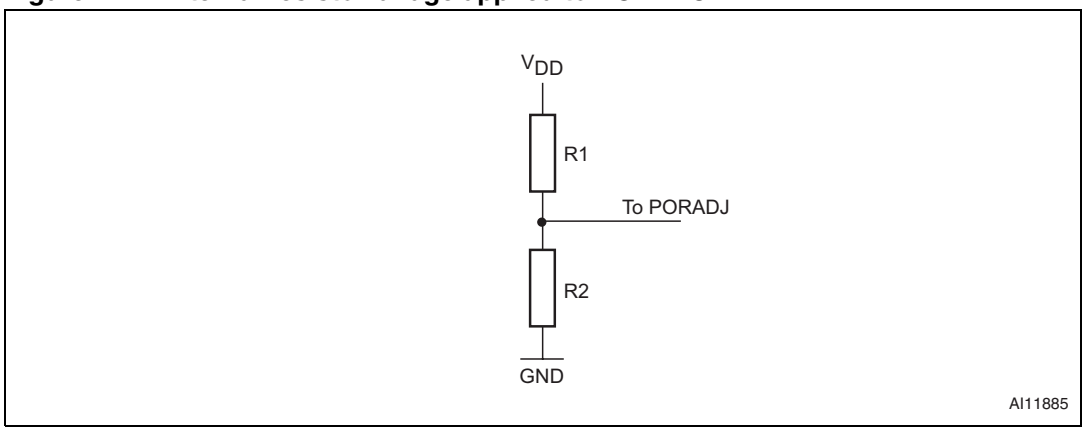
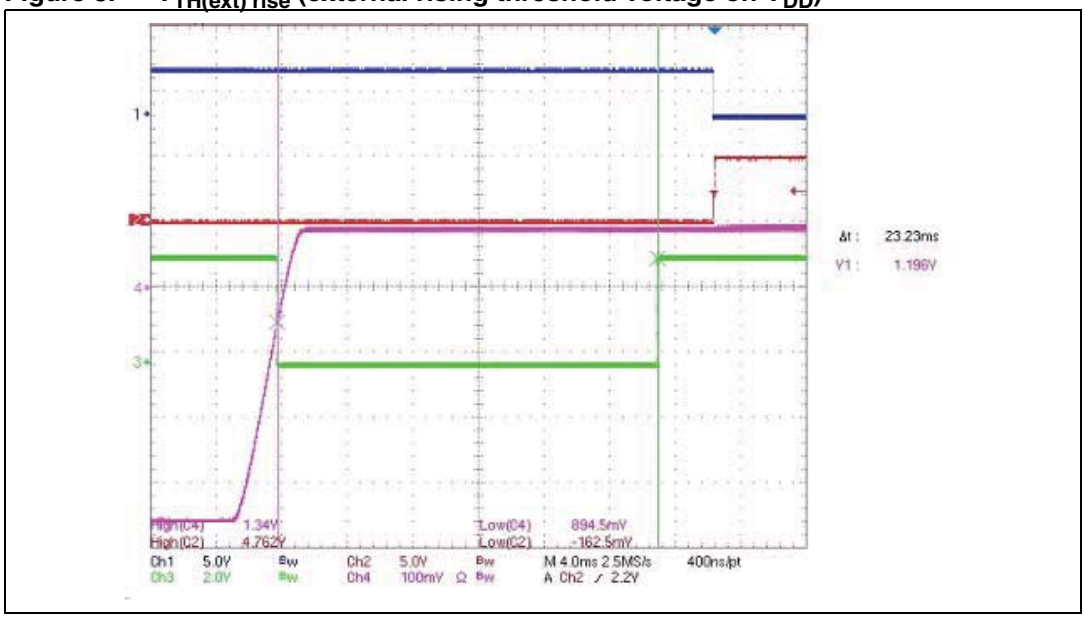


Figure 8. $V_{TH(ext)\ rise}$ (external rising threshold voltage on V_{DD})



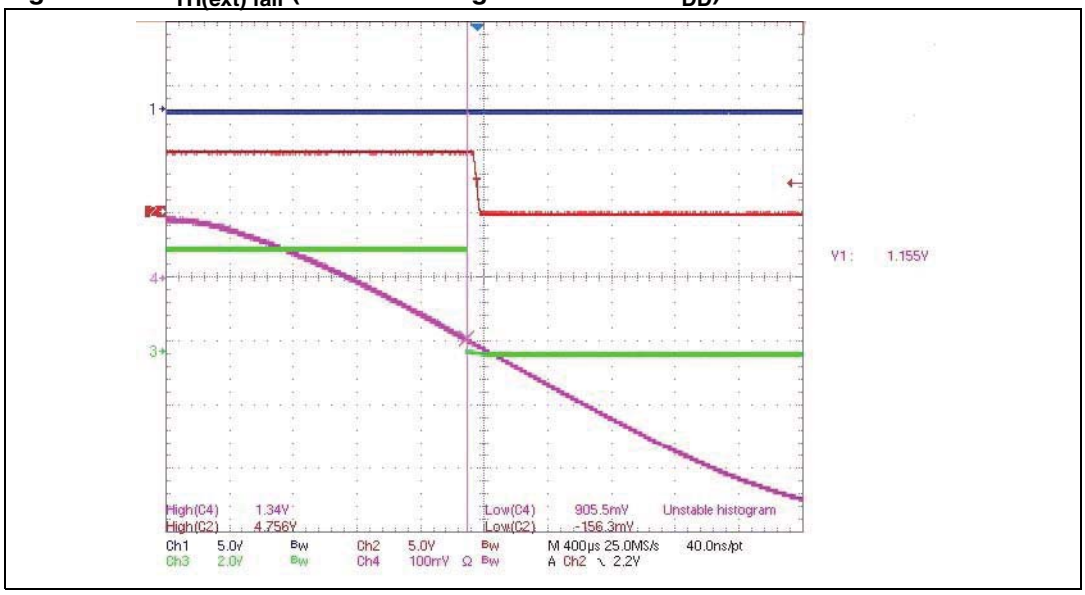
CH1 = $\overline{CMDVcc}$

CH2 = V_{CC}

CH3 = $\overline{OFF}$

CH4 = $V_{TH(ext)\ rise}$

Figure 9. $V_{TH(ext)\ fall}$ (external falling threshold on V_{DD})



CH1 = $\overline{CMDVcc}$

CH2 = V_{CC}

CH3 = $\overline{OFF}$

CH4 = $V_{TH(ext)\ fall}$

Note: When $V_{TH(ext)\ fall}$ = 1.155 V, the device starts switching off and V_{CC} goes low.

3.3 Fault on card removal

If the smartcard is pulled out from its socket ($\overline{PRES}$ goes high or PRES goes low), the deactivation sequence starts. The $\overline{OFF}$ pin goes low and the device switches off (see *Figure 10*). In order to avoid bouncing on the $\overline{PRES}$ (or PRES) signal at card insertion or extraction, as the card is inserted again, $\overline{OFF}$ goes high just after a period $t_{debounce}$ (≈8 ms). If $\overline{CMDVcc}$ goes low before this time, after card insertion, it will not initiate the activation. $\overline{CMDVcc}$ must wait for $t_{debounce}$ before toggling from high to low to initiate the activation. *Figure 11 on page 14* shows the start of the activation sequence after $t_{debounce}$ has elapsed.

Figure 10. Card extraction

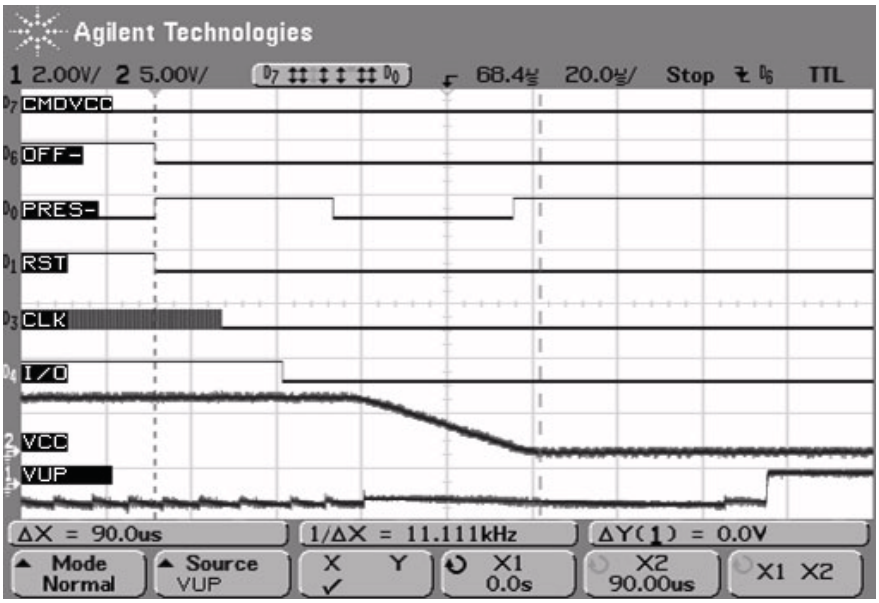
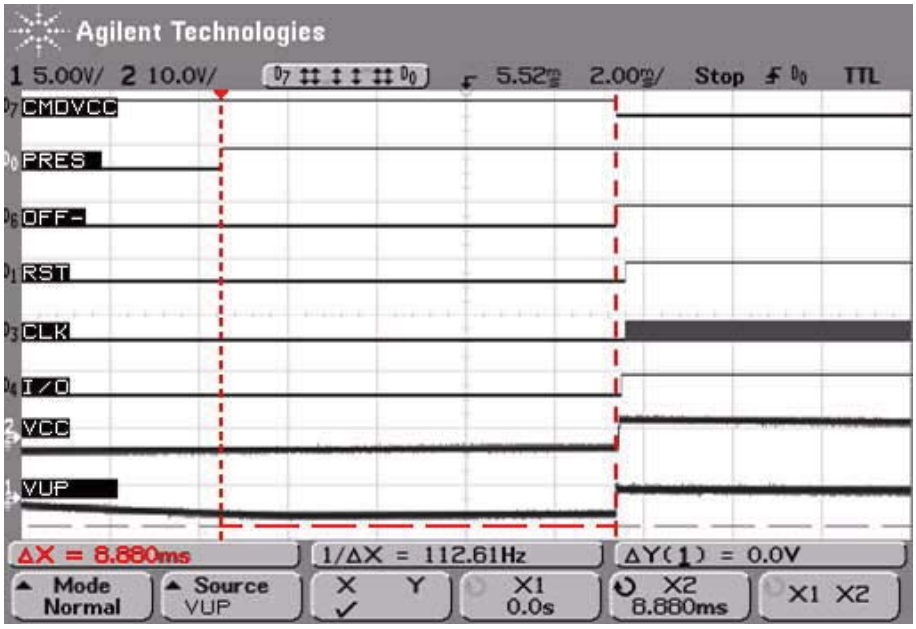


Figure 11. ST8024L activation sequence (after $t_{debounce}$)

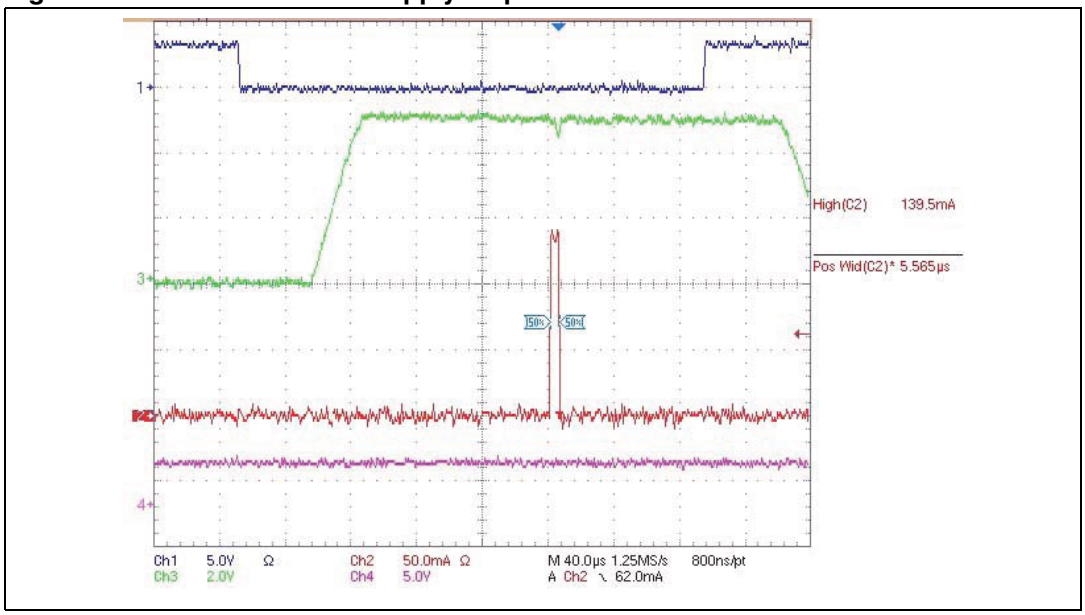


3.4 V_{CC} short-circuit fault protection

The ST8024L is able to supply the card with current pulses of about 140 mA for no longer than 5.5 µs, typical (see *Figure 12* and *Figure 13 on page 16*).

Short-circuit protection is an important interface feature that warns the sequencer block if the output current is higher than the short-circuit current limit (≈120 mA) for too long. This characteristic allows the device to supply the card with current pulses higher than the maximum allowed, if their duration is not too long. If the current pulses last for more than 5.5 µs, the deactivation sequence starts to protect the card. The $\overline{OFF}$ pin goes low so as to warn the microcontroller about the overcurrent fault. The sequence in *Figure 13 on page 16* shows how the current pulse becomes long enough to activate the short-circuit protection.

Figure 12. ST8024L current supply sequence



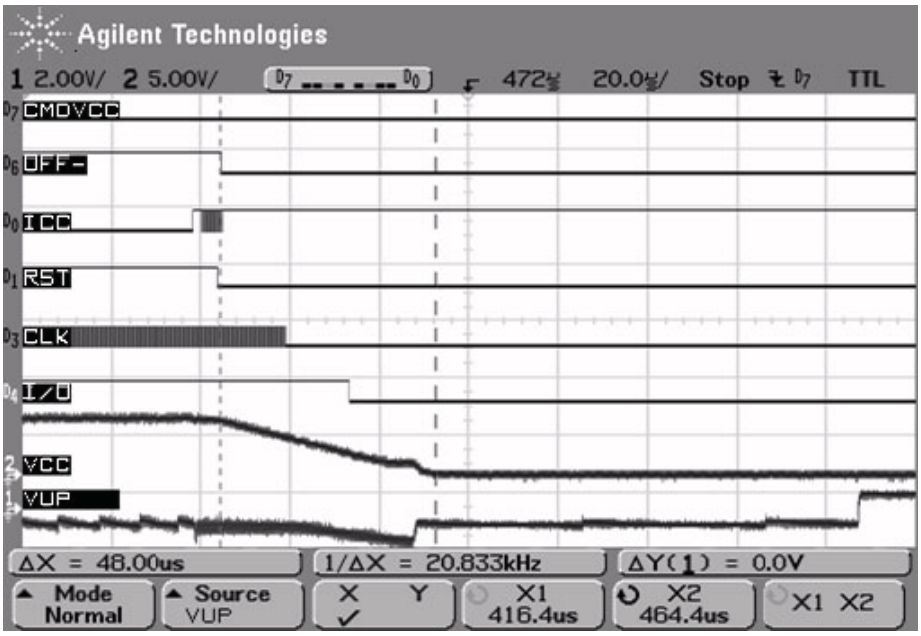
CH1 = $\overline{CMDVcc}$

CH2 = I_{SC} pulse

CH3 = V_{CC}

CH4 = $\overline{OFF}$

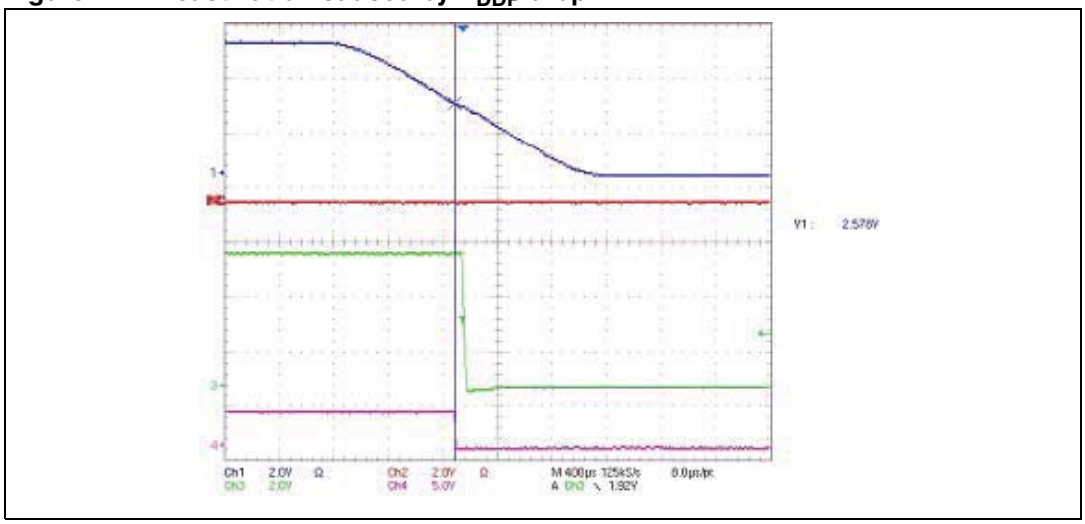
Figure 13. I_{SC} short-circuit protection



3.5 V_{DDP} drop

The voltage supervisor also monitors the drop in V_{DDP}. When V_{DDP} falls below the minimum threshold (see *Figure 14*), the deactivation sequence starts. The $\overline{OFF}$ pin goes low and V_{CC} goes off.

Figure 14. Deactivation caused by V_{DDP} drop



CH1 = V_{DDP}

CH2 = $\overline{CMDVcc}$

CH3 = V_{CC}

CH4 = $\overline{OFF}$

3.6 Overtemperature fault protection

Overtemperature protection is another important interface feature that warns the sequencer block of fault events. If the temperature is higher than the shutdown temperature (150 °C, typ), the deactivation sequence starts to protect the card. The $\overline{OFF}$ pin goes low so as to warn the microcontroller about the overtemperature fault.

4 ST8024L application hardware guidelines

This section contains some optimization guidelines concerning PCB layout as well as external component placement and connections. The referenced application board in *Figure 15* and *Figure 16 on page 19* has two layers and uses these guidelines to meet NDS application requirements (refer to *Figure 24 on page 29*).

The PCB layout provides completely separate supply and GND copper planes, which allow each plan to act as a shield for each group of noise-sensitive device pins. The PGND, and CGND and GND planes share a common point on the bottom layer of the PCB (see top, *Figure 16 on page 19*).

Figure 15. ST8024L application PCB top layer

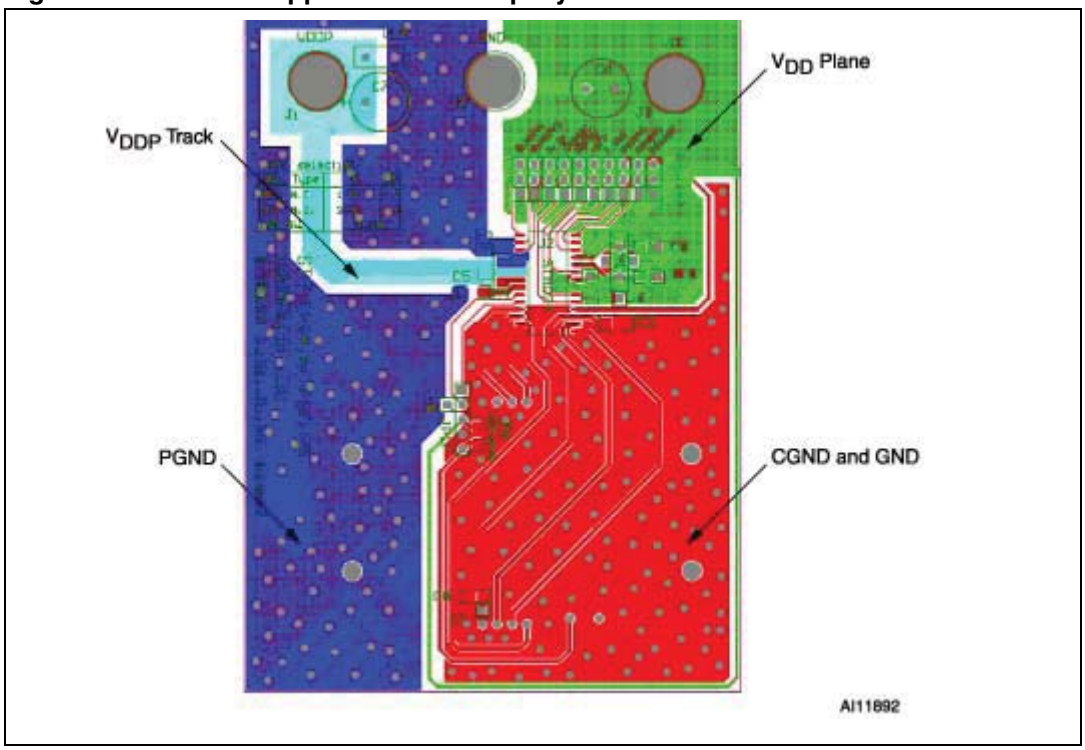
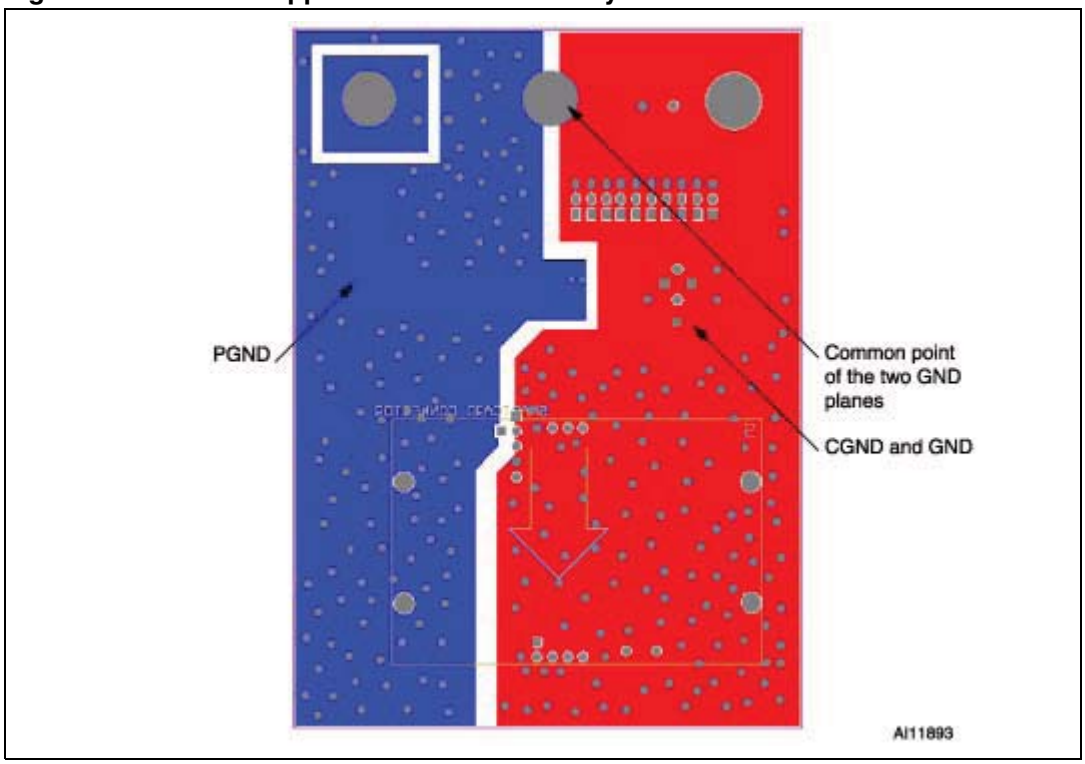


Figure 16. ST8024L application PCB bottom layer



4.1 Power supply optimization

The ST8024L devices support three smartcard V_{CC} voltages: 1.8 V, 3.0 V and 5.0 V. The ST8024LCDR and ST8024LCTR only support 3.0 V and 5.0 V V_{CC}. The V_{CC} selection is controlled by the supply voltage selector pin 5V/$\overline{3V}$ (pin 3) as shown in *Figure 1 on page 1*. If the 5V/$\overline{3V}$ pin is connected to V_{DD}, the V_{CC} voltage is 5 V and V_{CC} is 3 V if 5V/$\overline{3V}$ pin is connected to GND.

The ST8024LACDR and ST8024LTR support all 3 supply card voltages and are available in the SO-28 and TSSOP-20 packages. The V_{CC} selection is controlled by the supply voltage selector pins 5V/$\overline{3V}$ (pin 3) and 1.8V (pin 18). The 1.8 V signal has priority over the 5V/$\overline{3V}$ pin. When the 1.8V pin is connected to V_{DD}, the V_{CC} voltage is 1.8 V and it overrides any setting on the 5V/$\overline{3V}$ pin. When the 1.8V pin is connected to GND, the 5V/$\overline{3V}$ pin selects the 5 V or 3 V V_{CC}.

Table 4. V_{CC} selection settings

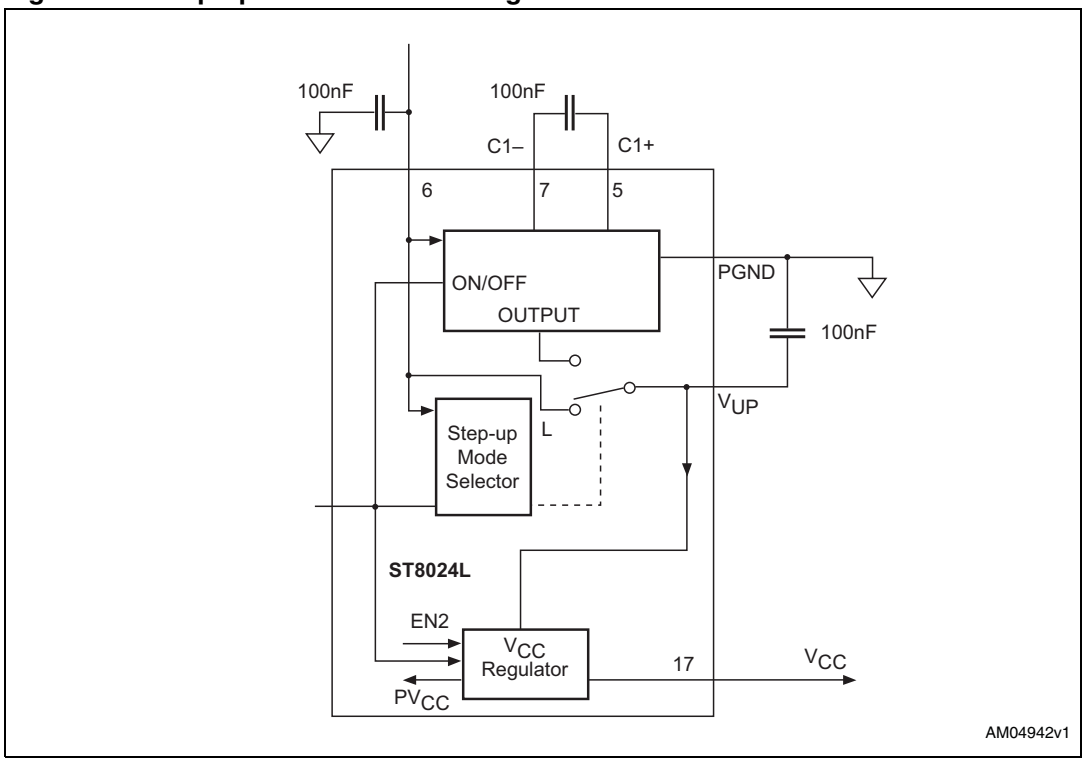
5V/$\overline{3V}$	1.8V pin	V_{CC} output
0	0	3 V
1	0	5 V
x	1	1.8 V

A step-up converter supplied by V_{DDP} is used for the V_{CC} voltage generation. It doubles the input voltage V_{DDP} or follows it, depending on the 5/$\overline{3V}$ and V_{DDP} values:

- 5/$\overline{3V}$ = H and V_{DDP} > 5.8 V; voltage follower
- 5/$\overline{3V}$ = H and V_{DDP} < 5.7 V; voltage doubler
- 5/$\overline{3V}$ = L and V_{DDP} > 4.1 V; voltage follower
- 5/$\overline{3V}$ = L and V_{DDP} < 4.0 V; voltage doubler

The C1– and C1+ pins are used for duplicating the supply voltage V_{DDP} by using the 100 nF pumping capacitor (C4). The charge pump output pin (V_{UP}) has to be connected to a 100 nF storage capacitor (C5) to stabilize the voltage.

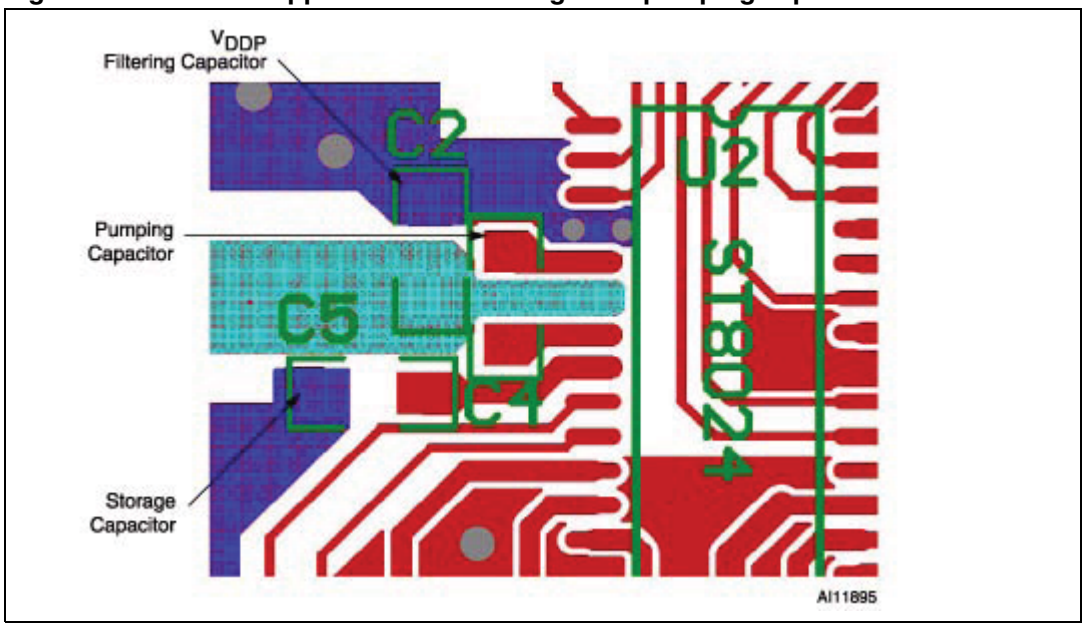
Figure 17. Step-up converter block diagram



A small amount of noise is introduced into the design because of the switching circuitry. In order to reduce it and improve the efficiency of the step-up converter, the capacitors must be connected as closely as possible to the pins (see *Figure 18*). An Equivalent Series Resistance (ESR) < 350 mΩ at 100 kHz is recommended.

The evaluation board is equipped with MURATA GRM31M7U1H104JA01B capacitors. However, other capacitors with an ESR of up to 350 mΩ at 100 kHz are sufficient to work within the specifications.

Figure 18. ST8024L application PCB storage and pumping capacitors

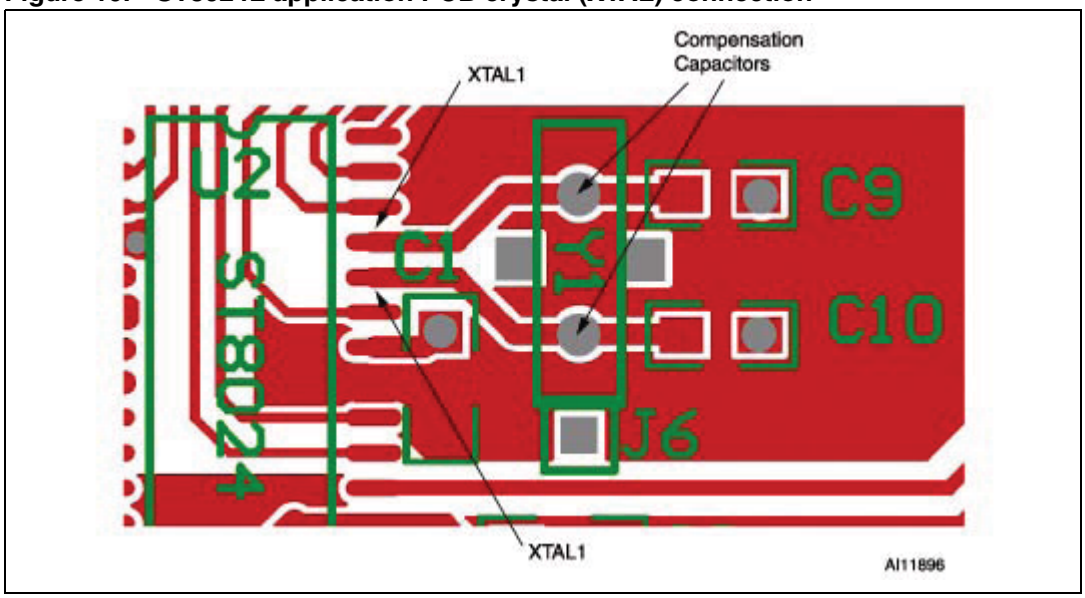


4.2 Clock section optimization

Recommendations for the PCB design clock area include:

- The XTAL should be connected as closely as possible to the XTAL pins to reduce signal reflections, especially for high frequency applications (see *Figure 19*).
- Two compensation capacitors (C9 and C10), each 15 pF (typ) can improve the oscillator startup performance. Even without these additional capacitors the CLK duty cycle is guaranteed between 45% and 55% (according to the NDS specifications), with frequencies up to 26 MHz.

Figure 19. ST8024L application PCB crystal (XTAL) connection



4.3 Smartcard connections

In typical applications, a 100 nF filter capacitor (C3) is connected to the V_{CC} output towards GND/CGND, near the ST8024L pins. A second 100 nF capacitor (C8) is connected between the card socket pins C1 (V_{CC}) and C5 (CGND), near the card slot (see *Figure 20*). In order to reduce noise and avoid coupling effects, the wire length between the ST8024L and card should be as short as possible.

Another recommendation is to keep the CLK track far away from the other signal tracks to limit coupling with the transceiver lines. Further decoupling is gained if the clock track is shielded by a GND/CGND plane or track on the PCB.

Keeping the PGND and GND/CGND planes as large as possible improves power supply noise rejection. With this in mind, the board design should connect these planes with a large number of vias between the top and bottom board layers (3-4 vias per cm^2).

The ST8024L has been enhanced to reduce the noise sensitivity in the charge pump and to improve the performance of the device. The V_{CC} spikes are much lower than 350 mV_{PP} even when a pulsed load of up to 80 mA is applied with V_{CC} = 5 V, up to 65 mA with V_{CC} = 3 V and up to 50 mA with V_{CC} = 1.8 V. *Figure 21 on page 26* shows a typical V_{CC} output waveform where an 80 mA pulsed load is applied and the measured ripple is lower than 95 mV. With a 65 mA pulsed load applied, the measured ripple is less than 65 mV, and when a 50mA pulsed load is applied, the measured ripple is less than 55 mV.

Figure 20. ST8024L application PCB smartcard connections

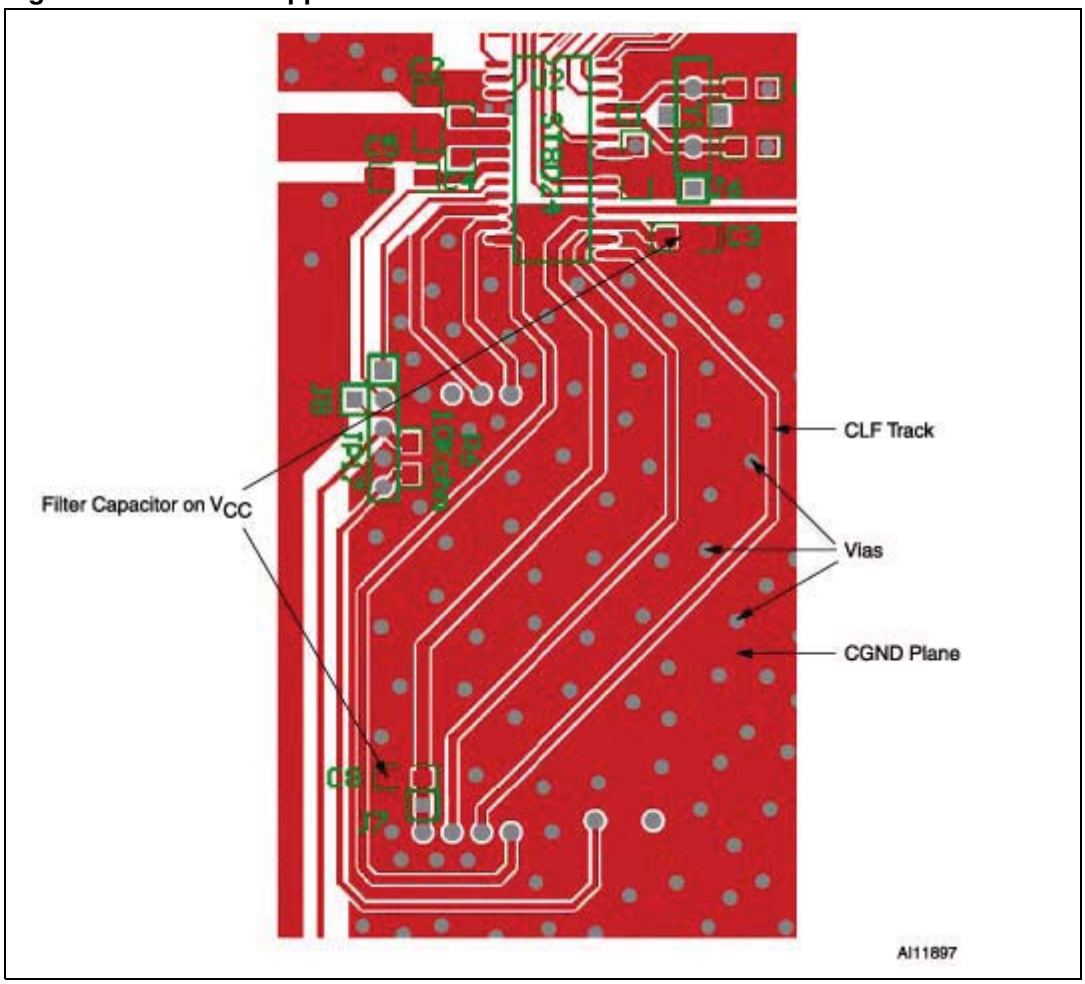
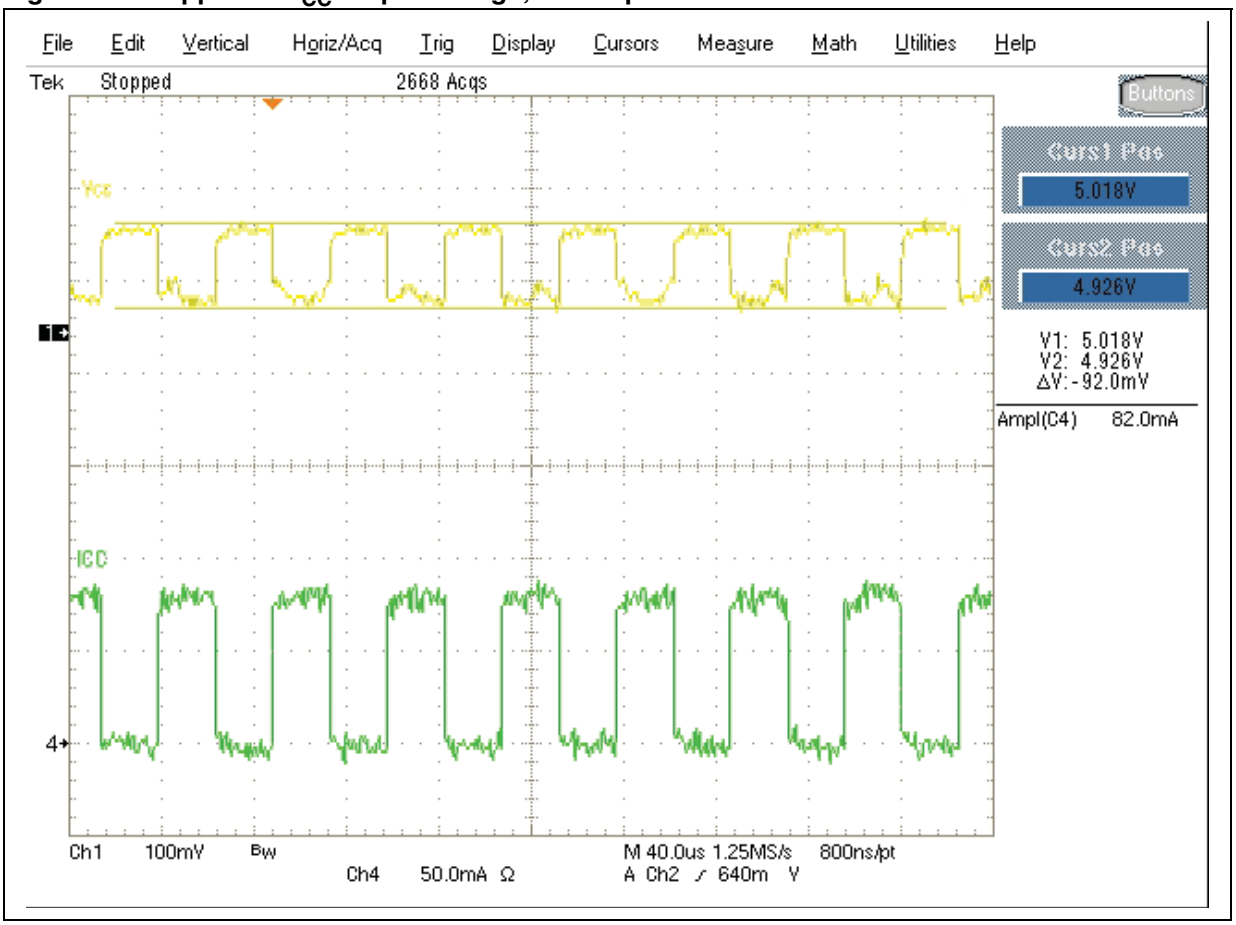


Figure 21. Ripple on V_{CC} output voltage, 80 mA pulsed load



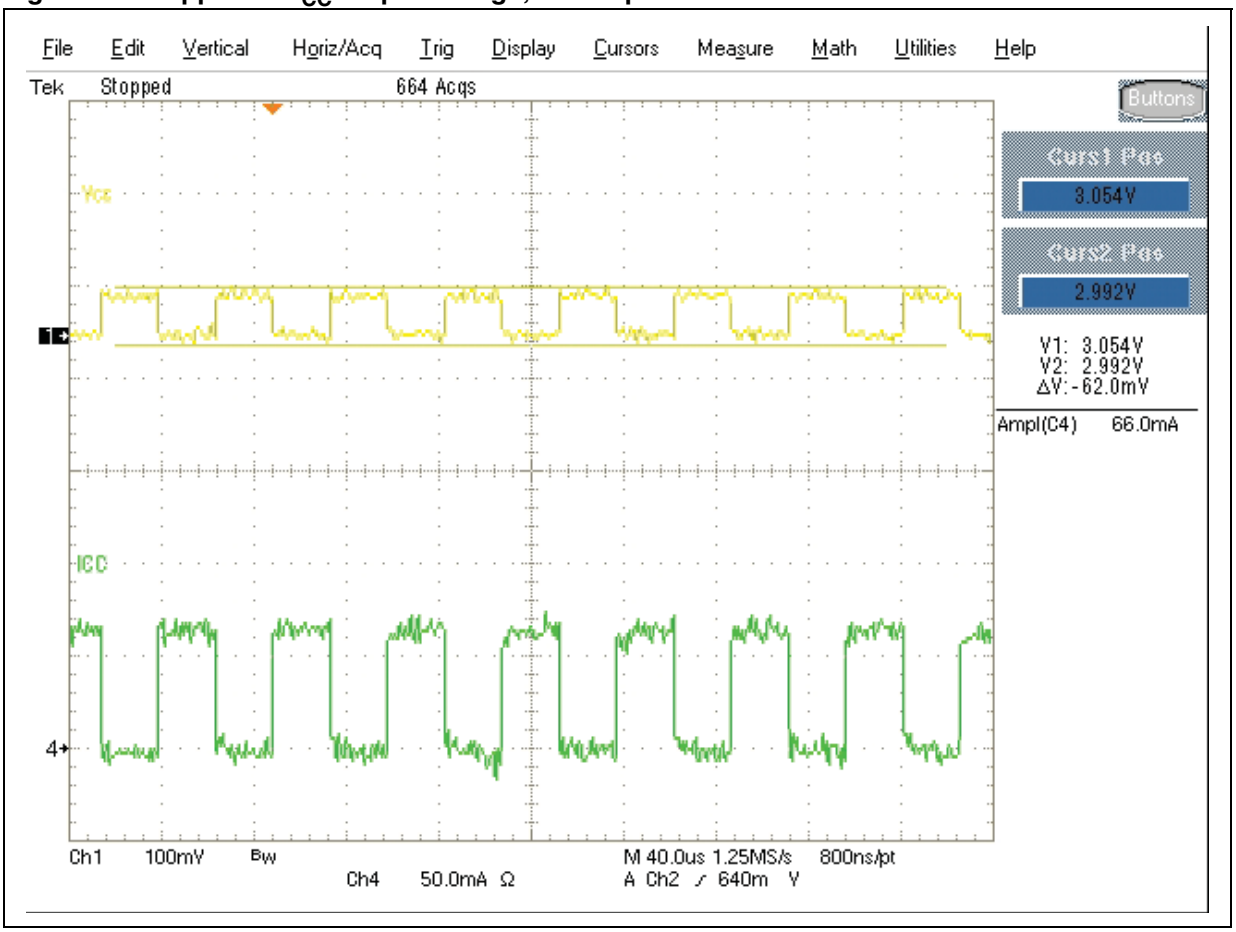
V_{DD} = 3.3 V

V_{DDP} = 5.5 V

CH1 = Ripple on V_{CC} output voltage

CH2 = 80 mA pulsed current I_{CC}

Figure 22. Ripple on V_{CC} output voltage, 65 mA pulsed load



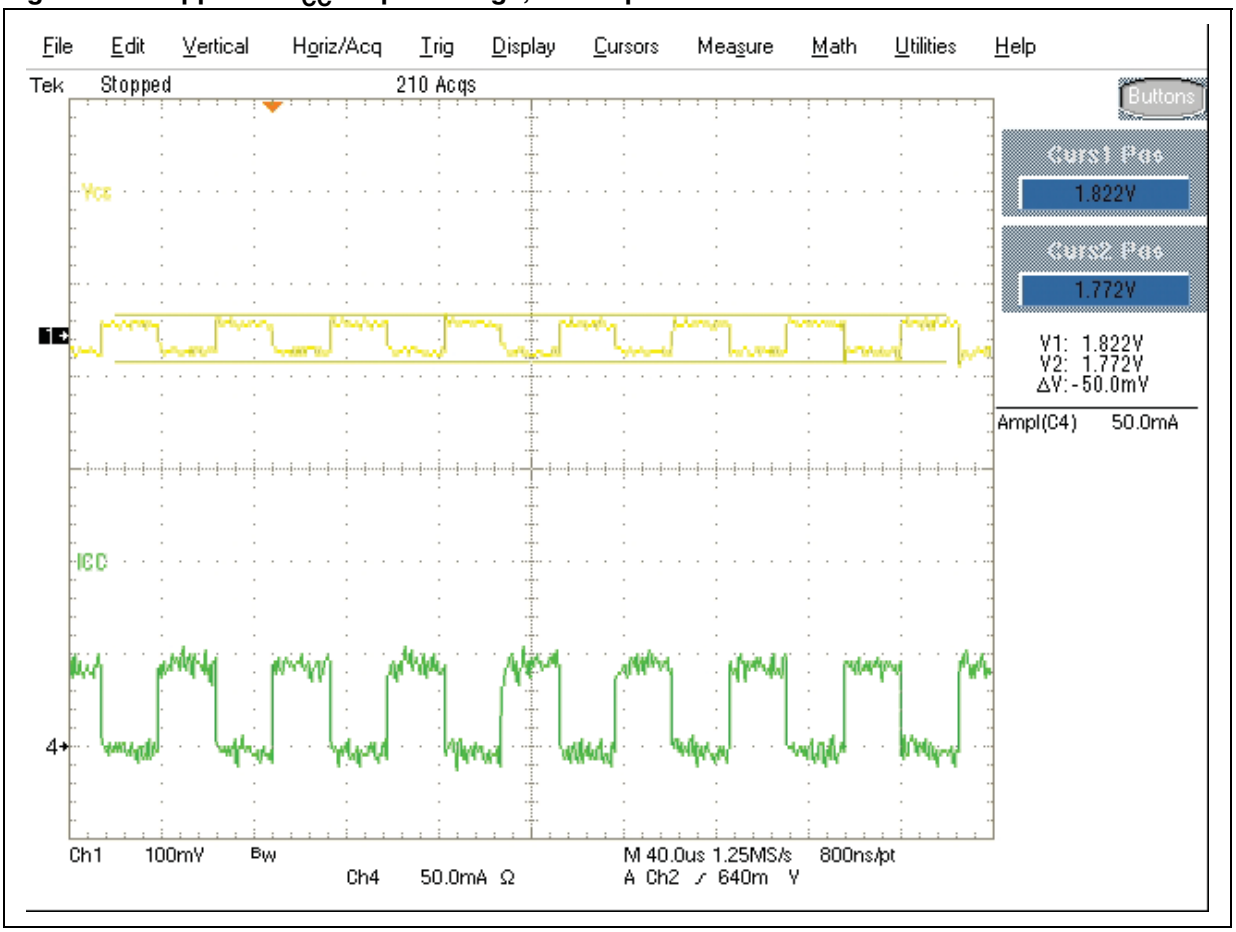
V_{DD} = 3.3 V

V_{DDP} = 5.5 V

CH1 = Ripple on V_{CC} output voltage

CH2 = 65 mA pulsed current I_{CC}

Figure 23. Ripple on V_{CC} output voltage, 50 mA pulsed load



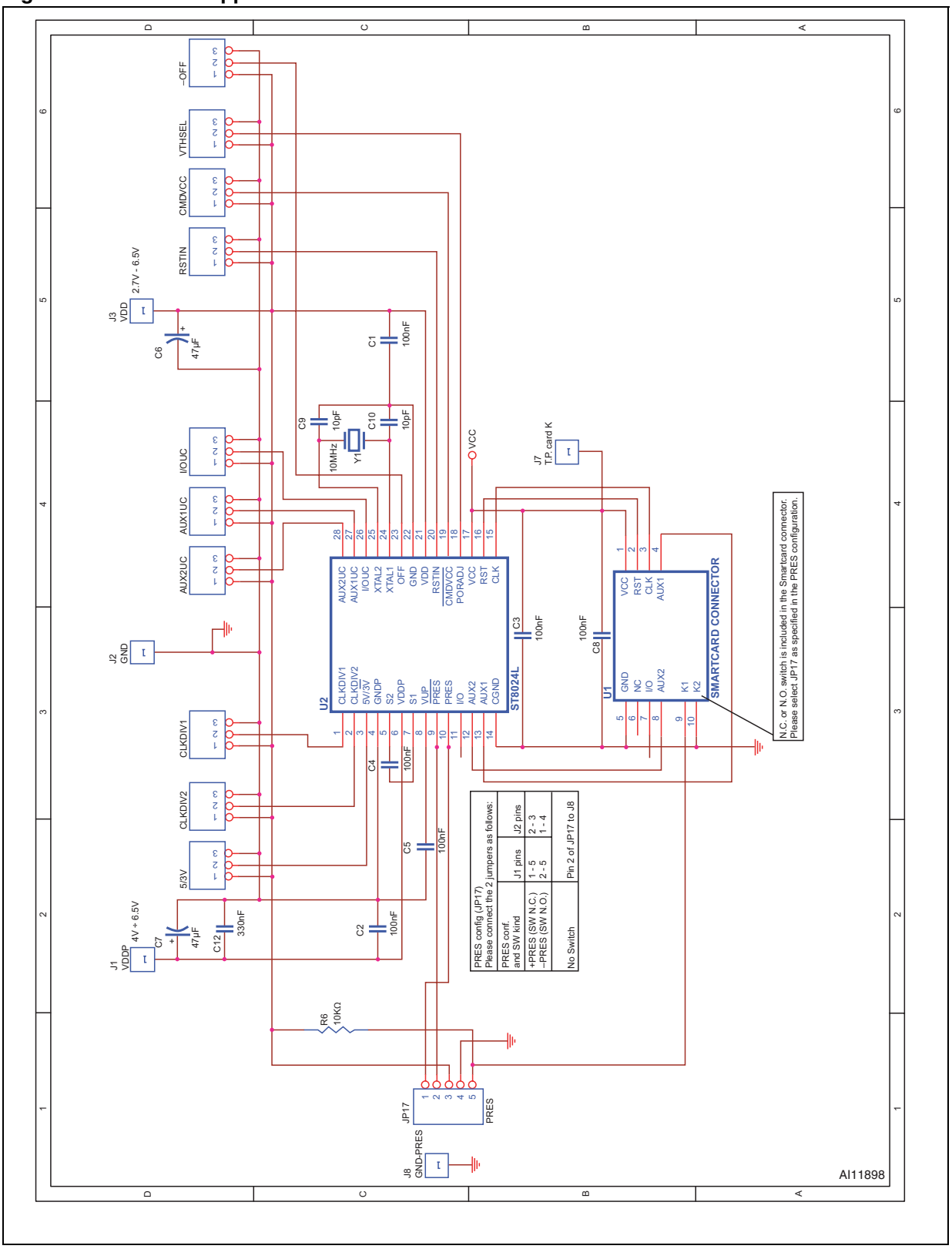
V_{DD} = 3.3 V

V_{DDP} = 5.5 V

CH1 = Ripple on V_{CC} output voltage

CH2 = 50 mA pulsed current I_{CC}

Figure 24. ST8024L application PCB schematic



4.4 Input and output connections

The three data lines of the smartcard signals are pulled high via an 11 kΩ resistor through V_{CC} and the three data lines of the microcontroller signals I/OUC, AUX1UC and AUX2UC are pulled high via an 11 kΩ resistor through V_{DD}, thus allowing operation when V_{CC} is not equal to V_{DD}.

The device and the microcontroller must use the same V_{DD} supply. Pins CLKDIV1, CLKDIV2, RSTIN, PRES, I/OUC, AUX1UC, AUX2UC, 5V/$\overline{3V}$, 1.8V, $\overline{CMDVcc}$ and $\overline{OFF}$ are referenced to V_{DD}. If the XTAL1 pin is to be driven by an external clock, also reference this pin to V_{DD}.

It is recommended that no control smartcard signals are to be shared with any other devices. Sharing could result in inadvertent activation or deactivation of the smartcard.

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
04-Oct-2010	1	Initial release.